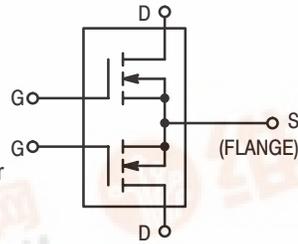


## The RF MOSFET Line RF Power Field-Effect Transistors N-Channel Enhancement-Mode

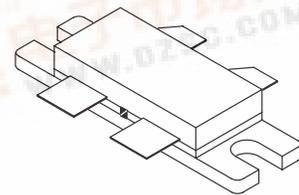
Designed for broadband commercial and military applications using push pull circuits at frequencies to 500 MHz. The high power, high gain and broadband performance of these devices makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Electrical Performance
  - MRF176GU @ 50 V, 400 MHz ("U" Suffix)
    - Output Power — 150 Watts
    - Power Gain — 14 dB Typ
    - Efficiency — 50% Typ
  - MRF176GV @ 50 V, 225 MHz ("V" Suffix)
    - Output Power — 200 Watts
    - Power Gain — 17 dB Typ
    - Efficiency — 55% Typ
- 100% Ruggedness Tested At Rated Output Power
- Low Thermal Resistance
- Low  $C_{RSS}$  — 7.0 pF Typ @  $V_{DS} = 50$  V



**MRF176GU  
 MRF176GV**

**200/150 W, 50 V, 500 MHz  
 N-CHANNEL MOS  
 BROADBAND  
 RF POWER FETs**



**CASE 375-04, STYLE 2**

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	125	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 40$	Vdc
Drain Current — Continuous	$I_D$	16	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	400 2.27	Watts W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.44	$^\circ\text{C/W}$

**Handling and Packaging** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS (1)

Drain-Source Breakdown Voltage ( $V_{GS} = 0$ , $I_D = 100$ mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 50$ V, $V_{GS} = 0$ )	$I_{DSS}$	—	—	2.5	mAdc
Gate-Body Leakage Current ( $V_{GS} = 20$ V, $V_{DS} = 0$ )	$I_{GSS}$	—	—	1.0	$\mu\text{Adc}$

1. Each side of device measured separately.

**ELECTRICAL CHARACTERISTICS — continued** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS (1)</b>					
Gate Threshold Voltage ( $V_{DS} = 10\text{ V}$ , $I_D = 100\text{ mA}$ )	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ V}$ , $I_D = 5.0\text{ A}$ )	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ V}$ , $I_D = 2.5\text{ A}$ )	$g_{fs}$	2.0	3.0	—	mhos

**DYNAMIC CHARACTERISTICS (1)**

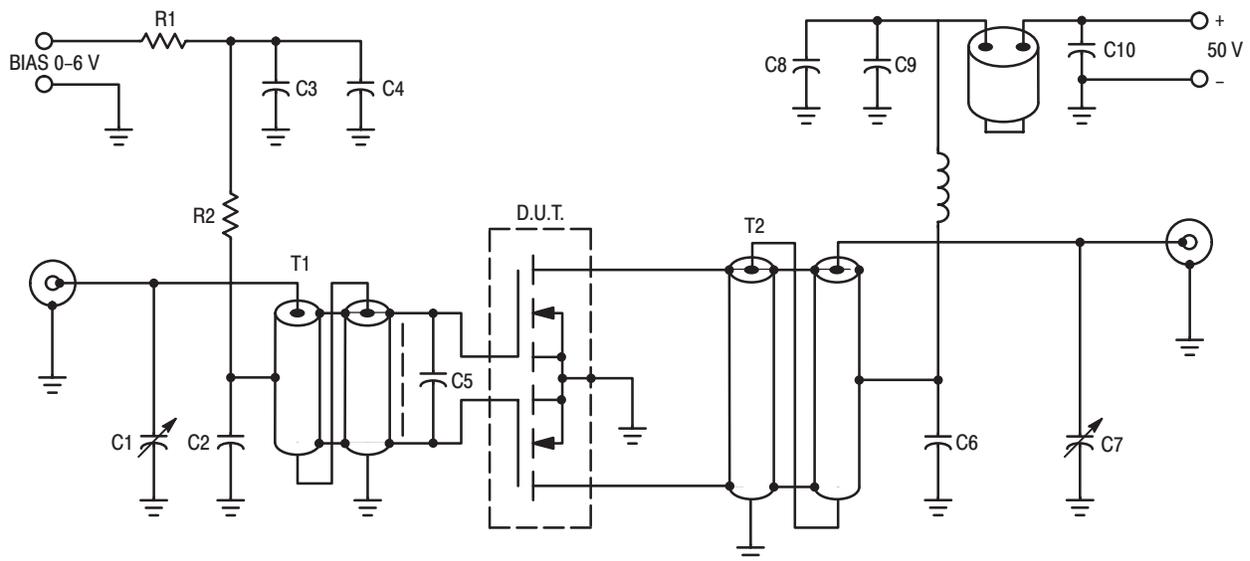
Input Capacitance ( $V_{DS} = 50\text{ V}$ , $V_{GS} = 0$ , $f = 1.0\text{ MHz}$ )	$C_{iss}$	—	180	—	pF
Output Capacitance ( $V_{DS} = 50\text{ V}$ , $V_{GS} = 0$ , $f = 1.0\text{ MHz}$ )	$C_{oss}$	—	100	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 50\text{ V}$ , $V_{GS} = 0$ , $f = 1.0\text{ MHz}$ )	$C_{rss}$	—	6.0	—	pF

**FUNCTIONAL CHARACTERISTICS — MRF176GV (2) (Figure 1)**

Common Source Power Gain ( $V_{DD} = 50\text{ Vdc}$ , $P_{out} = 200\text{ W}$ , $f = 225\text{ MHz}$ , $I_{DQ} = 2.0 \times 100\text{ mA}$ )	$G_{ps}$	15	17	—	dB
Drain Efficiency ( $V_{DD} = 50\text{ Vdc}$ , $P_{out} = 200\text{ W}$ , $f = 225\text{ MHz}$ , $I_{DQ} = 2.0 \times 100\text{ mA}$ )	$\eta$	50	55	—	%
Electrical Ruggedness ( $V_{DD} = 50\text{ Vdc}$ , $P_{out} = 200\text{ W}$ , $f = 225\text{ MHz}$ , $I_{DQ} = 2.0 \times 100\text{ mA}$ , VSWR 10:1 at all Phase Angles)	$\psi$	No Degradation in Output Power			

**NOTES:**

- Each side of device measured separately.
- Measured in push-pull configuration.



- C1 — Arco 404, 8.0–60 pF
- C2, C3, C6, C8 — 1000 pF Chip
- C4, C9 — 0.1  $\mu\text{F}$  Chip
- C5 — 180 pF Chip
- C7 — Arco 403, 3.0–35 pF
- C10 — 0.47  $\mu\text{F}$  Chip, Kemet 1215 or Equivalent
- L1 — 10 Turns AWG #16 Enameled Wire,  
Close Wound, 1/4" I.D.

Board material — .062" fiberglass (G10),  
Two sided, 1 oz. copper,  $\epsilon_r \approx 5$

Unless otherwise noted, all chip capacitors  
are ATC Type 100 or Equivalent

- L2 — Ferrite Beads of Suitable Material  
for 1.5–2.0  $\mu\text{H}$ , Total Inductance
- R1 — 100 Ohms, 1/2 W
- R2 — 1.0 kOhms, 1/2 W
- T1 — 4:1 Impedance Ratio RF Transformer.  
Can Be Made of 25 Ohm Semirigid  
Co-Ax, 47–62 Mils O.D.
- T2 — 1:4 Impedance Ratio RF Transformer.  
Can Be Made of 25 Ohm Semirigid  
Co-Ax, 62–90 Mils O.D.

NOTE: For stability, the input transformer T1 should be loaded  
with ferrite toroids or beads to increase the common  
mode inductance. For operation below 100 MHz. The  
same is required for the output transformer.

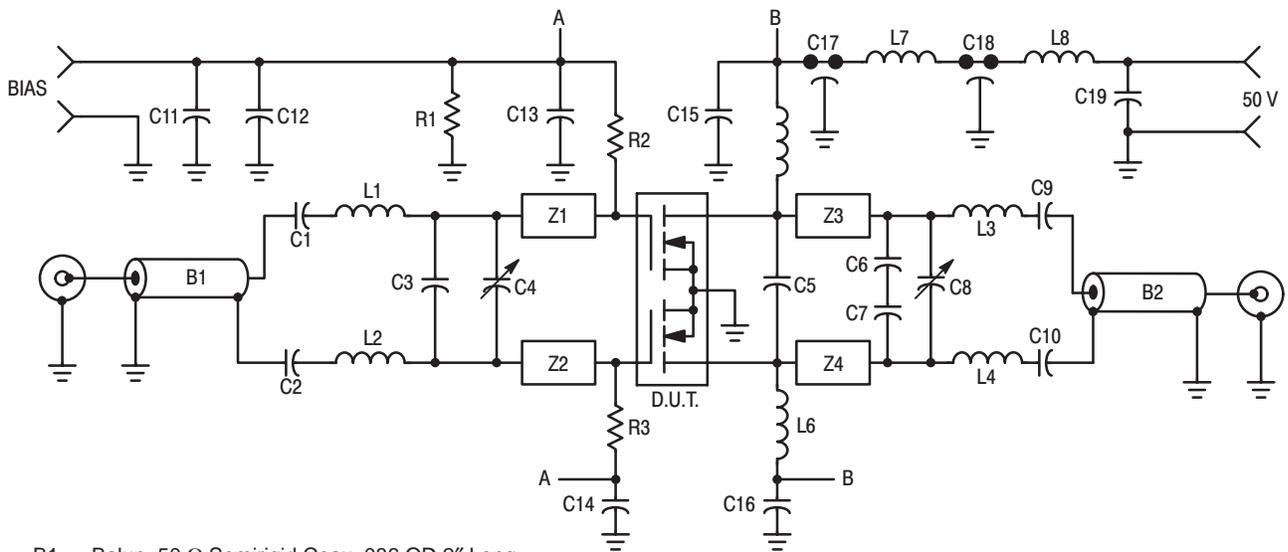
Figure 1. 225 MHz Test Circuit

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

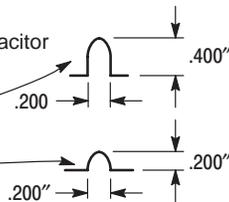
Characteristic	Symbol	Min	Typ	Max	Unit
<b>FUNCTIONAL CHARACTERISTICS — MRF176GU (1) (Figure 2)</b>					
Common Source Power Gain ( $V_{DD} = 50\text{ Vdc}$ , $P_{out} = 150\text{ W}$ , $f = 400\text{ MHz}$ , $I_{DQ} = 2.0 \times 100\text{ mA}$ )	$G_{ps}$	12	14	—	dB
Drain Efficiency ( $V_{DD} = 50\text{ Vdc}$ , $P_{out} = 150\text{ W}$ , $f = 400\text{ MHz}$ , $I_{DQ} = 2.0 \times 100\text{ mA}$ )	$\eta$	45	50	—	%
Electrical Ruggedness ( $V_{DD} = 50\text{ Vdc}$ , $P_{out} = 150\text{ W}$ , $f = 400\text{ MHz}$ , $I_{DQ} = 2.0 \times 100\text{ mA}$ , VSWR 10:1 at all Phase Angles)	$\psi$	No Degradation in Output Power			

**NOTE:**

1. Measured in push-pull configuration.



- B1 — Balun, 50  $\Omega$  Semirigid Coax .086 OD 2" Long
- B2 — Balun, 50  $\Omega$  Semirigid Coax .141 OD 2" Long
- C1, C2, C9, C10 — 270 pF ATC Chip Capacitor
- C3 — 15 pF ATC Chip Cap
- C4, C8 — 1.0–20 pF Piston Trimmer Cap
- C5 — 27 pF ATC Chip Cap
- C6, C7 — 22 pF Mini Unelco Capacitor
- C11, C13, C14, C15, C16 — 0.01  $\mu\text{F}$  Ceramic Capacitor
- C12 — 1.0  $\mu\text{F}$  50 V Tantalum Cap
- C17, C18 — 680 pF Feedthru Capacitor
- C19 — 10  $\mu\text{F}$  100 V Tantalum Cap
- L1, L2 — Hairpin Inductor #18 W
- L3, L4 — Hairpin Inductor #18 W

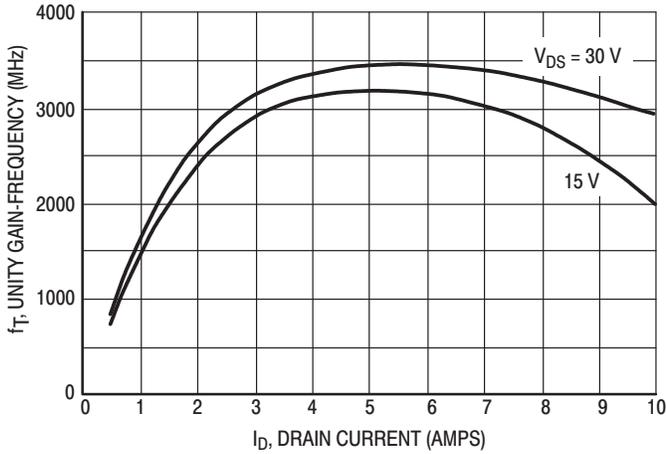


- L5, L6 — 13T #18 W .250 ID
- L7 — Ferroxcube VK-200 20/4B
- L8 — 3T #18 W .340 ID
- R1 — 1.0 k $\Omega$  1/4 W Resistor
- R2, R3 — 10 k $\Omega$  1/4 W Resistor
- Z1, Z2 — Microstrip Line .400L x .250W
- Z3, Z4 — Microstrip Line .450L x .250W

Ckt Board Material — .060" teflon-fiberglass, copper clad both sides, 2 oz. copper,  $\epsilon_r = 2.55$

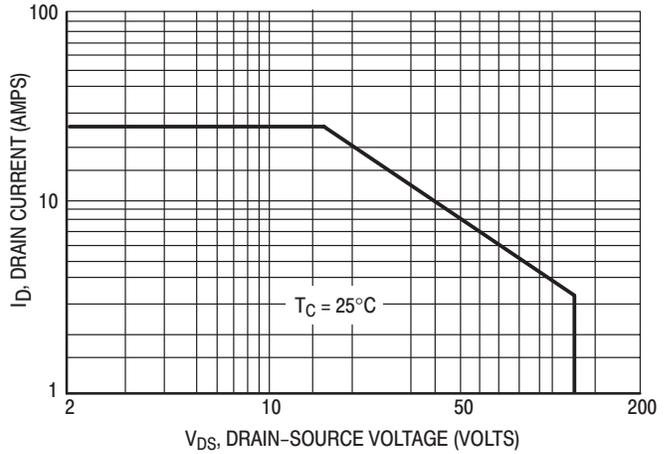
**Figure 2. 400 MHz Test Circuit**

## TYPICAL CHARACTERISTICS

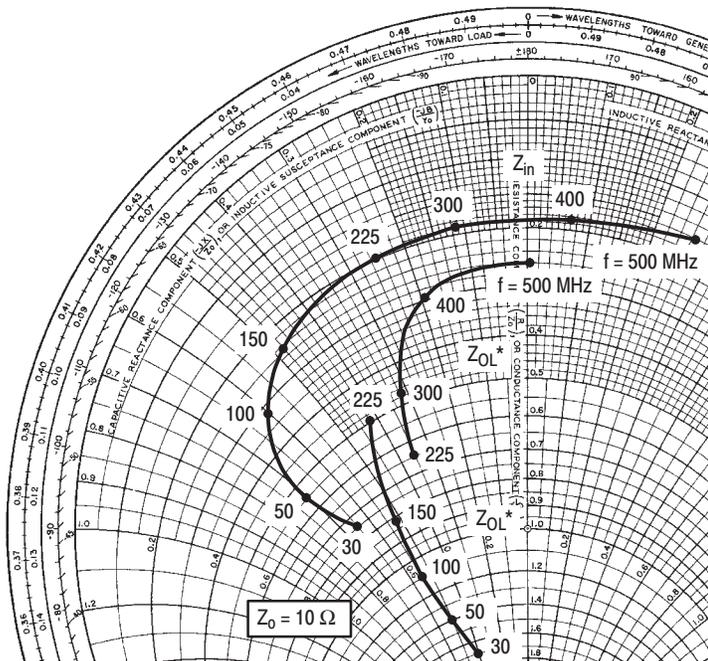


**Figure 3. Common Source Unity Current Gain\* Gain-Frequency versus Drain Current**

\* Data shown applies to each half of MRF176GU/GV



**Figure 4. DC Safe Operating Area**



NOTE: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

**Figure 5. Series Equivalent Input/Output Impedance**

### INPUT AND OUTPUT IMPEDANCE MRF176GU/GV

$V_{DD} = 50 \text{ V}$ ,  $I_{DQ} = 2 \times 100 \text{ mA}$

f MHz	$Z_{in}$ OHMS	$Z_{OL}^*$ OHMS
----------	------------------	--------------------

( $P_{out} = 150 \text{ W}$ )

225	2.05 - j2.50	6.50 - j3.50
300	2.00 - j1.10	4.80 - j3.10
400	1.85 + j0.75	3.00 - j1.90
500	1.60 + j2.70	2.60 + j0.10

( $P_{out} = 200 \text{ W}$ )

30	7.50 - j6.50	17.00 - j4.00
50	5.50 - j7.00	14.00 - j5.00
100	3.20 - j6.00	11.00 - j5.20
150	2.50 - j4.80	8.20 - j5.00
225	2.05 - j2.50	5.00 - j4.20

$Z_{OL}^*$  = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

## TYPICAL CHARACTERISTICS

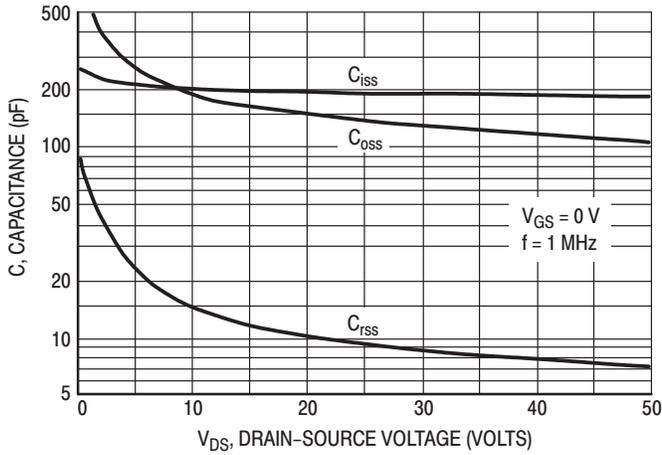


Figure 6. Capacitance versus Drain-Source Voltage\*

\* Data shown applies to each half of MRF176GU/GV

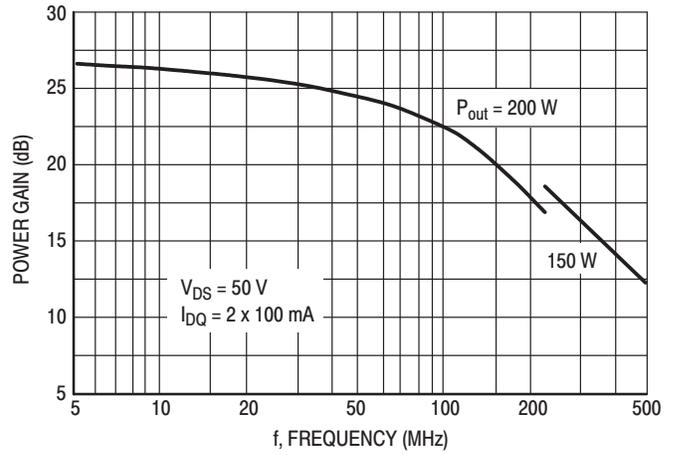


Figure 7. Power Gain versus Frequency

## MRF176GV

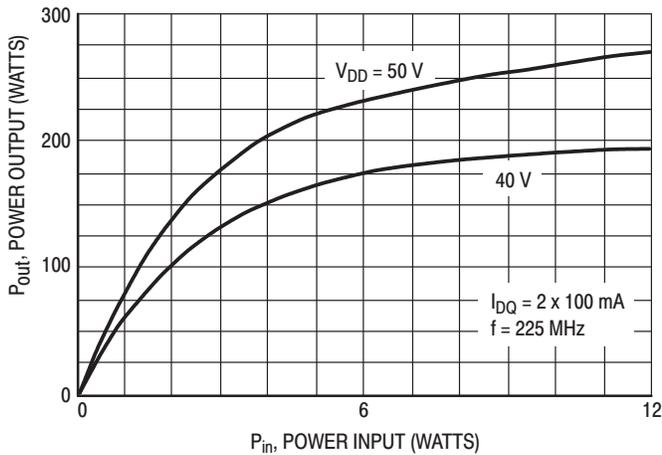


Figure 8. Power Input versus Power Output

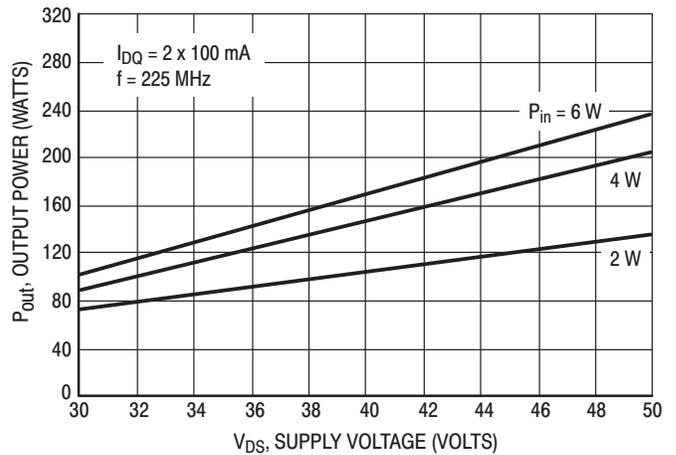
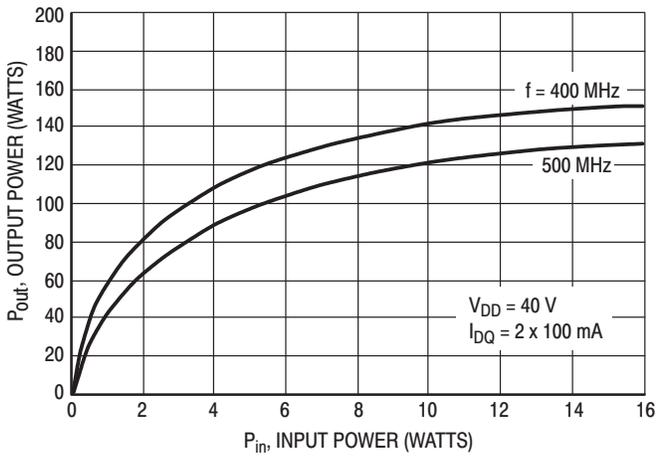
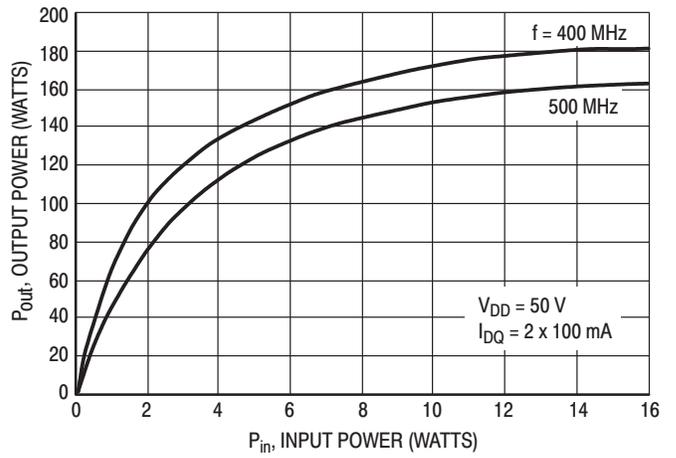


Figure 9. Output Power versus Supply Voltage

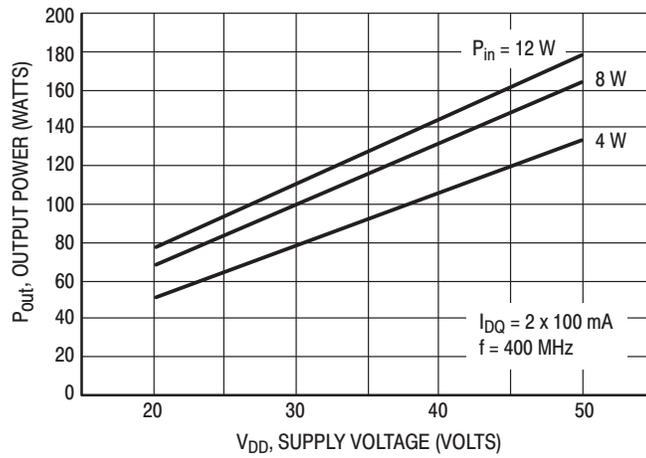
**TYPICAL CHARACTERISTICS**  
**MRF176GU**



**Figure 10. Output Power versus Input Power**



**Figure 11. Output Power versus Input Power**



**Figure 12. Output Power versus Supply Voltage**

NOTE: S-Parameter data represents measurements taken from one chip only.

Table 1. Common Source S-Parameters ( $V_{DS} = 50\text{ V}$ ,  $I_D = 0.35\text{ A}$ )

f MHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>	∠φ
30	0.804	-159	17.80	87	0.018	-1	0.602	-149
40	0.851	-163	12.50	77	0.018	-9	0.606	-147
50	0.846	-166	10.40	70	0.018	-14	0.610	-149
60	0.842	-167	8.45	67	0.017	-16	0.652	-154
70	0.846	-168	7.28	65	0.017	-15	0.708	-157
80	0.858	-169	6.13	63	0.016	-15	0.786	-159
90	0.875	-170	5.36	59	0.015	-17	0.883	-158
100	0.890	-171	4.61	53	0.014	-22	0.916	-157
110	0.902	-171	4.04	46	0.013	-29	0.919	-158
120	0.909	-172	3.41	41	0.012	-31	0.857	-156
130	0.915	-172	2.92	39	0.011	-29	0.819	-157
140	0.920	-173	2.61	38	0.010	-24	0.816	-160
150	0.924	-173	2.41	38	0.009	-20	0.858	-162
160	0.928	-174	2.24	38	0.008	-21	0.951	-164
170	0.934	-174	2.10	35	0.007	-24	1.046	-164
180	0.940	-175	1.96	30	0.008	-23	1.130	-163
190	0.945	-175	1.78	24	0.007	-18	1.120	-165
200	0.950	-176	1.56	22	0.006	-8	1.030	-165
210	0.953	-176	1.36	20	0.005	2	0.940	-165
220	0.955	-176	1.22	21	0.004	7	0.900	-164
230	0.956	-177	1.14	21	0.004	6	0.940	-167
240	0.958	-177	1.08	22	0.004	13	0.940	-170
250	0.960	-178	1.05	21	0.005	29	1.010	-169
260	0.963	-178	1.01	18	0.006	44	1.120	-170
270	0.965	-178	0.96	13	0.005	55	1.160	-172
280	0.967	-179	0.87	10	0.005	57	1.150	-172
290	0.968	-179	0.78	8	0.005	47	1.030	-171
300	0.969	-180	0.72	8	0.006	46	0.964	-170
310	0.970	-180	0.68	11	0.008	58	0.926	-169
320	0.971	180	0.65	11	0.009	72	0.940	-172
330	0.973	179	0.61	10	0.009	83	0.980	-173
340	0.973	179	0.61	11	0.008	82	1.053	-175
350	0.974	179	0.58	7	0.008	70	1.095	-174
360	0.975	178	0.55	3	0.010	61	1.135	-173
370	0.975	178	0.50	1	0.013	65	1.086	-175
380	0.976	178	0.47	-1	0.013	74	1.045	-175
390	0.976	177	0.44	1	0.012	84	0.979	-174
400	0.976	177	0.42	4	0.010	84	0.940	-174
410	0.977	177	0.40	4	0.011	71	1.015	-175
420	0.978	176	0.39	4	0.015	67	1.038	-177

Table 1. Common Source S-Parameters ( $V_{DS} = 50\text{ V}$ ,  $I_D = 0.35\text{ A}$ ) continued

f MHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>	∠φ
430	0.978	176	0.38	3	0.017	74	1.073	-178
440	0.979	176	0.37	0	0.017	83	1.091	-178
450	0.979	176	0.37	-2	0.015	86	1.107	-177
460	0.979	175	0.32	-6	0.013	71	1.118	-178
470	0.979	175	0.30	-5	0.015	60	1.003	-178
480	0.979	175	0.30	-3	0.019	66	0.975	-176
490	0.980	174	0.29	-1	0.021	80	0.963	-178
500	0.981	174	0.28	0	0.021	92	0.993	-179
600	0.972	172	0.24	-5	0.012	93	0.943	178
700	0.971	169	0.15	-8	0.027	75	0.999	176
800	0.971	166	0.13	-9	0.022	70	0.977	174
900	0.972	164	0.10	-5	0.032	73	0.972	172
1000	0.972	161	0.08	-9	0.030	83	0.999	169

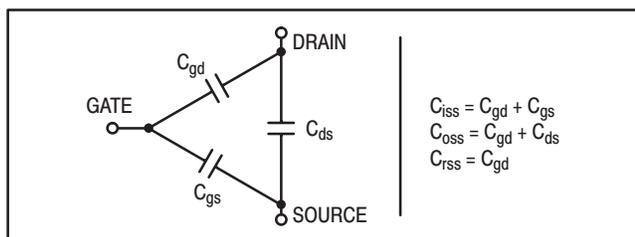
## RF POWER MOSFET CONSIDERATIONS

### MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain ( $C_{gd}$ ), and gate-to-source ( $C_{gs}$ ). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain-to-source ( $C_{ds}$ ).

These capacitances are characterized as input ( $C_{iss}$ ), output ( $C_{oss}$ ) and reverse transfer ( $C_{rss}$ ) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The  $C_{iss}$  can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



The  $C_{iss}$  given in the electrical characteristics table was measured using method 2 above. It should be noted that  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$  are measured at zero drain current and are provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

### LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain, data presented in Figure 3 may give the designer additional information on the capabilities of this device. The graph represents

the small signal unity current gain frequency at a given drain current level. This is equivalent to  $f_T$  for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

### DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance,  $V_{DS(on)}$ , occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs,  $V_{DS(on)}$  has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

### GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of  $10^9$  ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage,  $V_{GS(th)}$ .

**Gate Voltage Rating** — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated  $V_{GS}$  can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** — The gates of this device are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — This device does not have an internal monolithic zener diode from gate-to-source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

## HANDLING CONSIDERATIONS

The gate of the MOSFET, which is electrically isolated from the rest of the die by a very thin layer of SiO<sub>2</sub>, may be damaged if the power MOSFET is handled or installed improperly. Exceeding the 40 V maximum gate-to-source voltage rating,  $V_{GS(max)}$ , can rupture the gate insulation and destroy the FET. RF Power MOSFETs are not nearly as susceptible as CMOS devices to damage due to static discharge because the input capacitances of power MOSFETs are much larger and absorb more energy before being charged to the gate breakdown voltage. However, once breakdown begins, there is enough energy stored in the gate-source capacitance to ensure the complete perforation of the gate oxide. To avoid the possibility of device failure caused by static discharge, precautions similar to those taken with small-signal MOSFET and CMOS devices apply to power MOSFETs.

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with grounded equipment.

The gate of the power MOSFET could still be in danger after the device is placed in the intended circuit. If the gate may see voltage transients which exceed  $V_{GS(max)}$ , the circuit designer should place a 40 V zener across the gate and source terminals to clamp any potentially destructive spikes. Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

## DESIGN CONSIDERATIONS

The MRF176G is a RF power N-channel enhancement mode field-effect transistor (FETs) designed for VHF and UHF power amplifier applications. M/A-COM RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove MOS power FETs.

M/A-COM Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

## DC BIAS

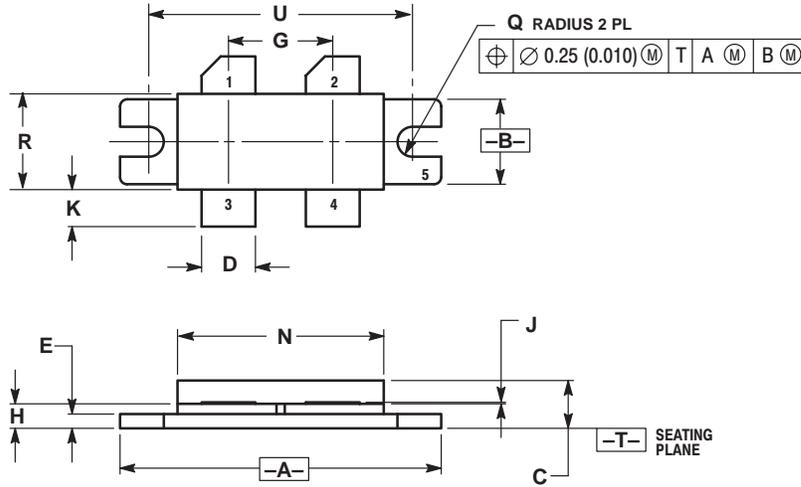
The MRF176G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current ( $I_{DQ}$ ) is not critical for many applications. The MRF176G was characterized at  $I_{DQ} = 100$  mA, each side, which is the suggested minimum value of  $I_{DQ}$ . For special applications such as linear amplification,  $I_{DQ}$  may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

## GAIN CONTROL

Power output of the MRF176G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

## PACKAGE DIMENSIONS



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.330	1.350	33.79	34.29
B	0.370	0.410	9.40	10.41
C	0.190	0.230	4.83	5.84
D	0.215	0.235	5.47	5.96
E	0.050	0.070	1.27	1.77
G	0.430	0.440	10.92	11.18
H	0.102	0.112	2.59	2.84
J	0.004	0.006	0.11	0.15
K	0.185	0.215	4.83	5.33
N	0.845	0.875	21.46	22.23
Q	0.060	0.070	1.52	1.78
R	0.390	0.410	9.91	10.41
U	1.100 BSC		27.94 BSC	

- STYLE 2:  
 PIN 1. DRAIN  
 2. DRAIN  
 3. GATE  
 4. GATE  
 5. SOURCE

**CASE 375-04  
 ISSUE D**

*Specifications subject to change without notice.*

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