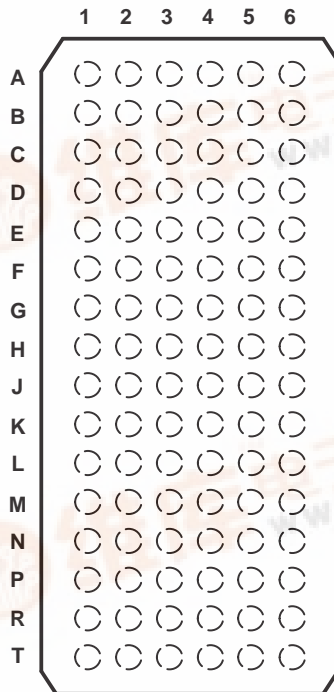


# 3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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- Member of the Texas Instruments Widebus+™ Family
- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

GKE OR ZKE PACKAGE  
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1Q2	1Q1	1 $\overline{OE}$	1CLK	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	V <sub>CC</sub>	V <sub>CC</sub>	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	V <sub>CC</sub>	V <sub>CC</sub>	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
H	2Q7	2Q8	2 $\overline{OE}$	2CLK	2D8	2D7
J	3Q2	3Q1	3 $\overline{OE}$	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	V <sub>CC</sub>	V <sub>CC</sub>	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	V <sub>CC</sub>	V <sub>CC</sub>	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	4 $\overline{OE}$	4CLK	4D8	4D7

NC – No internal connection

## description/ordering information

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	SN74LVTH322374KR	HW374
	LFBGA – ZKE (Pb-free)		74LVTH322374ZKER	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

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# SN74LVTH322374

## 3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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### description/ordering information (continued)

The SN74LVTH322374 is a 32-bit edge-triggered D-type flip-flop with 3-state outputs designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

This device can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- $\Omega$  series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

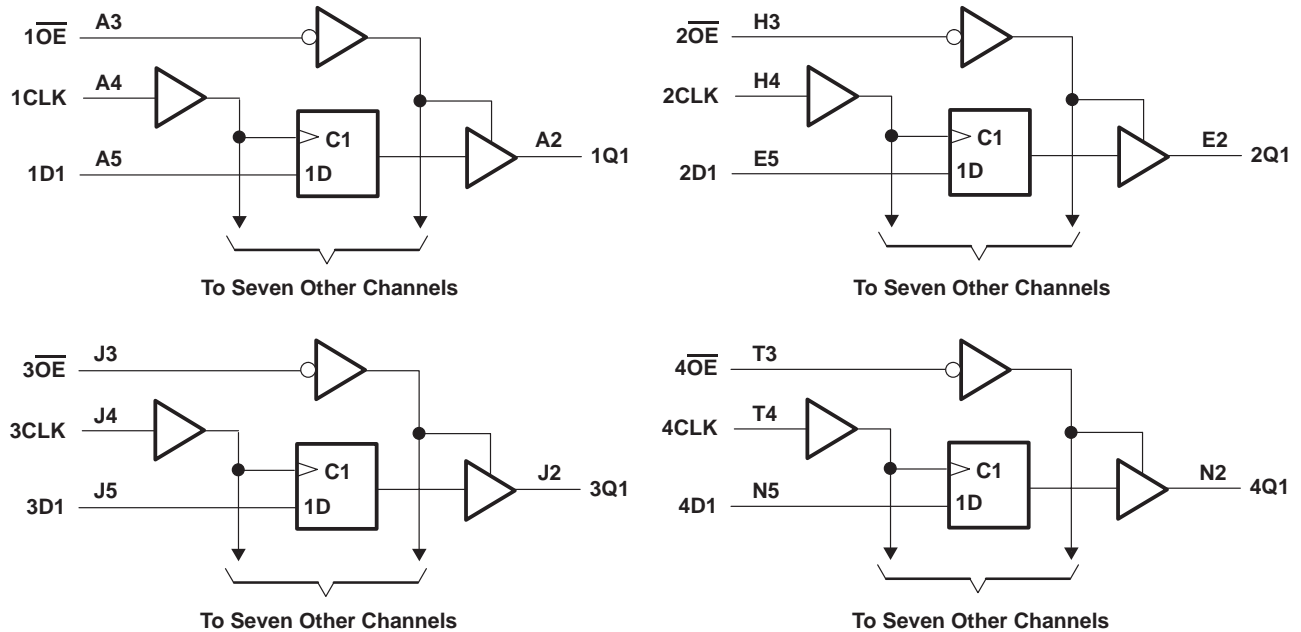
FUNCTION TABLE  
(each 8-bit flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z

# **SN74LVTH322374** **3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP** **WITH 3-STATE OUTPUTS**

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## **logic diagram (positive logic)**



## **absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$	30 mA
Current into any output in the high state, $I_O$ (see Note 2)	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): GKE/ZKE package	40°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN74LVTH322374

## 3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.7	3.6	V
V <sub>IH</sub>	High-level input voltage		2		V
V <sub>IL</sub>	Low-level input voltage			0.8	V
V <sub>I</sub>	Input voltage			5.5	V
I <sub>OH</sub>	High-level output current			−12	mA
I <sub>OL</sub>	Low-level output current			12	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		μs/V
T <sub>A</sub>	Operating free-air temperature		−40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 2.7$ V,	$I_I = -18$ mA			–1.2	V
$V_{OH}$		$V_{CC} = 3$ V,	$I_{OH} = -12$ mA	2			V
$V_{OL}$		$V_{CC} = 3$ V,	$I_{OL} = 12$ mA			0.8	V
$I_I$		$V_{CC} = 0$ or 3.6 V,	$V_I = 5.5$ V			10	$\mu$ A
	Control inputs	$V_{CC} = 3.6$ V,	$V_I = V_{CC}$ or GND			$\pm 1$	
	Data inputs	$V_{CC} = 3.6$ V	$V_I = V_{CC}$ $V_I = 0$			1 –5	
$I_{off}$		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 4.5 V			$\pm 100$	$\mu$ A
$I_{I(hold)}$	Data inputs	$V_{CC} = 3$ V	$V_I = 0.8$ V	75			$\mu$ A
			$V_I = 2$ V	–75			
		$V_{CC} = 3.6$ V‡,	$V_I = 0$ to 3.6 V			500 –750	
$I_{OZH}$		$V_{CC} = 3.6$ V,	$V_O = 3$ V			5	$\mu$ A
$I_{OZL}$		$V_{CC} = 3.6$ V,	$V_O = 0.5$ V			–5	$\mu$ A
$I_{OZPU}$		$V_{CC} = 0$ to 1.5 V, $V_O = 0.5$ V to 3 V, $\overline{OE} = \text{don't care}$				$\pm 100$	$\mu$ A
$I_{OZPD}$		$V_{CC} = 1.5$ V to 0, $V_O = 0.5$ V to 3 V, $\overline{OE} = \text{don't care}$				$\pm 100$	$\mu$ A
$I_{CC}$	$V_{CC} = 3.6$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND		Outputs high			0.38	mA
			Outputs low			10	
			Outputs disabled			0.38	
$\Delta I_{CC}§$	$V_{CC} = 3$ V to 3.6 V, One input at $V_{CC} - 0.6$ V, Other inputs at $V_{CC}$ or GND					0.2	mA
$C_i$	$V_I = 3$ V or 0					3	pF
$C_o$	$V_O = 3$ V or 0					9	pF

† All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$ .

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

**SN74LVTH322374**  
**3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

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**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		160		160		MHz
$t_W$	Pulse duration, CLK high or low		3		3		ns
$t_{\text{su}}$	Setup time, data before CLK $\uparrow$	High or low	1.8		2		ns
$t_h$	Hold time, data after CLK $\uparrow$	High or low	0.8		0.1		ns

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		UNIT
			MIN	TYP†	MAX	MIN	MAX	
f <sub>max</sub>			160			160		MHz
t <sub>PLH</sub>	CLK	Q	2	3.4	5.3	6.2		ns
t <sub>PHL</sub>			2.2	3.3	4.9	5.1		
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q	1.8	3.5	5.6	6.9		ns
t <sub>PZL</sub>			1.8	3.5	4.9	6		
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q	2.4	4.2	5.4	5.7		ns
t <sub>PLZ</sub>			2	3.8	5	5.1		
t <sub>sk(o)</sub>			0.5					ns

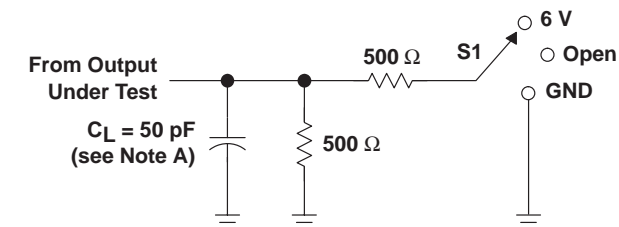
$\dagger$  All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

# SN74LVTH322374

## 3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

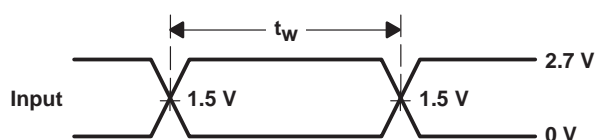
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### PARAMETER MEASUREMENT INFORMATION

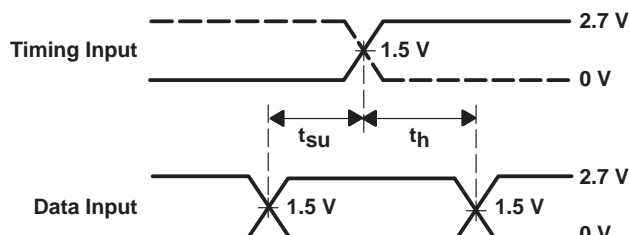


LOAD CIRCUIT

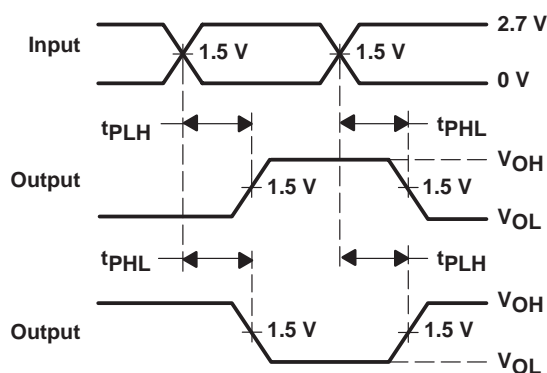
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



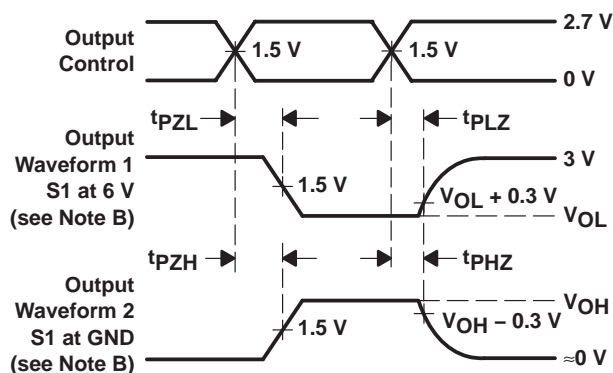
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

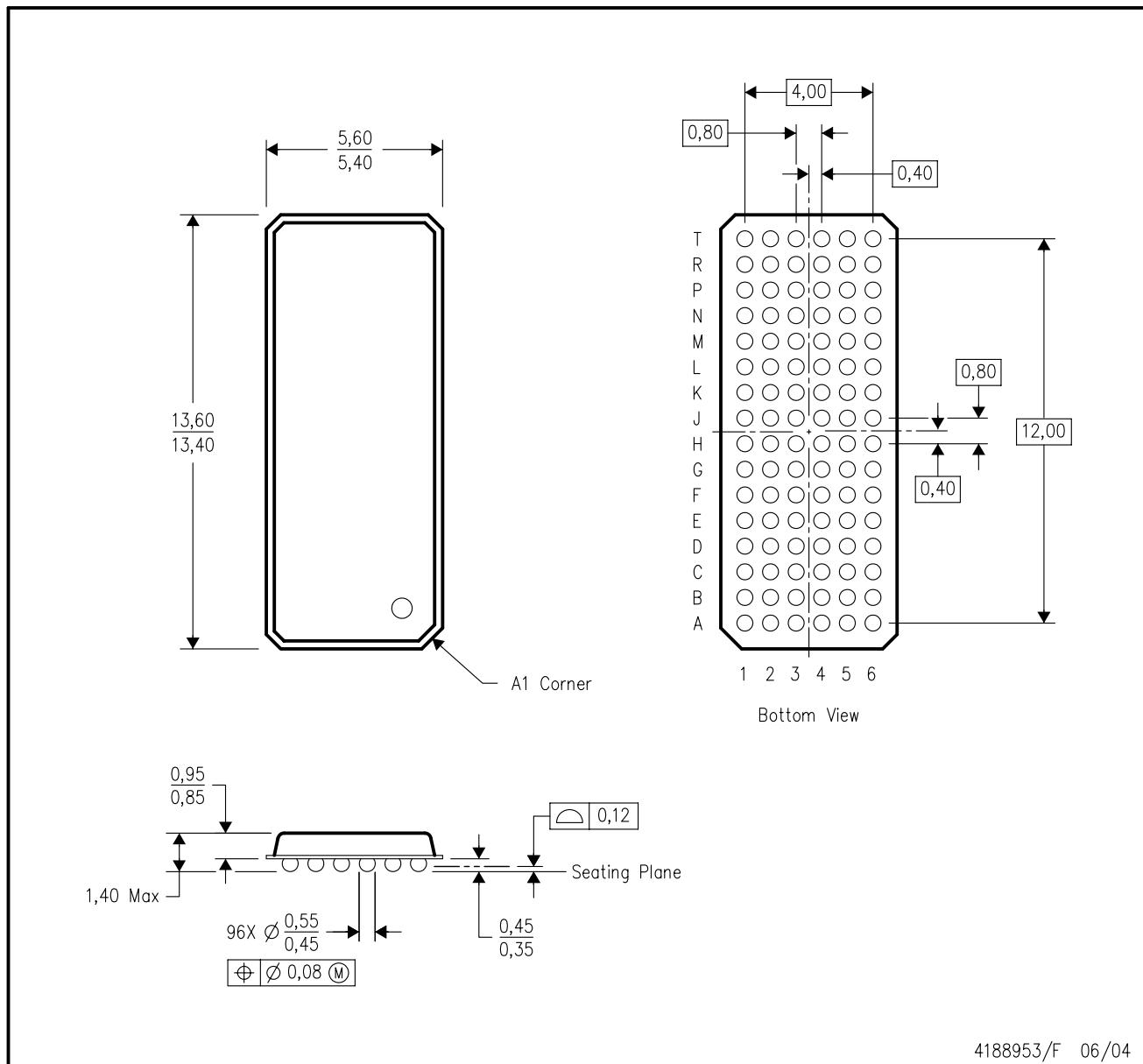
- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# MECHANICAL DATA

GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY

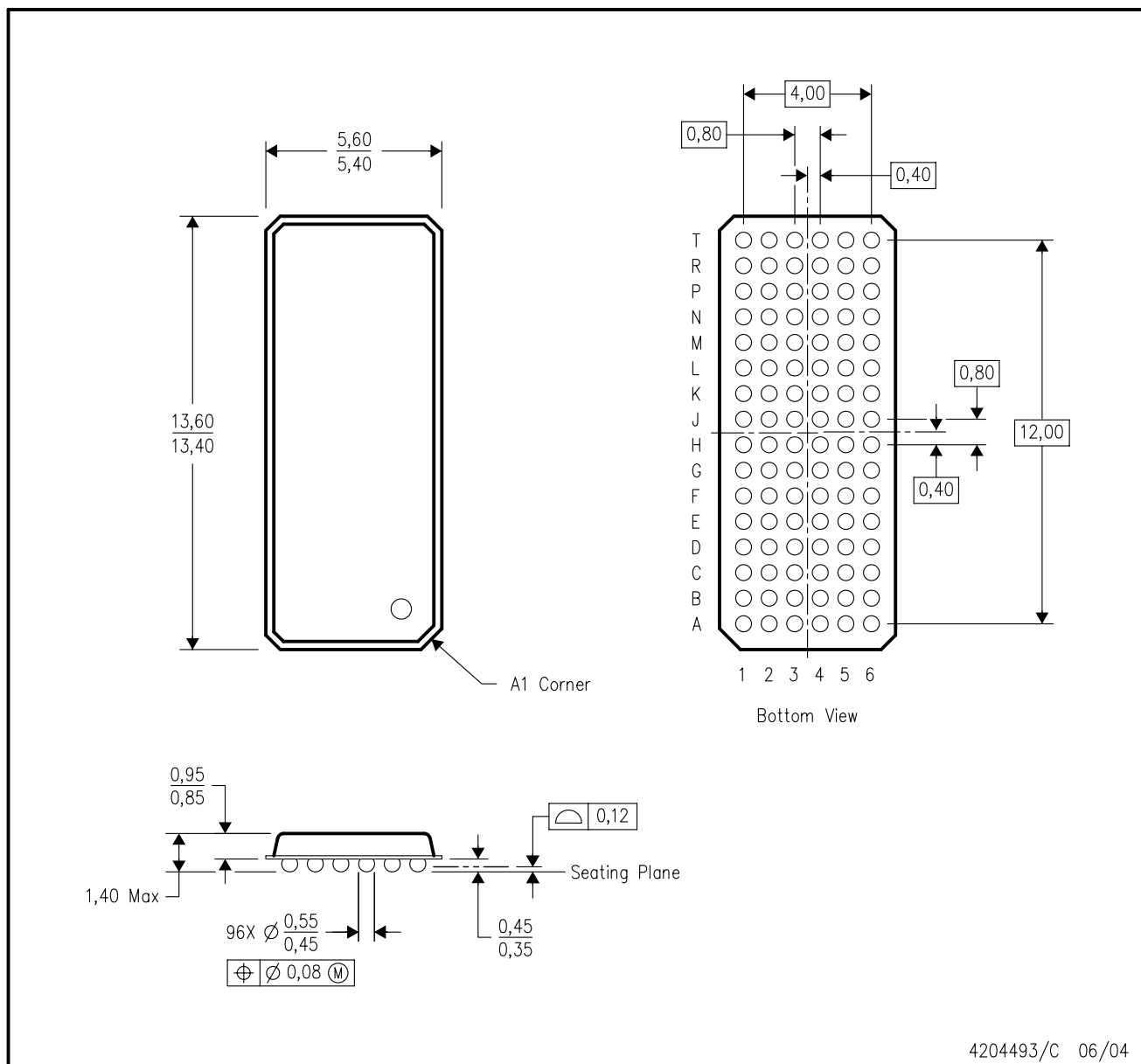


4188953/F 06/04

## MECHANICAL DATA

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Falls within JEDEC MO-205 variation CC.
  - This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).



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Mailing Address: Texas Instruments  
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