

SN54HC594 SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS040C – DECEMBER 1982 – REVISED FEBRUARY 1998

- **8-Bit Serial-In, Parallel-Out Shift Registers With Storage**
- **Independent Direct Overriding Clears on Shift and Storage Registers**
- **Independent Clocks for Both Shift and Storage Registers**
- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

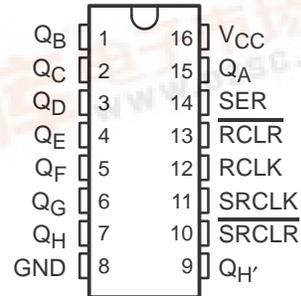
The 'HC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear (\overline{RCLR} , \overline{SRCLR}) inputs are provided on both the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

Both the shift register (RCLK) and storage register (SRCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register is always one count pulse ahead of the storage register.

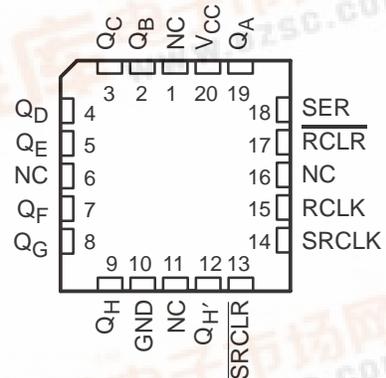
The parallel (Q_A – Q_H) outputs have high-current capability. $Q_{H'}$ is a standard output.

The SN54HC594 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC594 is characterized for operation from -40°C to 85°C .

SN54HC594 . . . J OR W PACKAGE
SN74HC594 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54HC594 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

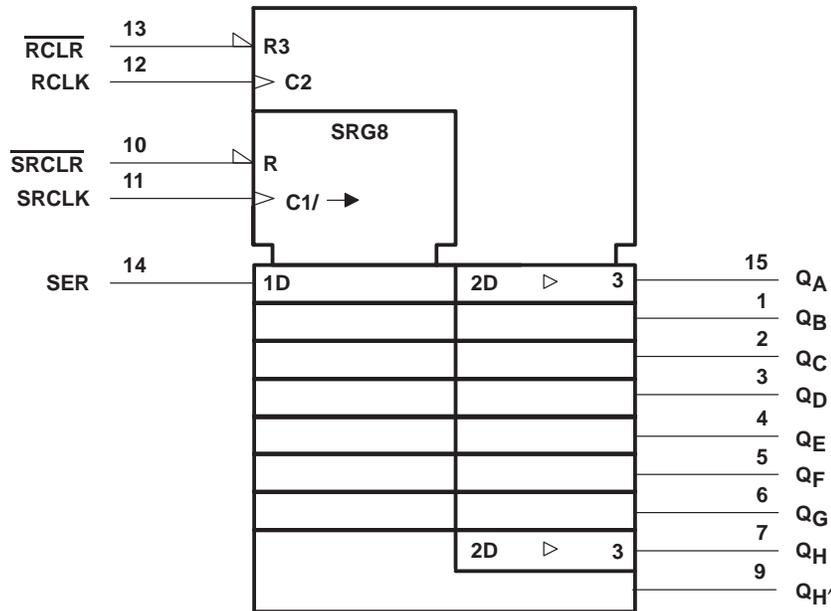


SN54HC594, SN74HC594

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logic symbol†

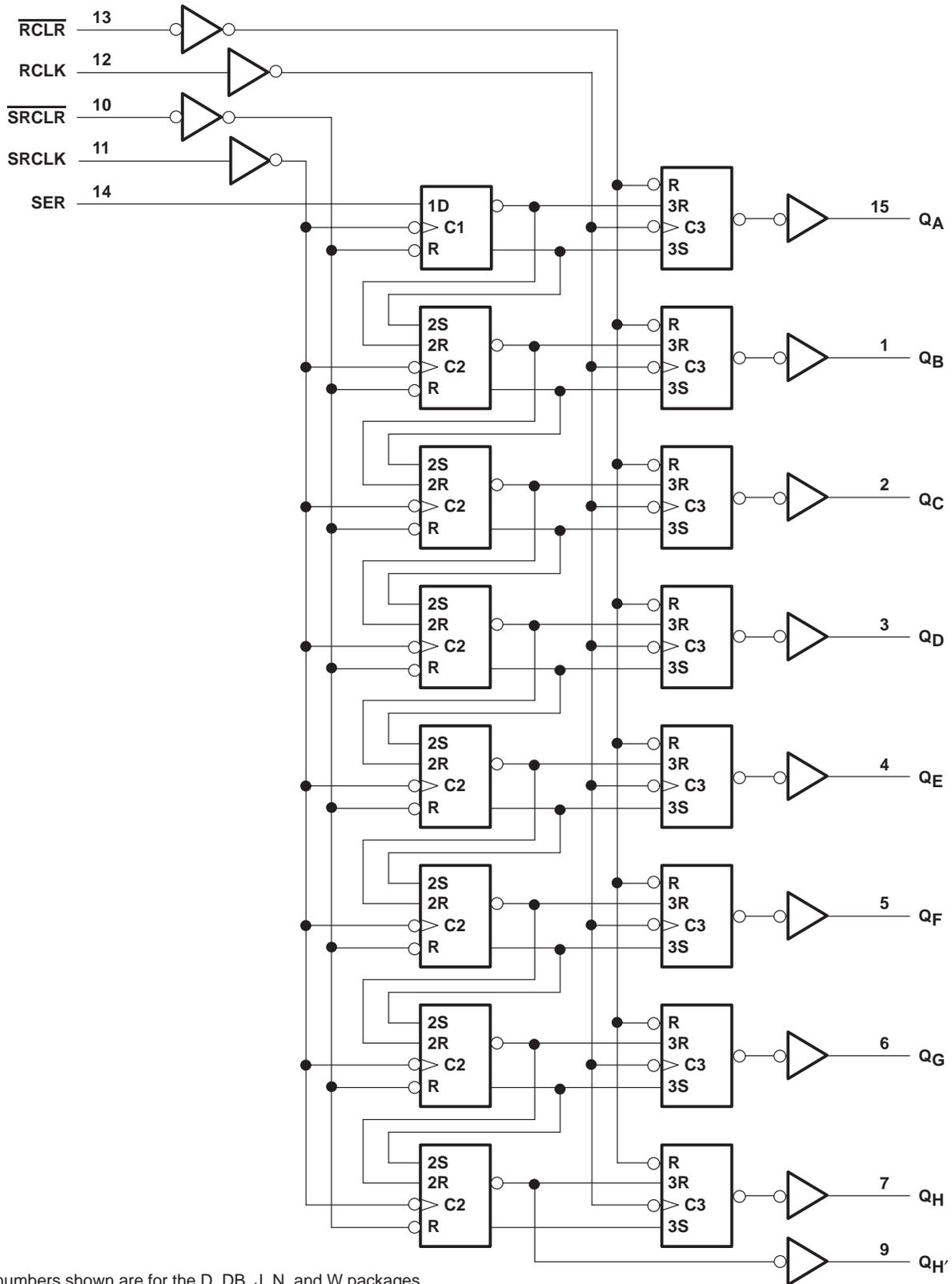


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, N, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, and W packages.

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absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	113°C/W
DB package	131°C/W
N package	78°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54HC594			SN74HC594			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5		V	
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 6$ V		4.2	4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0	0.5	0	0.5	V
		$V_{CC} = 4.5$ V		0	1.35	0	1.35	
		$V_{CC} = 6$ V		0	1.8	0	1.8	
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	$V_{CC} = 2$ V		0	1000	0	1000	ns
		$V_{CC} = 4.5$ V		0	500	0	500	
		$V_{CC} = 6$ V		0	400	0	400	
T_A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		4.5 V	Q _{H'} , I _{OH} = -4 mA	3.98	4.3		3.7		3.84		
			Q _A -Q _H , I _{OH} = -6 mA	3.98	4.3		3.7		3.84		
			Q _{H'} , I _{OH} = -5.2 mA	5.48	5.8		5.2		5.34		
6 V	Q _A -Q _H , I _{OH} = -7.8 mA	5.48	5.8		5.2		5.34				
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		4.5 V	Q _{H'} , I _{OL} = 4 mA		0.17	0.26		0.4		0.33	
			Q _A -Q _H , I _{OL} = 6 mA		0.17	0.26		0.4		0.33	
			Q _{H'} , I _{OL} = 5.2 mA		0.15	0.26		0.4		0.33	
6 V	Q _A -Q _H , I _{OL} = 7.8 mA		0.15	0.26		0.4		0.33			
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	V _O = V _{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			8		160		80	μA
C _i			2 V to 6 V		3	10		10		10	pF

SN54HC594, SN74HC594

8-BIT SHIFT REGISTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HC594		SN74HC594		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	2 V	5		3.3		4		MHz
		4.5 V	25		17		20		
		6 V	29		20		24		
t _w	SRCLK or RCLK high or low	2 V	100		150		125	ns	
		4.5 V	20		30		25		
		6 V	17		25		21		
	SRCLR or RCLR low	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		25		21		
t _{su}	SER before SRCLK↑	2 V	90		135		110	ns	
		4.5 V	18		27		22		
		6 V	15		23		19		
	SRCLK↑ before RCLK↑↑	2 V	90		135		110		
		4.5 V	18		27		22		
		6 V	15		23		19		
	SRCLR low before RCLK↑	2 V	50		75		63		
		4.5 V	10		15		13		
		6 V	9		13		11		
	SRCLR high (inactive) before SRCLK↑	2 V	20		20		20		
		4.5 V	10		10		10		
		6 V	10		10		10		
RCLR high (inactive) before SRCLK↑	2 V	5		5		5			
	4.5 V	5		5		5			
	6 V	5		5		5			
t _h	Hold time, SER after SRCLK↑	2 V	5		5		5	ns	
		4.5 V	5		5		5		
		6 V	5		5		5		

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	5	8		3.3		4	MHz	
			4.5 V	25	35		17		20		
			6 V	29	40		20		24		
t _{pd}	SRCLK	Q _{H'}	2 V		50	150		225		185	ns
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
	RCLK	Q _A -Q _H	2 V		50	150		225		185	
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
t _{PHL}	SRCLR	Q _{H'}	2 V		50	150		225		185	ns
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
	RCLR	Q _A -Q _H	2 V		50	125		185		155	
			4.5 V		20	25		37		31	
			6 V		15	21		31		26	
t _t		Q _{H'}	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	
		Q _A -Q _H	2 V		38	60		90		75	
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	RCLK	Q _A -Q _H	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t _{PHL}	RCLR	Q _A -Q _H	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t _t		Q _A -Q _H	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

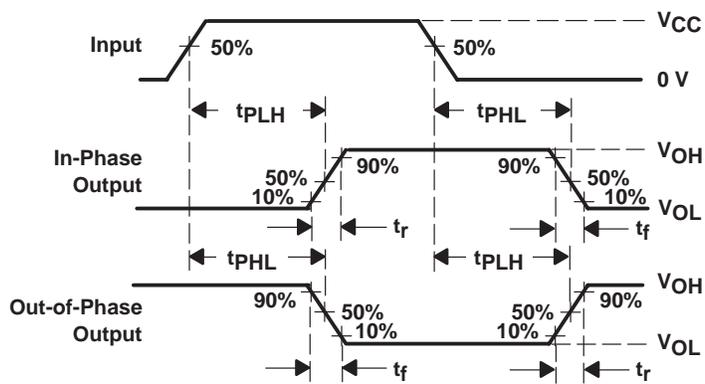
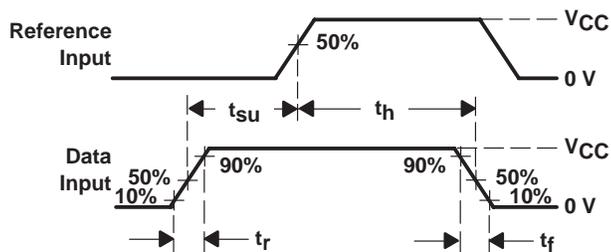
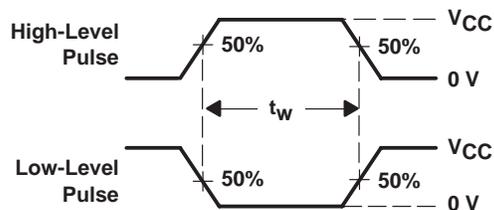
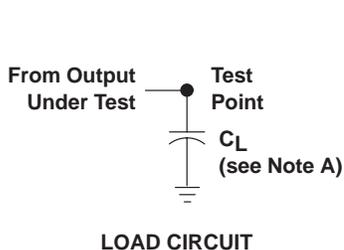
operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load	395	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - F. t_f and t_r are the same as t_t .

Figure 1. Load Circuit and Voltage Waveforms

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