intersil™

380MHz, SOT-23, Low Power Current Feedback Operational Amplifier

The HFA1155 is a low power, high-speed op amp and is the most recent addition to Intersil's HFA1XX5 series of low power op amps and buffers. Intersil's proprietary complementary bipolar UHF-1 process, coupled with the current feedback architecture deliver superb bandwidth even at very high gains (>250MHz at $A_V = 10$). The excellent video parameters make this amplifier ideal for professional video applications.

Though specified for ±5V operation, the HFA1155 operates with single supply voltages as low as 4.5V, and requires only 1.4mA of I_{CC} in 5V applications (see Application Information section, and Application Note AN9897).

For a lower distortion, higher bandwidth amplifier in a SOT-23 package, please refer to the HFA1150 data sheet.

Features

- Low Power 5.5mA
- Low Distortion (10MHz, HD2). . . . . -53dBc
- -3dB Bandwidth 380MHz
- High Slew Rate. 1700V/µs
- Fast Settling Time (0.1%) 30ns
- Excellent Gain Flatness . . . . ±0.04dB to 50MHz
- High Output Current 55mA
- Fast Overdrive Recovery . . . . <7ns
- Operates with 5V Single Supply (See AN9897)

Applications

- Video Switching and Routing
- Pulse and Video Amplifiers
- IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems
- Related Literature
  - AN9420, Current Feedback Theory
  - AN9897, Single 5V Supply Operation

Ordering Information

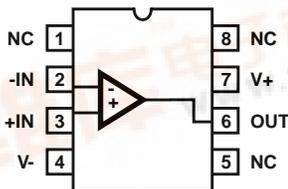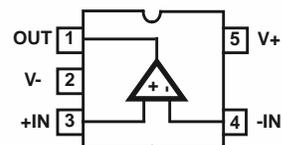| PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1155IB (H1155I)	-40 to 85	8 Ld SOIC	M8.15
HFA1155IB96 (H1155I)	-40 to 85	8 Ld SOIC Tape and Reel	M8.15
HFA1155IH96 (1155)	-40 to 85	5 Ld SOT-23 Tape and Reel	P5.064
HFA11XXEVAL	DIP Evaluation Board for High-Speed Op Amps		
OPAMPSOT23EVAL	SOT-23 Evaluation Board for High-Speed Op Amps		

Pinouts

HFA1155 (SOIC) TOP VIEW

```
NC  [1]        [8] NC
-IN [2]        [7] V+
+IN [3]        [6] OUT
V-  [4]        [5] NC
```

HFA1155 (SOT23) TOP VIEW

```
OUT [1]        [5] V+
V-  [2]
+IN [3]        [4] -IN
```

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

HFA1155

Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- 12V
Input Voltage . . . . V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA
ESD Rating
   Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 600V

Operating Conditions

Temperature Range . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (^{o}C/W)
   SOIC Package 175
   SOT-23 Package 225
Moisture Sensitivity (see Technical Brief TB363)
   SOIC Package . . . . Level 1
   SOT-23 Package . . . . Level 1
Maximum Junction Temperature (Plastic Package) . . . . .150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
   (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (^{o}C)	HFA1155IB (SOIC)			HFA1155IH (SOT-23)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS										
Input Offset Voltage (Note 3)		A	25	-	2	6	-	2	6	mV
		A	Full	-	-	10	-	-	10	mV
Input Offset Voltage Drift		C	Full	-	10	-	-	10	-	$\mu V/^oC$
V_{IO} CMRR	$\Delta V_{CM} = \pm2V$	A	25	40	46	-	40	46	-	dB
		A	Full	38	-	-	38	-	-	dB
V_{IO} PSRR	$\Delta V_S = \pm1.25V$	A	25	45	50	-	45	50	-	dB
		A	Full	42	-	-	42	-	-	dB
Non-Inverting Input Bias Current (Note 3)	+IN = 0V	A	25	-	25	40	-	25	40	μA
		A	Full	-	-	65	-	-	65	μA
+I_{BIAS} Drift		C	Full	-	40	-	-	40	-	$nA/^oC$
+I_{BIAS} CMS	$\Delta V_{CM} = \pm2V$	A	25	-	20	40	-	20	40	$\mu A/V$
		A	Full	-	-	50	-	-	50	$\mu A/V$
Inverting Input Bias Current (Note 3)	-IN = 0V	A	25	-	12	50	-	12	50	μA
		A	Full	-	-	60	-	-	60	μA
-I_{BIAS} Drift		C	Full	-	40	-	-	40	-	$nA/^oC$
-I_{BIAS} CMS	$\Delta V_{CM} = \pm2V$	A	25	-	1	7	-	1	7	$\mu A/V$
		A	Full	-	-	10	-	-	10	$\mu A/V$
-I_{BIAS} PSS	$\Delta V_S = \pm1.25V$	A	25	-	6	15	-	6	15	$\mu A/V$
		A	Full	-	-	27	-	-	27	$\mu A/V$
Non-Inverting Input Resistance		A	25	25	50	-	25	50	-	$k\Omega$
Inverting Input Resistance		C	25	-	40	-	-	40	-	Ω
Input Capacitance (Either Input)		B	25	-	2	-	-	2	-	pF
Input Common Mode Range		C	Full	±2.5	±3.0	-	±2.5	±3.0	-	V
Input Noise Voltage (Note 3)	100kHz	B	25	-	4.7	-	-	4.7	-	$nV/\sqrt{Hz}$
+Input Noise Current (Note 3)	100kHz	B	25	-	26	-	-	26	-	$pA/\sqrt{Hz}$
-Input Noise Current (Note 3)	100kHz	B	25	-	35	-	-	35	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS										
Open Loop Transimpedance Gain (Note 3)		B	25	-	630	-	-	630	-	$k\Omega$
Minimum Stable Gain		A	Full	1	-	-	1	-	-	V/V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified   **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (°C)	HFA1155IB (SOIC)			HFA1155IH (SOT-23)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
AC CHARACTERISTICS $A_V = +2$, (Note 4) Unless Otherwise Specified										
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$, Note 3)	$A_V = -1$	B	25	-	370	-	-	360	-	MHz
	$A_V = +1$	B	25	-	370	-	-	365	-	MHz
	$A_V = +2$	B	25	-	380	-	-	355	-	MHz
-3dB Bandwidth ($V_{OUT} = 2V_{P-P}$)	$A_V = +2$	B	25	-	175	-	-	170	-	MHz
Gain Flatness ($V_{OUT} = 0.2V_{P-P}$, Note 3)	To 25MHz	B	25	-	±0.03	-	-	±0.06	-	dB
	To 50MHz	B	25	-	±0.04	-	-	±0.06	-	dB
	To 100MHz	B	25	-	±0.15	-	-	±0.1	-	dB
Full Power Bandwidth ($V_{OUT} = 5V_{P-P}$ at $A_V = +2$; $V_{OUT} = 4V_{P-P}$ at $A_V = +1$, Note 3)	$A_V = +1$	B	25	-	50	-	-	45	-	MHz
	$A_V = +2$	B	25	-	75	-	-	75	-	MHz
OUTPUT CHARACTERISTICS $A_V = +2$, (Note 4) Unless Otherwise Specified										
Output Voltage	$A_V = -1$	A	25	±3.0	±3.3	-	±3.0	±3.3	-	V
		A	Full	±2.5	±3.0	-	±2.5	±3.0	-	V
Output Current	$R_L = 50\Omega$, $A_V = -1$	A	25, 85	±40	±55	-	±40	±55	-	mA
		A	-40	±35	±50	-	±35	±50	-	mA
DC Closed Loop Output Resistance (Note 3)		B	25	-	0.09	-	-	0.09	-	Ω
2nd Harmonic Distortion (Note 3)	10MHz, $V_{OUT} = 2V_{P-P}$	B	25	-	-53	-	-	-53	-	dBc
	20MHz, $V_{OUT} = 2V_{P-P}$	B	25	-	-47	-	-	-47	-	dBc
3rd Harmonic Distortion (Note 3)	10MHz, $V_{OUT} = 2V_{P-P}$	B	25	-	-66	-	-	-66	-	dBc
	20MHz, $V_{OUT} = 2V_{P-P}$	B	25	-	-60	-	-	-60	-	dBc
TRANSIENT CHARACTERISTICS $A_V = +2$, (Note 4) Unless Otherwise Specified										
Rise and Fall Times	$V_{OUT} = 0.5V_{P-P}$	B	25	-	1.1	-	-	1.1	-	ns
Overshoot	$V_{OUT} = 0.5V_{P-P}$	B	25	-	12	-	-	11	-	%
Slew Rate ($V_{OUT} = 5V_{P-P}$ at $A_V = +2, -1$; $V_{OUT} = 4V_{P-P}$ at $A_V = +1$)	$A_V = -1$	B	25	-	1700	-	-	1650	-	V/µs
	$A_V = +1$	B	25	-	290	-	-	270	-	V/µs
	$A_V = +2$	B	25	-	535	-	-	510	-	V/µs
Settling Time ($V_{OUT} = 2V$ to $0V$, Note 3)	To 0.1%	B	25	-	30	-	-	38	-	ns
	To 0.05%	B	25	-	40	-	-	50	-	ns
	To 0.01%	B	25	-	70	-	-	75	-	ns
Overdrive Recovery Time	$V_{IN} = \pm2V$	B	25	-	7	-	-	7	-	ns
VIDEO CHARACTERISTICS $A_V = +2$, (Note 4) Unless Otherwise Specified										
Differential Gain	NTSC, $R_L = 150\Omega$	B	25	-	0.02	-	-	0.02	-	%
	NTSC, $R_L = 75\Omega$	B	25	-	0.02	-	-	0.02	-	%
Differential Phase	NTSC, $R_L = 150\Omega$	B	25	-	0.06	-	-	0.06	-	Degrees
	NTSC, $R_L = 75\Omega$	B	25	-	0.12	-	-	0.12	-	Degrees
POWER SUPPLY CHARACTERISTICS										
Power Supply Range	Note 5	B	Full	±2.25	-	±5.5	±2.25	-	±5.5	V
Power Supply Current (Note 3)		A	Full	-	5.5	8	-	5.5	8	mA

NOTES:

2. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.

3. See Typical Performance Curves for more information.

4. The feedback resistor value depends on closed loop gain and package type. See the "Optimum Feedback Resistor" table in the Application Information section for values used for characterization.

5. The minimum supply voltage entry is a typical value.

Application Information

Relevant Application Notes

The following Application Notes pertain to the HFA1155:

- AN9787-An Intuitive Approach to Understanding Current Feedback Amplifiers

- AN9420-Current Feedback Amplifier Theory and Applications

- AN9663-Converting from Voltage Feedback to Current Feedback Amplifiers

- AN9897-Operating the HFA1155 from 5V Single Supply

These publications may be obtained from Intersil's web site (www.intersil.com) or via our AnswerFax system.

Performance Differences Between Packages

The HFA1155 is a high frequency current feedback amplifier. As such, it is sensitive to parasitic capacitances which influence the amplifier's operation. The different parasitic capacitances of the SOIC and SOT-23 packages yield performance differences (notably bandwidth and bandwidth related parameters) between the two devices - see Electrical Specification tables for details.

Because of these performance differences, designers should evaluate and breadboard with the same package style to be used in production.

Note that some "Typical Performance Curves" have separate graphs for each package type. Graphs not labeled with a specific package type are applicable to both packages.

Optimum Feedback Resistor

The enclosed frequency response graphs detail the performance of the HFA1155 in various gains. Although the bandwidth dependency on A_{CL} isn't as severe as that of a voltage feedback amplifier, there is an appreciable decrease in bandwidth at higher gains. This decrease can be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and the R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1155 is optimized for $R_F = 715\Omega/604\Omega$ (SOIC/SOT-23), at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth. The table below lists recommended R_F values for various gains, and the expected bandwidth.

OPTIMUM FEEDBACK RESISTOR

A_{CL}	R_F (Ω) SOIC/SOT-23	BANDWIDTH (MHz) SOIC/SOT-23
-1	576/576	370/360
+1	453, ($+R_S = 348$)/ 453, ($+R_S = 221$)	370/365
+2	715/604	380/355
+5	402/475	300/300
+10	182/182	230/250

5V Single Supply Operation

This amplifier operates at single supply voltages down to 4.5V. The dramatic supply current reduction at this operating condition (refer also to Figure 25) makes this op amp an even better choice for low power 5V systems. Refer to Application Note AN9897 for further information.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 380MHz/355MHz (SOIC/SOT-23, $A_V = +2$). By decreasing R_S as C_L increases (as illustrated by the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth still decreases as the load capacitance increases. For example, at $A_V = +2$, $R_S = 30\Omega$, $C_L = 22pF$, the SOIC bandwidth is 290MHz, but the bandwidth drops to 90MHz at $A_V = +2$, $R_S = 6\Omega$, $C_L = 390pF$.
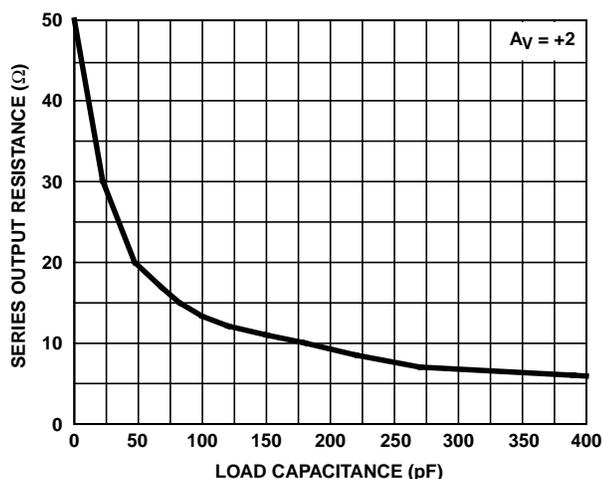
FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value chip (0.1μF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line, will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and eventual instability. To reduce this capacitance, remove the ground plane under traces connected to -IN and keep these traces as short as possible.

Examples of good high frequency layouts are the evaluation boards shown below.

Evaluation Boards

The performance of the HFA1155IB (SOIC) may be evaluated using the HFA11XX Evaluation Board and a SOIC to DIP adaptor like the Aries Electronics Part Number 08-350000-10. The SOT-23 version can be evaluated using the OPAMPSOT23EVAL board.

Note that the feedback and gain setting resistors on both boards must be changed to the appropriate values listed in the "Optimum Feedback Resistor" table.

To order evaluation boards (part number HFA11XXEVAL or OPAMPSOT23EVAL), please contact your local sales office.

The schematic and layout of the HFA11XXEVAL and OPAMPSOT23EVAL boards are shown below.
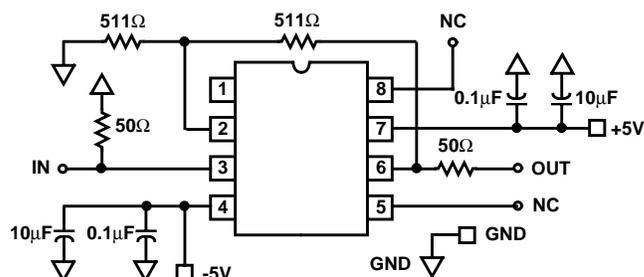
FIGURE 2. HFA11XXEVAL SCHEMATIC

HFA11XXEVAL TOP LAYOUT
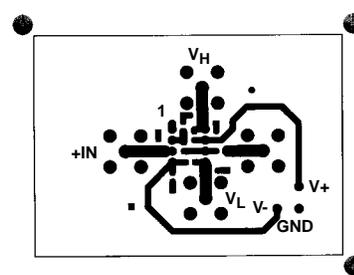
HFA11XXEVAL BOTTOM LAYOUT
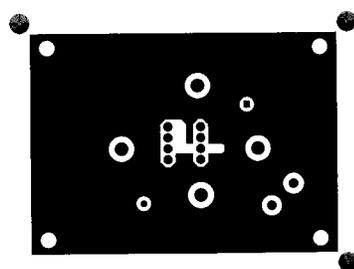
OPAMPSOT23EVAL TOP LAYOUT
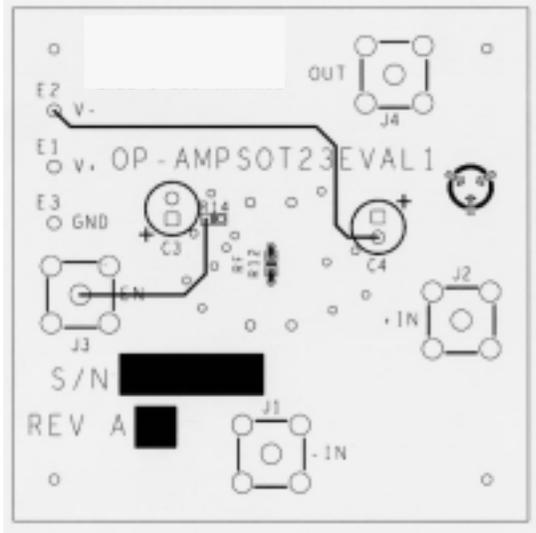
OPAMPSOT23EVAL GND LAYOUT
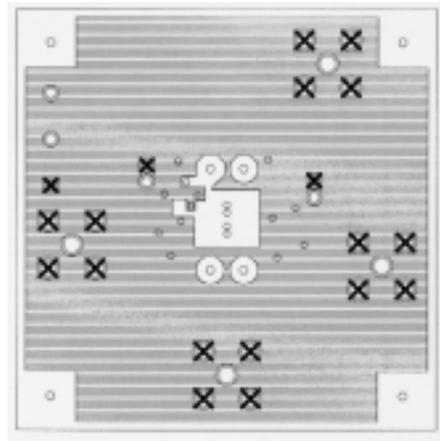
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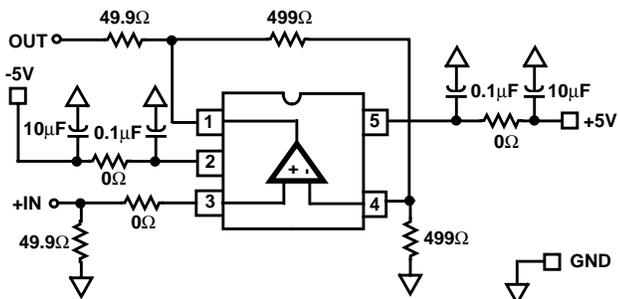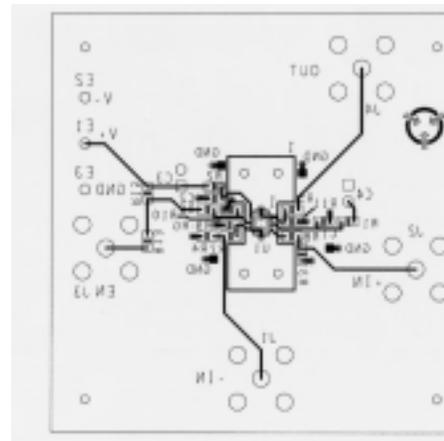
FIGURE 3. OPAMPSOT23EVAL SCHEMATIC

Typical Performance Curves

$V_{SUPPLY} = \pm 5V$, R_F = Value From the "Optimum Feedback Resistor" Table, $T_A = 25^{\circ}C$, $R_L = 100\Omega$, Unless Otherwise Specified
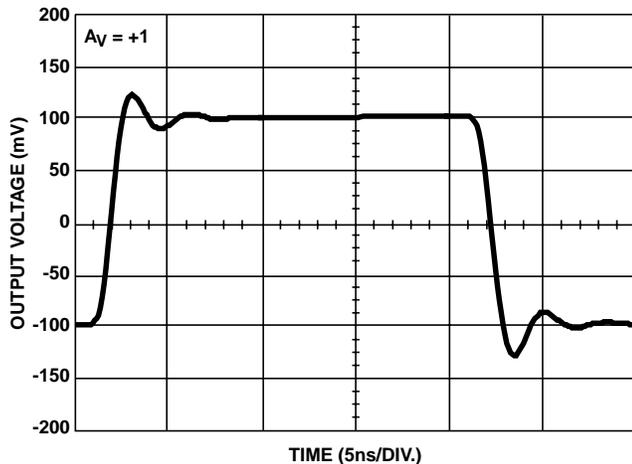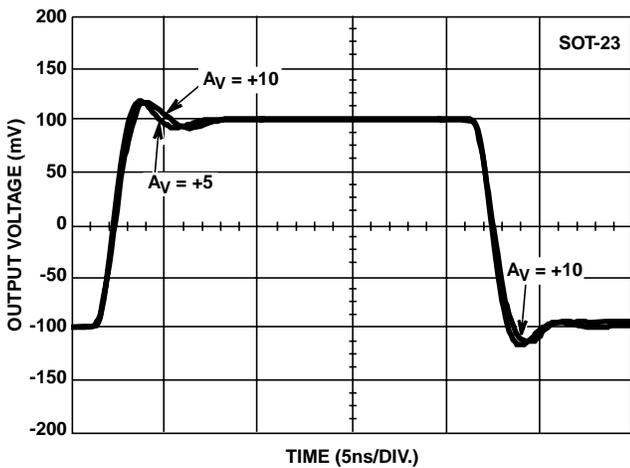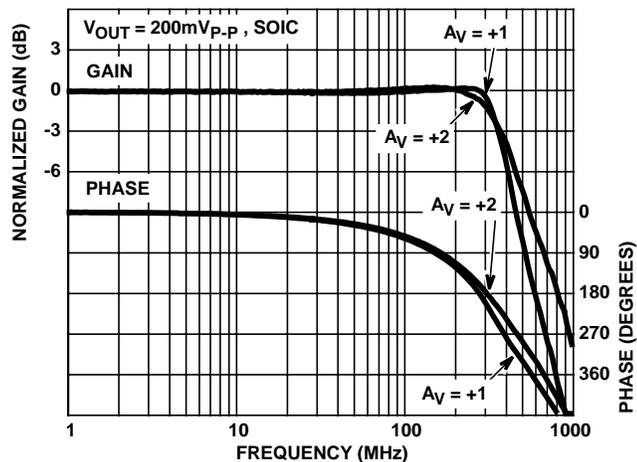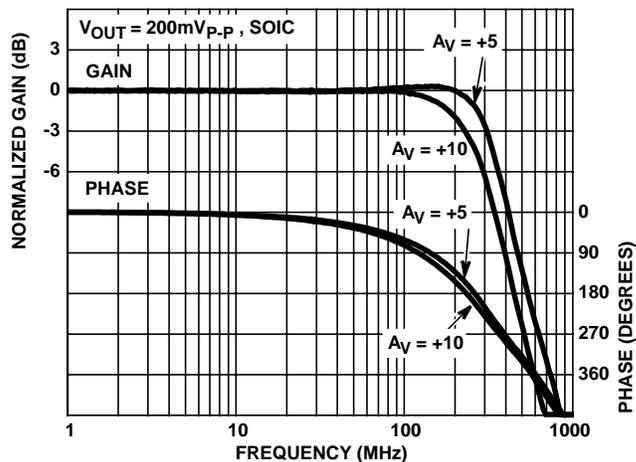
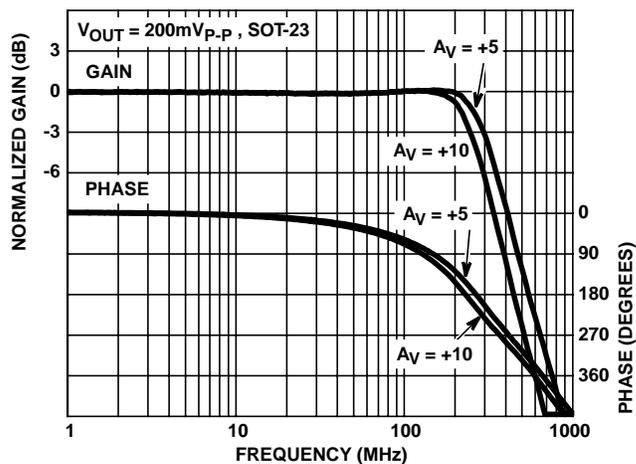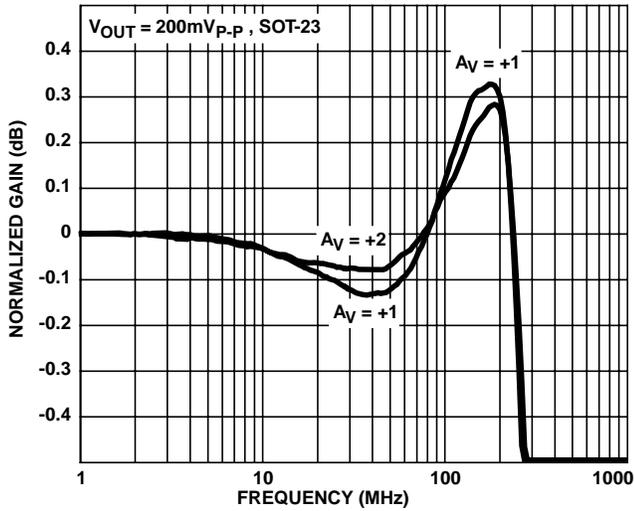**FIGURE 4. SMALL SIGNAL PULSE RESPONSE**
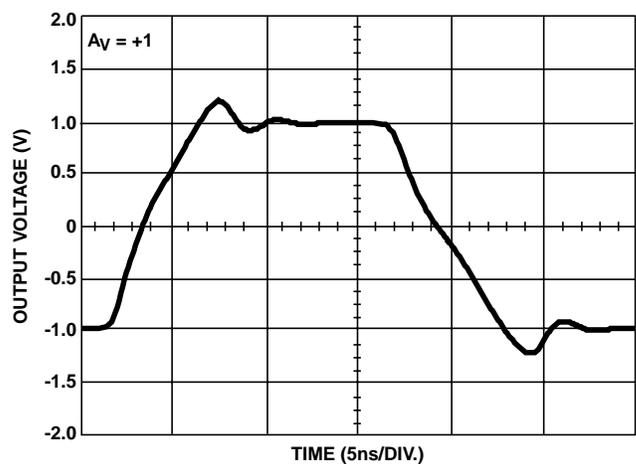
FIGURE 5. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, R_F = Value From the "Optimum Feedback Resistor" Table, $T_A = 25^{\circ}C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**
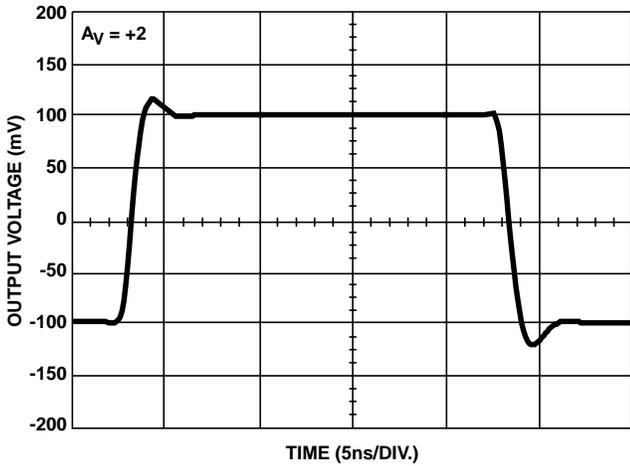
FIGURE 6. SMALL SIGNAL PULSE RESPONSE
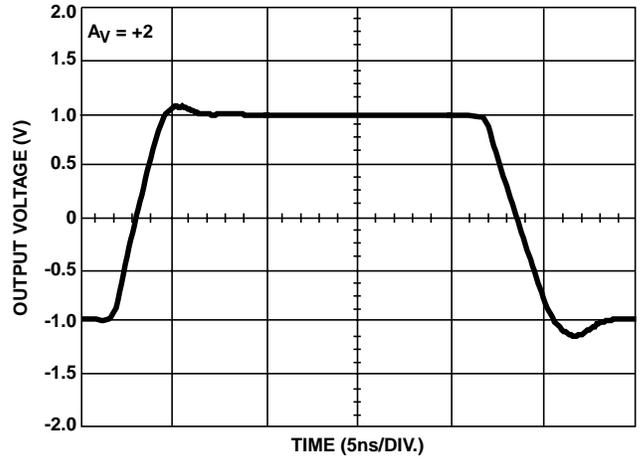
FIGURE 7. LARGE SIGNAL PULSE RESPONSE
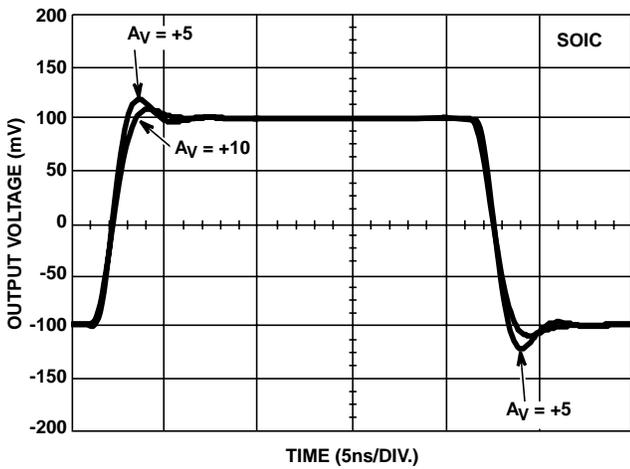
FIGURE 8. SMALL SIGNAL PULSE RESPONSE
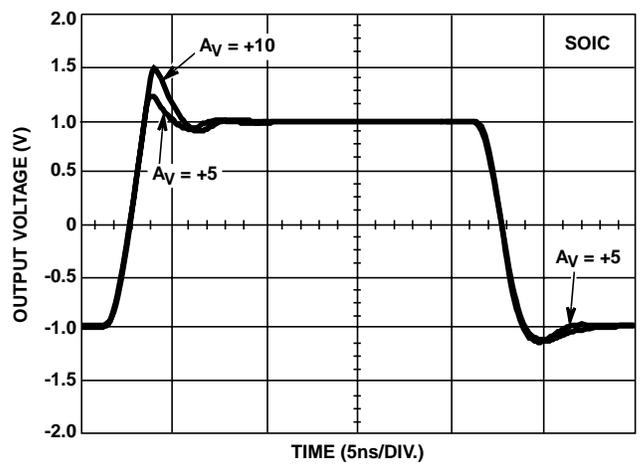
FIGURE 9. LARGE SIGNAL PULSE RESPONSE

FIGURE 10. SMALL SIGNAL PULSE RESPONSE
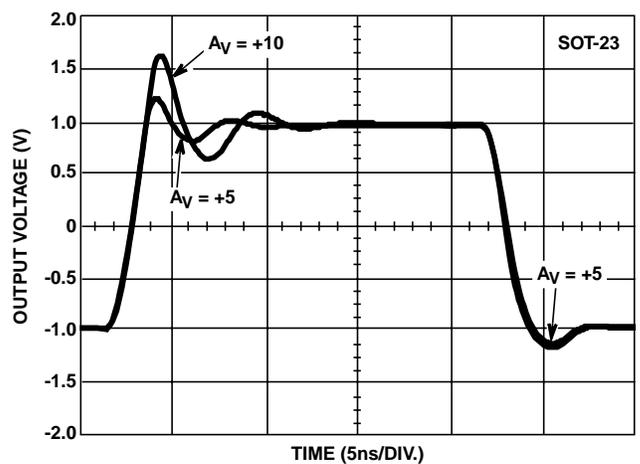
FIGURE 11. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, R_F = Value From the "Optimum Feedback Resistor" Table, $T_A = 25^{\circ}C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

FIGURE 12. FREQUENCY RESPONSE

FIGURE 13. FREQUENCY RESPONSE
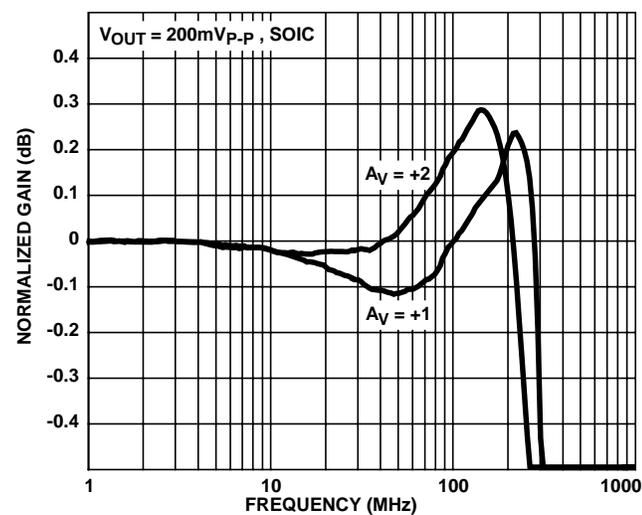
FIGURE 14. GAIN FLATNESS
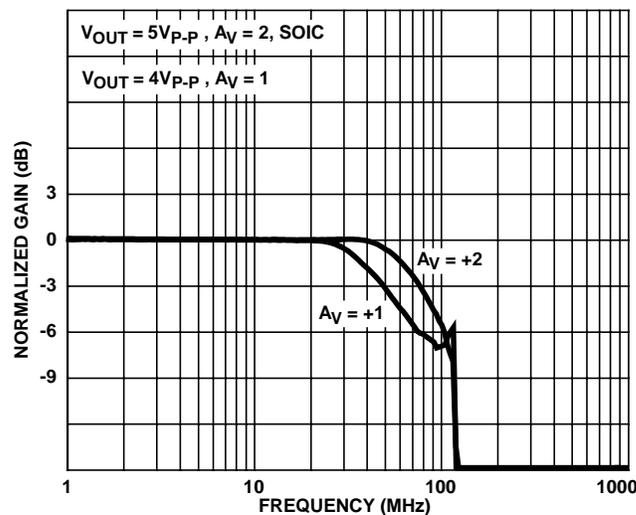
FIGURE 15. FULL POWER BANDWIDTH
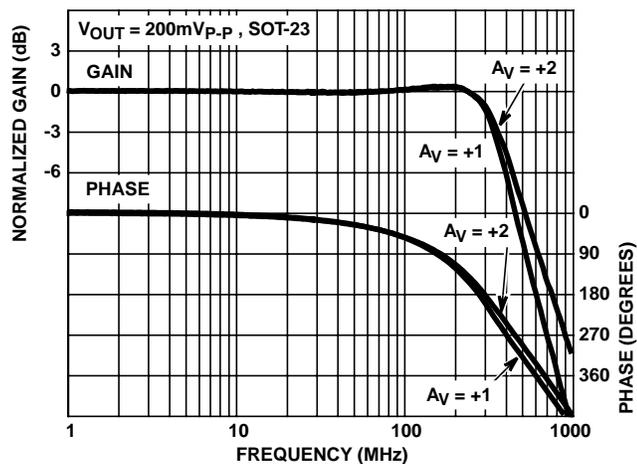
FIGURE 16. FREQUENCY RESPONSE

FIGURE 17. FREQUENCY RESPONSE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, R_F = Value From the "Optimum Feedback Resistor" Table, $T_A = 25^{\circ}C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

FIGURE 18. GAIN FLATNESS
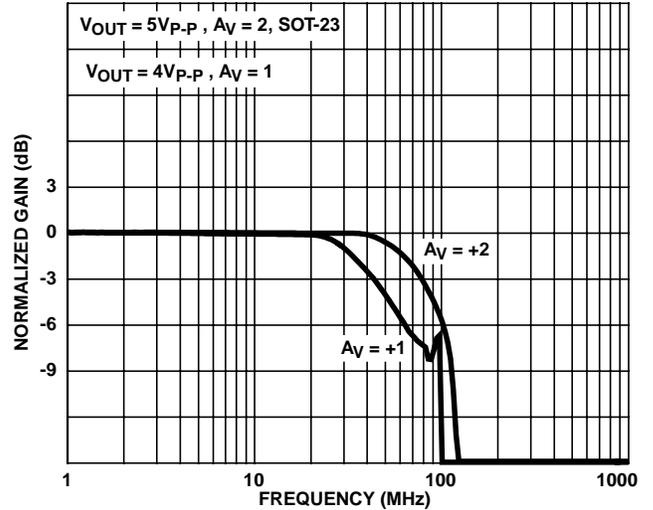
FIGURE 19. FULL POWER BANDWIDTH
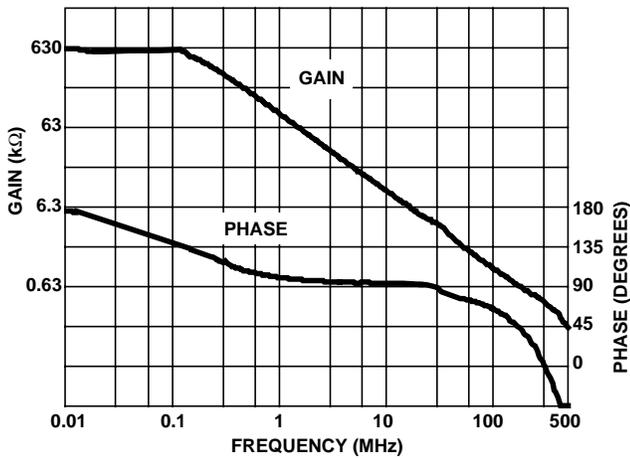
FIGURE 20. OPEN LOOP TRANSIMPEDANCE
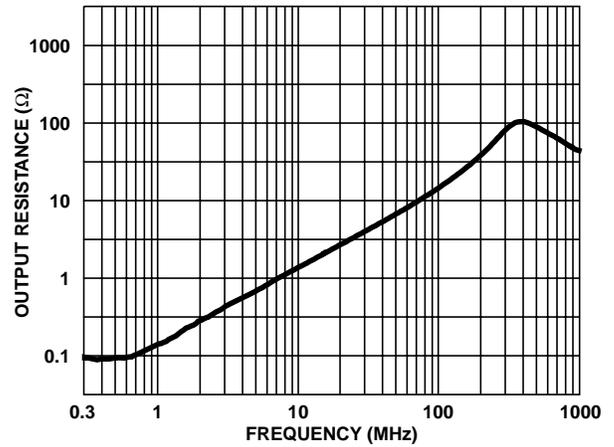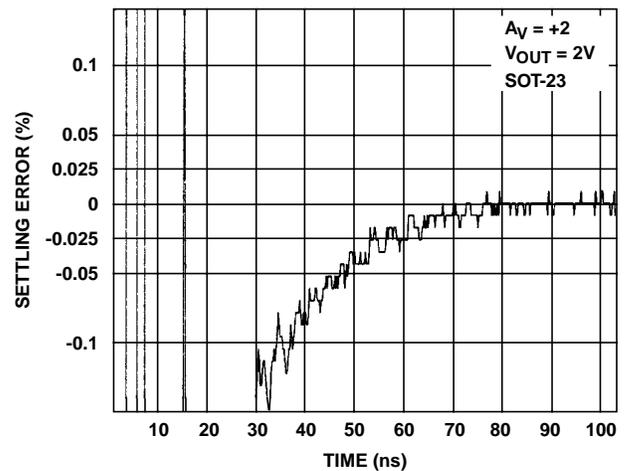

FIGURE 21. CLOSED LOOP OUTPUT RESISTANCE
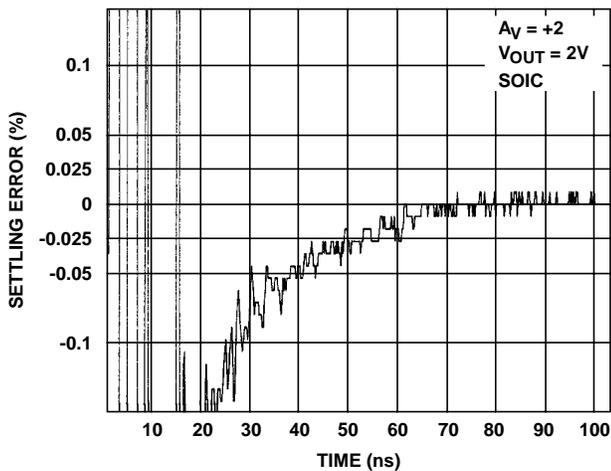
FIGURE 22. SETTLING RESPONSE

FIGURE 23. SETTLING RESPONSE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, R_F = Value From the "Optimum Feedback Resistor" Table, $T_A = 25^{O}C$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**
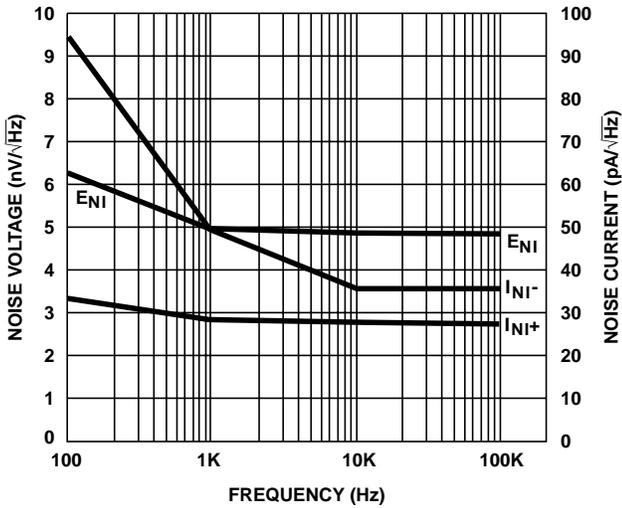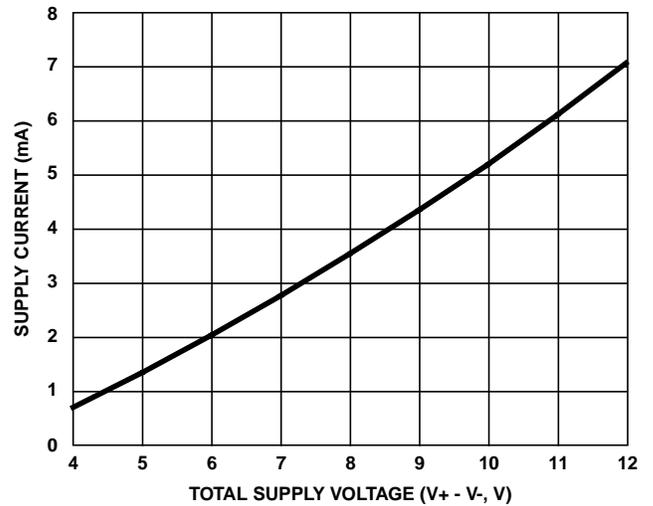
FIGURE 24. INPUT NOISE vs FREQUENCY
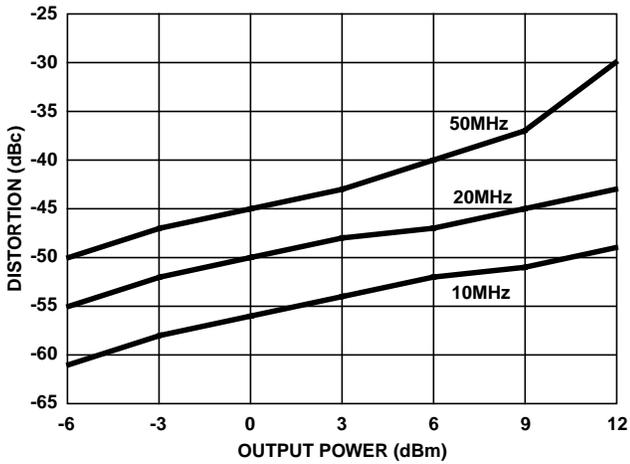
FIGURE 25. SUPPLY CURRENT vs SUPPLY VOLTAGE

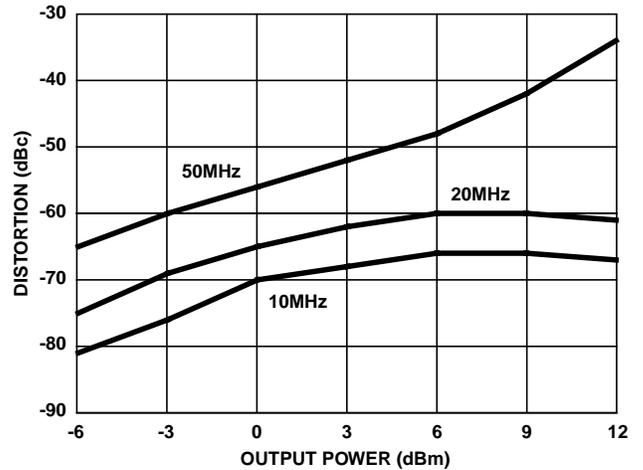**FIGURE 26. 2nd HARMONIC DISTORTION vs P_{OUT}**

FIGURE 27. 3rd HARMONIC DISTORTION vs P_{OUT}

Die Characteristics

DIE DIMENSIONS:

53 mils x 25mils
1350µm x 630µm

METALLIZATION:

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

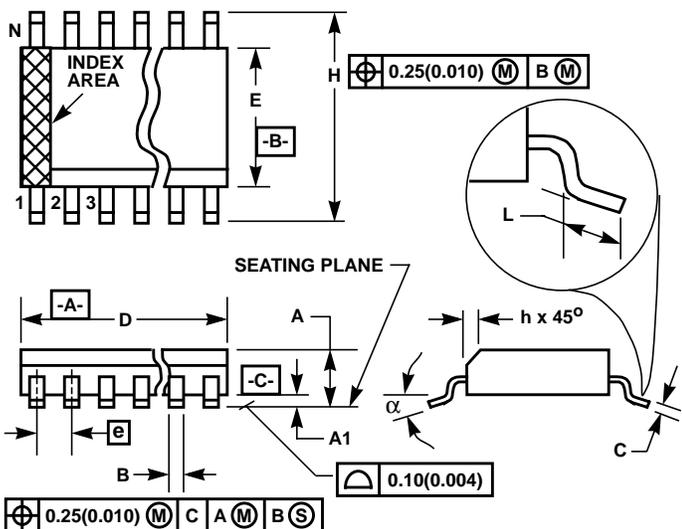**TRANSISTOR COUNT:**

40

SUBSTRATE POTENTIAL (POWERED UP):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1155

V+   OUT

V-

-IN   +IN

Small Outline Plastic Packages (SOIC)

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

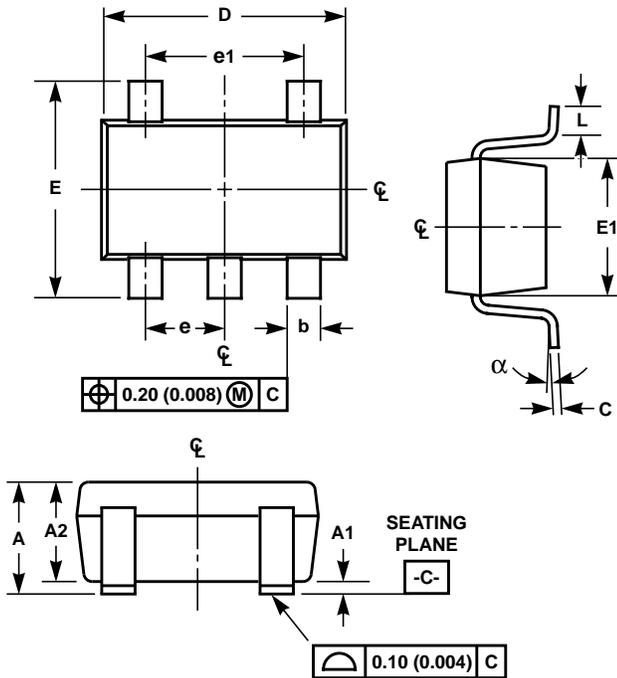| SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).

10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Transistor Plastic Packages (SOT23-5)

P5.064
5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.036	0.057	0.90	1.45	-
A1	0.000	0.0059	0.00	0.15	-
A2	0.036	0.051	0.90	1.30	-
b	0.0138	0.0196	0.35	0.50	-
C	0.0036	0.0078	0.09	0.20	-
D	0.111	0.118	2.80	3.00	3
E	0.103	0.118	2.60	3.00	-
E1	0.060	0.068	1.50	1.75	3
e	0.0374 Ref		0.95 Ref		-
e1	0.0748 Ref		1.90 Ref		-
L	0.004	0.023	0.10	0.60	4, 5
N	5		5		6
α	0°	10°	0°	10°	-

Rev. 0 10/98

NOTES:

1. Dimensioning and tolerances per ANSI 14.5M-1982.

2. Package conforms to EIAJ SC-74A (1992).

3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.

4. Footlength L measured at reference to seating plane.

5. "L" is the length of flat foot surface for soldering to substrate.

6. "N" is the number of terminal positions.

7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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