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Tachyon TL
33 MHz PCI to Fibre Channel Controller

Technical Data

HPFC-5100C

Features

- **Second Generation Controller IC, Based on TACHYON Family Architecture**
- **Supports All Fibre Channel Topologies; Arbitrated Loop (FC-AL) and N_Port Fabric Attachment**
- **Supports Both Class 3 and Class 2 (via Software)**
- **33 MHz, 32/64-Bit PCI Interface**
- **1 Gigabit/Second Fibre Channel Rate**
- **Full Duplex Support with Parallel Inbound and Outbound Processing**
- **32/64-Bit PCI Interface, Compliant to PCI v2.1**
- **Complete Hardware Handling of Entire SCSI I/O via FCP On-Chip Assists**
- **Full Initiator and Target Mode Functionality**

Applications

- **Motherboard Integration**
- **Host-Based Adapters**
- **Storage Sub-systems**
- **I_2O Designs**

Description

The HPFC-5100C, Tachyon TL, is a second-generation controller that leverages extensive experience in Fibre Channel, established with the original TACHYON controller. Tachyon TL carries forward the assurance of interoperability and true Fibre Channel performance.

Tachyon TL focuses on mass storage applications for any topology that require Class 3 and 2 (via software) and SCSI upper layer protocol handling. Coupled with a high performance 33 MHz, 32/64-bit PCI bus interface, Tachyon TL provides a cost-effective, high-performance mass storage solution.

TACHYON Architecture

Tachyon TL continues with the TACHYON architecture, a complete hardware-based state machine design. This architecture does not require an additional on-board microprocessor and therefore avoids reduced performance issues relating to processor cycles per second and access time to firmware. Rather, the TACHYON architecture is designed to be a single chip Fibre Channel solution.

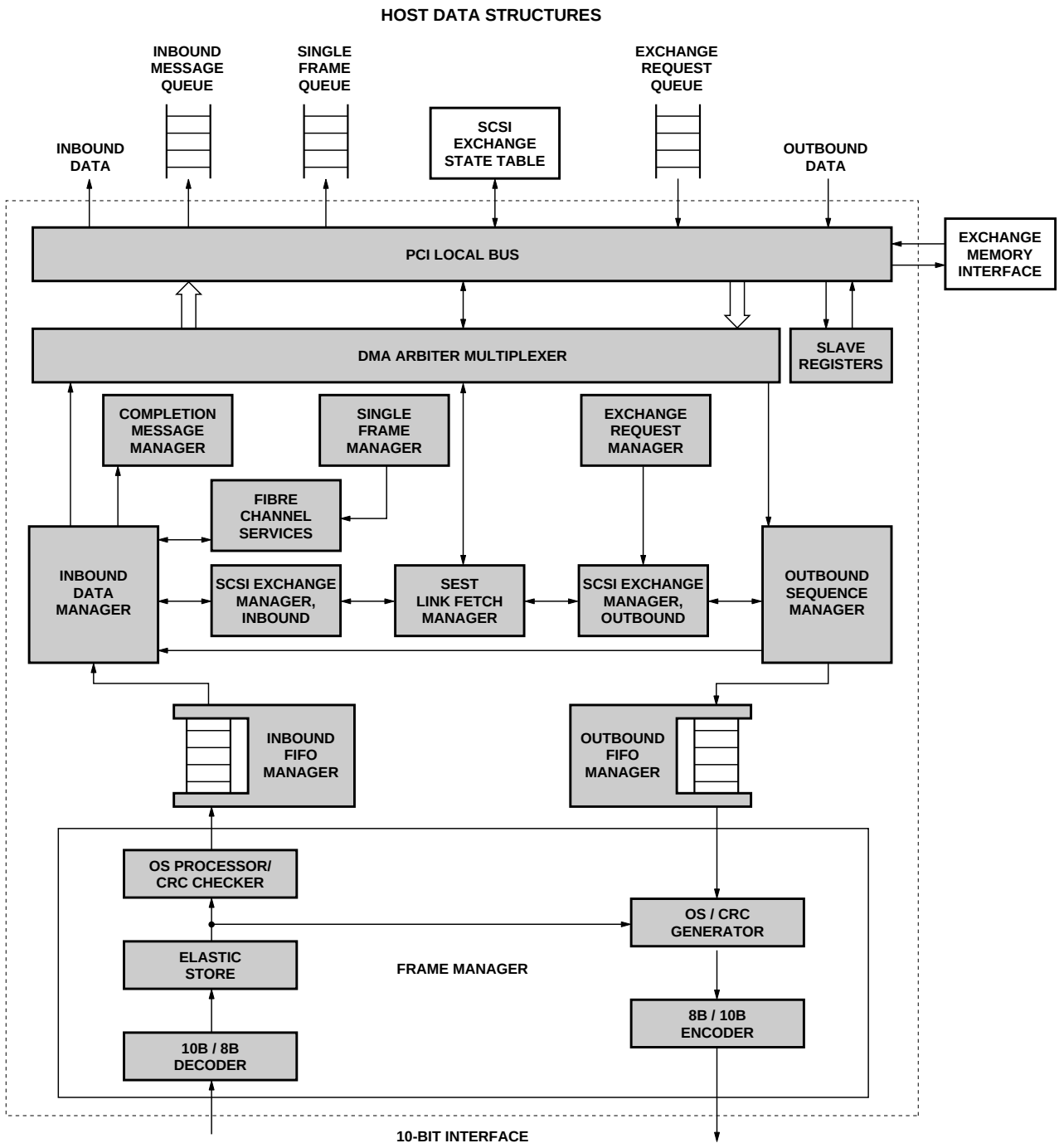
Tachyon TL provides the highest levels of concurrency via numerous independent functional blocks providing parallel processing of data, control, and commands. In addition, these blocks process at hardware speeds versus firmware speeds, and automate the entire SCSI I/O in hardware. The result is minimized latency and I/O overhead, coupled with the highest levels of parallelism to provide maximum I/O rates and bandwidth.

FC-AL Features

In addition to the high-performance architecture, Tachyon TL offers FC-AL-1 Fibre Channel features, such as Auto Status, multiple I/Os in the same loop arbitration cycle, loop map, loop broadcast, and loop directed reset. These features allow the designer to achieve higher performance in an arbitrated loop topology.

Physical Layer

The physical layer interface is the popular 10-bit wide specification that allows interfacing to a low-cost serializer/deserializer (SerDes) IC. This is the same physical layer interface that is popular on Fibre Channel disk drives today due to its quality gigabit signaling, small form factor, and low cost.



HPFC-5100C Block Diagram.

Tachyon TL Specifications

Fibre Channel Operation	
Fibre Channel Rate	1 Gbit/sec, 100 MBytes/sec, each direction w/full duplex support
Frame Payload Size	Up to 1024 bytes
Topology	Arbitrated Loop, Public & Private, and N_Port Fabric attachment
Classes of Operation	Class 3 and Class 2 (via software)
Upper Layer Protocol	FCP – On-chip automation for complete SCSI I/O
Loop Initialization	Completely hardware-based for high availability
Arbitrated Loop Capabilities	Loop map, loop-directed reset, loop broadcast, loop port bypass
Buffer-to-Buffer Credit	Four via on-chip buffers
Physical Layer Interface	10-bit Interface
Link Diagnostics	Link status indicators, internal/external loopback, user-definable signal pins
Compliance	FC-PH, FC-AL, FC-AL2, FC-PLDA, FC-FLA, FCP, 10-bit profile
Fibre Channel Protocol (FCP) for SCSI Features	
SCSI I/O	Complete hardware-based management and processing of entire I/O on chip, including multiple data phases
Initiator & Target Mode	Yes, simultaneously
Maximum # of Concurrent I/Os	32,768
I/O Request Queue	Up to 8,000 commands
Interrupts per I/O	1 or less
Arbitration Avoidance Techniques	Status and chained commands to same AL_PA sent in same loop tenancy
Error Recovery	Simplified error notification and recovery
Addressability	Byte-level addressability on all data buffers, inbound and outbound
PCI	
	Intended compliance for future Revision 2.2
DMA Channels	6
Width and Rate	32-bit or 64-bit selectable; 16 to 33 MHz. Operation to 0 MHz guaranteed by design.
Burst Transfer Rate	132 or 264 Mbytes/second, guaranteed for length of frame, inbound and outbound (at 64-bit, 33 MHz)
Dual Address Cycle Support	Yes
Voltage	3.3 V, 5 V tolerant
External Sub-system ID Support	Yes
Additional PCI Features	Zero wait state multiple cache line bursting capable up to full frame size, configurable latency timer, 32-byte cache line, Boot BIOS capable
Advanced Configuration and Power Interface	Yes, D0 and D3 power management states supported
Tachyon TL Architectural Features	
Complete Hardware-Based Design	Numerous independent functional blocks concurrently processing inbound data, outbound data, control and commands in hardware Six DMA channels Automation of complete I/O on-chip in hardware Results in lowest latency and I/O overhead and highest levels of parallelism

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Tachyon TL Specifications, continued

Command & Data Management	
Context Switching	16-entry on-chip cache for low latency context save and restore, as well as extensive pipelining techniques
Reduced PCI Control Overhead	Through the use of local memory option
Full Duplex Support	Yes, independent inbound and outbound FIFOs with automatic hardware management of buffer-to-buffer credit
Full Scatter/Gather List Support	Yes, with support for local and extended Scatter/Gather lists for unlimited “chaining” of Length/Address pairs
DMA Channels	6 to optimize concurrency and PCI utilization
Parity Protection	All data paths at byte level
Optional External Memory Interface	
Interface	32-bit @ 33 MHz for 132 MBytes/second
Memory Supported	128 K or 256 K bytes of synchronous static RAM for optional low latency control access Flash and ROM support for Boot BIOS and Subsystem Vendor ID
Parity Protection	No
Test & Debug	
JTAG	Yes
Full Internal Scan	Yes, IEEE Standard 1149.1 Boundary Scan
Hardware Debug Capability	Yes
Link Status Indicators	Yes
User Definable Signal Pins	Link up/down, low-speed serial interface or custom
Packaging	
Package	272-pin Enhanced Plastic Ball Grid Array (PBGA+)

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