

Supertex inc.

HV6810

10-Channel Serial-Input Latched Display Driver

Ordering Information

Device	Package Options			
	18-Pin Plastic DIP	20-Pin Small Outline Package	20-Pin Plastic Chip Carrier	Die
HV6810	HV6810P	HV6810WG	HV6810PJ	HV6810X

*For Hi-Rel process flow, refer to page 5-3 of the Databook.

Features

- High output voltage 80V
- High speed 5MHz @ 5V_{DD}
- Low power I_{BB} ≤ 0.1mA (All high)
- Active pull down 100µA min
- Output source current 100mA at 60V V_{PP}
- Each device drives 10 lines
- High-speed serially-shifted data input
- 5V CMOS-compatible inputs
- Latches on all driver outputs
- Pin-compatible improved replacement for UCN5810A and TL4810A, TL4810B

General Description

The HV6810 is a monolithic integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). These devices feature a serial data output to cascade additional devices for large displays.

A 10-bit data word is serially loaded into the shift register on the positive-going transition of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high and is latched when the latch enable is low. When the blanking input is high, all outputs are low.

Outputs are structures formed by double-diffused MOS (DMOS) transistors with output voltage ratings of 80 volts and 25 milliamperes source-current capability. All inputs are compatible with CMOS levels.

Absolute Maximum Ratings¹

Logic supply voltage, V _{DD} ²	7.5V
Driver supply voltage, V _{BB} ²	90V
Output voltage ²	90V
Input voltage ²	-0.3V to V _{DD} + 0.3V
Continuous total power dissipation at 25°C free-air temperature ³	18-Pin P-DIP ³ 900mW 20-Pin SOIC ⁴ 1000mW 20-Pin PLCC ⁴ 1000mW
Operating Temperature Range	-40° to +85°C

Notes:

1. Over operating free-air temperature.
2. All voltages are referenced to V_{SS}.
3. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.
4. For operation above 25°C ambient derate linearly to 85°C at 16.7mW/°C.



Electrical Characteristics

DC Characteristics ($V_{DD} = 5V \pm 10\%$, $V_{BB} = 60V$, $V_{SS} = 0$, $T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	High-level output voltage	Q outputs	57.5	58		V	$I_{OH} = 25mA$
		Serial output	4	4.5		V	$V_{DD} = 4.5V$, $I_{OH} = -100\mu A$
V_{OL}	Low-level output voltage	Q outputs		0.15	1	V	$I_{OH} = 100\mu A$, Blanking input at V_{DD}
		Serial output		0.05	0.1	V	$V_{DD} = 4.5V$, $I_{OL} = 100\mu A$
I_{OL}	Low-level Q output current (pull-down current)	60	80		μA	$T_A = \text{Max}$, $V_{OL} = 0.7V$	
$I_{O(OFF)}$	Off-state output current		-1	-15	μA	$V_O = 0$, Blanking input $T_A = \text{Max}$ at V_{DD}	
I_H	High-level input current			1	μA	$V_I = V_{DD}$	
I_{DD}	Supply current from V_{DD} (standby)		10	50	μA	All inputs at 0V, one Q output high	
			10	50	μA	All inputs at 0V, all Q outputs low	
I_{BB}	Supply current from V_{BB}		0.05	0.1	mA	All outputs low, all Q outputs open	
			0.05	0.1	mA	All outputs high, all Q outputs open	

* All typical values are at $T_A = 25^\circ C$, except for I_O .

AC Characteristics (Timing requirements over recommended operating conditions)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$t_{W(CKH)}$	Pulse duration, clock high	100			ns	
$t_{W(LEH)}$	Pulse duration, latch enable high	100			ns	
$t_{SU(D)}$	Setup time, data before clock	50			ns	
$t_{H(D)}$	Hold time, data after clock	50			ns	
$t_{CKH-LEH}$	Delay time, clock to latch enable high	50			ns	
t_{pd}^*	Propagation delay time, latch enable to output		0.3		μs	

* Switching characteristics, $V_{BB} = 60V$, $T_A = 25^\circ C$.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	
V_{DD}	Supply voltage	4.5		5.5	V	
V_{BB}	Supply voltage	20		80	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage (for $V_{DD} = 5V$)	3.5		5.3	V	
V_{IL}	Low-level input voltage	-0.3		0.8	V	
I_{OH}	Continuous high-level Q output current	-25			mA	
f_{CLK}	Clock frequency			5	MHz	
T_A	Operating free-air temperature	Plastic		-40	+85	$^\circ C$

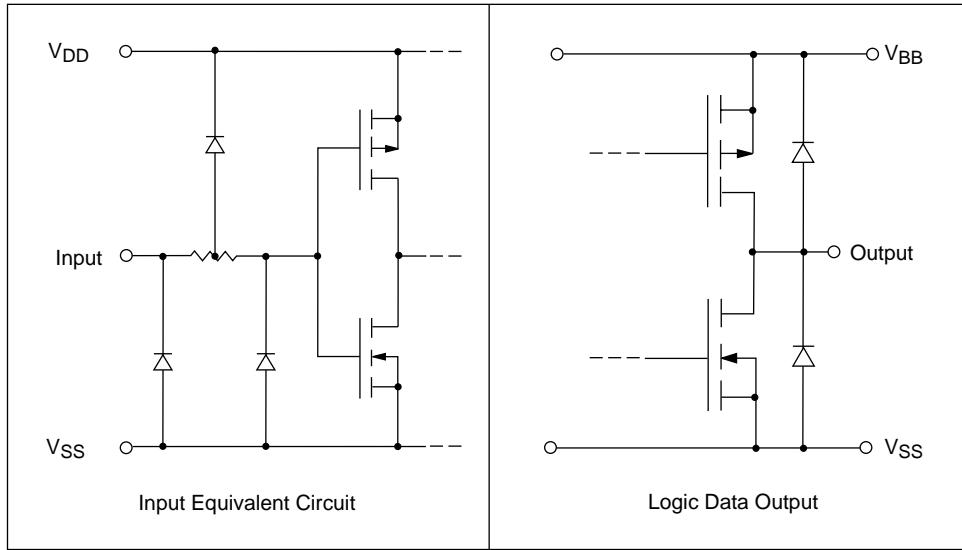
Note:

Power-up sequence should be the following:

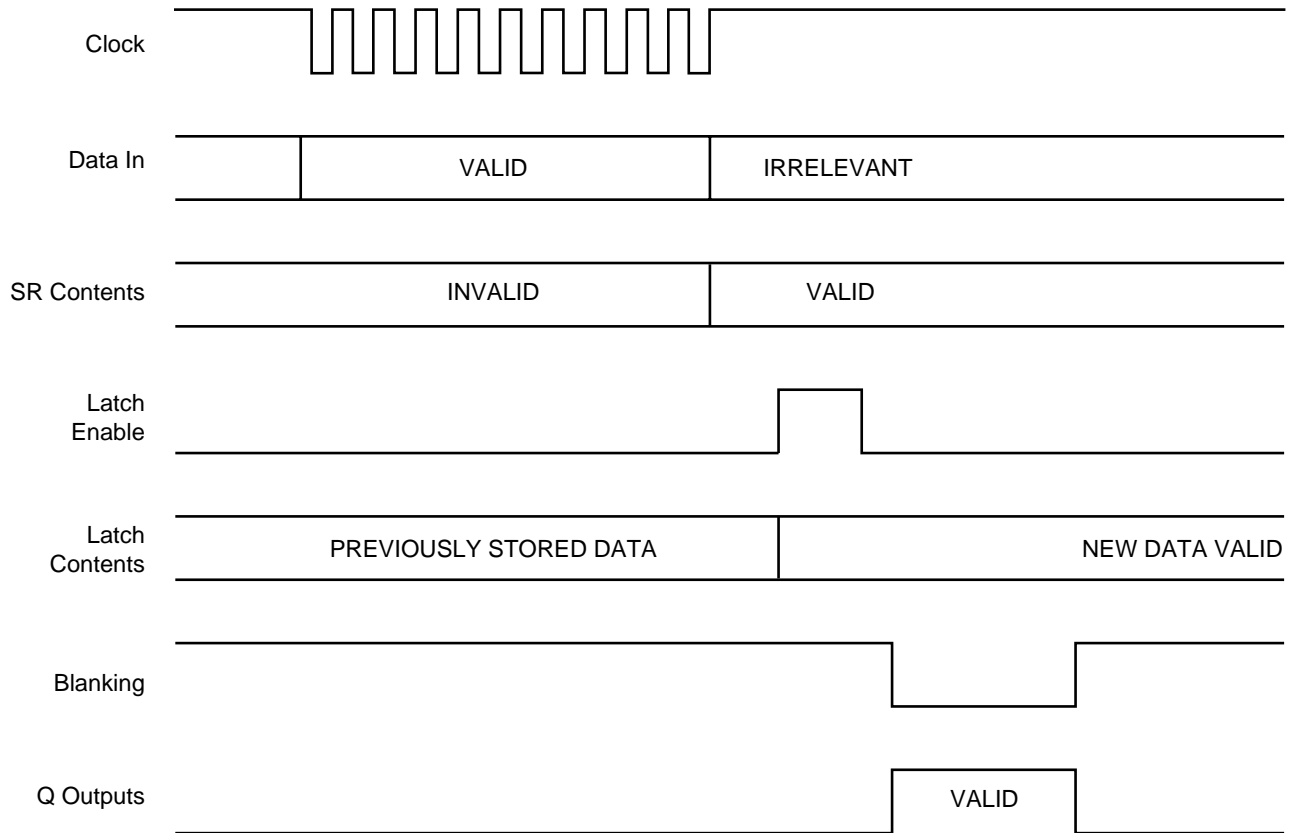
1. Connect ground.
2. Apply V_{DD} .
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP} .

Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits

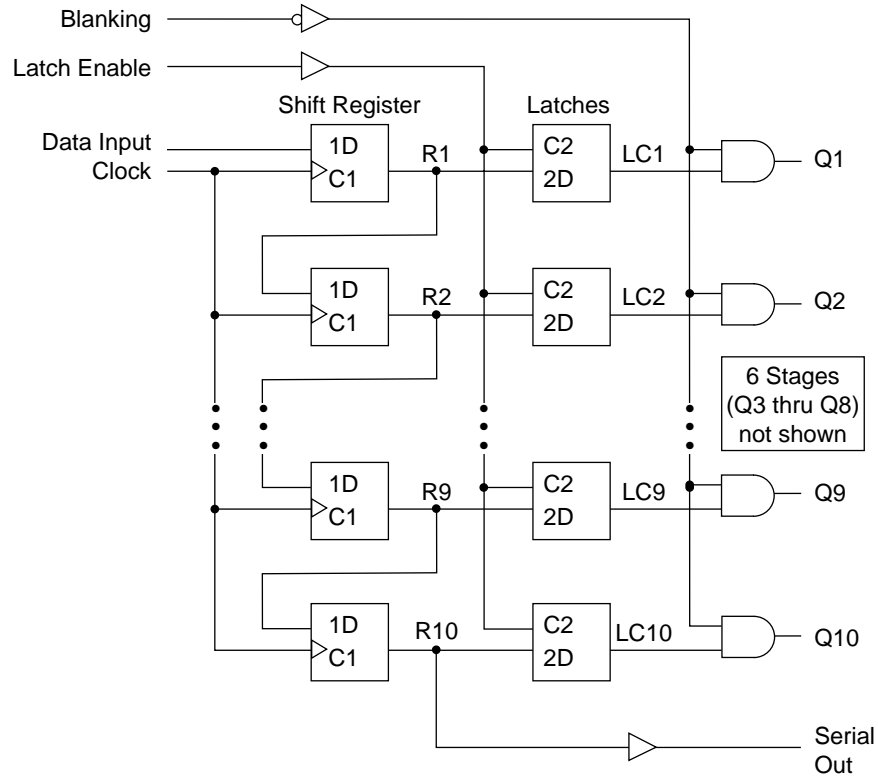


Timing Diagram



Functional Block Diagram

Logic Diagram (positive logic)

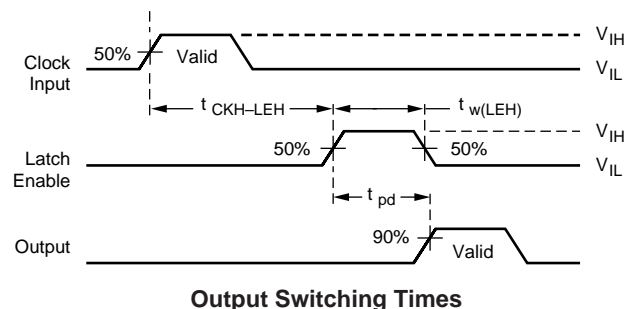
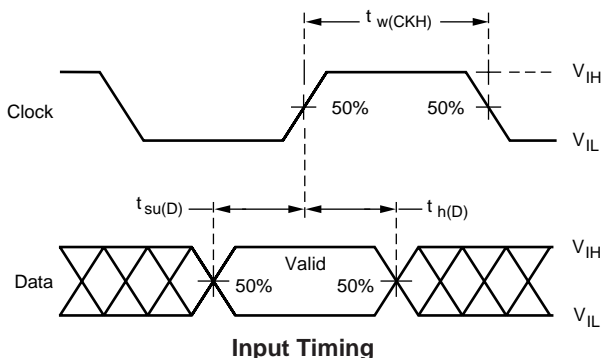


Function Table

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Blanking Input	Output Contents					
		I ₁	I ₂	I ₃	...	I _{N-1}	I _N			I ₁	I ₂	I ₃	...	I _{N-1}	I _N		I ₁	I ₂	I ₃	...	I _{N-1}	I _N
H		H	R ₁	R ₂	...	R _{N-2}	R _{N-1}	R _{N-1}														
L		L	R ₁	R ₂	...	R _{N-2}	R _{N-1}	R _{N-1}														
X		R ₁	R ₂	R ₃	...	R _{N-1}	R _N	R _N														
		X	X	X	...	X	X	X	L	R ₁	R ₂	R ₃	...	R _{N-1}	R _N							
		P ₁	P ₂	P ₃	...	P _{N-1}	P _N	P _N	H	P ₁	P ₂	P ₃	...	P _{N-1}	P _N	L						
										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low logic level
 H = High logic level
 X = Irrelevant
 P = Present state
 R = Previous state

Switching Waveforms



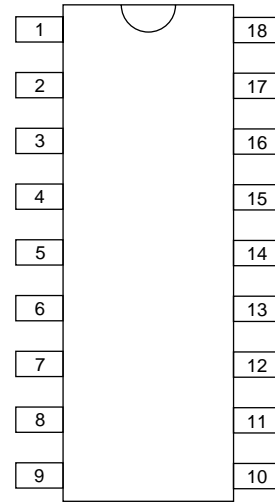
Pin Configurations

Package Outlines

HV6810

18-Pin DIP

Pin	Function	Pin	Function
1	Q8	10	Q3
2	Q7	11	Q2
3	Q6	12	Q1
4	Clock	13	Blanking
5	V _{SS}	14	Data in
6	V _{DD}	15	V _{BB}
7	LE (strobe)	16	Serial data out
8	Q5	17	Q10
9	Q4	18	Q9

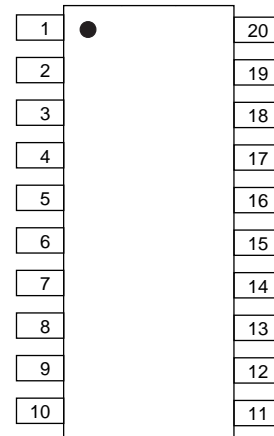


top view
18-pin DIP

HV6810

20-Pin SOW

Pin	Function	Pin	Function
1	Q8	11	Q3
2	Q7	12	Q2
3	Q6	13	Q1
4	Clock	14	Blanking
5	V _{SS}	15	Data in
6	N/C	16	V _{BB}
7	V _{DD}	17	Serial data out
8	LE (strobe)	18	N/C
9	Q5	19	Q10
10	Q4	20	Q9

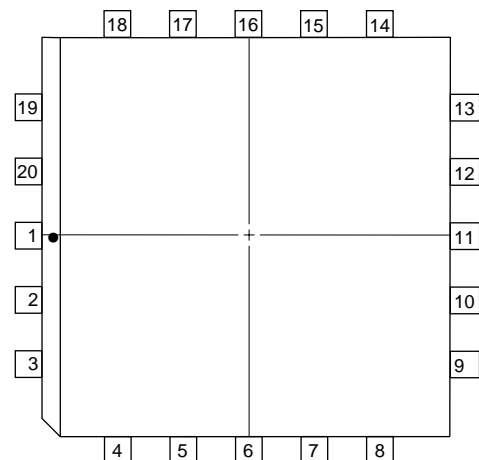


top view
SOW-20

HV6810

20-Pin Plastic PLCC

Pin	Function	Pin	Function
1	Q8	11	Q3
2	Q7	12	Q2
3	Q6	13	Q1
4	Clock	14	Blanking
5	N/C	15	Data In
6	V _{SS}	16	N/C
7	V _{DD}	17	V _{BB}
8	LE(Strobe)	18	Serial data out
9	Q5	19	Q10
10	Q4	20	Q9



top view
20-pin PLCC