

# HYUNDAI

## HY514400A Series

### 1M x 4-bit CMOS DRAM

#### DESCRIPTION

The HY514400A is the 2nd generation and fast dynamic RAM organized 1,048,576 x 4-bit. The HY514400A utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY514400A to be packaged in a standard 20/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of  $5V \pm 10\%$  tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

#### FEATURES

- Low power dissipation  
Max. battery back-up 2.2mW (L-part)  
Max. CMOS standby 1.1mW (L-part)  
5.5mW  
Max. TTL standby 11.0mW  
Max. operating

| Speed | Power   |
|-------|---------|
| 50    | 715.0mW |
| 60    | 632.5mW |
| 70    | 550.0mW |

- Single power supply of  $5V \pm 10\%$
- TTL compatible inputs and outputs
- Fast access and cycle time

| Speed | t <sub>RAC</sub> | t <sub>CAC</sub> | t <sub>PC</sub> |
|-------|------------------|------------------|-----------------|
| 50    | 50ns             | 15ns             | 35ns            |
| 60    | 60ns             | 15ns             | 40ns            |
| 70    | 70ns             | 20ns             | 45ns            |

- Fast page mode operation
- Multi-bit test capability
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh
- 1024 refresh cycles / 128ms (L-part)  
1024 refresh cycles / 16ms

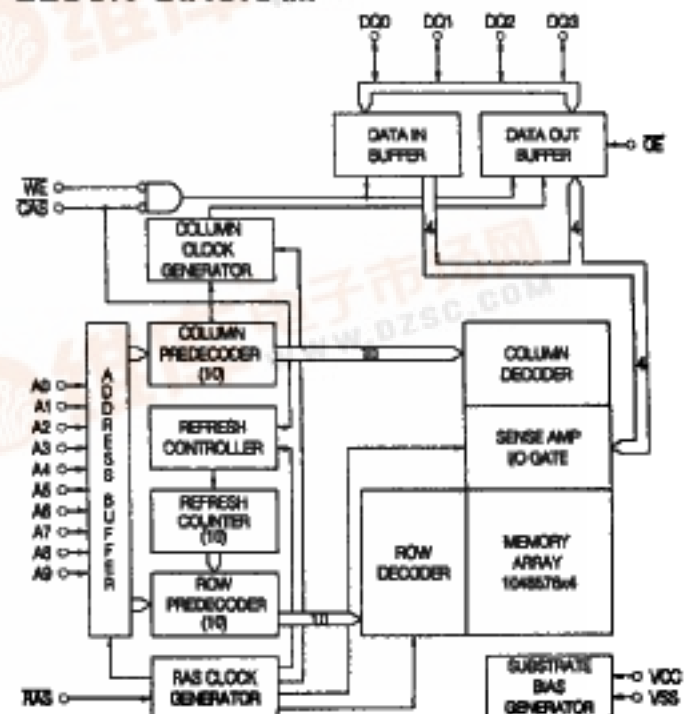
#### PIN DESCRIPTION

|         |                       |
|---------|-----------------------|
| RAS     | Row Address Strobe    |
| CAS     | Column Address Strobe |
| WE      | Write Enable          |
| OE      | Output Enable         |
| A0-A9   | Address Input         |
| DQ0-DQ3 | Data Input/Output     |
| Vcc     | Power (+5V)           |
| Vss     | Ground                |

#### PIN CONNECTION



#### BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATING**

| SYMBOL    | PARAMETER                          | RATING      | UNIT     |
|-----------|------------------------------------|-------------|----------|
| TA        | Ambient Temperature                | 0 to 70     | °C       |
| TSTG      | Storage Temperature                | -55 to 150  | °C       |
| VIN, VOUT | Voltage on Any Pin Relative to Vss | -1.0 to 7.0 | V        |
| VCC       | Voltage on VCC Relative to Vss     | -1.0 to 7.0 | V        |
| Ios       | Short Circuit Output Current       | 50          | mA       |
| Pd        | Power Dissipation                  | 0.90        | W        |
| TSOLDER   | Soldering Temperature • Time       | 260 • 10    | °C • sec |

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(TA = 0°C to 70°C)

| SYMBOL | PARAMETER          | MIN. | TYP. | MAX.    | UNIT |
|--------|--------------------|------|------|---------|------|
| VCC    | Supply Voltage     | 4.5  | 5.0  | 5.5     | V    |
| VIH    | Input High Voltage | 2.4  | -    | Vcc+1.0 | V    |
| VIL    | Input Low Voltage  | -1.0 | -    | 0.8     | V    |

NOTE: All voltage are referenced to Vss.

# DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5.0V±10%, VSS=0V, unless otherwise noted.)

| SYMBOL           | PARAMETER                                                           | TEST CONDITIONS                                                                                                                                                                            | SPEED/<br>POWER             | MIN. | MAX.     | UNIT | NOTE  |
|------------------|---------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|------|----------|------|-------|
| I <sub>I</sub>   | Input Leakage Current<br>(Any Input Pins)                           | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ 6.5V<br>All other pins not under test = V <sub>SS</sub>                                                                                                |                             | -10  | 10       | μA   |       |
| I <sub>LO</sub>  | Output Leakage Current<br>(High impedance State)                    | V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ 5.5V<br>RAS & CAS at V <sub>IH</sub>                                                                                                                  |                             | -10  | 10       | μA   |       |
| I <sub>CC1</sub> | V <sub>CC</sub> Supply Current,<br>Operating                        | t <sub>RC</sub> = t <sub>RC</sub> (min.)                                                                                                                                                   | 50                          | -    | 130      | mA   | 1,2,3 |
|                  |                                                                     |                                                                                                                                                                                            | 60                          | -    | 115      |      |       |
|                  |                                                                     |                                                                                                                                                                                            | 70                          | -    | 100      |      |       |
| I <sub>CC2</sub> | V <sub>CC</sub> Supply Current, TTL<br>Standby                      | RAS & CAS at V <sub>IH</sub> ,<br>other inputs ≥ V <sub>SS</sub>                                                                                                                           |                             | -    | 2        | mA   |       |
| I <sub>CC3</sub> | V <sub>CC</sub> Supply Current,<br>RAS-only refresh                 | t <sub>RC</sub> = t <sub>RC</sub> (min.)                                                                                                                                                   | 50                          | -    | 130      | mA   | 1,3   |
|                  |                                                                     |                                                                                                                                                                                            | 60                          | -    | 115      |      |       |
|                  |                                                                     |                                                                                                                                                                                            | 70                          | -    | 100      |      |       |
| I <sub>CC4</sub> | V <sub>CC</sub> Supply Current,<br>Fast Page mode                   | t <sub>PC</sub> = t <sub>PC</sub> (min.)                                                                                                                                                   | 50                          | -    | 80       | mA   | 1,2,3 |
|                  |                                                                     |                                                                                                                                                                                            | 60                          | -    | 70       |      |       |
|                  |                                                                     |                                                                                                                                                                                            | 70                          | -    | 60       |      |       |
| I <sub>CC5</sub> | V <sub>CC</sub> Supply Current,<br>CMOS Standby                     | RAS & CAS ≥ V <sub>CC</sub> -0.2V                                                                                                                                                          | L-Part                      | -    | 1<br>0.2 | mA   | 5     |
| I <sub>CC6</sub> | V <sub>CC</sub> Supply Current,<br>CAS-before- RAS<br>refresh       | t <sub>RC</sub> = t <sub>RC</sub> (min.)                                                                                                                                                   | 50                          | -    | 130      | mA   | 1,3   |
|                  |                                                                     |                                                                                                                                                                                            | 60                          | -    | 115      |      |       |
|                  |                                                                     |                                                                                                                                                                                            | 70                          | -    | 100      |      |       |
| I <sub>CC7</sub> | V <sub>CC</sub> Supply Current,<br>Battery Back up<br>(L-part only) | t <sub>RC</sub> = 125μs,<br>CAS = CBR cycling or<br>0.2V OE & WE =<br>V <sub>CC</sub> -0.2V,<br>A0-A9 = V <sub>CC</sub> -0.2V or 0.2V<br>DQ 0-DQ3 = 0.2V,<br>V <sub>CC</sub> -0.2V or open | t <sub>RAS</sub> ≤<br>300ns | -    | 300      | μA   | 1,4,5 |
|                  |                                                                     |                                                                                                                                                                                            | t <sub>RAS</sub> ≤<br>1μs   | -    | 400      |      |       |
| V <sub>OL</sub>  | Output Low Voltage                                                  | I <sub>OL</sub> = 4.2mA                                                                                                                                                                    |                             | -    | 0.4      | V    |       |
| V <sub>OH</sub>  | Output High Voltage                                                 | I <sub>OH</sub> = -5mA                                                                                                                                                                     |                             | 2.4  | -        | V    |       |

## NOTE :

- I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub>, I<sub>CC6</sub> and I<sub>CC7</sub> depend on cycle rate.
- I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> depend on output loading. Specified values are obtained with the output open.
- It depends on user whether column address is changed or not at least once while RAS=V<sub>IL</sub> and CAS=V<sub>IH</sub>.
- Only t<sub>RAS</sub>(max.) = 1μs is applied to refresh of battery backup but t<sub>RAS</sub>(max.) = 10μs is applied to normal functional operation .
- I<sub>CC5</sub>(max.) = 0.2mA and I<sub>CC7</sub> are applied to L-parts only (HY514400ALJ, HY514400ALT and HY514400ALR).

**AC CHARACTERISTICS**

(TA=0°C to 70°C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted.) NOTE1,2,3,13

| #  | SYMBOL | PARAMETER                                                         | HY514400AJ/AT/AR/ALJ/ALT/ALR |      |      |      |      |      | UNIT | NOTE   |
|----|--------|-------------------------------------------------------------------|------------------------------|------|------|------|------|------|------|--------|
|    |        |                                                                   | - 50                         |      | - 60 |      | - 70 |      |      |        |
|    |        |                                                                   | MIN.                         | MAX. | MIN. | MAX. | MIN. | MAX. |      |        |
| 1  | tRC    | Random Read or Write Cycle Time                                   | 90                           | -    | 110  | -    | 130  | -    | ns   |        |
| 2  | tRWC   | Read-Modify-Write Cycle Time                                      | 130                          | -    | 150  | -    | 180  | -    | ns   |        |
| 3  | tPC    | Fast Page Mode Cycle Time                                         | 35                           | -    | 40   | -    | 45   | -    | ns   |        |
| 4  | tPRWC  | Fast Page Mode Read-Modify-Write Cycle Time                       | 75                           | -    | 80   | -    | 95   | -    | ns   |        |
| 5  | tRAC   | Access Time from $\overline{\text{RAS}}$                          | -                            | 50   | -    | 60   | -    | 70   | ns   | 4,9,10 |
| 6  | tCAC   | Access Time from $\overline{\text{CAS}}$                          | -                            | 15   | -    | 15   | -    | 20   | ns   | 4,9    |
| 7  | tAA    | Access Time from Column Address                                   | -                            | 25   | -    | 30   | -    | 35   | ns   | 4,10   |
| 8  | tCPA   | Access Time from $\overline{\text{CAS}}$ Precharge                | -                            | 30   | -    | 35   | -    | 40   | ns   | 4,15   |
| 9  | tCLZ   | $\overline{\text{CAS}}$ to Output Low Impedance                   | 0                            | -    | 0    | -    | 0    | -    | ns   | 4      |
| 10 | tOFF   | Output Buffer Turn-off Delay                                      | 0                            | 15   | 0    | 15   | 0    | 20   | ns   | 5      |
| 11 | tT     | Transition Time (Rise and Fall)                                   | 3                            | 50   | 3    | 50   | 3    | 50   | ns   | 3      |
| 12 | tRP    | $\overline{\text{RAS}}$ Precharge Time                            | 30                           | -    | 40   | -    | 50   | -    | ns   |        |
| 13 | tRAS   | $\overline{\text{RAS}}$ Pulse Width                               | 50                           | 10K  | 60   | 10K  | 70   | 10K  | ns   |        |
| 14 | tRASP  | $\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)              | 50                           | 200K | 60   | 200K | 70   | 200K | ns   |        |
| 15 | tRSH   | $\overline{\text{RAS}}$ Hold Time                                 | 15                           | -    | 15   | -    | 20   | -    | ns   |        |
| 16 | tCSH   | $\overline{\text{CAS}}$ Hold Time                                 | 50                           | -    | 60   | -    | 70   | -    | ns   |        |
| 17 | tCAS   | $\overline{\text{CAS}}$ Pulse width                               | 15                           | 10K  | 15   | 10K  | 20   | 10K  | ns   |        |
| 18 | tRCD   | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay          | 15                           | 35   | 20   | 45   | 20   | 50   | ns   | 9      |
| 19 | tRAD   | $\overline{\text{RAS}}$ to Column Address Delay Time              | 10                           | 25   | 15   | 30   | 15   | 35   | ns   | 10     |
| 20 | tCRP   | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | 5                            | -    | 5    | -    | 5    | -    | ns   | 15     |
| 21 | tCP    | $\overline{\text{CAS}}$ Precharge Time                            | 10                           | -    | 10   | -    | 10   | -    | ns   | 17     |
| 22 | tASR   | Row Address Set-up Time                                           | 0                            | -    | 0    | -    | 0    | -    | ns   |        |
| 23 | tRAH   | Row Address Hold time                                             | 8                            | -    | 10   | -    | 10   | -    | ns   |        |
| 24 | tASC   | Column Address Set-up Time                                        | 0                            | -    | 0    | -    | 0    | -    | ns   | 14     |
| 25 | tCAH   | Column Address Hold Time                                          | 15                           | -    | 15   | -    | 15   | -    | ns   | 14     |
| 26 | tAR    | Column Address Hold Time from $\overline{\text{RAS}}$             | 45                           | -    | 50   | -    | 55   | -    | ns   |        |
| 27 | tRAL   | Column Address to $\overline{\text{RAS}}$ Lead Time               | 25                           | -    | 30   | -    | 35   | -    | ns   |        |
| 28 | tRCS   | Read Command Set-up Time                                          | 0                            | -    | 0    | -    | 0    | -    | ns   | 14     |
| 29 | tRCH   | Read Command Hold Time Referenced to $\overline{\text{CAS}}$      | 0                            | -    | 0    | -    | 0    | -    | ns   | 6,14   |
| 30 | tRRH   | Read Command Hold Time Referenced to $\overline{\text{RAS}}$      | 0                            | -    | 0    | -    | 0    | -    | ns   | 6      |
| 31 | tWCH   | Write Command Hold Time                                           | 10                           | -    | 15   | -    | 15   | -    | ns   | 14     |
| 32 | tWCR   | Write Command Hold Time from $\overline{\text{RAS}}$              | 40                           | -    | 50   | -    | 55   | -    | ns   |        |
| 33 | tWP    | Write Command Pulse Width                                         | 10                           | -    | 15   | -    | 15   | -    | ns   |        |
| 34 | tRWL   | Write Command to $\overline{\text{RAS}}$ Lead Time                | 15                           | -    | 15   | -    | 20   | -    | ns   |        |
| 35 | tCWL   | Write Command to $\overline{\text{CAS}}$ Lead Time                | 15                           | -    | 15   | -    | 20   | -    | ns   | 16     |
| 36 | tDS    | Data-In Set-up Time                                               | 0                            | -    | 0    | -    | 0    | -    | ns   | 7      |
| 37 | tDH    | Data-In Hold Time                                                 | 10                           | -    | 15   | -    | 15   | -    | ns   | 7      |
| 38 | tDHR   | Data-In Hold Time Referenced to $\overline{\text{RAS}}$           | 40                           | -    | 50   | -    | 55   | -    | ns   |        |
| 39 | tREF   | Refresh Period (1024 cycles)                                      | -                            | 16   | -    | 16   | -    | 16   | ms   | 12     |
|    |        | L-part                                                            | -                            | 128  | -    | 128  | -    | 128  | ms   | 11     |
| 40 | tWCS   | Write Command Set up Time                                         | 0                            | -    | 0    | -    | 0    | -    | ns   | 8,14   |

**AC CHARACTERISTICS**

(continued)

| #  | SYMBOL | PARAMETER                                    | HY514400AJ/AT/AR/ALJ/ALT/ALR |      |      |      |      |      | UNIT | NOTE |
|----|--------|----------------------------------------------|------------------------------|------|------|------|------|------|------|------|
|    |        |                                              | - 50                         |      | - 60 |      | - 70 |      |      |      |
|    |        |                                              | MIN.                         | MAX. | MIN. | MAX. | MIN. | MAX. |      |      |
| 41 | tCWD   | CAS to WE Delay Time                         | 35                           | -    | 35   | -    | 40   | -    | ns   | 8    |
| 42 | tRWD   | RAS to WE Delay Time                         | 70                           | -    | 80   | -    | 95   | -    | ns   | 8    |
| 43 | tAWD   | Column Address to WE Delay Time              | 45                           | -    | 50   | -    | 60   | -    | ns   | 8    |
| 44 | tCSR   | CAS Set-up Time (CBR Cycle)                  | 5                            | -    | 5    | -    | 5    | -    | ns   | 14   |
| 45 | tCHR   | CAS Hold Time (CBR Cycle)                    | 10                           | -    | 10   | -    | 10   | -    | ns   | 15   |
| 46 | tRPC   | RAS to CAS Precharge Time                    | 5                            | -    | 5    | -    | 5    | -    | ns   | 14   |
| 47 | tCPT   | CAS Precharge Time<br>(CBR Counter Test)     | 25                           | -    | 30   | -    | 35   | -    | ns   | 17   |
| 48 | tROH   | RAS Hold Time Referenced to OE               | 10                           | -    | 10   | -    | 10   | 20   | ns   |      |
| 49 | tOEA   | OE Access Time                               | -                            | 15   | -    | 15   | -    | 20   | ns   |      |
| 50 | tOED   | OE to Data Delay                             | 15                           | -    | 15   | -    | 20   | -    | ns   |      |
| 51 | tOEZ   | Output Buffer Turn Off Delay Time<br>from OE | 0                            | 15   | 0    | 15   | 0    | 20   | ns   | 5    |
| 52 | tOEH   | OE Command Hold Time                         | 15                           | -    | 15   | -    | 20   | -    | ns   |      |
| 53 | tCPWD  | WE Delay time from CAS Precharge             | 50                           | -    | 55   | -    | 65   | -    | ns   | 8    |
| 54 | tRHCP  | RAS Hold Time from CAS Precharge             | 30                           | -    | 35   | -    | 40   | -    | ns   |      |
| 55 | tWRP   | WE to RAS Precharge Time<br>(CBR Cycle)      | 10                           | -    | 10   | -    | 10   | -    | ns   |      |
| 56 | tWRH   | WE to RAS Hold Time (CBR Cycle)              | 10                           | -    | 10   | -    | 10   | -    | ns   |      |
| 57 | tWTS   | Write Command Set-up Time<br>(Test Mode In)  | 10                           | -    | 10   | -    | 10   | -    | ns   |      |
| 58 | tWTH   | Write Command Hold Time<br>(Test Mode In)    | 10                           | -    | 10   | -    | 10   | -    | ns   |      |

AC CHARACTERISTICS IN TEST MODE NOTE 18

| #  | SYMBOL | PARAMETER                                   | HY514400AJ/AT/AR/ALJ/ALT/ALR |      |      |      |      |      | UNIT | NOTE   |
|----|--------|---------------------------------------------|------------------------------|------|------|------|------|------|------|--------|
|    |        |                                             | - 50                         |      | - 60 |      | - 70 |      |      |        |
|    |        |                                             | MIN.                         | MAX. | MIN. | MAX. | MIN. | MAX. |      |        |
| 1  | tRC    | Random Read or Write Cycle Time             | 95                           | -    | 115  | -    | 135  | -    | ns   |        |
| 2  | tRWC   | Read-Modify-Write Cycle Time                | 135                          | -    | 155  | -    | 185  | -    | ns   |        |
| 3  | tPC    | Fast Page Mode Cycle Time                   | 40                           | -    | 45   | -    | 50   | -    | ns   |        |
| 4  | tPRWC  | Fast Page Mode Read-Modify-Write Cycle Time | 80                           | -    | 85   | -    | 100  | -    | ns   |        |
| 5  | tRAC   | Access Time from RAS                        | -                            | 55   | -    | 65   | -    | 75   | ns   | 4,9,10 |
| 6  | tCAC   | Access Time from CAS                        | -                            | 20   | -    | 20   | -    | 25   | ns   | 4,9    |
| 7  | tAA    | Access Time from Column Address             | -                            | 30   | -    | 35   | -    | 40   | ns   | 4,10   |
| 8  | tCPA   | Access Time from CAS Precharge              | -                            | 35   | -    | 40   | -    | 45   | ns   | 4      |
| 13 | tRAS   | RAS Pulse Width                             | 55                           | 10K  | 65   | 10K  | 75   | 10K  | ns   |        |
| 14 | tRASP  | RAS Pulse Width (Fast Page Mode)            | 55                           | 200K | 65   | 200K | 75   | 200K | ns   |        |
| 15 | tRSH   | RAS Hold Time                               | 20                           | -    | 20   | -    | 25   | -    | ns   |        |
| 16 | tCSH   | CAS Hold Time                               | 55                           | -    | 65   | -    | 75   | -    | ns   |        |
| 17 | tCAS   | CAS Pulse Width                             | 20                           | 10K  | 20   | 10K  | 25   | 10K  | ns   |        |
| 27 | tRAL   | Column Address to RAS Lead Time             | 30                           | -    | 35   | -    | 40   | -    | ns   |        |
| 41 | tCWD   | CAS to WE Delay Time                        | 40                           | -    | 40   | -    | 50   | -    | ns   | 8      |
| 42 | tRWD   | RAS to WE Dealy Time                        | 75                           | -    | 85   | -    | 100  | -    | ns   | 8      |
| 43 | tAWD   | Column Address to WE Delay Time             | 50                           | -    | 55   | -    | 65   | -    | ns   | 8      |
| 49 | tOEA   | OE Access Time                              | -                            | 20   | -    | 20   | -    | 25   | ns   |        |
| 50 | tOED   | OE to Data Delay                            | 20                           | -    | 20   | -    | 25   | -    | ns   |        |
| 52 | tOEH   | OE Command Hold Time                        | 20                           | -    | 20   | -    | 25   | -    | ns   |        |

**NOTE:**

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$ -only or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles before proper device operation is achieved.
2. If  $\overline{\text{RAS}}=\text{V}_{\text{SS}}$  during power-up, the HY514400A could begin an active cycle. These condition results in higher current than necessary current which is demanded from the power supply during power-up. It is recommended that  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  track with  $\text{V}_{\text{CC}}$  during power-up or be held at a valid  $\text{V}_{\text{IH}}$  in order to minimize the power-up current.
3.  $\text{V}_{\text{IH}}(\text{min.})$  and  $\text{V}_{\text{IL}}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $\text{V}_{\text{IH}}(\text{min.})$  and  $\text{V}_{\text{IL}}(\text{max.})$ , and are assumed to be 5ns for all inputs.
4. Measured at  $\text{V}_{\text{OH}}=2.4\text{V}$  and  $\text{V}_{\text{OL}}=0.4\text{V}$  with a load equivalent to 2 TTL loads and 100pF.
5.  $\text{t}_{\text{OFF}}(\text{max.})$  define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either  $\text{tr}_{\text{CH}}$  or  $\text{tr}_{\text{RH}}$  must be satisfied for a read cycle.
7. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in Read-Modify-Write cycles.
8.  $\text{tw}_{\text{CS}}$ ,  $\text{tr}_{\text{WD}}$ ,  $\text{tc}_{\text{WD}}$ ,  $\text{t}_{\text{AWD}}$  and  $\text{tc}_{\text{PWD}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $\text{tw}_{\text{CS}} \geq \text{tw}_{\text{CS}}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If  $\text{tr}_{\text{WD}} \geq \text{tr}_{\text{WD}}(\text{min.})$ ,  $\text{tc}_{\text{WD}} \geq \text{tc}_{\text{WD}}(\text{min.})$ ,  $\text{t}_{\text{AWD}} \geq \text{t}_{\text{AWD}}(\text{min.})$ , and  $\text{tc}_{\text{PWD}} \geq \text{tc}_{\text{PWD}}(\text{min.})$ , the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the  $\text{tr}_{\text{CD}}(\text{max.})$  limit insures that  $\text{tr}_{\text{AC}}(\text{max.})$  can be met.  $\text{tr}_{\text{CD}}(\text{max.})$  is specified as a reference point only. If  $\text{tr}_{\text{CD}}$  is greater than the specified  $\text{tr}_{\text{CD}}(\text{max.})$  limit, then access time is controlled by  $\text{tc}_{\text{AC}}$ .
10. Operation within the  $\text{tr}_{\text{AD}}(\text{max.})$  limit insures that  $\text{tr}_{\text{AC}}(\text{max.})$  can be met.  $\text{tr}_{\text{AD}}(\text{max.})$  is specified as a reference point only. If  $\text{tr}_{\text{AD}}$  is greater than the specified  $\text{tr}_{\text{AD}}(\text{max.})$  limit, then access time is controlled by  $\text{t}_{\text{AA}}$ .
11.  $\text{t}_{\text{REF}}(\text{max.})=128\text{ms}$  is applied to L-Parts(HY514400ALJ, HY514400ALT and HY514400ALR).
12. A burst of 1024  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles must be executed within 16ms(128ms for L-part) after exiting self refresh.
13. When  $\overline{\text{CAS}}$  goes low, 4-bits data are written into the device.
14. These parameters are determined by the earlier falling edge of  $\overline{\text{CAS}}$ .
15. These parameters are determined by the later rising edge of  $\overline{\text{CAS}}$ .
16.  $\text{tc}_{\text{WL}}$  must be satisfied by  $\overline{\text{CAS}}$  for 16-bits access cycles.
17.  $\text{tc}_{\text{P}}$  and  $\text{tc}_{\text{PT}}$  are measured when  $\overline{\text{CAS}}$  is high state.
18. These specifications are applied to the test Mode.

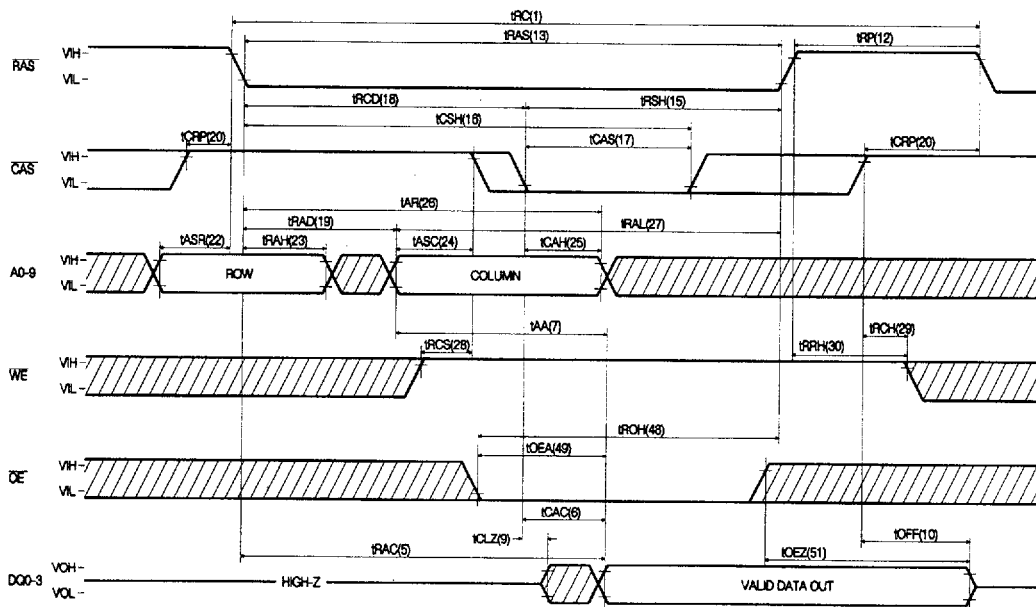
**CAPACITANCE**

( $\text{T}_{\text{A}}=25^{\circ}\text{C}$ ,  $\text{V}_{\text{CC}}=5\text{V} \pm 10\%$ ,  $\text{V}_{\text{SS}}=0\text{V}$ ,  $f=1\text{MHz}$ , unless otherwise noted.)

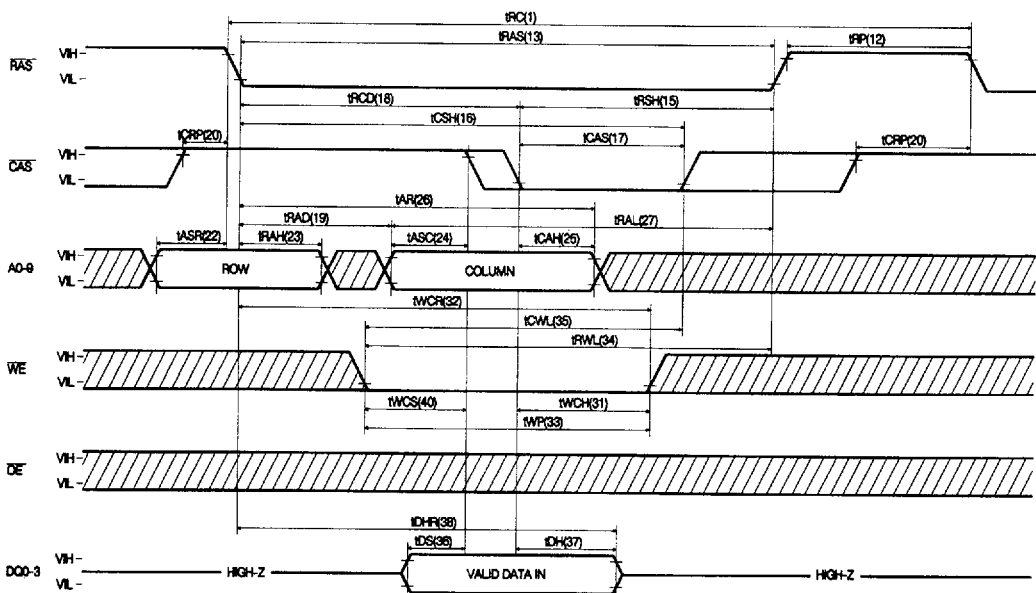
| SYMBOL | PARAMETER                               | TYP. | MAX. | UNIT |
|--------|-----------------------------------------|------|------|------|
| CIN1   | Input Capacitance (A0-A9)               | -    | 5    | pF   |
| CIN2   | Input Capacitance (RAS,CAS,WE, OE)      | -    | 7    | pF   |
| CDQ    | Data Input/Output Capacitance (DQ0-DQ3) | -    | 7    | pF   |

# TIMING DIAGRAM

## READ CYCLE



## EARLY WRITE CYCLE

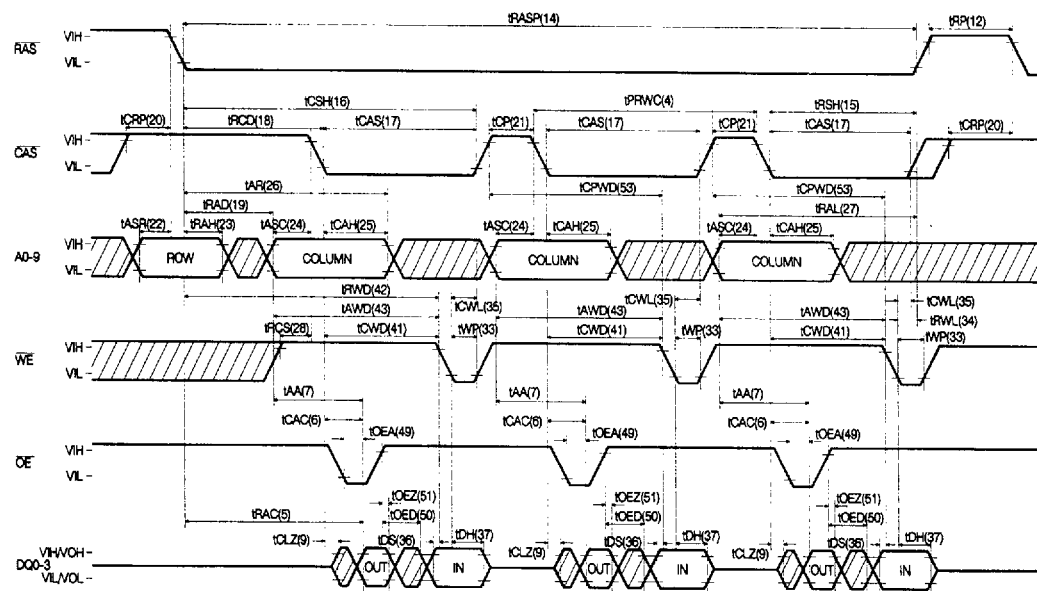


The timing diagram illustrates the relationship between several control and data signals for the 64K16020. The signals shown are RAS, CAS, A0-9, WE, OE, and DQ0-3. The diagram includes various timing parameters such as  $t_{RC}(1)$ ,  $t_{RCD}(18)$ ,  $t_{CSH}(16)$ ,  $t_{CAS}(17)$ ,  $t_{CRP}(20)$ ,  $t_{RAD}(19)$ ,  $t_{RAH}(23)$ ,  $t_{ASC}(24)$ ,  $t_{CAH}(25)$ ,  $t_{RAL}(27)$ ,  $t_{ASR}(22)$ ,  $t_{OVL}(35)$ ,  $t_{RML}(34)$ ,  $t_{WP}(33)$ ,  $t_{OEH}(32)$ ,  $t_{OE}(50)$ ,  $t_{DS}(36)$ ,  $t_{DH}(37)$ , and  $t_{IOED}(50)$ . The signals are shown as waveforms with high (VH) and low (VIL) levels, and the data bus DQ0-3 is shown as a bus with high-Z and valid data states.

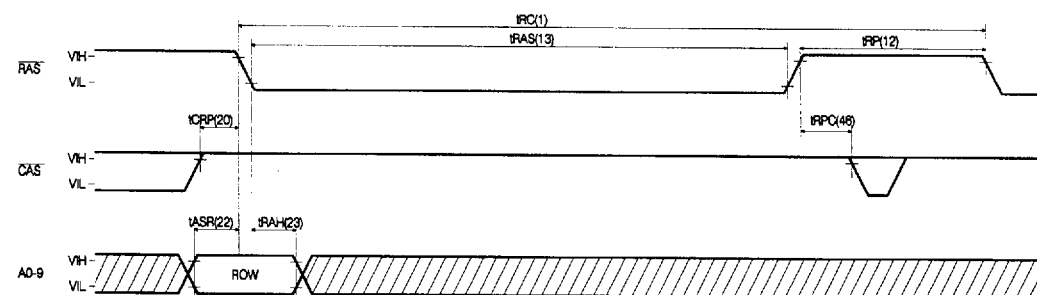
The timing diagram illustrates the relationship between the 64K1602 LCD module and the microcontroller. The signals and their timing parameters are as follows:

- RAS:** Row Address Strobe. Timing parameters include  $t_{RASP}(14)$  (high pulse),  $t_{ICRP}(20)$  (low pulse),  $t_{ICSH}(16)$  (high-to-low transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICP}(3)$  (low-to-high transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICRP}(20)$  (low pulse), and  $t_{ICP}(12)$  (high pulse).
- CAS:** Column Address Strobe. Timing parameters include  $t_{ICRP}(20)$  (low pulse),  $t_{ICSH}(16)$  (high-to-low transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICP}(3)$  (low-to-high transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICRP}(20)$  (low pulse), and  $t_{ICP}(12)$  (high pulse).
- A0-9:** Data/Address Bus. Timing parameters include  $t_{ICRP}(20)$  (low pulse),  $t_{ICSH}(16)$  (high-to-low transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICP}(3)$  (low-to-high transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICRP}(20)$  (low pulse), and  $t_{ICP}(12)$  (high pulse).
- WE:** Write Enable. Timing parameters include  $t_{ICRP}(20)$  (low pulse),  $t_{ICSH}(16)$  (high-to-low transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICP}(3)$  (low-to-high transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICRP}(20)$  (low pulse), and  $t_{ICP}(12)$  (high pulse).
- OE:** Output Enable. Timing parameters include  $t_{ICRP}(20)$  (low pulse),  $t_{ICSH}(16)$  (high-to-low transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICP}(3)$  (low-to-high transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICRP}(20)$  (low pulse), and  $t_{ICP}(12)$  (high pulse).
- DQ0-3:** Data Bus. Timing parameters include  $t_{ICRP}(20)$  (low pulse),  $t_{ICSH}(16)$  (high-to-low transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICP}(3)$  (low-to-high transition),  $t_{ICP}(21)$  (low-to-high transition),  $t_{ICAS}(17)$  (high-to-low transition),  $t_{ICRP}(20)$  (low pulse), and  $t_{ICP}(12)$  (high pulse).

**FAST PAGE MODE READ-MODIFY-WRITE CYCLE**

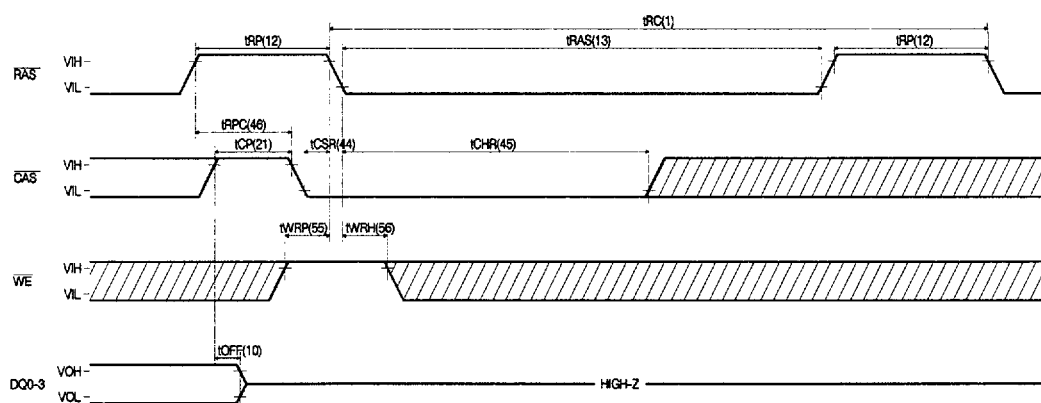


**RAS-ONLY REFRESH CYCLE**



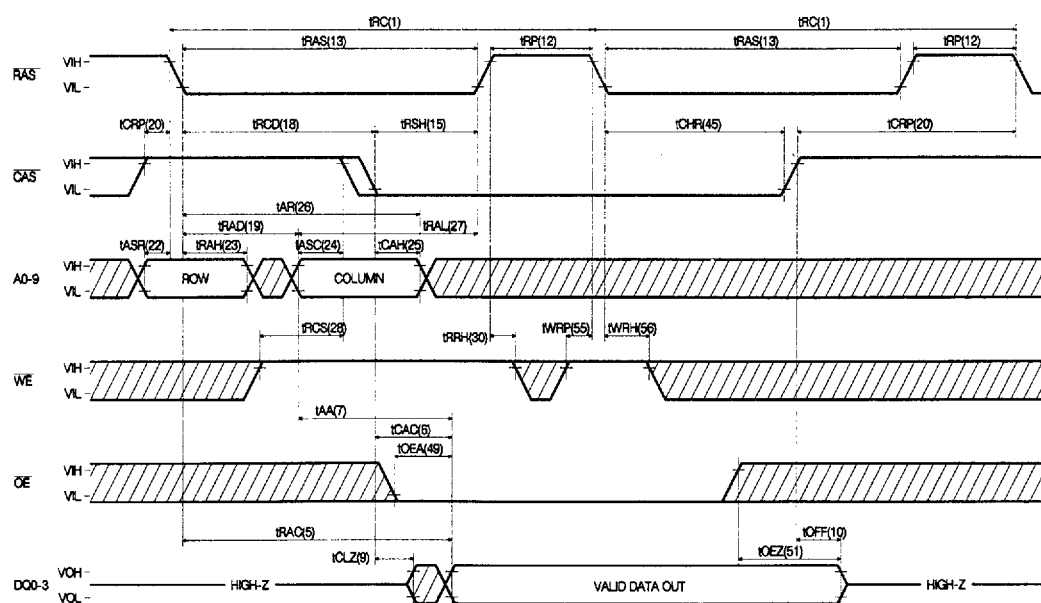
NOTE: A0-10 = "H" or "L"

**CAS-BEFORE-RAS REFRESH CYCLE**

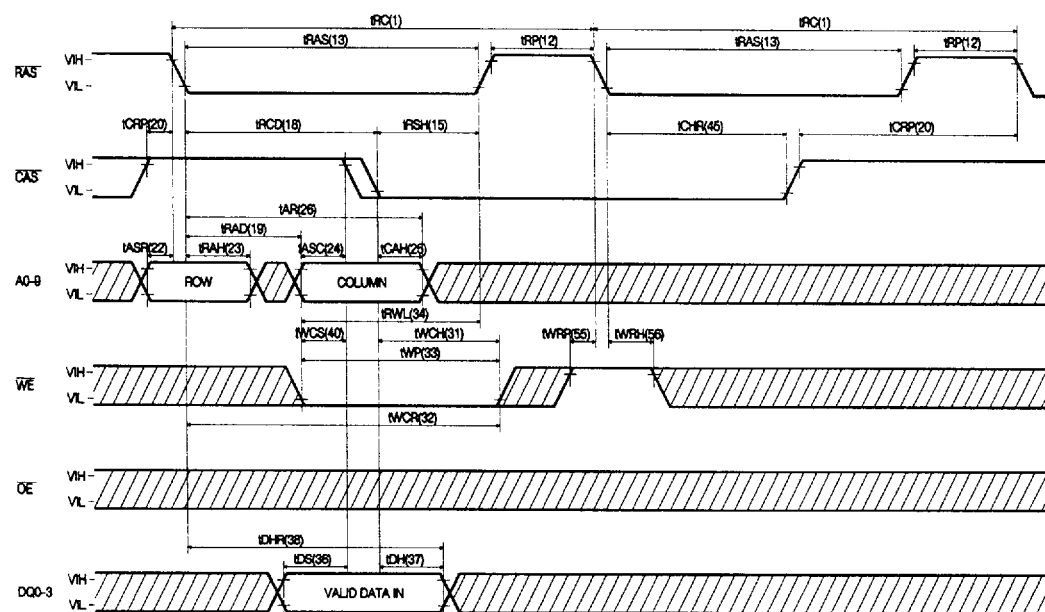


NOTE: A0-9 and OE="H" or "L"

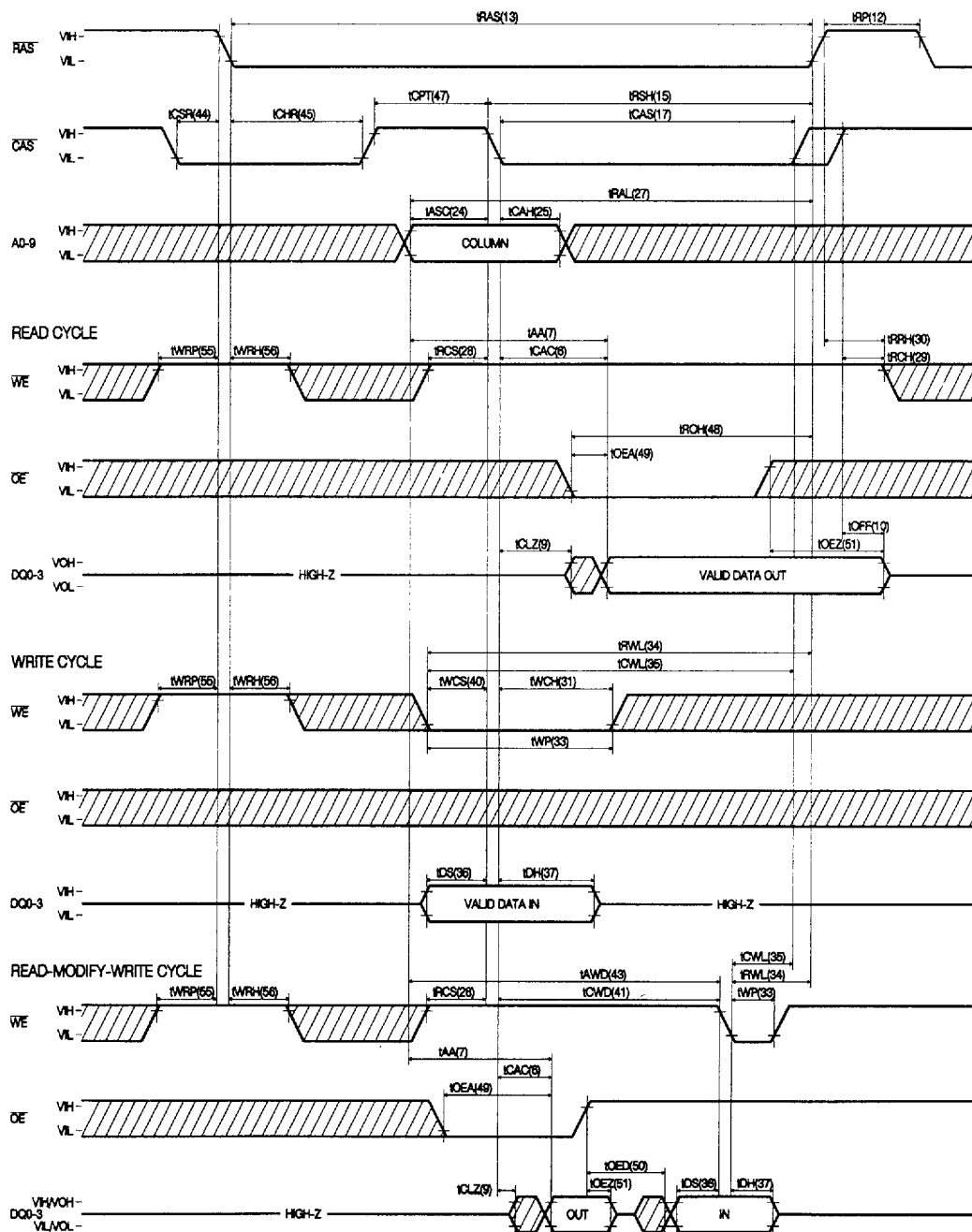
**HIDDEN REFRESH CYCLE (READ)**



HIDDEN REFRESH CYCLE (WRITE)



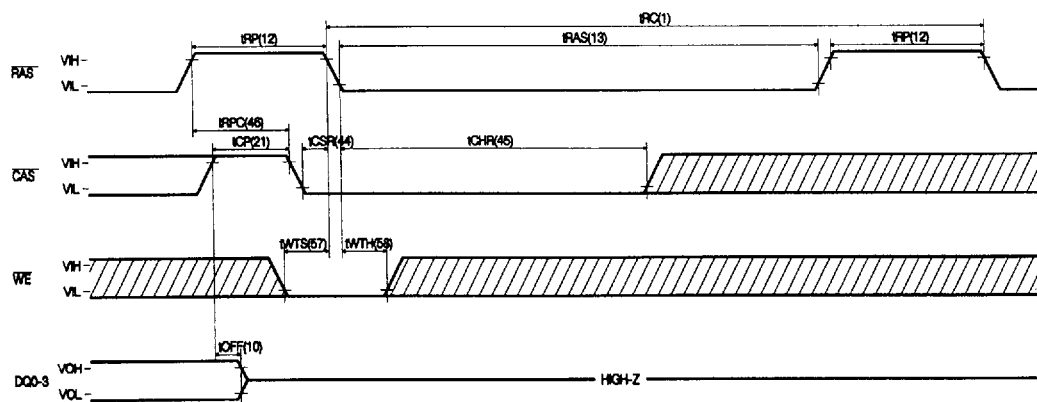
**CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE**



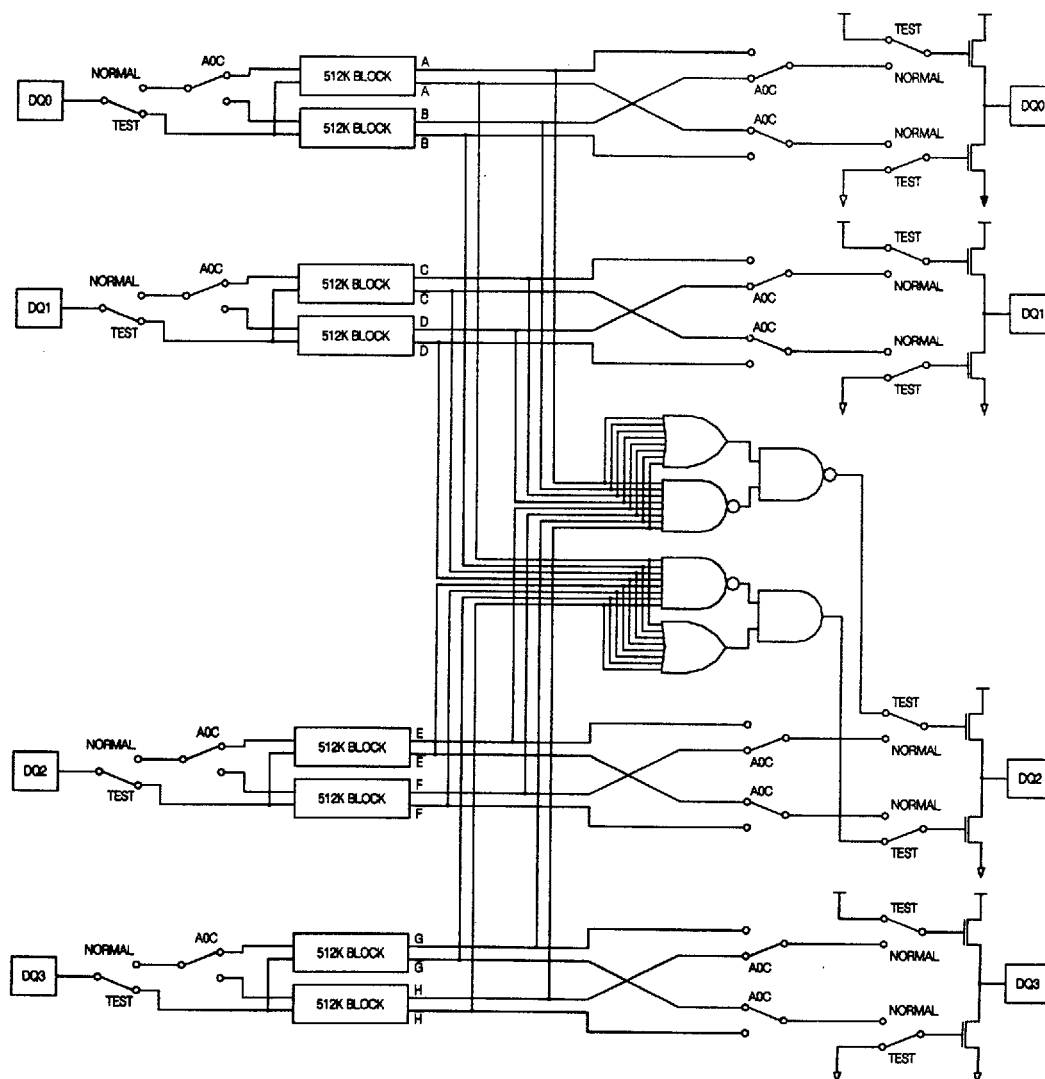
## TEST MODE

The HY514400A is a DRAM organized 1,048,576 x 4-bit. It is internally organized 524,288 x 8-bit. In Test Mode, data are written into 8 sectors (Each is composed of 512K bits) in parallel and retrieved the same way. Column address A0 is not used. If, upon reading, all 8-bit data from 8 sectors are equal (all "1"s or "0"s), the DQ2 pin indicates a "1". If they are not equal, the DQ2 pin indicates a "0". The DQ0, DQ1 and DQ3 pins always indicate a "1" in Test Mode Read cycles. The diagram below shows the timing of the HY514400A to enter Test Mode. In Test Mode, the 1Mx4 DRAM can be tested as if it were a 512Kx4 DRAM.  $\overline{WE}$ ,  $\overline{CAS}$ -before- $\overline{RAS}$  cycle (Test Mode In Cycle) puts the HY514400A into Test Mode and  $\overline{CAS}$ -before- $\overline{RAS}$  or  $\overline{RAS}$ -only refresh cycle puts it back into Normal Mode. In Test Mode,  $\overline{WE}$ ,  $\overline{CAS}$ -before- $\overline{RAS}$  cycle shall be used for the refresh operation. The Test Mode function reduces test time. (1/2 in case of N test pattern)

## TEST MODE IN CYCLE

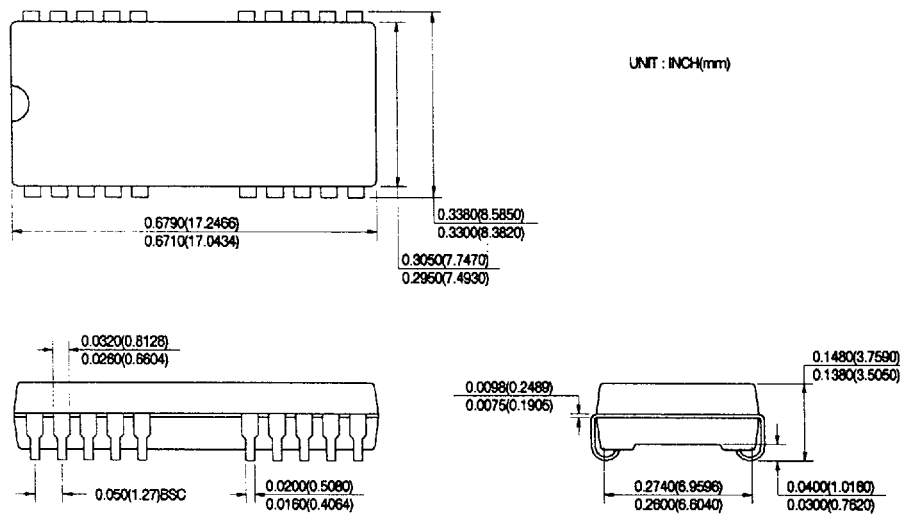


BLOCK DIAGRAM IN TEST MODE

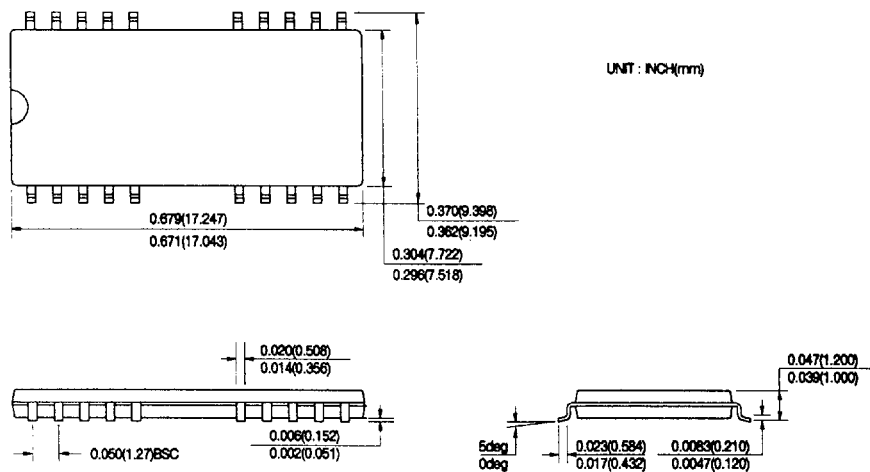


PACKAGE INFORMATION

300 mil 20/26 pin Small Out line J-form Package (J)



300 mil 20/26 pin Thin Small Outline Package (T) (R)



**HYUNDAI**

**HY514400A Series**

**ORDERING INFORMATION**

| PART NUMBER | SPEED    | POWER  | PACKAGE    |
|-------------|----------|--------|------------|
| HY514400AJ  | 50/60/70 |        | SOJ        |
| HY514400ALJ | 50/60/70 | L-part | SOJ        |
| HY514400AT  | 50/60/70 |        | TSOP-II    |
| HY514400ALT | 50/60/70 | L-part | TSOP-II    |
| HY514400AR  | 50/60/70 |        | TSOP-II(P) |
| HY514400ALR | 50/60/70 | L-part | TSOP-II(P) |