OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
HI-5043

March 2000 File Number 3130.3

Dual SPDT CMOS Analog Switch

The IH5043 analog switch uses an improved, high voltage CMOS monolithic technology. These devices provide ease of use and performance advantages not previously available from solid state switches.

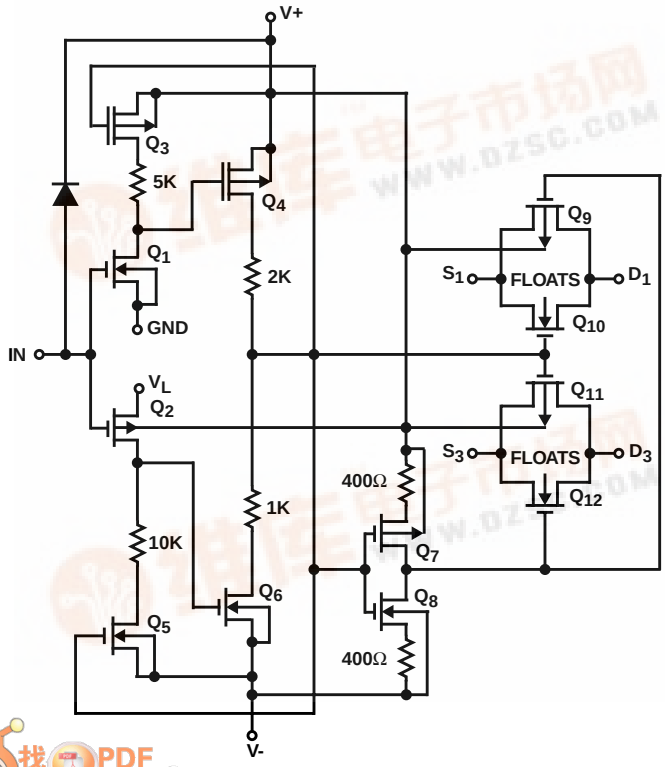
Key performance advantage is TTL compatibility and ultra low power operation. The quiescent current requirement is less than 1mA. Also, the IH5043 guarantees Break-Before-Make switching, accomplished by extending the t_{ON} time (300ns Typ), so that it exceeds t_{OFF} time (200ns Typ). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is eliminated.

Part Number Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
IH5043CPE	0 to 70	16 Ld PDIP	E16.3
IH5043CY	0 to 70	16 Ld SOIC	M16.15

Schematic Diagram

FUNCTIONAL DRIVER, TYPICAL DRIVER, GATE ($^1/_2$ AS SHOWN)

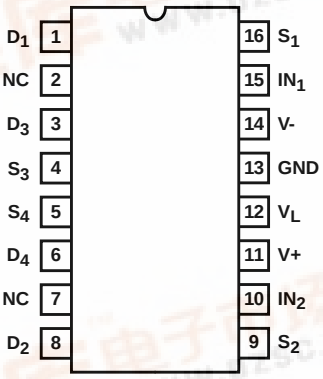


Features

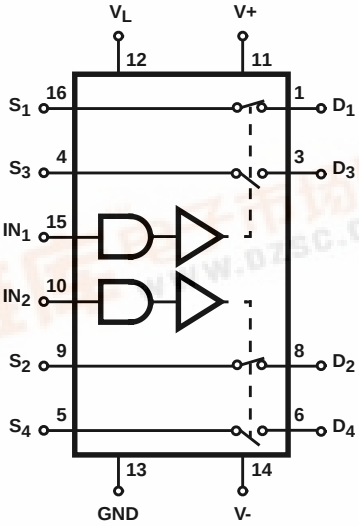
- See HI504X for Other Functions
- Dual SPDT
- Switches Greater than $20V_{P-P}$ Signals with ±15V Supplies
- Quiescent Current Less than 1mA
- Break-Before-Make Switching t_{OFF} 200ns, t_{ON} 300ns (Typ)
- TTL, DTL, CMOS, PMOS Compatible

Pinout

IH5043
(PDIP, SOIC)
TOP VIEW



Functional Diagram



SWITCH STATES SHOWN ARE FOR LOGIC "1" INPUT

TRUTH TABLE

LOGIC	SWITCH 1, 2	SWITCH 3, 4
0	Off	On
1	On	Off

Absolute Maximum Ratings

V+ to V- . . . . . <36V
V+ to V_D . . . . . <30V
V_D to V- . . . . . <30V
V_D to V_S . . . . . <±22V
V_L to V- . . . . . <33V
V_L to V_{IN} . . . . . <30V
V_L to GND . . . . . <20V
V_{IN} to GND . . . . . <20V
Continuous Current (S-D) 30mA
Peak Current S-D (Pulsed 1ms, 10% Duty Cycle Max) 70mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
PDIP Package	90
SOIC Package	115

Maximum Junction Temperature (Plastic Packages) . . . . . 150^{o}C
Maximum Storage Temperature . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . 0^{o}C to 70^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V+ = +15V, V- = -15V, V_L = +5V

PER CHANNEL PARAMETER	TEST CONDITIONS	(NOTES 2, 3) 0^{o}C	25^{o}C	70^{o}C	UNITS
DYNAMIC CHARACTERISTICS					
Turn ON Time, t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V, See Figure 6	-	1000	-	ns
Turn OFF Time, t_{OFF}		-	500	-	ns
Charge Injection, Q	See Figure 7	-	20 (Typ)	-	mV
OFF Isolation, OIRR	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF, See Figure 4	-	50 (Typ)	-	dB
Crosstalk, CCRR	One Channel Off; Any Other Channel Switches as per Figure 3	-	-50 (Typ)	-	dB
DIGITAL INPUT CHARACTERISTICS					
Input Logic Current, $I_{IN(ON)}$	V_{IN} = 2.4V	±1	±1	10	µA
Input Logic Current, $I_{IN(OFF)}$	V_{IN} = 0.8V	±1	±1	10	µA
ANALOG SWITCH CHARACTERISTICS					
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = 10mA, V_{ANALOG} = -10V to +10V	80	80	130	Ω
Channel-to-Channel $r_{DS(ON)}$ Match, $\Delta r_{DS(ON)}$		-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}		-	±10 (Typ)	-	V
Switch OFF Leakage Current, $I_{D(OFF)}$, $I_{S(OFF)}$	V_{ANALOG} = -10V to +10V	-	±5	100	nA
Switch ON Leakage Current, $I_{D(ON)}+I_{S(ON)}$	V_D = V_S = -10V to +10V	-	±10	100	nA
POWER SUPPLY CHARACTERISTICS					
+ Power Supply Quiescent Current, I+		10	10	100	µA
- Power Supply Quiescent Current, I-		10	10	100	µA
+5V Supply Quiescent Current, I_L		10	10	100	µA
Ground Quiescent Current, I_{GND}		10	10	100	µA

NOTES:

2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. Min or Max value unless otherwise specified.

Test Circuits and Waveforms

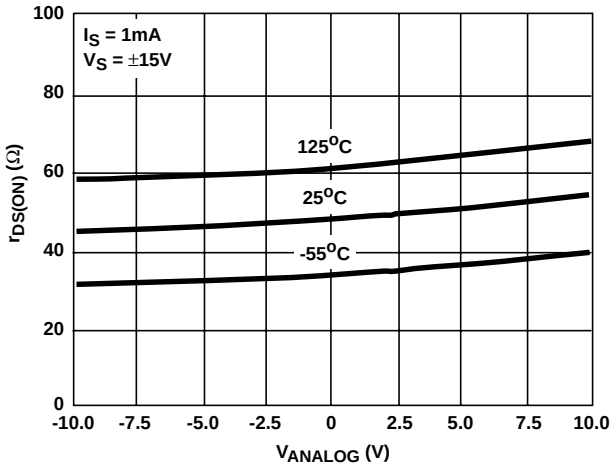


FIGURE 1. $r_{DS(ON)}$ vs ANALOG INPUT VOLTAGE

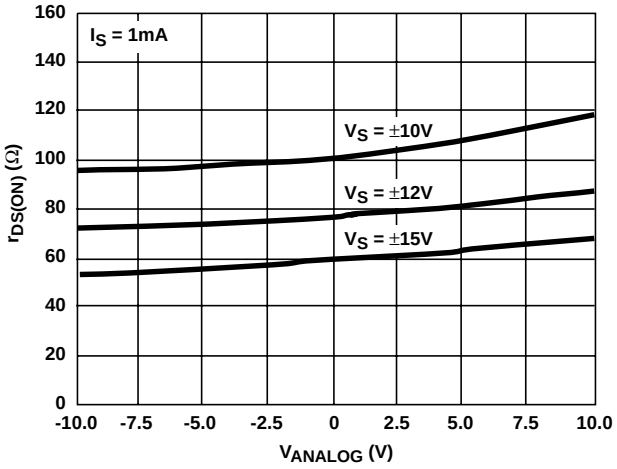


FIGURE 2. $r_{DS(ON)}$ vs POWER SUPPLY VOLTAGE

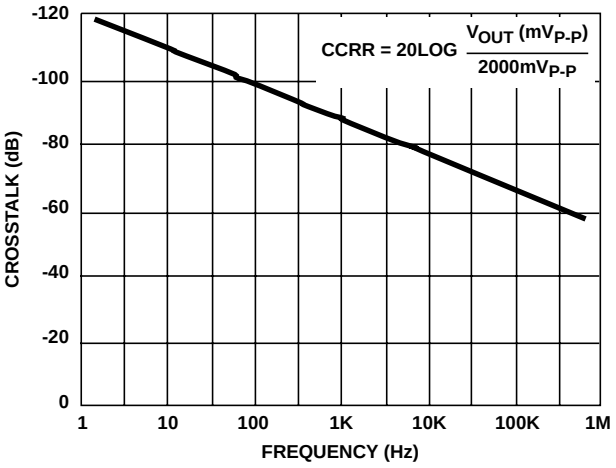


FIGURE 3A. CROSSTALK vs FREQUENCY

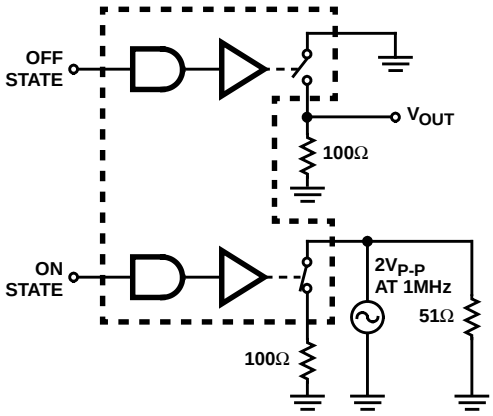


FIGURE 3B. TEST CIRCUIT

FIGURE 3. CROSSTALK

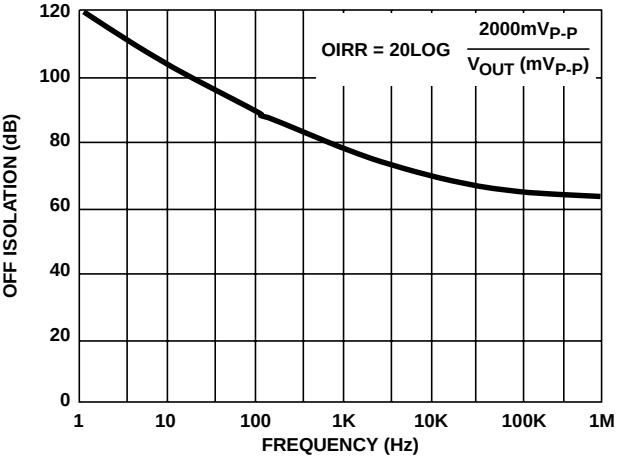


FIGURE 4A. OFF ISOLATION vs FREQUENCY

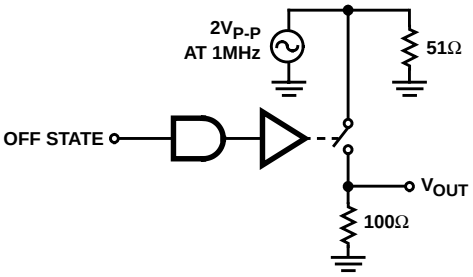


FIGURE 4B. TEST CIRCUIT

FIGURE 4. OFF ISOLATION

Test Circuits and Waveforms (Continued)

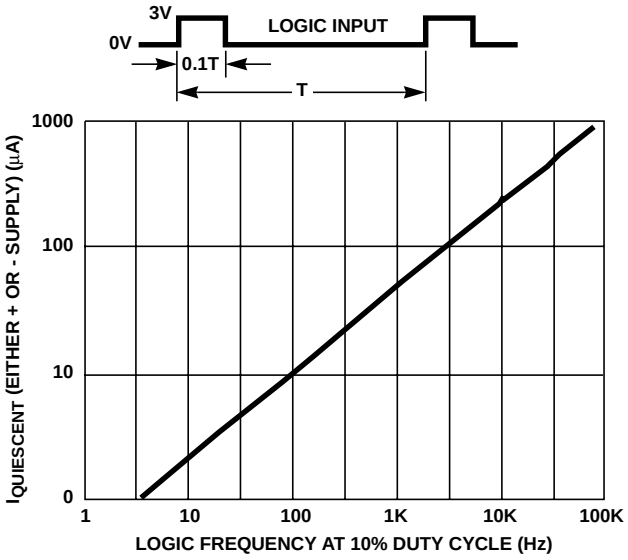


FIGURE 5. SUPPLY CURRENT vs LOGIC FREQUENCY

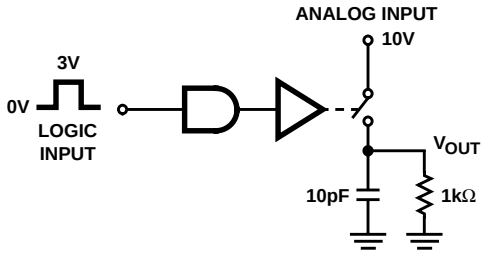


FIGURE 6. t_{ON} AND t_{OFF} TEST CIRCUIT

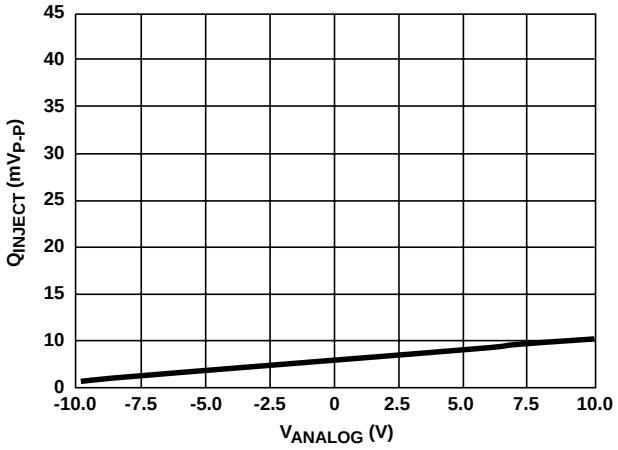


FIGURE 7A. CHARGE INJECTION vs ANALOG INPUT VOLTAGE

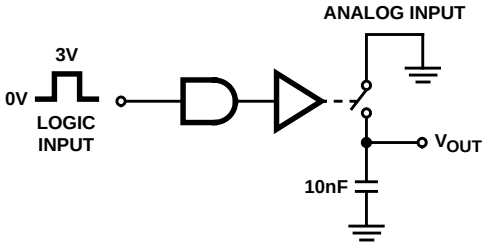


FIGURE 7B. TEST CIRCUIT

FIGURE 7. CHARGE INJECTION

Typical Applications

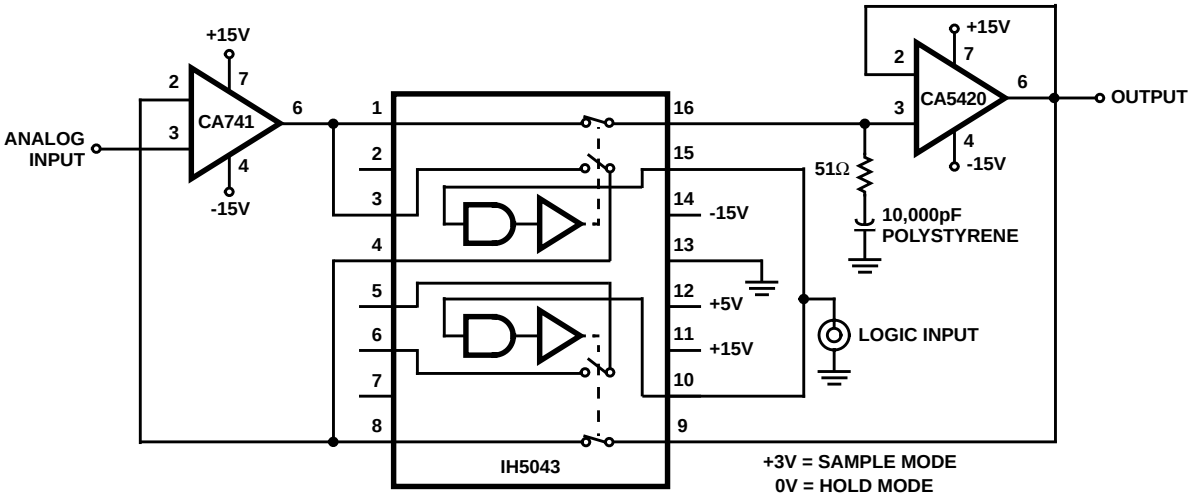


FIGURE 8. IMPROVED SAMPLE AND HOLD

EXAMPLE: If $-V_{ANALOG}$ = $-10V_{DC}$ and $+V_{ANALOG}$ = $+10V_{DC}$, then Ladder Legs are switched between $\pm 10V_{DC}$, depending upon state of Logic Strobe.

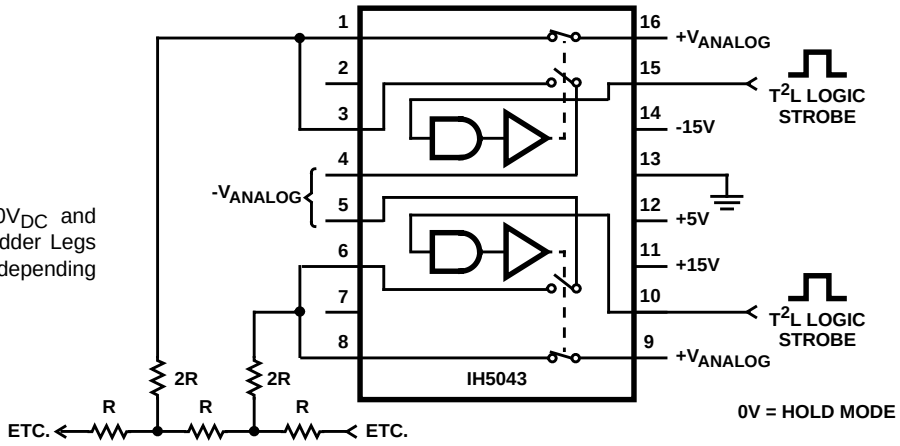
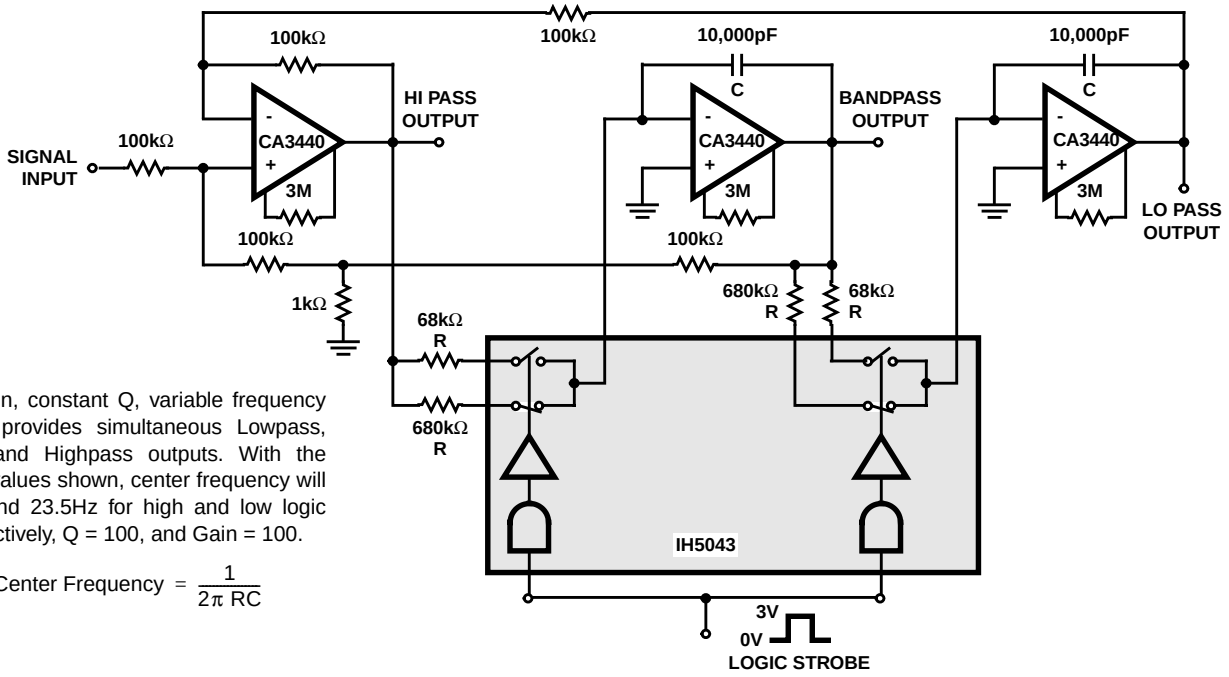


FIGURE 9. USING THE CMOS SWITCH TO DRIVE AN R/2R LADDER NETWORK (2 LEGS)

Typical Applications (Continued)



Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_N = \text{Center Frequency} = \frac{1}{2\pi RC}$$

FIGURE 10. DIGITALLY TUNED LOW POWER ACTIVE FILTER

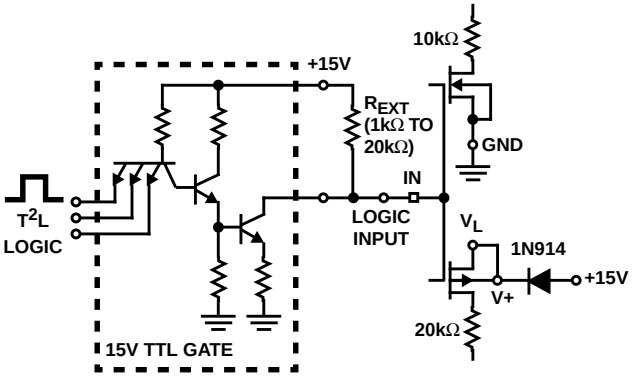


FIGURE 11. INTERFACING WITH TTL OPEN COLLECTOR LOGIC (TYP EXAMPLE FOR +15V CASE SHOWN)

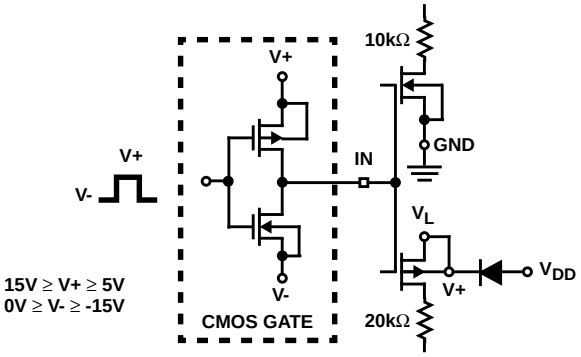


FIGURE 12. INTERFACING WITH CMOS LOGIC

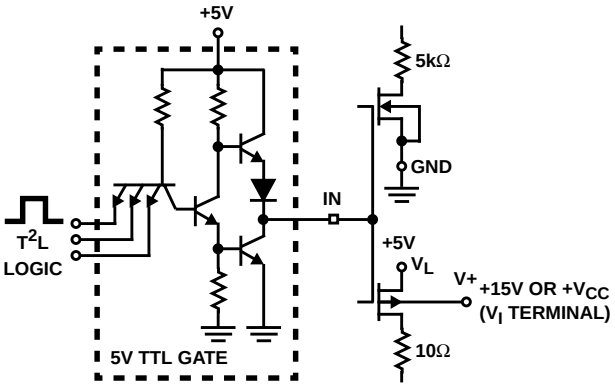


FIGURE 13. TTL LOGIC INTERFACE

Die Characteristics

DIE DIMENSIONS:

1778µm x 1905µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

Type: PSG/Nitride
PSG Thickness: 7kÅ ±1.4kÅ
Nitride Thickness: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

IH5043