

TLV2354, TLV2354Y LinCMOS™ QUADRUPLE LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS012B – MAY 1992 – REVISED MARCH 1999

- **Wide Range of Supply Voltages**
2 V to 8 V
- **Fully Characterized at 3 V and 5 V**
- **Very-Low Supply-Current Drain**
240 μ A Typ at 3 V
- **Common-Mode Input Voltage Range**
Includes Ground
- **High Input Impedance . . . $10^{12} \Omega$ Typ**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Extremely Low Input Bias Current**
5 pA Typ
- **Output Compatible With TTL, MOS, and CMOS**
- **Built-In ESD Protection**

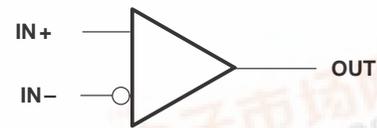
description

The TLV2354 consists of four independent, low-power comparators specifically designed for single power-supply applications and operate with power-supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 240 μ A.

The TLV2354 is designed using the Texas Instruments LinCMOS™ technology and, therefore, features an extremely high input impedance (typically greater than $10^{12} \Omega$), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2354I is fully characterized for operation from -40°C to 85°C . The TLV2354M is fully characterized for operation from -55°C to 125°C .

The TLV2354 has internal electrostatic-discharge (ESD)-protection circuits and has been classified with a 1000-V ESD rating using Human Body Model testing. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

symbol (each comparator)



AVAILABLE OPTIONS

T _A	V _{IO} max at 25°C	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D) [†]	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW) [‡]	CERAMIC FLATPACK (W)	
-40°C to 85°C	5 mV	TLV2354ID	—	—	TLV2354IN	TLV2354IPWLE	—	TLV2354Y
-55°C to 125°C	5 mV	—	TLV2354MFK	TLV2354MJ	—	—	TLV2354MW	

[†] The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR).

[‡] The PW packages are only available left-ended taped and reeled (e.g., TLV2354IPWLE).



These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

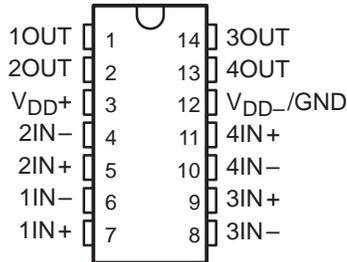


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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

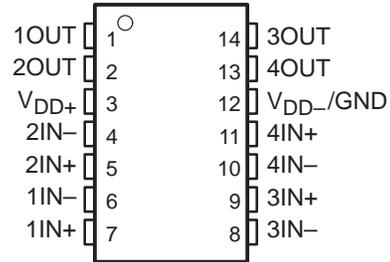
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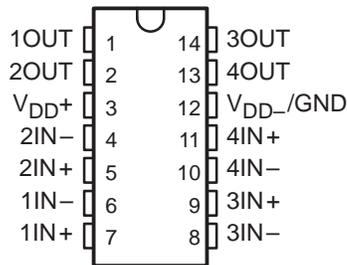
TLV2354I
D OR N PACKAGE
(TOP VIEW)



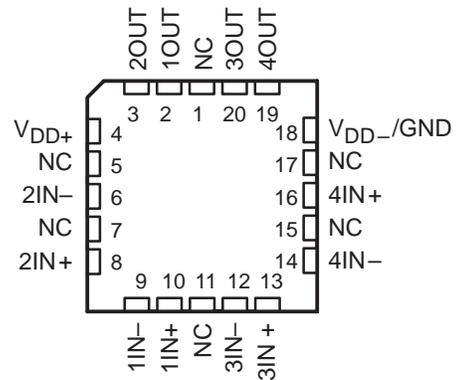
TLV2354I
PW PACKAGE
(TOP VIEW)



TLV2354M
J OR W PACKAGE
(TOP VIEW)



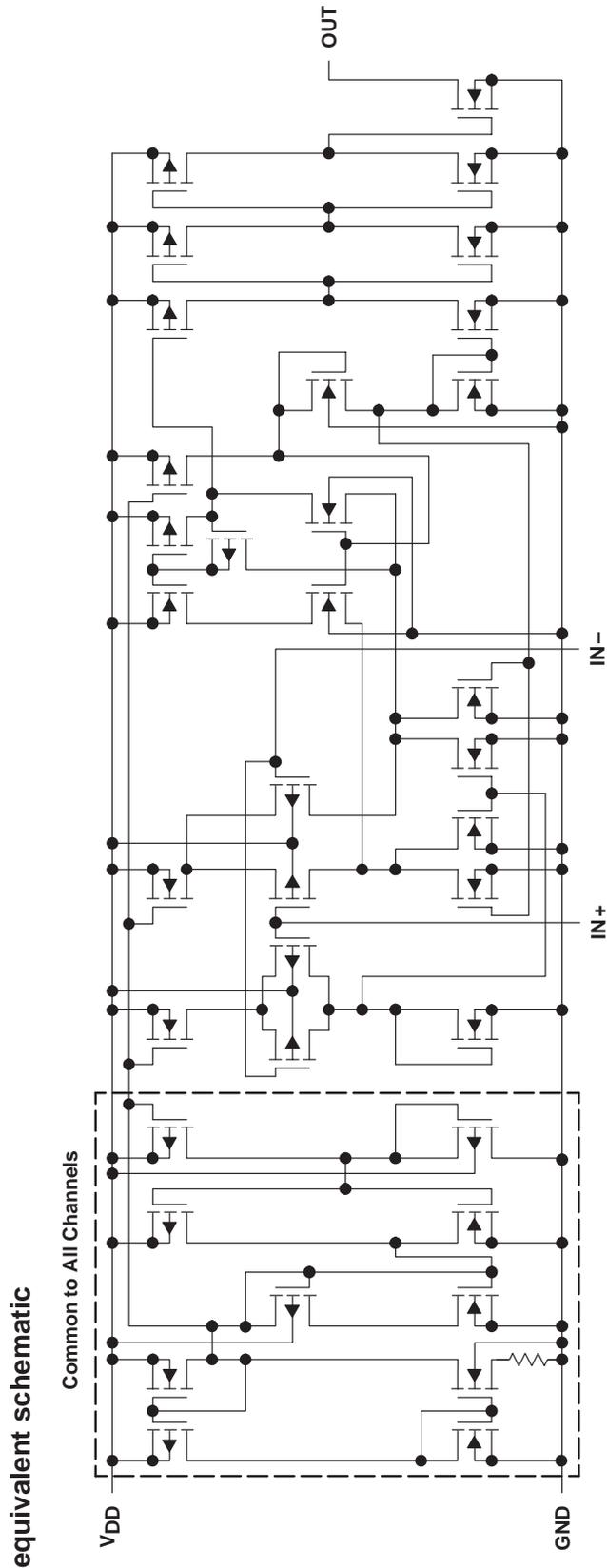
TLV2354AM, TLV2354M
FK PACKAGE
(TOP VIEW)



NC – No internal connection

TLV2254, TLV2254Y LinCMOS™ QUADRUPLE LOW-VOLTAGE DIFFERENTIAL COMPARATORS

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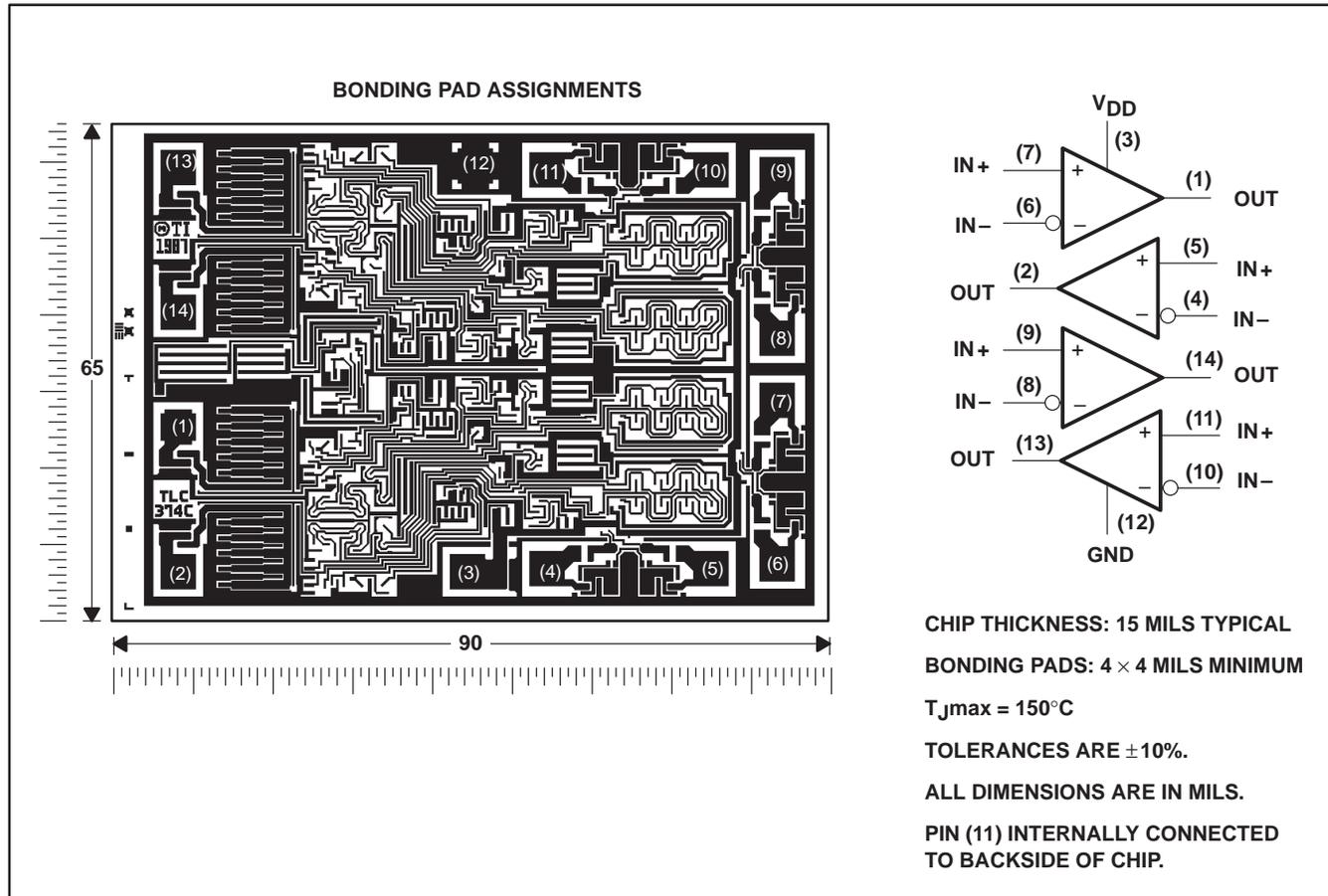


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TLV2354Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2354. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	8 V
Differential input voltage, V_{ID} (see Note 2)	± 8 V
Input voltage range, V_I	–0.3 to 8 V
Output voltage, V_O	8 V
Input current, I_I	± 5 mA
Output current, I_O	20 mA
Duration of output short-circuit current to GND (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : TLV2354I	–40°C to 85°C
TLV2354M	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FK, J, or W package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
 3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW	—
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
J	1375 mW	11.0 mW/°C	715 mW	275 mW
N	1150 mW	9.2 mW/°C	598 mW	—
PW	700 mW	5.6 mW/°C	364 mW	—
W	700 mW	5.5 mW/°C	370 mW	150 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	$V_{DD} = 3$ V	0	1.75	V
	$V_{DD} = 5$ V	0	3.75	
Operating free-air temperature, T_A	TLV2354I	–40	85	°C
	TLV2354M	–55	125	

TLV2354, TLV2354Y

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electrical characteristics at specified free-air temperature†

PARAMETER	TEST CONDITIONS	T _A ‡	TLV2354I						UNIT
			V _{DD} = 3 V			V _{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO} Input offset voltage	V _{IC} = V _{ICRmin} , See Note 4	25°C	1		5	1		5	mV
		Full range	7			7			
I _{IO} Input offset current		25°C	1			1			pA
		85°C	1			1			nA
I _{IB} Input bias current		25°C	5			5			pA
		85°C	2			2			nA
V _{ICR} Common-mode input voltage range		25°C	0 to 2			0 to 4			V
		Full range	0 to 1.75			0 to 3.75			
I _{OH} High-level output current	V _{ID} = 1 V	25°C	0.1			0.1			nA
		Full range	1			1			μA
V _{OL} Low-level output voltage	V _{ID} = -1 V, I _{OL} = 2 mA	25°C	115		300	150		400	mA
		Full range	600			700			
I _{OL} Low-level output current	V _{ID} = -1 V, V _{OL} = 1.5 V	25°C	6	16		6	16		mA
I _{DD} Supply current	V _{ID} = 1 V, No load	25°C	240		500	290		600	μA
		Full range	700			800			

† All characteristics are measured with zero common-mode input voltage unless otherwise noted.

‡ Full range is -40°C to 85°C. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV2354I			UNIT
			MIN	TYP	MAX	
Response time	R _L = 5.1 kΩ, See Note 5	C _L = 15 pF§, 100-mV input step with 5-mV overdrive	640			ns

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 with V_{DD} = 5 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV2354I			UNIT
			MIN	TYP	MAX	
Response time	R _L = 5.1 kΩ, See Note 5	100-mV input step with 5-mV overdrive	650			ns
		TTL-level input step	200			

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 with V_{DD} = 5 V.

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electrical characteristics at specified free-air temperature†

PARAMETER	TEST CONDITIONS	T _A ‡	TLV2354M						UNIT			
			V _{DD} = 3 V			V _{DD} = 5 V						
			MIN	TYP	MAX	MIN	TYP	MAX				
V _{IO}	Input offset voltage	V _{IC} = V _{ICRmin} , See Note 4	25°C	1		5		1		5		mV
			Full range				10			10		
I _{IO}	Input offset current		25°C	1			1					pA
			125°C				10			10		nA
I _{IB}	Input bias current		25°C	5			5					pA
			125°C				20			20		nA
V _{ICR}	Common-mode input voltage range		25°C	0 to 2			0 to 4					V
			Full range	0 to 1.75			0 to 3.75					
I _{OH}	High-level output current	V _{ID} = 1 V	25°C	0.1			0.1					nA
			Full range				1			1		μA
V _{OL}	Low-level output voltage	V _{ID} = -1 V, I _{OL} = 2 mA	25°C	115		300		150		400		mA
			Full range				600			700		
I _{OL}	Low-level output current	V _{ID} = -1 V, V _{OL} = 1.5 V	25°C	6	16		6	16				mA
I _{DD}	Supply current	V _{ID} = 1 V, No load	25°C	240		500		290		600		μA
			Full range				700			800		

† All characteristics are measured with zero common-mode input voltage unless otherwise noted.

‡ Full range is -55°C to 125°C. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV2354M			UNIT
			MIN	TYP	MAX	
Response time	R _L = 5.1 kΩ, See Note 5	C _L = 100 pF§, 100-mV input step with 5-mV overdrive	1400			ns

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 with V_{DD} = 5 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV2354M			UNIT
			MIN	TYP	MAX	
Response time	R _L = 5.1 kΩ, See Note 5	C _L = 100 pF§, 100-mV input step with 5-mV overdrive	1300			ns
		TTL-level input step	900			

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 with V_{DD} = 5 V.

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electrical characteristics at specified free-air temperature, $T_A = 25^\circ\text{C}^\dagger$

PARAMETER	TEST CONDITIONS	TLV2354Y						UNIT
		$V_{DD} = 3\text{ V}$			$V_{DD} = 5\text{ V}$			
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = V_{ICRmin}$, See Note 4		1	5		1	5	mV
I_{IO} Input offset current			1			1		pA
I_{IB} Input bias current			5			5		pA
V_{ICR} Common-mode input voltage range		0 to 2			0 to 4			V
I_{OH} High-level output current	$V_{ID} = 1\text{ V}$		0.1			0.1		nA
V_{OL} Low-level output voltage	$V_{ID} = -1\text{ V}$, $I_{OL} = 2\text{ mA}$		115	300		150	400	mV
I_{OL} Low-level output current	$V_{ID} = -1\text{ V}$, $V_{OL} = 1.5\text{ V}$	6	16		6	16		mA
I_{DD} Supply current	$V_{ID} = 1\text{ V}$, No load		240	500		290	600	μA

[†] All characteristics are measured with zero common-mode input voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with $V_{DD} = 5\text{ V}$, 2 V with $V_{DD} = 3\text{ V}$, or below 400 mV with a 10-k Ω resistor between the output and V_{DD} . They can be verified by applying the limit value to the input and checking for the appropriate output state.

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TYPICAL CHARACTERISTICS

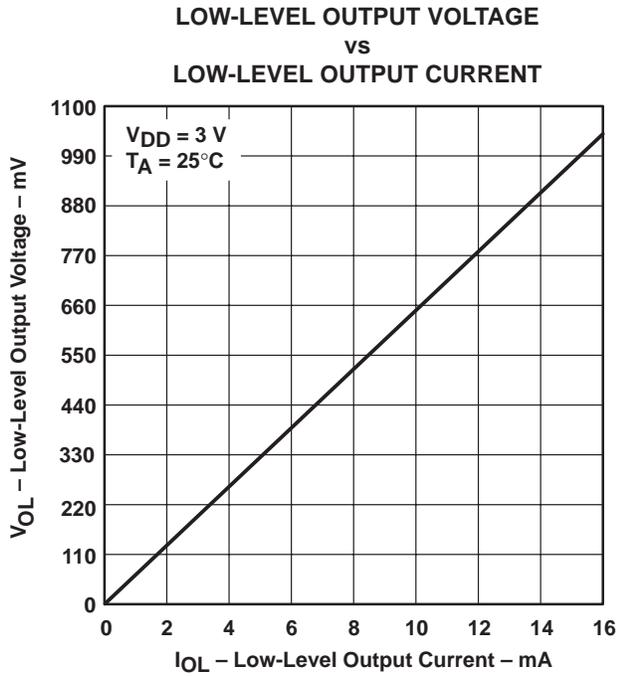


Figure 1

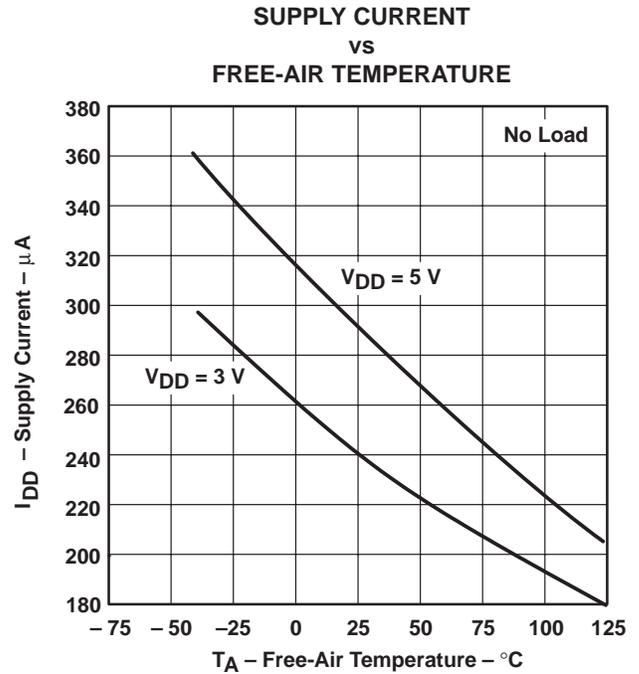


Figure 2

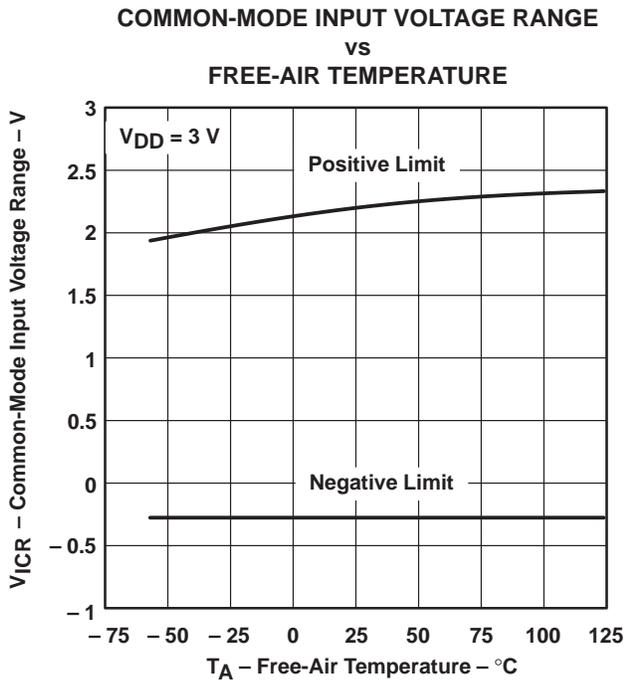


Figure 3

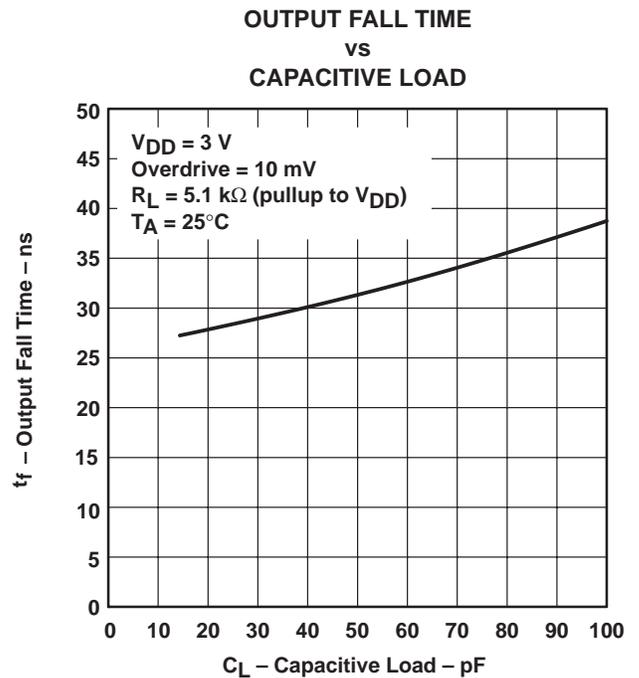


Figure 4

TLV2354, TLV2354Y

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TYPICAL CHARACTERISTICS

HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES

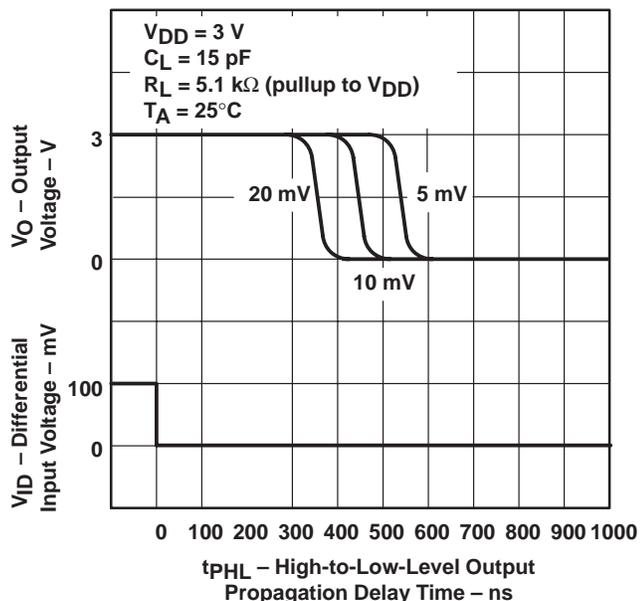


Figure 5

HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS CAPACITIVE LOADS

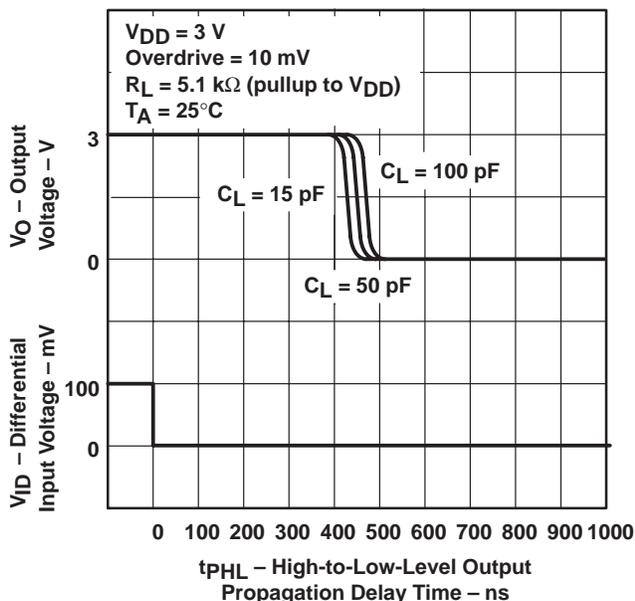


Figure 6

LOW-TO-HIGH-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES

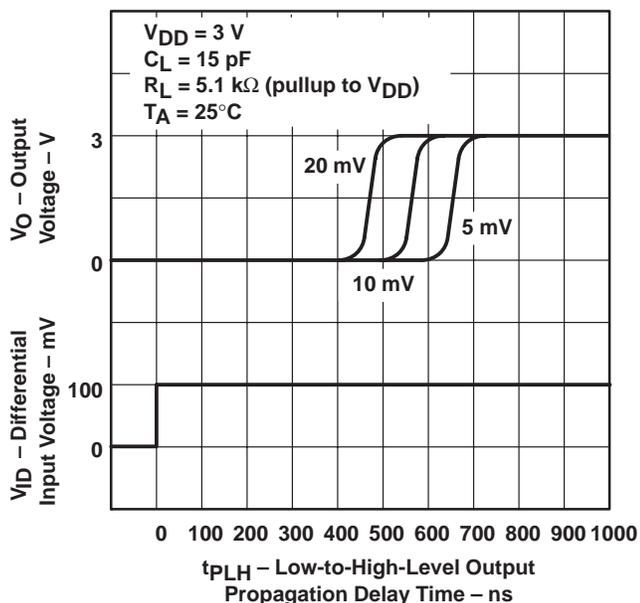


Figure 7

LOW-TO-HIGH-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS CAPACITIVE LOADS

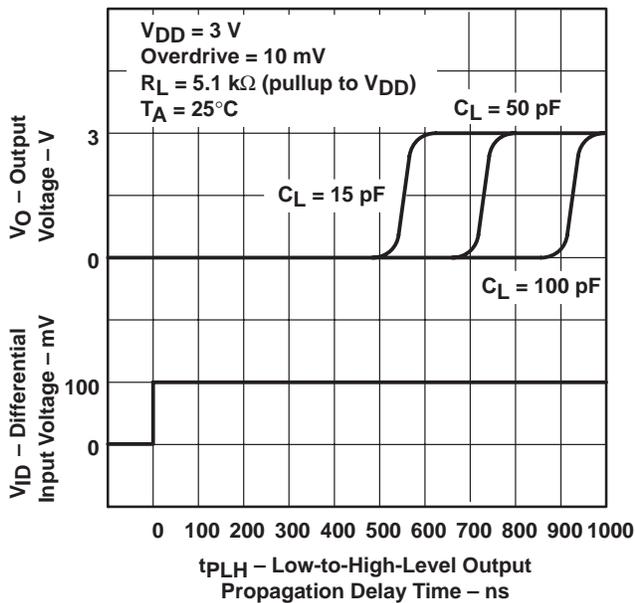


Figure 8

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PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLV2354 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the V_{ICR} test rather than changing the input voltages to provide greater accuracy.

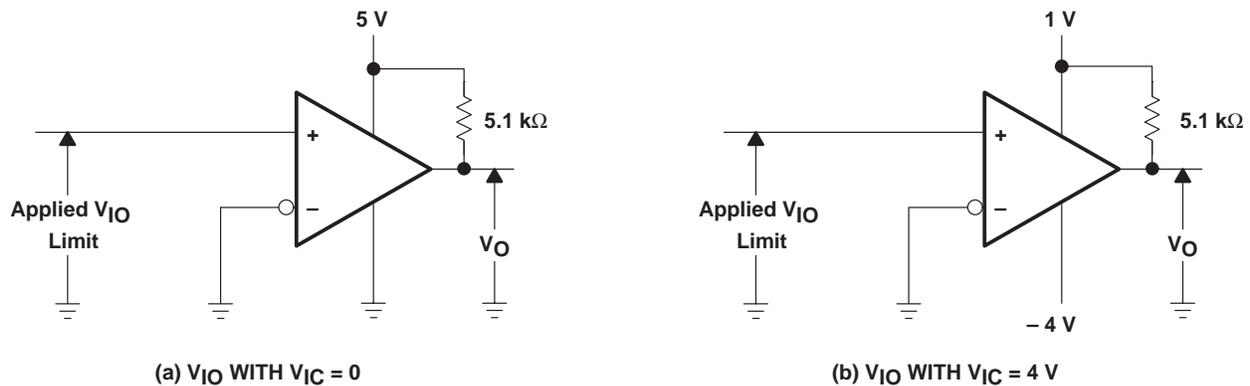


Figure 9. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes states.

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PARAMETER MEASUREMENT INFORMATION

Figure 10 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R9 and R10 provide a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

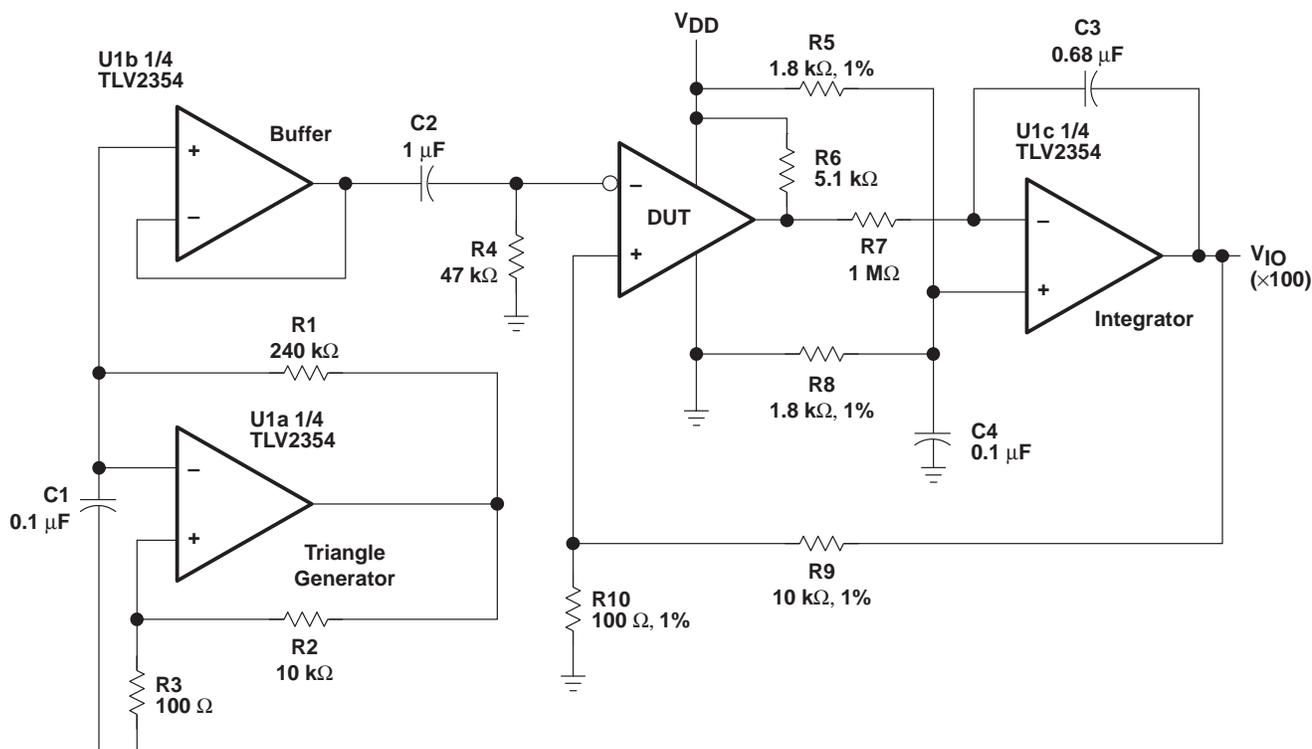


Figure 10. Circuit for Input Offset Voltage Measurement

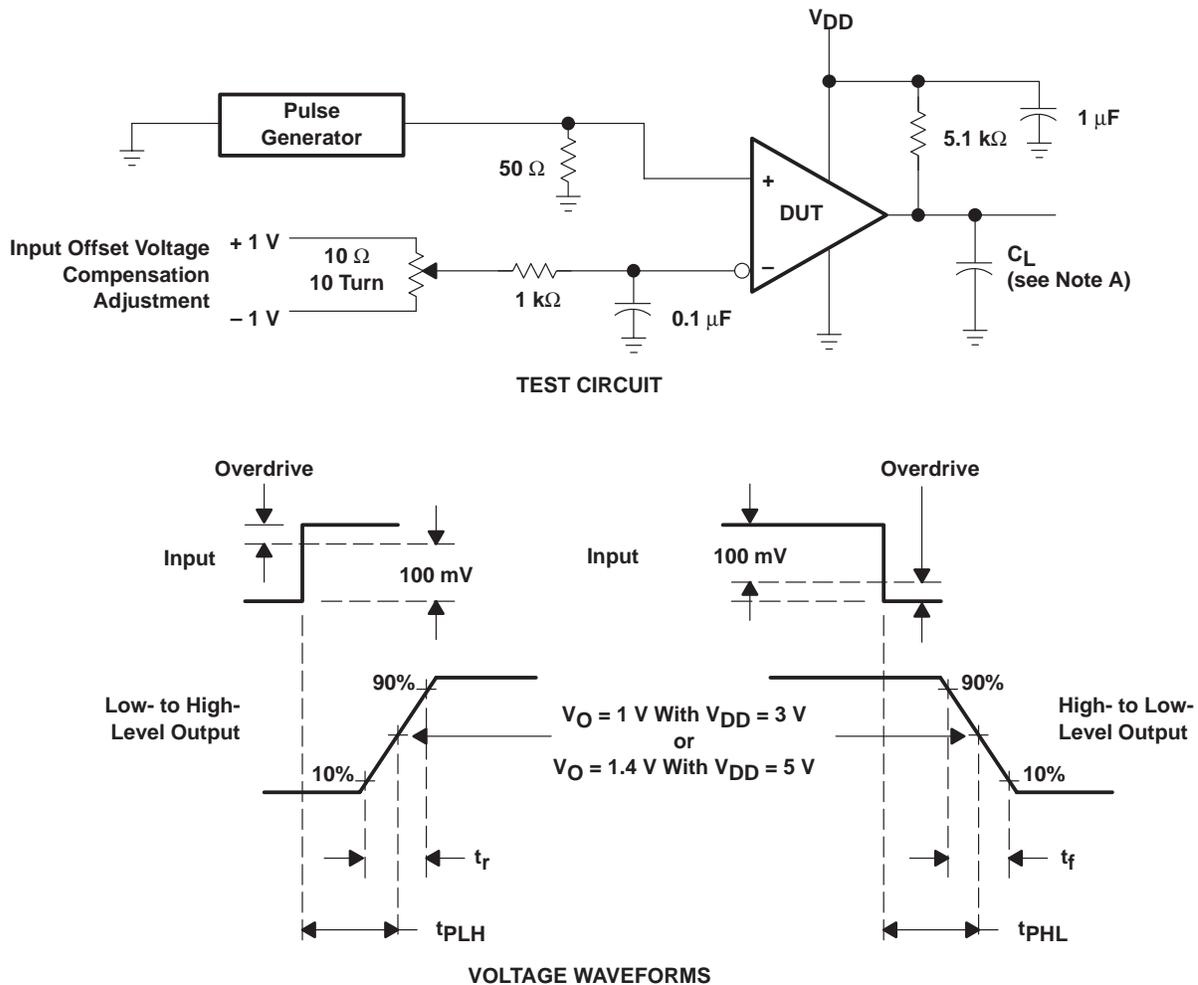
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PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses $V_O = 1\text{ V}$ with $V_{DD} = 3\text{ V}$ or when the output crosses $V_O = 1.4\text{ V}$ with $V_{DD} = 5\text{ V}$. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example a 105-mV or 5-mV overdrive, causes the output to change state.



NOTE A: C_L includes probe and jig capacitance.

Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

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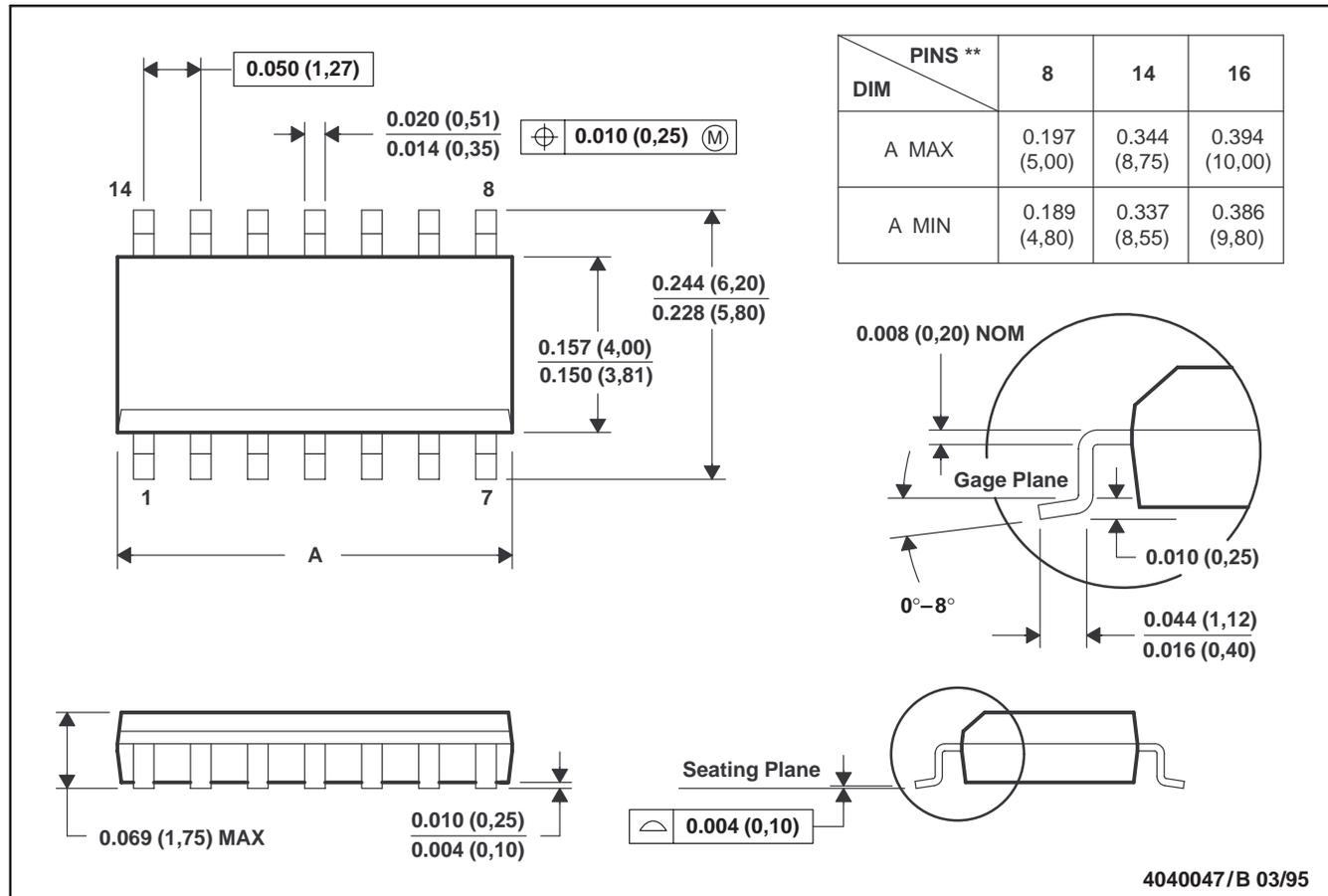
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MECHANICAL INFORMATION

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Four center pins are connected to die mount pad.
 E. Falls within JEDEC MS-012

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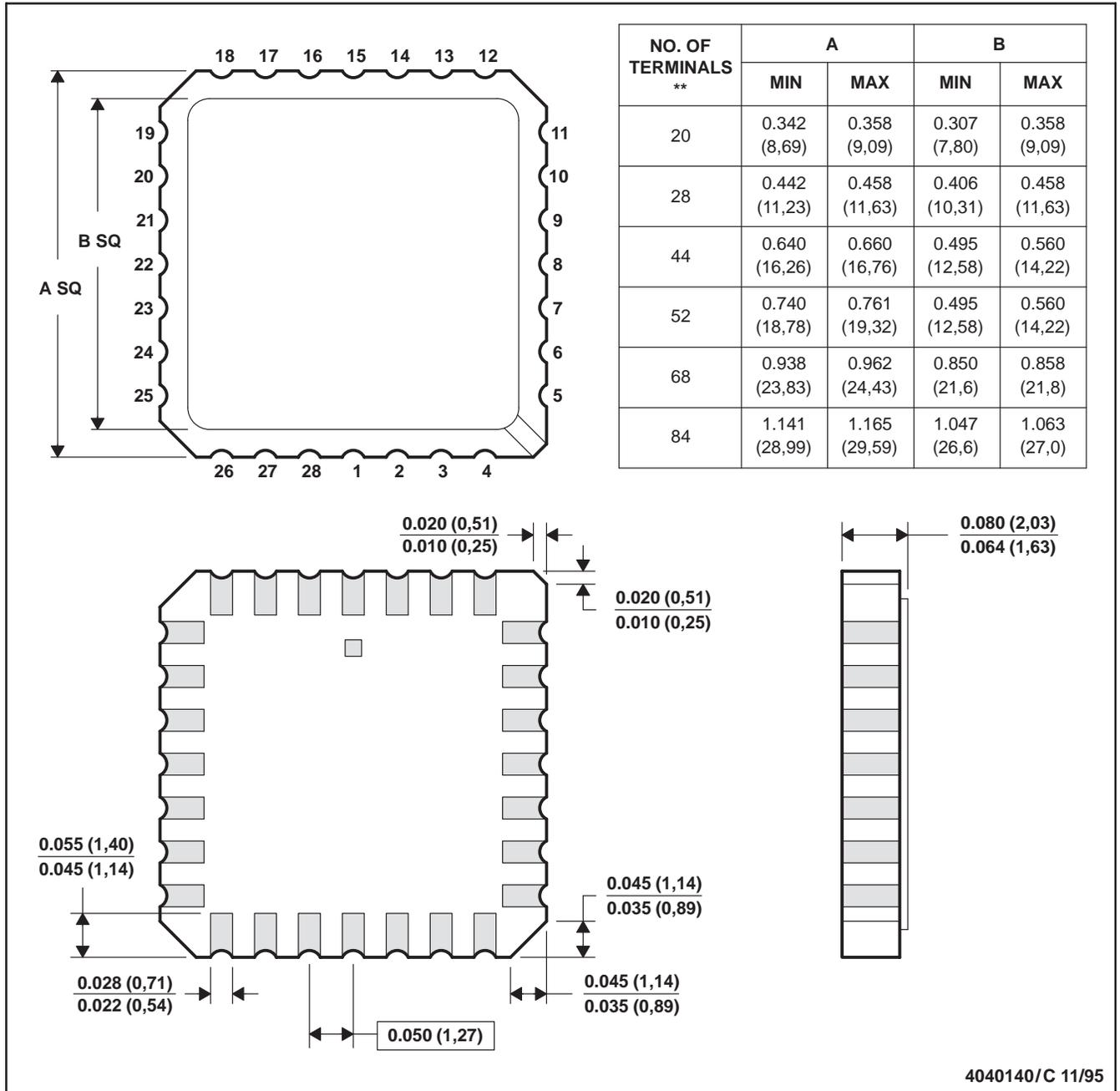
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MECHANICAL INFORMATION

FK (S-CQCC-N)**

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

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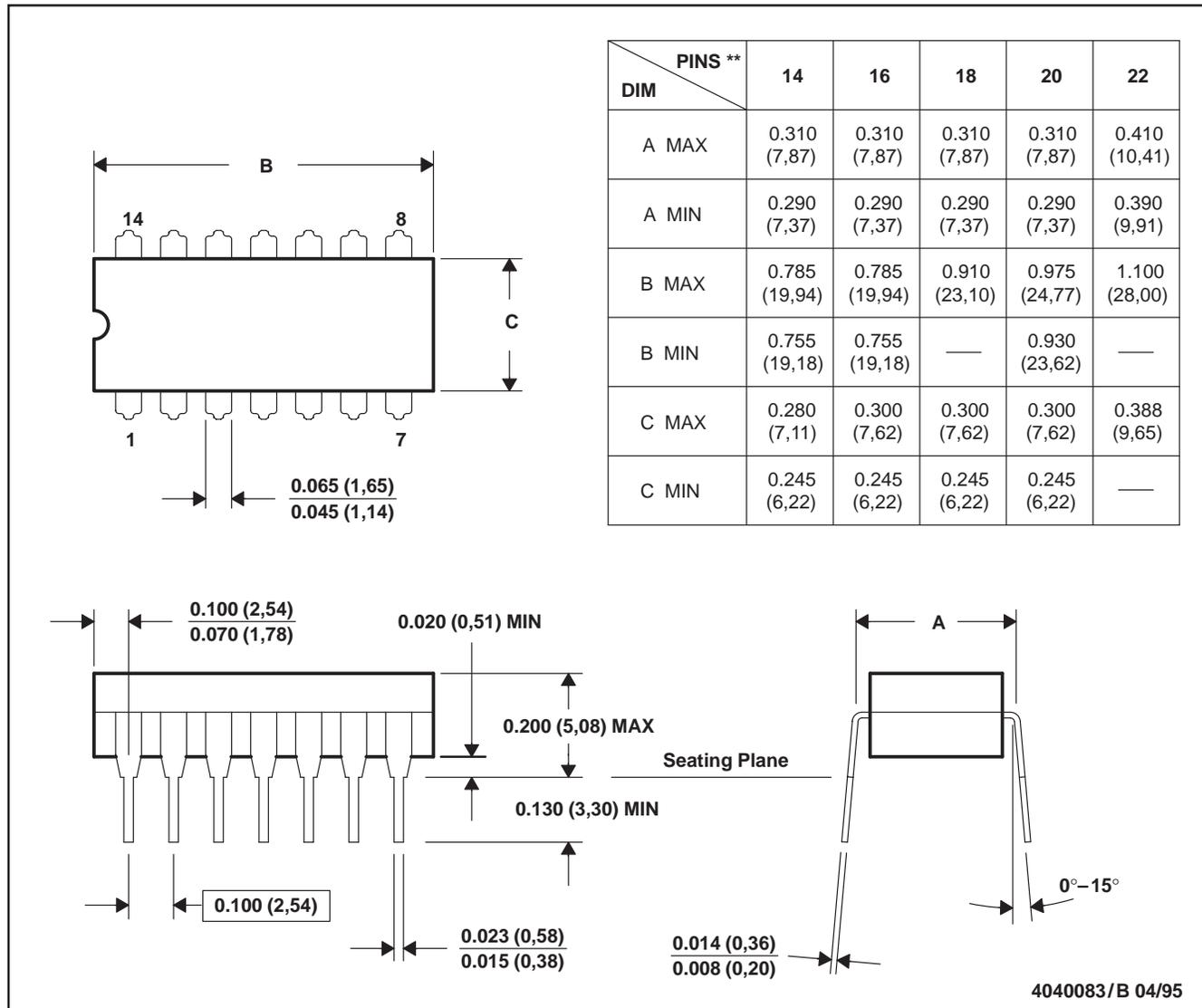
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MECHANICAL INFORMATION

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22

TLV2354, TLV2354Y

LinCMOS™ QUADRUPLE LOW-VOLTAGE DIFFERENTIAL COMPARATORS

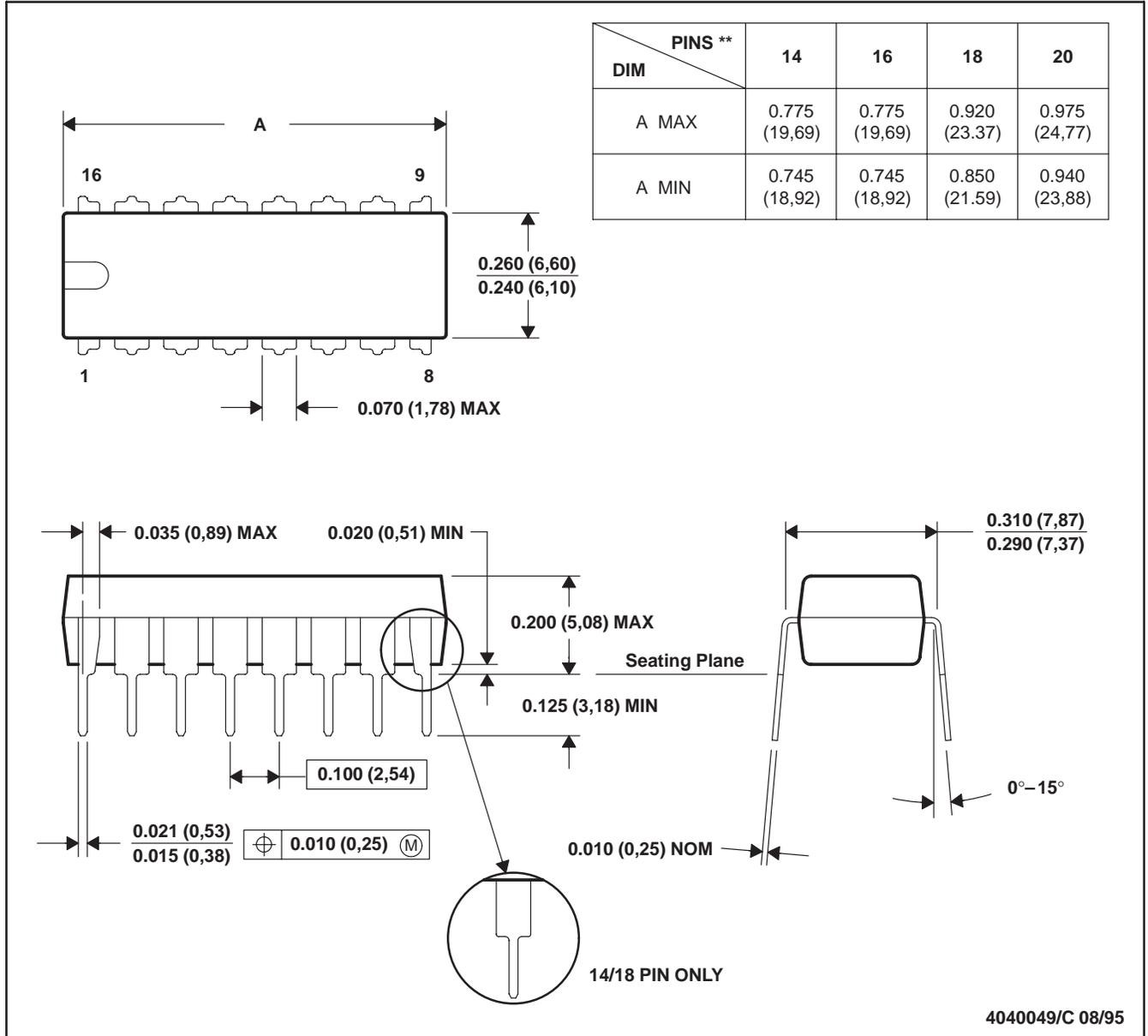
SLCS012B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

TLV2354, TLV2354Y LinCMOS™ QUADRUPLE LOW-VOLTAGE DIFFERENTIAL COMPARATORS

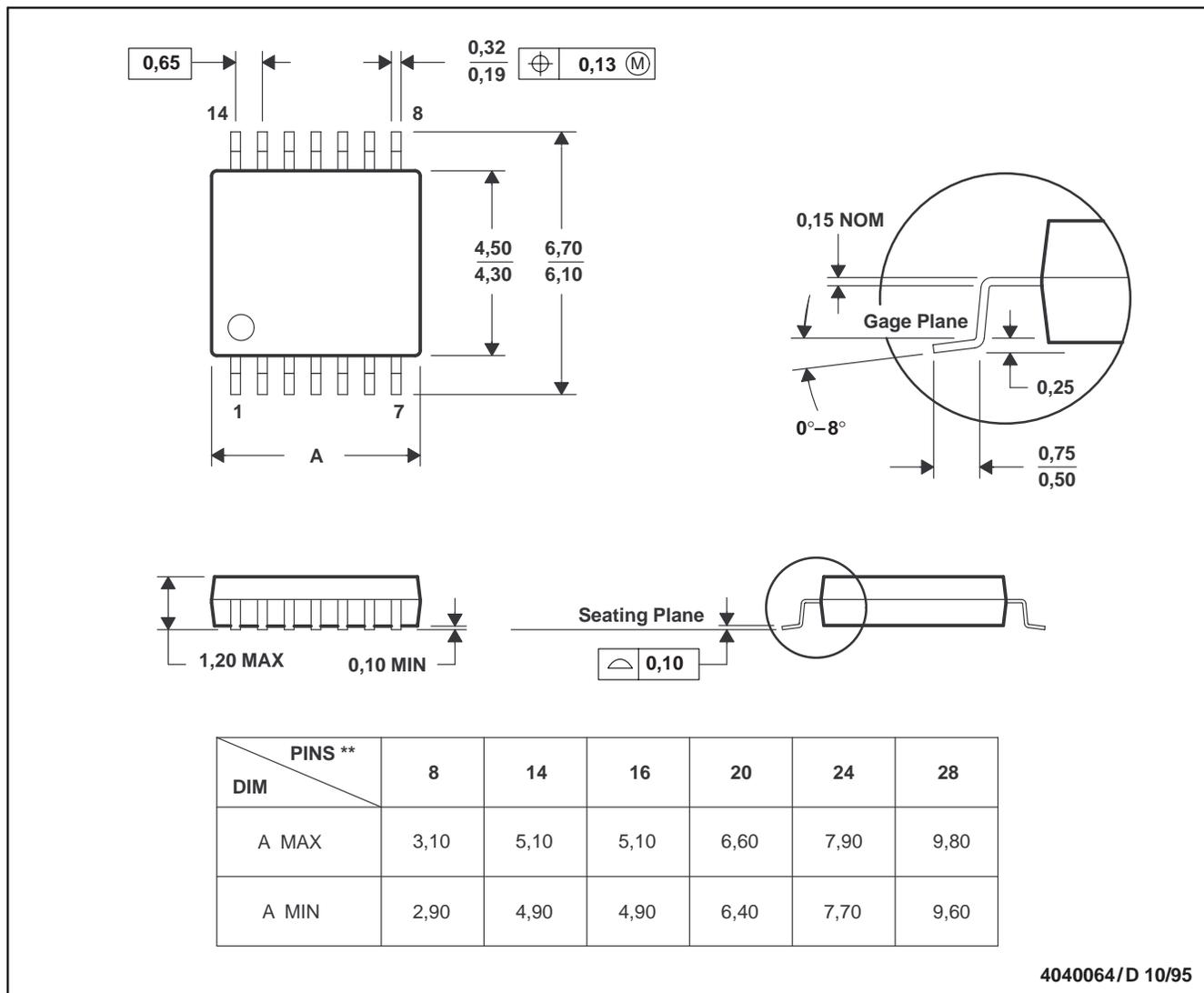
SLCS012B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



4040064/D 10/95

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

TLV2354, TLV2354Y

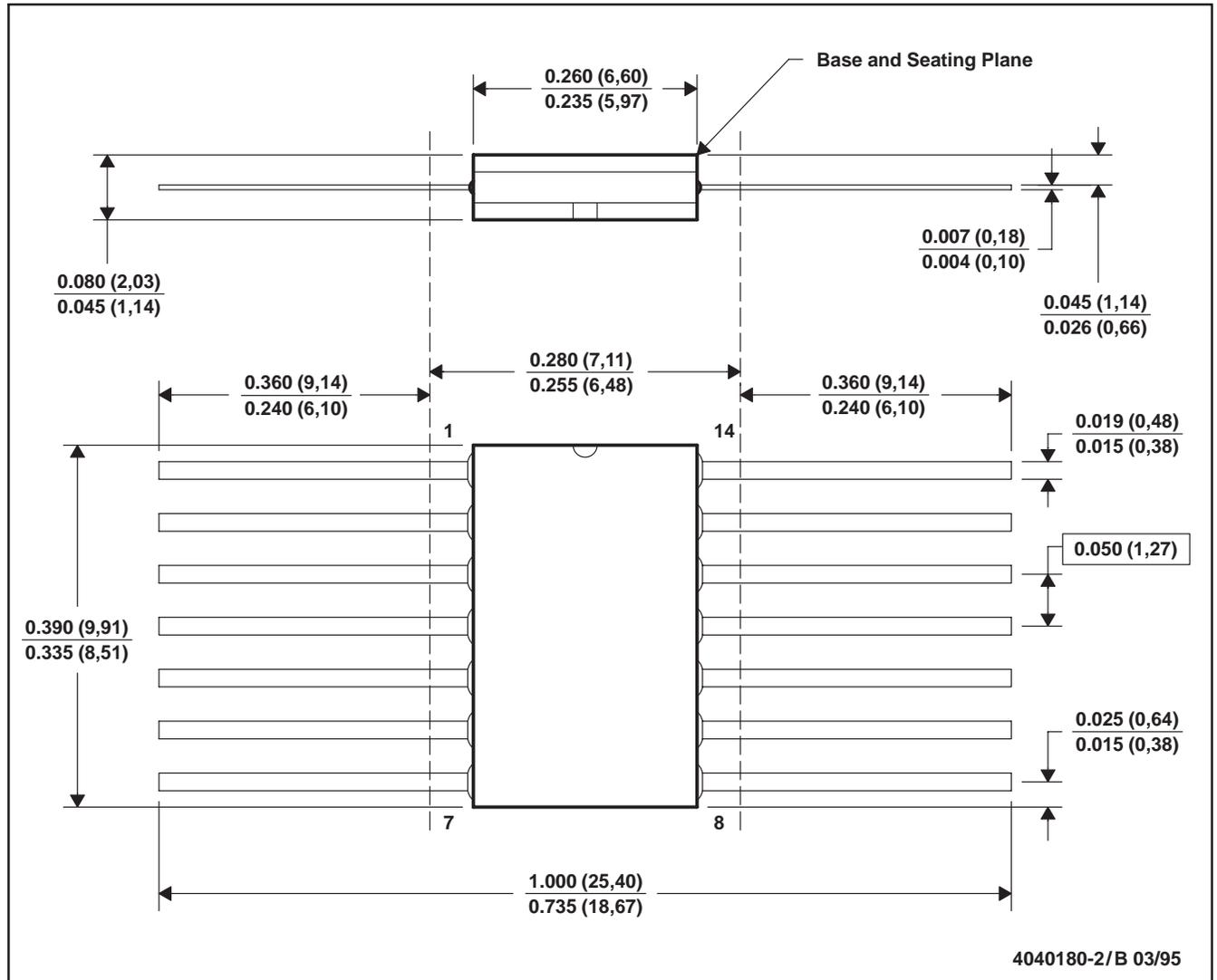
LinCMOS™ QUADRUPLE LOW-VOLTAGE DIFFERENTIAL COMPARATORS

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MECHANICAL INFORMATION

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

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