

International IOR Rectifier

Preliminary Data Sheet No. PD60083I

IR51H(D)224
IR51H(D)320
IR51H(D)420

SELF-OSCILLATING HALF BRIDGE

Features

- Output Power MOSFETs in half-bridge configuration
- High side gate drive designed for bootstrap operation
- Bootstrap diode integrated into package (HD type)
- Accurate timing control for both Power MOSFETs
Matched delay to get 50% duty cycle
Matched deadtime of 1.2 μ s
- Internal oscillator with programmable frequency

$$f = \frac{1}{1.4 \times (R_T + 75\Omega) \times C_T}$$

- 15.6V Zener clamped Vcc for offline operation
- Half-bridge output is out of phase with R_T
- Micropower startup

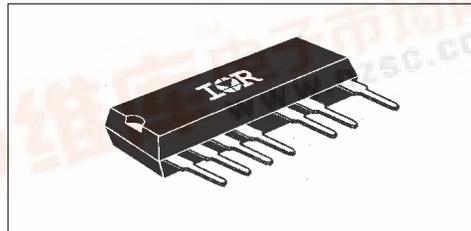
Description

The IR51H(D)XXX are complete high voltage, high speed, self-oscillating half-bridge circuits. Proprietary HVIC and latch immune CMOS technologies, along with the HEXFET[®] power MOSFET technology, enable ruggedized single package construction. The front-end features a programmable oscillator which functions similar to the CMOS 555 timer. The supply to the control circuit has a zener clamp to simplify offline operation. The output features two HEXFETs in a half-bridge configuration with an internally set deadtime designed for minimum cross-conduction in the half-bridge. Propagation delays for the high and low side

Product Summary

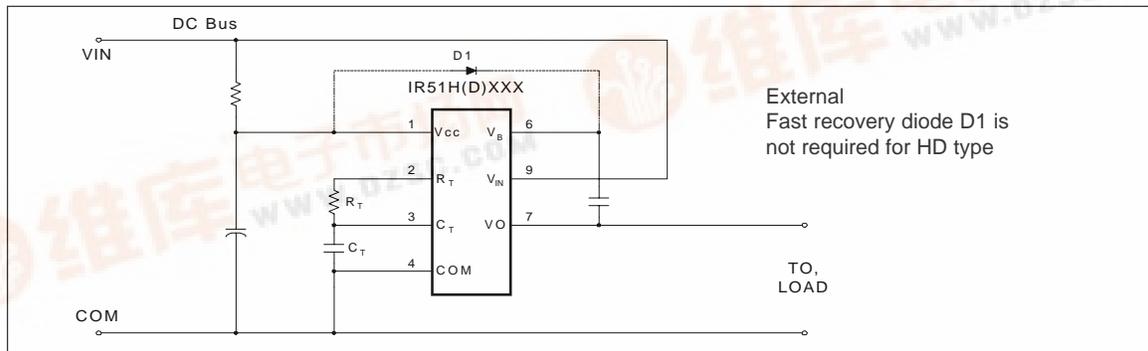
| | |
|---|--|
| V _{IN} (max) | 250V (IR51H(D)224) 400V (IR51H(D)310) 500V (IR51H(D)420) |
| Duty Cycle | 50% |
| Deadtime | 1.2 μ s |
| R _{ds(on)} | 1.1W (IR51H(D)224) 3.0W (IR51H(D)310) 3.6W (IR51H(D)420) |
| P _D (T _A = 25 $^{\circ}$ C) | 2.0W |

Package



power MOSFETs are matched to simplify use in 50% duty cycle applications. The device can operate up to 500 volts.

Typical Connection



IR51H(D)224
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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Minimum | Maximum | Units |
|-------------------|--|----------------------|-----------------------|-------|
| V _{IN} | High voltage supply | -224 | - 0.3 | 250 |
| | | -320 | - 0.3 | 400 |
| | | -420 | - 0.3 | 500 |
| V _B | High side floating supply | V _O - 0.3 | V _O +2.5 | V |
| V _O | Half-bridge output | -0.3 | V _{IN} + 0.3 | |
| V _{RT} | R _T voltage | - 0.3 | V _{CC} + 0.3 | |
| V _{CT} | C _T voltage | - 0.3 | V _{CC} + 0.3 | |
| I _{CC} | Supply current (note 1) | — | 25 | mA |
| I _{RT} | R _T output current | - 5 | 5 | |
| dV/dt | Peak diode recovery | — | 3.5 | V/ns |
| P _D | Package power dissipation @ T _A ≤ +25°C | — | 2.00 | W |
| R _{thJA} | Thermal resistance, junction to ambient | — | 60 | °C/W |
| T _J | Junction temperature | -55 | 150 | °C |
| T _S | Storage temperature | -55 | 150 | |
| T _L | Lead temperature (soldering, 10 seconds) | — | 300 | |

NOTE 1:

This IC contains a zener clamp structure between V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics Section

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation, the device should be used within the recommended conditions.

| Symbol | Definition | Minimum | Maximum | Units | |
|----------|---|----------------------------|-------------------|------------------|-----|
| V_B | High side floating supply absolute voltage | $V_O + 10$ | $V_O + V_{clamp}$ | V | |
| V_{IN} | High voltage supply | -224 | 250 | | |
| | | -320 | 400 | | |
| | | -420 | 500 | | |
| V_O | Half-bridge output voltage | -3.0 (note 2) | V_{IN} | A | |
| I_D | Continuous drain current ($T_A = 25^\circ\text{C}$) | -224 | 1.1 | | |
| | | -320 | 0.9 | | |
| | | -420 | 0.7 | | |
| | | $(T_A = 85^\circ\text{C})$ | -224 | | 0.7 |
| | | | -320 | | 0.6 |
| | | | -420 | | 0.5 |
| I_{CC} | Supply current | (note 3) | 5 | mA | |
| T_A | Ambient temperature | -40 | 125 | $^\circ\text{C}$ | |

NOTE 2:

Care should be taken to avoid switching conditions where the V_S node flies inductively below ground by more than 5V.

NOTE 3:

Enough current should be supplied to the V_{CC} lead of the IC to keep the internal 15.6V zener diode clamping the voltage at this lead.

Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 12\text{V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|----------|---|------|------|------|---------------|--|
| t_{rr} | Reverse recovery time (MOSFET body diode) | -224 | 200 | — | ns | $I_F = 1.1\text{A}$ $I_F = 900\text{mA}$ $I_F = 700\text{mA}$ $di/dt = 100$ |
| | | -320 | 270 | — | | |
| | | -420 | 240 | — | | |
| Q_{rr} | Reverse recovery charge (MOSFET body diode) | -224 | 0.7 | — | μC | $I_F = 1.1\text{A}$ $I_F = 900\text{mA}$ $I_F = 700\text{mA}$ $A/\mu\text{s}$ |
| | | -320 | 0.6 | — | | |
| | | -420 | 0.5 | — | | |
| D | R_T duty cycle | — | 50 | — | % | $f_{osc} = 20\text{ kHz}$ |

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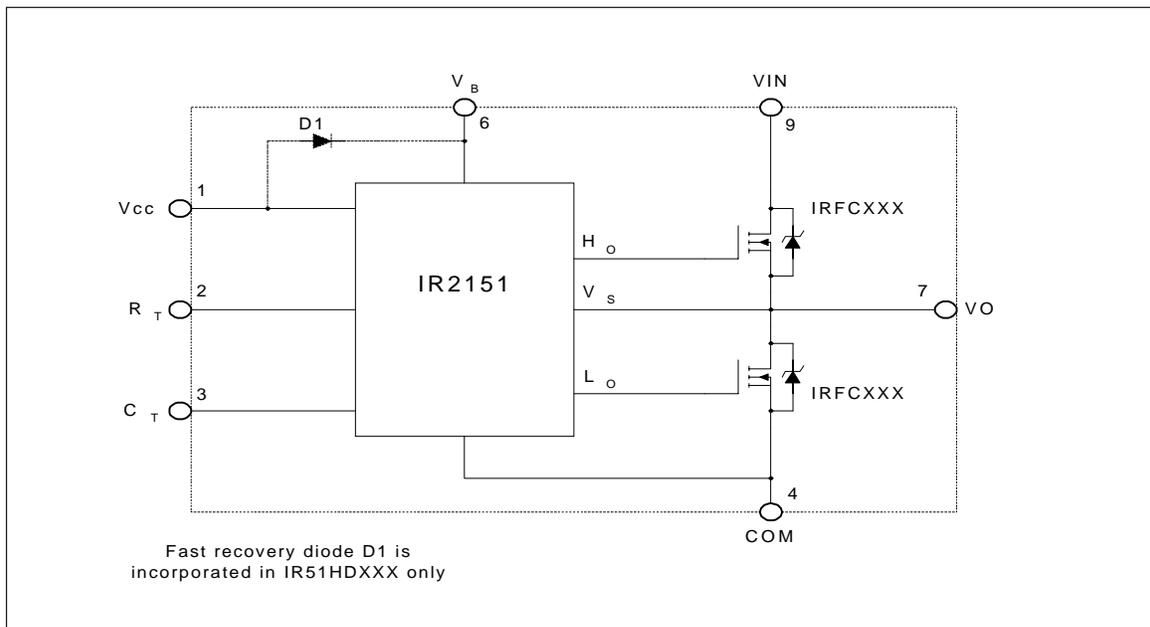
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Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_B) = 12V, T_A = 25^\circ C$ unless otherwise specified.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions | |
|-------------|---|------|-------|------|--|--|-----------------------------|
| V_{CCUV+} | V_{CC} supply undervoltage positive going threshold | — | 8.4 | — | V | | |
| V_{CCUV-} | V_{CC} supply undervoltage negative going threshold | — | 8.0 | — | V | | |
| I_{QCC} | Quiescent V_{CC} supply current | — | 300 | — | μA | $V_{CC} > V_{CCUV}$ | |
| V_{CLAMP} | V_{CC} zener shunt clamp voltage | — | 15.6 | — | V | $I_{CC} = 5mA$ | |
| I_{QBS} | Quiescent V_{BS} supply current | — | 30 | — | μA | | |
| I_{OS} | Offset supply leakage current | — | — | 50 | μA | $V_B = V_{IN} = 500V$ | |
| f_{OSC} | Oscillator frequency | — | 20 | — | kHz | $R_T = 35.7 k\Omega$ $C_T = 1 nF$ | |
| | | — | 100 | — | | $R_T = 7.04 k\Omega$ $C_T = 1 nF$ | |
| I_{CT} | C_T input current | — | 0.001 | 1.0 | μA | | |
| V_{CTUV} | C_T undervoltage lockout | — | 100 | — | mV | Note 2 | |
| V_{RT+} | R_T high level output voltage, $V_{CC} - R_T$ | — | 20 | — | | $I_{RT} = 100\mu A$ $I_{RT} = -1mA$ | |
| | | — | 200 | — | | $I_{RT} = 100\mu A$ $I_{RT} = -1mA$ | |
| V_{RT-} | R_T low level output voltage | — | 20 | — | $I_{RT} = 100\mu A$ $I_{RT} = -1mA$ | | |
| V_{RTUV} | R_T undervoltage lockout, $V_{CC} - R_T$ | — | 100 | — | | $I_{RT} = 100\mu A$ | |
| V_{CT+} | 2/3 V_{CC} threshold | — | 8.0 | — | kHz | | |
| V_{CT-} | 1/3 V_{CC} threshold | — | 4.0 | — | | | |
| Rds(on) | Static-drain-to-source on-resistance | -224 | — | 1.1 | Ω | $I_F = 1.1A$ | di/dt =100 A/ μs |
| | | -320 | — | 1.8 | | $I_F = 900mA$ | |
| | | -420 | — | 3.0 | | $I_F = 700mA$ | |
| VSD | Diode forward voltage | -224 | — | 0.85 | V | $I_F = 1.1A$ | |
| | | -320 | — | 0.7 | | $I_F = 900mA$ | |
| | | -420 | — | 0.8 | | $I_F = 700mA$ | |

Functional Block Diagram



Lead Definitions

| Symbol | Lead Description |
|-----------------|--|
| V _{CC} | Logic and internal gate drive supply voltage. An internal zener clamp diode at 15.6 V nominal is included to allow the V _{CC} to be current fed directly from VIN typically by means of a high value resistor. |
| R _T | Oscillator timing resistor output; a resistor is connected from R _T to C _T . RT is out of phase with the half-bridge output (VO). |
| C _T | Oscillator timing capacitor input; a capacitor is connected from C _T to COM in order to program the oscillator frequency according to the following equation: $f = \frac{1}{1.4 \times (R_T + 75\Omega) \times C_T}$ C _T PIN also invokes shutdown function (see note 2) where 75Ω is the effective impedance of the R _T output stage. |
| V _B | High side gate drive floating supply. For bootstrap operation a high voltage fast recovery diode is needed to feed from V _{CC} to V _B . (HD type circuits incorporate this diode). |
| V _{IN} | High voltage supply |
| VO | Half Bridge output |
| COM | Logic and low side of half bridge return |

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Lead Assignments

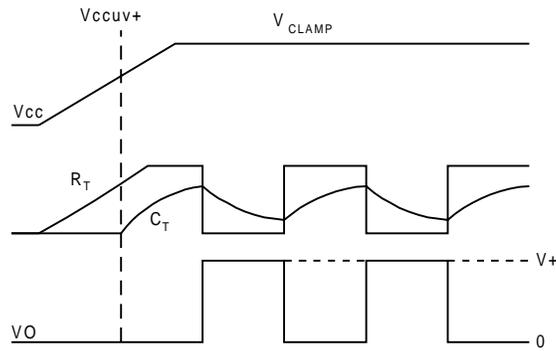
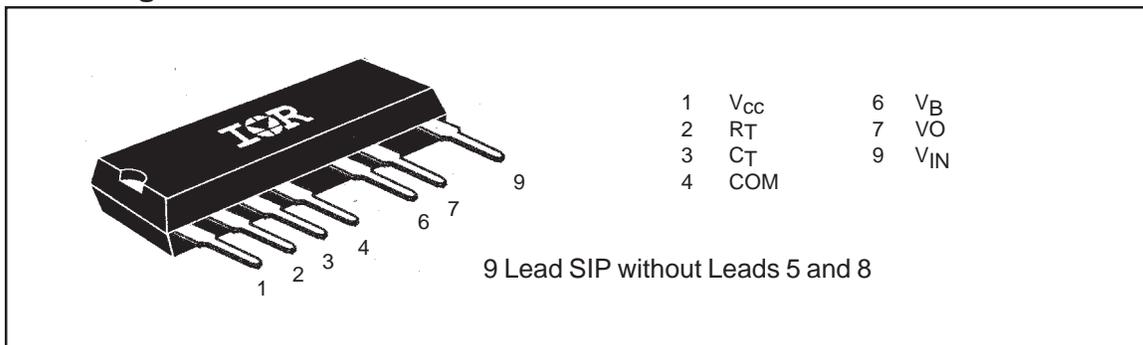


Figure 1. Input/Output Timing Diagram

Case Outline - 9 Lead SIP

