



### TRIPLE DIGITAL ISOLATORS

#### **FEATURES**

- 1, 25, and 150-Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew;
     1 ns max
  - Low Pulse-Width Distortion (PWD);2 ns max
  - Low Jitter Content; 1 ns Typ at 150 Mbps
- Typical 25-Year Life at Rated Working Voltage (see application note SLLA197 and Figure 14)
- 4000-V<sub>peak</sub> Isolation, 560-V<sub>peak</sub> Working Voltage
- UL 1577 Certified
- 4 kV ESD Protection
- Operate With 3.3-V or 5-V Supplies

- High Electromagnetic Immunity (see application note SLLA181)
- -40°C to 125°C Operating Range

#### **APPLICATIONS**

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

### **DESCRIPTION**

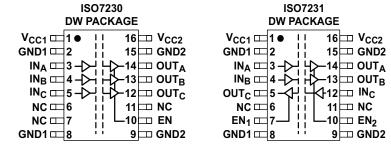
The ISO7230 and ISO7231 are triple-channel digital isolators each with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by Tl's silicon dioxide (SiO<sub>2</sub>) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

The ISO7230 triple-channel device has all three channels in the same direction while the ISO7231 has two channels in one direction and one channel in opposition. These devices have an active-high output enable that when driven to a low level, places the output in a high-impedance state and turns off internal bias circuitry to conserve power.

The ISO7230A, ISO7231C, ISO7231A, and ISO7231C have TTL input thresholds and a noise-filter at the input that prevents transient pulses of up to 2 ns in duration from being passed to the output of the device, while the ISO7230M and ISO7231M have CMOS  $V_{\rm CC}/2$  input thresholds and do not have the input noise-filter or the additional propagation delay.

In each device a periodic update pulse is sent across the isolation barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (Contact TI for a logic low failsafe option).

These devices require two supply voltages of 3.3-V, 5-V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS. These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### **FUNCTION DIAGRAM**

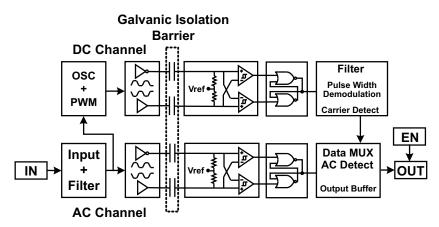


Table 1. Device Function Table ISO723x (1)

V <sub>CC1</sub>	V <sub>CC2</sub>	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
		Н	H or Open	Н
PU	PU	L	H or Open	L
PU	PU	Х	L	Z
		Open	H or Open	Н
PD	PU	Х	H or Open	Н
PD	PU	Х	L	Z

(1) PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level

#### **AVAILABLE OPTIONS**

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION	MARKED AS	ORDERING NUMBER <sup>(1)</sup>		
ISO7230ADW	1 Mbps	~1.5 V (TTL)		ISO7230A	ISO7230ADW (rail)		
1307230ADW	i iviops	(CMOS compatible)		1301230A	ISO7230ADWR (reel)		
1007000DW	OF Mhma	~1.5 V (TTL)	3/0	ISO7230C	ISO7230CDW (rail)		
ISO7230CDW	25 Mbps	(CMOS compatible)	3/0	15072300	ISO7230CDWR (reel)		
ICOZO20MDW	450 Mb = 5	\/aa/0 (OMOC)		ISO7230M	ISO7230MDW (rail)		
ISO7230MDW	150 Mbps	Vcc/2 (CMOS)		1507230IVI	ISO7230MDWR (reel)		
1007004 A DVA/	4 Mb = 5	~1.5 V (TTL)		10070244	ISO7231ADW (rail)		
ISO7231ADW	1 Mbps	(CMOS compatible)		ISO7231A	ISO7231ADWR (reel)		
1007004 CDW	OF Mhma	~1.5 V (TTL)	0/4	10070040	ISO7231CDW (rail)		
ISO7231CDW	25 Mbps	(CMOS compatible)	2/1	ISO7231C	ISO7231CDWR (reel)		
1007004MDW 450 Mb		Vec/2 (CMOC)		ICO7224M	ISO7231MDW (rail)		
ISO7231MDW	150 Mbps	Vcc/2 (CMOS)		ISO7231M	ISO7231MDWR (reel)		

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI
website at www.ti.com.



### ABSOLUTE MAXIMUM RATINGS(1)

					VALUE	UNIT
$V_{CC}$	Supply voltage	ge <sup>(2)</sup> , V <sub>CC1</sub> , V <sub>CC2</sub>			-0.5 to 6	V
$V_{I}$	Voltage at IN	, OUT, EN			-0.5 to 6	V
Io	Output current				±15	mA
	'	Human Body Model	JEDEC Standard 22, Test Method A114-C.01		±4	
ESD	Electrostatic discharge	Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1	kV
		Machine Model	ANSI/ESDS5.2-1996		±200	V
$T_{J}$	Maximum jur	action temperature			170	°C

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### **RECOMMENDED OPERATING CONDITIONS**

			MIN	TYP	MAX	UNIT
.,	Complex soltens V		4.5		5.5	V
V <sub>CC</sub>	Supply voltage, V <sub>CC1</sub> , V <sub>CC2</sub>		3.15		3.6	V
I <sub>OH</sub>	High-level output current				4	mA
I <sub>OL</sub>	Low-level output current		-4			mA
		ISO723xA	1			μs
t <sub>ui</sub>	Input pulse width	ISO723xC	40			
		ISO723xM	6.67	5		ns
		ISO723xA	0	1500 <sup>(1)</sup>	1000	kbps
1/t <sub>ui</sub>	<sub>ui</sub> Signaling rate	ISO723xC	0	30 <sup>(1)</sup>	25	N.41
		ISO723xM	0	200 <sup>(1)</sup>	150	Mbps
$V_{IH}$	High-level input voltage (IN)	100702014	0.7 V <sub>CC</sub>		V <sub>CC</sub>	V
$V_{IL}$	Low-level input voltage (IN)	ISO723xM	0		0.3 V <sub>CC</sub>	V
$V_{IH}$	High-level input voltage (IN) (EN on all devices)	ICO722VA ICO722VC	2		V <sub>CC</sub>	V
$V_{IL}$	Low-level input voltage (IN) (EN on all devices)	- ISO723xA, ISO723xC	0		0.8	V
TJ	Junction temperature				150	°C
Н	External magnetic field-strength immunity per IEC certification	C 61000-4-8 and IEC 61000-4-9			1000	A/m

<sup>(1)</sup> Typical sigalling rate under ideal conditions at 25°C.

<sup>(2)</sup> All voltage values are with respect to network ground terminal and are peak voltage values.



### **ELECTRICAL CHARACTERISTICS**

 $V_{\text{CC1}}$  and  $V_{\text{CC2}}$  at 5-V operation, over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN TYP	MAX	UNIT
SUPPLY	CURRENT					
	ISO7230A/C/M	Quiescent		1	3	
	ISO7230A	1 Mbps	$V_1 = V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V	1	3	mA
	ISO7230C/M	25 Mbps	LIN2 at 3 V	7	9.5	
I <sub>CC1</sub>	ISO7231A/C/M	Quiescent	., ., .,	6.5	11	
	ISO7231A	1 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V	6.5	11	mA
	ISO7231C/M	25 Mbps		11	17	
	ISO7230A/C/M	Quiescent		15	22	
	ISO7230A	1 Mbps	$V_1 = V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V	16	22	mA
	ISO7230C/M	25 Mbps	2.172 dt 0 7	17	24	
I <sub>CC2</sub>	ISO7231A/C/M	Quiescent		13	20	
	ISO7231A	1 Mbps	$V_1 = V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V	13	20	mA
	ISO7231C/M	25 Mbps		17.5	27	
ELECTR	ICAL CHARACTERISTICS					
I <sub>OFF</sub>	Sleep mode output curren	t	EN at VCC, Single channel	0		μΑ
\/	High-level output voltage		I <sub>OH</sub> = -4 mA, See Figure 1	V <sub>CC</sub> - 0.8		V
V <sub>OH</sub>	nign-ievei output voitage		I <sub>OH</sub> = -20 μA, See Figure 1	V <sub>CC</sub> - 0.1		V
\/	Low-level output voltage		I <sub>OL</sub> = 4 mA, See Figure 1		0.4	V
$V_{OL}$	Low-level output voltage		I <sub>OL</sub> = 20 μA, See Figure 1		0.1	
V <sub>I(HYS)</sub>	Input voltage hysteresis			150		mV
I <sub>IH</sub>	High-level input current		INI from 0 V/ to V/		10	
I <sub>IL</sub>	Low-level input current		IN from 0 V to V <sub>CC</sub>	-10		μΑ
C <sub>I</sub>	Input capacitance to grour	nd	IN at V <sub>CC</sub> , V <sub>I</sub> = 0.4 sin (4E6πt)	2		pF
CMTI	Common-mode transient i	mmunity	V <sub>I</sub> = V <sub>CC</sub> or 0 V, See Figure 4	25 50		kV/μs



### **SWITCHING CHARACTERISTICS**

V<sub>CC1</sub> and V<sub>CC2</sub> at 5-V operation, over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay	10070244		40		95	
PWD	Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	ISO723xA				10	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay	ISO723xC	See Figure 4	18		42	ns
PWD	Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	130723XC	See Figure 1			2.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay	ISO723xM		10		23	20
PWD	Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	130723XIVI			1	2	ns
	Character shared autout along (2)	ISO723xA/C			0	2	
t <sub>sk(o)</sub>	Channel-to-channel output skew (2)	ISO723xM			0	1	ns
t <sub>r</sub>	Output signal rise time		See Figure 4		2		
t <sub>f</sub>	Output signal fall time		See Figure 1		2		ns
t <sub>PHZ</sub>	Propagation delay, high-level-to-high-im	pedance output			15	20	
t <sub>PZH</sub>	Propagation delay, high-impedance-to-h	nigh-level output	0 5'		15	20	
t <sub>PLZ</sub>	Propagation delay, low-level-to-high-imp	pedance output	See Figure 2		15	20	ns
t <sub>PZL</sub>	Propagation delay, high-impedance-to-l	ow-level output			15	20	•
t <sub>fs</sub>	Failsafe output delay time from input power loss		See Figure 3		12		μs
t <sub>jit(pp)</sub>	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity inputon all channels, See Figure 5		1		ns

<sup>(1)</sup> Also referred to as pulse skew.

t<sub>sk(o)</sub> is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.



### **ELECTRICAL CHARACTERISTICS**

 $V_{\text{CC1}}$  at 5-V,  $V_{\text{CC2}}$  at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

	PARAMETE	R	TEST CONDITION	NS	MIN	TYP	MAX	UNIT
SUPPLY	CURRENT							
	ISO7230A/C/M	Quiescent				1	3	
	ISO7230A	1 Mbps	V <sub>I</sub> = V <sub>CC</sub> or 0 V, All channels, no I	oad, EN <sub>2</sub> at 3 V		1	3	mA
	ISO7230C/M	25 Mbps				7	9.5	
I <sub>CC1</sub>	ISO7231A/C/M	Quiescent				6.5	11	
	ISO7231A	1 Mbps	V <sub>I</sub> = V <sub>CC</sub> or 0 V, All channels, no I EN <sub>2</sub> at 3 V	oad, EN <sub>1</sub> at 3 V,		6.5	11	mA
	ISO7231C/M	25 Mbps	Live at 5 v			11	17	
	ISO7230A/C/M	Quiescent				9	15	
	ISO7230A	1 Mbps	V <sub>I</sub> = V <sub>CC</sub> or 0 V, All channels, no I	oad, EN <sub>2</sub> at 3 V		9.5	15	mA
	ISO7230C/M	25 Mbps				10	17	
I <sub>CC2</sub>	ISO7231A/C/M	Quiescent		V V and V All sharpele no load EN at 2 V				
	ISO7231A	1 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V			8	12	mA
	ISO7231C/M	25 Mbps	LIV2 at 3 V	2.12 4. 0 7				
ELECTR	RICAL CHARACTER	RISTICS			II.			
I <sub>OFF</sub>	Sleep mode outp	ut current	EN at VCC, Single channel			0		μΑ
				ISO7230	V <sub>CC</sub> - 0.4			
$V_{OH}$	High-level output	voltage	I <sub>OH</sub> = -4 mA, See Figure 1	ISO7231 (5-V side)	V <sub>CC</sub> - 0.8			V
			$I_{OH} = -20 \mu A$ , See Figure 1		V <sub>CC</sub> - 0.1			
1/	I avvilaval avviavit		I <sub>OL</sub> = 4 mA, See Figure 1				0.4	V
$V_{OL}$	Low-level output	voitage	I <sub>OL</sub> = 20 μA, See Figure 1				0.1	V
V <sub>I(HYS)</sub>	Input voltage hys	teresis				150		mV
I <sub>IH</sub>	High-level input of	current	N/ 0 // //				10	
I <sub>IL</sub>	Low-level input co	urrent	IN from 0 V to V <sub>CC</sub>		-10			μΑ
Cı	Input capacitance	e to ground	IN at $V_{CC}$ , $V_I = 0.4 \sin (4E6\pi t)$			2		pF
CMTI	Common-mode to immunity	ransient	V <sub>I</sub> = V <sub>CC</sub> or 0 V, See Figure 4		25	50		kV/μs



### **SWITCHING CHARACTERISTICS**

V<sub>CC1</sub> at 5-V, V<sub>CC2</sub> at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH},t_{PHL}$	Propagation delay, low-to-high-level output	ISO723xA		40		100	
PWD	Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>					11	20
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay, low-to-high-level output	ISO723xC	See Figure 1	20		50	ns
PWD	Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>					3	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay, low-to-high-level output	ISO723xM		12		29	ns
PWD	Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $				1	2	
	Channel-to-channel output skew (2)				0	2.5	20
t <sub>sk(o)</sub>	Charmer to-charmer output skew	ISSO723xM			0	1	ns
t <sub>r</sub>	Output signal rise time		See Figure 1		2		20
t <sub>f</sub>	Output signal fall time		See Figure 1		2		ns
t <sub>PHZ</sub>	Propagation delay, high-level-to-high-impe	dance output			15	20	
t <sub>PZH</sub>	Propagation delay, high-impedance-to-high	n-level output	Soo Figure 2		15	20	
t <sub>PLZ</sub>	Propagation delay, low-level-to-high-imped	lance output	See Figure 2		15	20	ns
t <sub>PZL</sub>	Propagation delay, high-impedance-to-low-level output				15	20	
t <sub>fs</sub>	Failsafe output delay time from input power	See Figure 3		18		μs	
t <sub>jit(pp)</sub>	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 5		1		ns

 <sup>(1)</sup> Also known as pulse skew
 (2) t<sub>sk(o)</sub> is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.



### **ELECTRICAL CHARACTERISTICS**

 $V_{\text{CC1}}$  at 3.3-V,  $V_{\text{CC2}}$  at 5-V operation, over recommended operating conditions (unless otherwise noted)

	PARAMETE	R	TEST CONDITION	IS	MIN	TYP	MAX	UNIT
SUPPLY	CURRENT							
	ISO7230A/C/M	Quiescent				0.5	1	
	ISO7230A	1 Mbps	V <sub>I</sub> = V <sub>CC</sub> or 0 V, All channels, no le	oad, EN <sub>2</sub> at 3 V		1	2	mA
	ISO7230C/M	25 Mbps				3	5	
I <sub>CC1</sub>	ISO7231A/C/M	Quiescent				4.5	7	
	ISO7231A	1 Mbps	V <sub>I</sub> = V <sub>CC</sub> or 0 V, All channels, no le EN <sub>2</sub> at 3 V	oad, EN <sub>1</sub> at 3 V,		4.5	7	mA
	ISO7231C/M	25 Mbps	Live at 5 v			6.5	11	
	ISO7230A/C/M	Quiescent					22	
	ISO7230A	1 Mbps	V <sub>I</sub> = V <sub>CC</sub> or 0 V, All channels, no l	oad, EN <sub>2</sub> at 3 V		16	22	mA
	ISO7230C/M	25 Mbps				17	24	
I <sub>CC2</sub>	ISO7231A/C/M	Quiescent				13	20	
	ISO7231A	1 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no leading $EN_2$ at 3 V		13	20	mA	
ISO7231C/M		25 Mbps	Live at 5 V		17.5	27		
ELECTR	RICAL CHARACTER	RISTICS						
I <sub>OFF</sub>	Sleep mode outp	ut current	EN at VCC, Single channel			0		μΑ
			I <sub>OH</sub> = -4 mA, See Figure 1 ISO7230		V <sub>CC</sub> - 0.4			
$V_{OH}$	High-level output	voltage		ISO7231 (5-V side)	V <sub>CC</sub> - 0.8			V
			$I_{OH} = -20 \mu A$ , See Figure 1		V <sub>CC</sub> - 0.1			
	Landanal andana	11	I <sub>OL</sub> = 4 mA, See Figure 1	1			0.4	V
$V_{OL}$	Low-level output	voitage	I <sub>OL</sub> = 20 μA, See Figure 1				0.1	V
V <sub>I(HYS)</sub>	Input voltage hys	teresis				150		mV
I <sub>IH</sub>	High-level input of	current	IN CONTRACTOR OF THE PROPERTY				10	
I <sub>IL</sub>	Low-level input co	urrent	IN from 0 V to V <sub>CC</sub>		-10			μΑ
Cı	Input capacitance	e to ground	IN at $V_{CC}$ , $V_{I} = 0.4 \sin (4E6\pi t)$	IN at $V_{CC}$ , $V_{I} = 0.4 \sin (4E6\pi t)$		2		pF
CMTI	Common-mode to immunity	ransient	V <sub>I</sub> = V <sub>CC</sub> or 0 V, See Figure 4		25	50		kV/μs



### **SWITCHING CHARACTERISTICS**

V<sub>CC1</sub> at 3.3-V and V<sub>CC2</sub> at 5-V operation, over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay	ISO723xA		40		100	
PWD	Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	150723XA				11	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay	10072240	Can Figure 4	22		51	
PWD	Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	ISO723xC	See Figure 1			3	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay	100700-14		12		30	
PWD	Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	ISO723xM			1	2	
	Oh   4	ISO723xA/C			0	2.5	
t <sub>sk(o)</sub>	o) Channel-to-channel output skew (2)	ISO723xM			0	1	ns
t <sub>r</sub>	Output signal rise time		See Figure 1		2		
t <sub>f</sub>	Output signal fall time				2		ns
t <sub>PHZ</sub>	Propagation delay, high-level-to-high-impedar	ice output			15	20	
t <sub>PZH</sub>	Propagation delay, high-impedance-to-high-le	vel output	Can Figure 0		15	20	
t <sub>PLZ</sub>	Propagation delay, low-level-to-high-impedance	ce output	See Figure 2		15	20	ns
t <sub>PZL</sub>	Propagation delay, high-impedance-to-low-lev	el output			15	20	
t <sub>fs</sub>	Failsafe output delay time from input power loss		See Figure 3		12		μs
t <sub>jit(pp)</sub>	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 5		1		ns

 <sup>(1)</sup> Also known as pulse skew
 (2) t<sub>sk(o)</sub> is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.



### **ELECTRICAL CHARACTERISTICS**

 $V_{\text{CC1}}$  and  $V_{\text{CC2}}$  at 3.3 V operation, over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY	CURRENT						
	ISO7230A/C/M	Quiescent			0.5	1	
	ISO7230A	1 Mbps	$V_1 = V_{CC}$ or 0 V, all channels, no load, $EN_2$ at 3 V		1	2	mA
	ISO7230C/M	25 Mbps			3	5	
I <sub>CC1</sub>	ISO7231A/C/M	Quiescent			4.5	7	
ı	ISO7231A	1 Mbps	$V_1 = V_{CC}$ or 0 V, all channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V		4.5	7	mA
	ISO7231C/M	25 Mbps			0.5 1 3 4.5 4.5 6.5 9 9.5 10 8 8 10.5 0 - 0.4 - 0.1	11	
	ISO7230A/C/M	Quiescent			9	15	
	ISO7230A	1 Mbps	$V_1 = V_{CC}$ or 0 V, all channels, no load, $EN_2$ at 3 V		9.5	15	mA
	ISO7230C/M	25 Mbps			10	17	
I <sub>CC2</sub>	ISO7231A/C/M	Quiescent			12		
	100120000	1 Mbps	V <sub>I</sub> = V <sub>CC</sub> or 0 V, all channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V		8	12	mA
	ISO7231C/M	25 Mbps	1 , 2		10.5	1 2 3 5 4.5 7 4.5 7 6.5 11 9 15 9.5 15 10 17 8 12 8 12 10.5 16 0 0.4 0.1 150 10	
ELECTR	ICAL CHARACTERISTICS						
I <sub>OFF</sub>	Sleep mode output current		EN at V <sub>CC</sub> , single channel		0		μΑ
$V_{OH}$	High-level output voltage		I <sub>OH</sub> = -4 mA, See Figure 1	V <sub>CC</sub> - 0.4			V
OH	r ligit-level output voltage		$I_{OH} = -20 \mu A$ , See Figure 1	V <sub>CC</sub> - 0.1			V
$V_{OL}$	Low-level output voltage		I <sub>OL</sub> = 4 mA, See Figure 1			0.4	V
VOL	Low-level output voltage		I <sub>OL</sub> = 20 μA, See Figure 1			0.1	V
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
$I_{\mathrm{IH}}$	High-level input current		IN from 0 V or V <sub>CC</sub>			10	μА
$I_{\rm IL}$	Low-level input current		IN HOLL O A OL ACC	-10			μΑ
C <sub>I</sub>	Input capacitance to ground	<u> </u>	IN at $V_{CC}$ , $V_I = 0.4 \sin (4E6\pi t)$		2		pF
CMTI	Common-mode transient immu	nity	V <sub>I</sub> = V <sub>CC</sub> or 0 V, See Figure 4	25	50		kV/μs



### **SWITCHING CHARACTERISTICS**

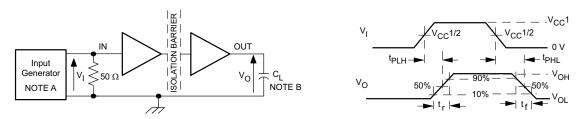
 $V_{CC1}$  and  $V_{CC2}$  at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay	ISO723xA		45		110	
PWD	Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	150723XA				12	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay	ISO723xC	See Figure 4	25		56	
PWD	Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	150723XC	See Figure 1			4	ns
t <sub>pLH</sub> , t <sub>pHL</sub>	Propagation delay	ISO722xM		12		34	ns
PWD	Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	150722XIVI			1	2	
	Channel to shannel output alsour (2)	ISO723xA/C			0	3	
t <sub>sk(o)</sub>	Channel-to-channel output skew (2)	ISO723xM			0	1	ns
t <sub>r</sub>	Output signal rise time		See Figure 1		2		
t <sub>f</sub>	Output signal fall time				2		ns
t <sub>PHZ</sub>	Propagation delay, high-level-to-high-impe	edance output			15	20	
t <sub>PZH</sub>	Propagation delay, high-impedance-to-hig	h-level output	0 Firm 0		15	20	
t <sub>PLZ</sub>	Propagation delay, low-level-to-high-imper	dance output	See Figure 2		15	20	ns
t <sub>PZL</sub>	Propagation delay, high-impedance-to-low-level output				15	20	
t <sub>fs</sub>	Failsafe output delay time from input power loss		See Figure 3		18		μs
t <sub>jit(pp)</sub>	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, same polarity input on all channels, See Figure 5		1		ns

 <sup>(1)</sup> Also referred to as pulse skew.
 (2) t<sub>sk(o)</sub> is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

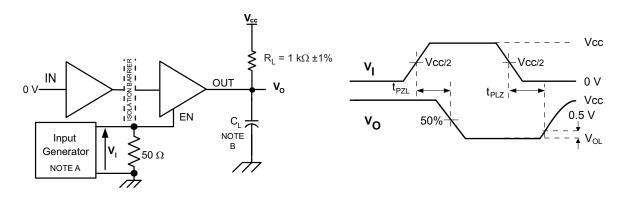


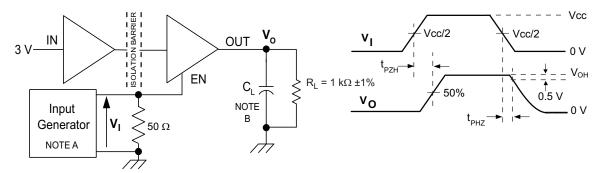
#### PARAMETER MEASUREMENT INFORMATION



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns,  $Z_O = 50\Omega$ .
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



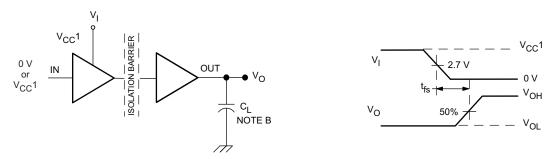


- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns,  $Z_O = 50\Omega$ .
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

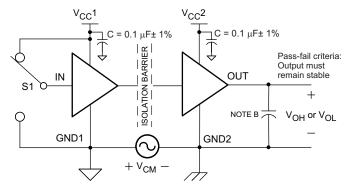


### PARAMETER MEASUREMENT INFORMATION (continued)



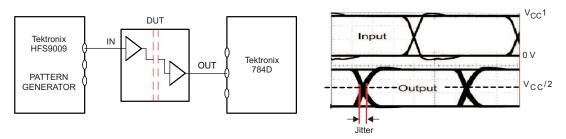
- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns,  $Z_O = 50\Omega$ .
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns,  $Z_O = 50\Omega$ .
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



NOTE: PRBS bit pattern run length is  $2^{16} - 1$ . Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 5. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform



### **DEVICE INFORMATION**

### **PACKAGE CHARACTERISTICS**

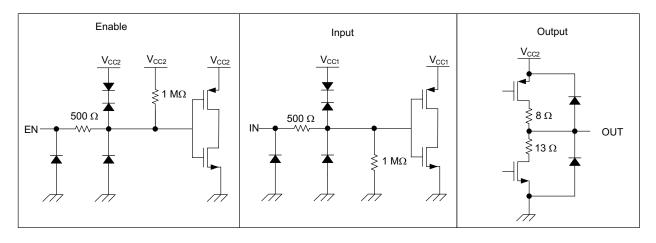
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	7.7			mm
L(102)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R <sub>IO</sub>	Isolation resistance	Input to output, $V_{IO}$ = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, $T_A < 100^{\circ} C$		>10 <sup>12</sup>		Ω
		Input to output, $V_{IO} = 500 \text{ V}$ , $100^{\circ}\text{C} \le T_{A} \le T_{A} \text{ max}$		>10 <sup>11</sup>		Ω
C <sub>IO</sub>	Barrier capacitance Input to output	V <sub>I</sub> = 0.4 sin (4E6πt)		2		pF
Cı	Input capacitance to ground	$V_I = 0.4 \sin (4E6\pi t)$		2		pF

### **REGULATORY INFORMATION**

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program <sup>(1)</sup>
File Number: Pending	File Number: Pending	File Number: E181974

<sup>(1)</sup> Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

### **DEVICE I/O SCHEMATICS**





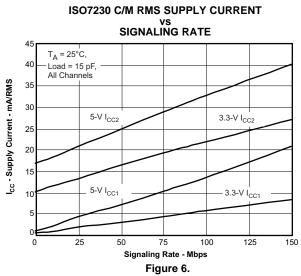
#### THERMAL CHARACTERISTICS

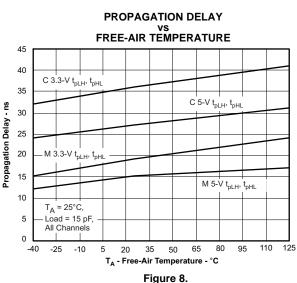
over recommended operating conditions (unless otherwise noted)

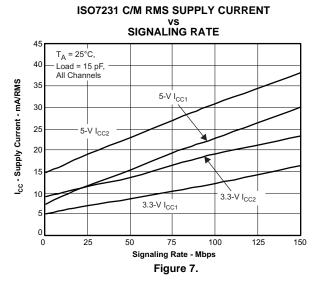
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
0	lunation to air	Low-K Thermal Resistance <sup>(1)</sup>		168		°C/W
θ <sub>JA</sub> Junction-to-air		High-K Thermal Resistance		96.1		C/VV
$\theta_{JB}$	Junction-to-Board Thermal Resistance			61		°C/W
$\theta_{\text{JC}}$	Junction-to-Case Thermal Resistance			48		°C/W
P <sub>D</sub>	Device Power Dissipation	$V_{CC1} = V_{CC2} = 5.5 \text{ V}, T_J = 150^{\circ}\text{C}, C_L = 15 \text{ pF},$ Input a 50% duty cycle square wave	·		220	mW

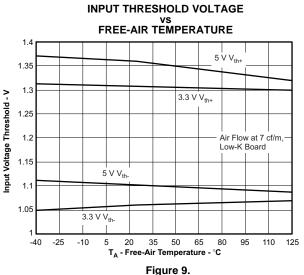
<sup>(1)</sup> Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

### TYPICAL CHARACTERISTIC CURVES



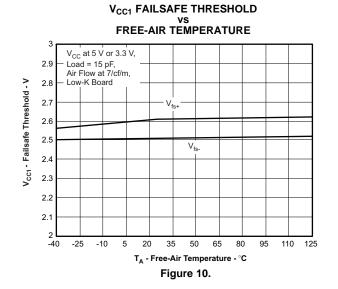


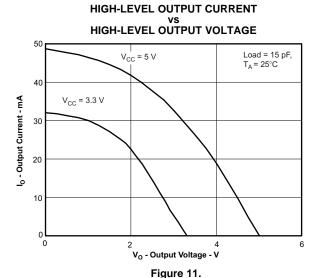




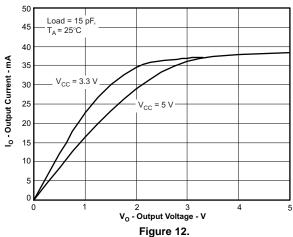


### **TYPICAL CHARACTERISTIC CURVES (continued)**





# LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE





### **APPLICATION INFORMATION**

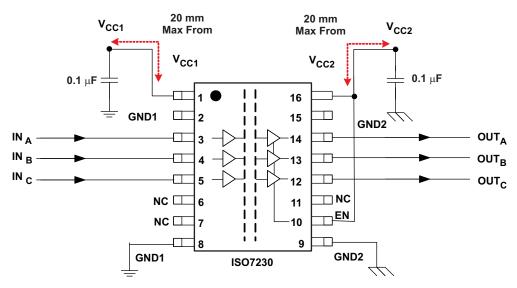


Figure 13. Typical ISO723x Application Circuit

### LIFE EXPECTANCY vs WORKING VOLTAGE

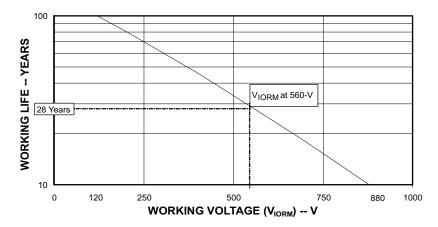


Figure 14. Time Dependant Dielectric Breakdown Testing Results



### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
ISO7230ADW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230ADWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230ADWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230CDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230CDWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230MDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230MDWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7230MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231ADW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231ADWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231ADWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231CDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231CDWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231MDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231MDWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7231MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

 $<sup>^{(1)}</sup>$  The marketing status values are defined as follows:



#### PACKAGE OPTION ADDENDUM

20-Mar-2008

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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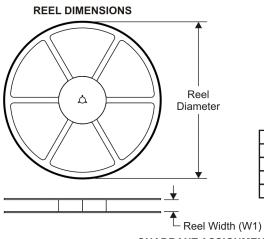
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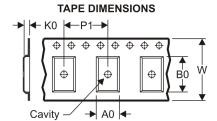




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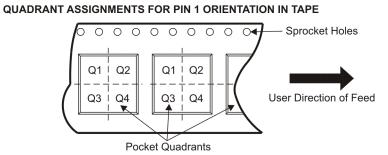
### TAPE AND REEL INFORMATION





I		Dimension designed to accommodate the component width
ſ	B0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
ſ	W	Overall width of the carrier tape
Ι	P1	Pitch between successive cavity centers

- Reel Width (WT)



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7230ADWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1
ISO7230CDWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1
ISO7230MDWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1
ISO7231ADWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1
ISO7231CDWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1
ISO7231MDWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1



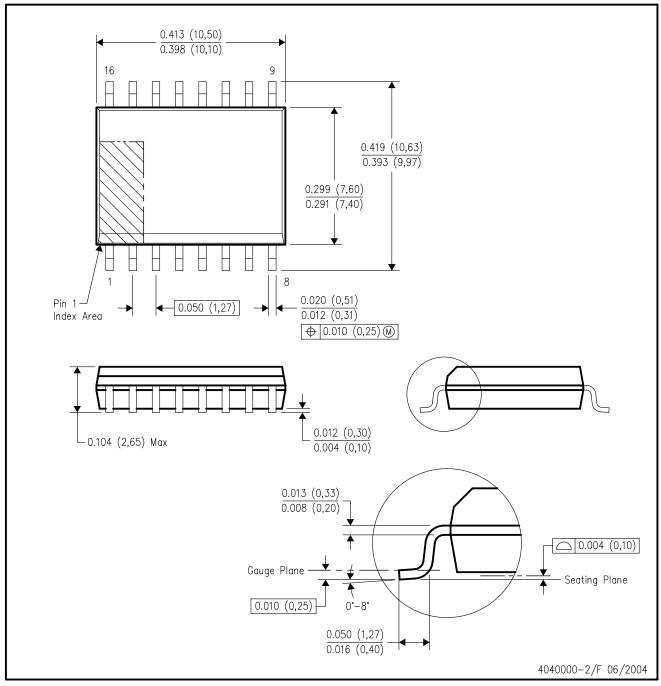


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7230ADWR	SOIC	DW	16	2000	406.0	348.0	63.0
ISO7230CDWR	SOIC	DW	16	2000	406.0	348.0	63.0
ISO7230MDWR	SOIC	DW	16	2000	406.0	348.0	63.0
ISO7231ADWR	SOIC	DW	16	2000	406.0	348.0	63.0
ISO7231CDWR	SOIC	DW	16	2000	406.0	348.0	63.0
ISO7231MDWR	SOIC	DW	16	2000	406.0	348.0	63.0

## DW (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



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