



## 9-BIT LATCHED ECL-TO-TTL

**SY10H603**  
**SY100H603**

### FEATURES

- 9-bit ideal for byte-parity applications
- 3-state TTL outputs
- Flow-through configuration
- Extra TTL and ECL power/ground pins to minimize switching noise
- Dual supply
- 6.0ns max. delay into 50pF, 12ns into 200pF (all outputs switching)
- PNP TTL inputs for low loading
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Fully compatible with Motorola MC10H/100H603
- Available in 28-pin PLCC package

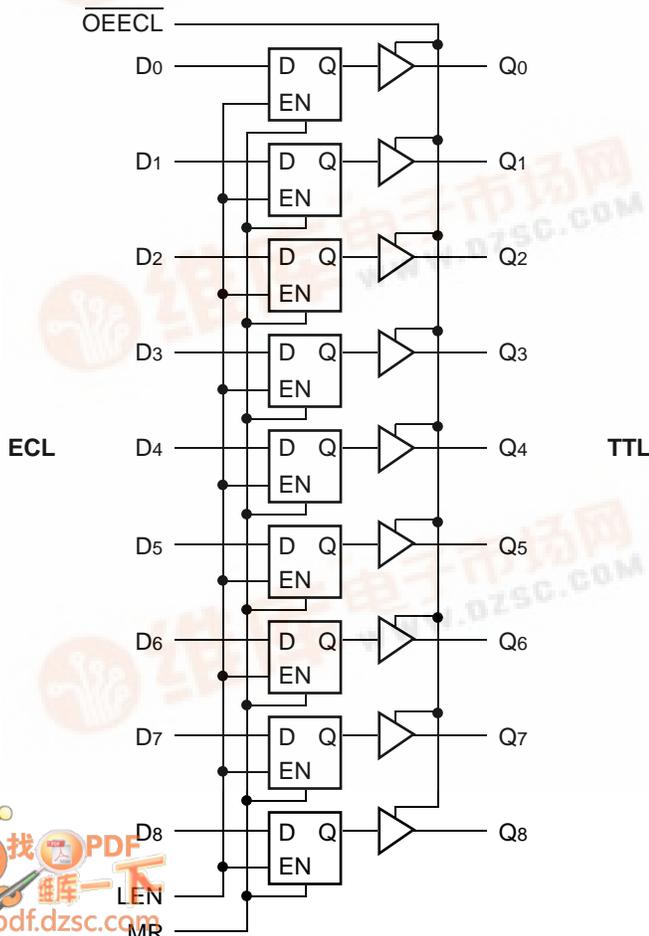
### DESCRIPTION

The SY10/100H603 are 9-bit, dual supply ECL-to-TTL translators. Devices in the Micrel-Synergy 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

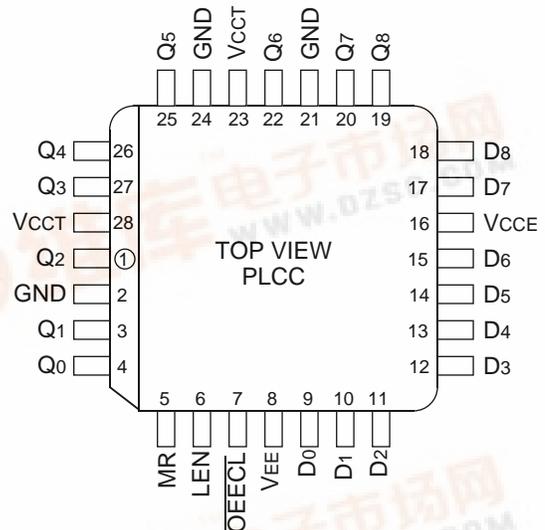
The devices feature a 48mA TTL output stage and AC performance is specified into both a 50pF and 200pF load capacitance. Latching is controlled by Latch Enable (LEN) and Master Reset (MR) resets the latches. A HIGH on  $\overline{OE}ECL$  sends the outputs into the high impedance state. All control inputs are ECL level.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

### BLOCK DIAGRAM



### PIN CONFIGURATION



### PIN NAMES

Pin	Function
GND	TTL Ground (0V)
VCCCE	ECL Vcc (0V)
VCCCT	TTL Supply (+5.0V)
VEE	ECL Supply (-5.2/-4.5V)
D0-D8	Data Inputs (ECL)
Q0-Q8	Data Outputs (TTL)
$\overline{OE}ECL$	3-state Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)



**TRUTH TABLE**

D	LEN	MR	$\overline{OE}ECL$	Q
L	L	L	L	L
H	L	L	L	H
X	H	L	L	Q <sub>0</sub>
X	X	H	L	L
X	X	X	H	Z

**DC ELECTRICAL CHARACTERISTICS**

V<sub>CC</sub>T = 5.0V ± 10%; V<sub>EE</sub> = -4.75V to -5.5V (10H Version); V<sub>EE</sub> = -4.2V to -5.5V (100H Version)

Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I <sub>EE</sub>	Power Supply Current, ECL	45	63	45	64	45	68	mA	—
I <sub>CC</sub>	Power Supply Current, TTL	80	110	80	110	80	110	mA	—
I <sub>OS</sub>	Output Short Circuit Current	-100	-225	-100	-225	-100	-225	mA	V <sub>OUT</sub> = 0V
I <sub>OZH</sub>	Output Disable Current, HIGH	—	50	—	50	—	50	μA	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Disable Current, LOW	—	-50	—	-50	—	-50	μA	V <sub>OUT</sub> = 0.5V

**AC ELECTRICAL CHARACTERISTICS**

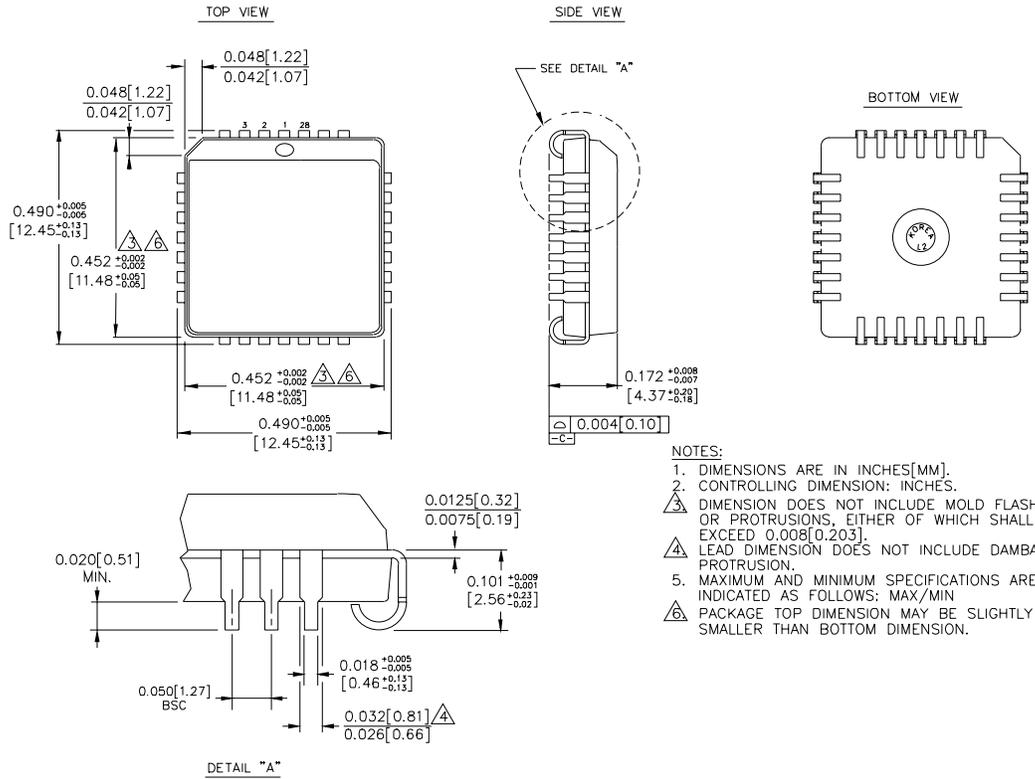
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Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output	D	3.2 6.4	6.0 12	3.2 6.4	6.0 12	3.2 6.4	6.0 12	ns CL = 50pF CL = 200pF
		LEN	3.5 7.0	6.5 13	3.5 7.0	6.5 13	3.5 7.0	6.5 13	ns CL = 50pF CL = 200pF
		MR	3.0 6.0	6.0 12	3.0 6.0	6.0 12	3.0 6.0	6.0 12	ns CL = 50pF CL = 200pF
t <sub>S</sub>	Set-up Time, D to LEN	1.5	—	1.5	—	1.5	—	ns	—
t <sub>H</sub>	Hold Time, D to LEN	0.8	—	0.8	—	0.8	—	ns	—
t <sub>w(L)</sub>	LEN Pulse Width, LOW	2.0	—	2.0	—	2.0	—	ns	—
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	2.5 4.2	6.5 13	2.5 4.2	6.5 13	2.5 4.2	6.5 13	ns	CL = 50pF CL = 200pF
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	2.0 4.0	5.0 10	2.0 4.0	5.0 10	2.0 4.0	5.0 10	ns	CL = 50pF CL = 200pF
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Time 1.0V – 2.0V	0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	ns	CL = 50pF CL = 200pF

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY10H603JC	J28-1	Commercial
SY10H603JCTR	J28-1	Commercial
SY100H603JC	J28-1	Commercial
SY100H603JCTR	J28-1	Commercial

**28 LEAD PLCC (J28-1)**



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
  2. CONTROLLING DIMENSION: INCHES.
  3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
  4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
  5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
  6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

