



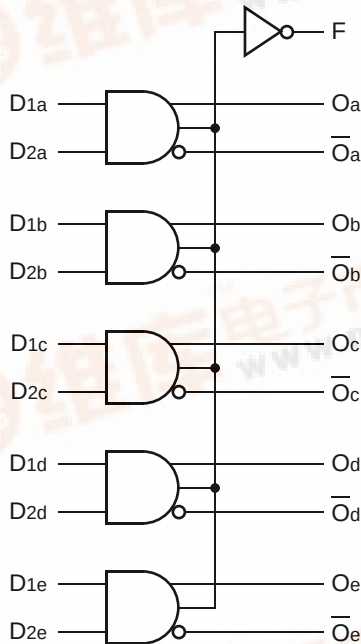
QUINT AND/NAND GATE

SY100S304

FEATURES

- Max. propagation delay of 1050ps
- IEE min. of -60mA
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75K Ω input pull-down resistors
- 40% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

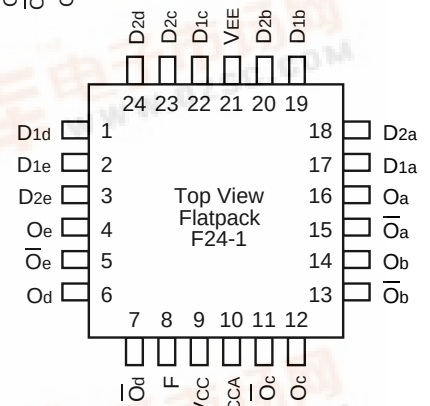
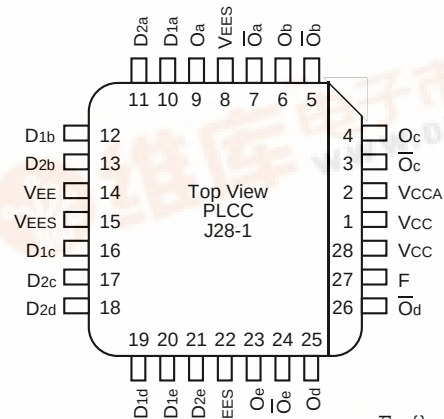
BLOCK DIAGRAM



DESCRIPTION

The SY100S304 is an ultra-fast quint AND/NAND gate designed for use in high-performance ECL systems. This device also features a Function (F) output which is the wire-NOR of the AND gate outputs. The inputs on the device have 75K Ω pull-down resistors.

PIN CONFIGURATIONS



PIN NAMES

Pin	Function
Dna – Dne	Data Inputs (n-1...5)
E	Enable Input
Oa – Oe	Data Outputs
Oa – Oe	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current				μA	$V_{IN} = V_{IH} (Max.)$
	D _{2a} — D _{2e}	—	—	250		
	D _{1a} — D _{1e}	—	—	250		
I _{EE}	Power Supply Current	−60	−40	−30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

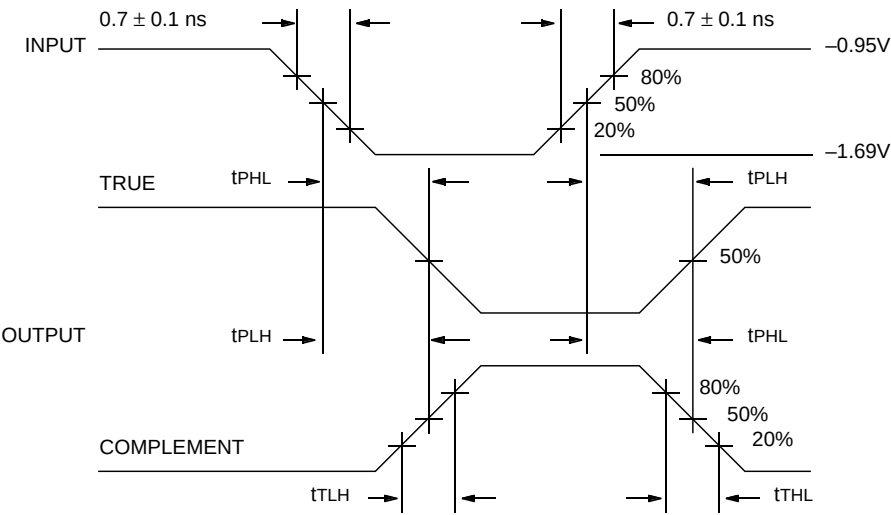
Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D _{na} — D _{ne} to O, $\bar{O}$	300	1150	300	1150	300	1150	ps	
t _{PLH} t _{PHL}	Propagation Delay Data to F	600	1650	600	1650	600	1650	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D _{na} — D _{ne} to O, $\bar{O}$	300	1050	300	1050	300	1050	ps	
t _{PLH} t _{PHL}	Propagation Delay Data to F	600	1550	600	1550	600	1550	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



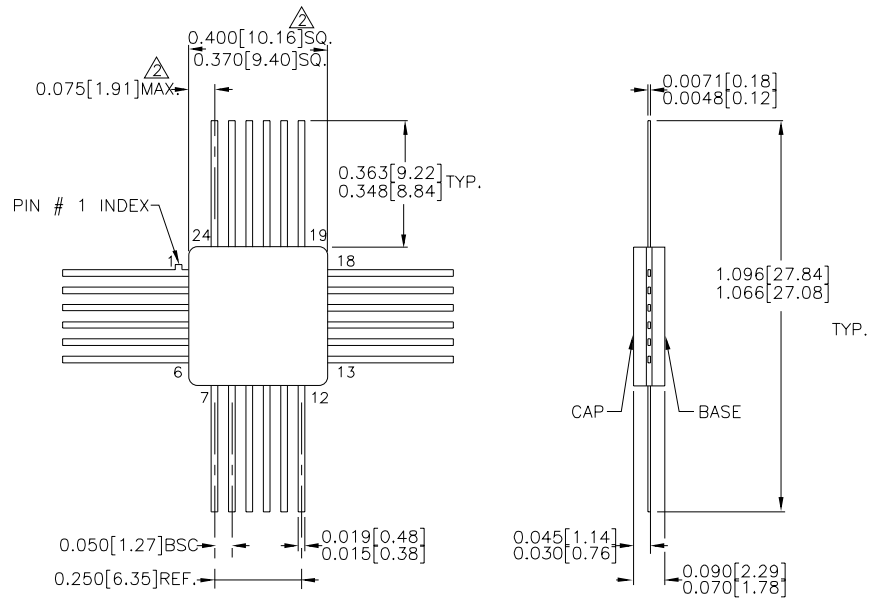
Propagation Delay and Transition Times

NOTE:
 $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S304FC	F24-1	Commercial
SY100S304JC	J28-1	Commercial
SY100S304JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)



NOTES:

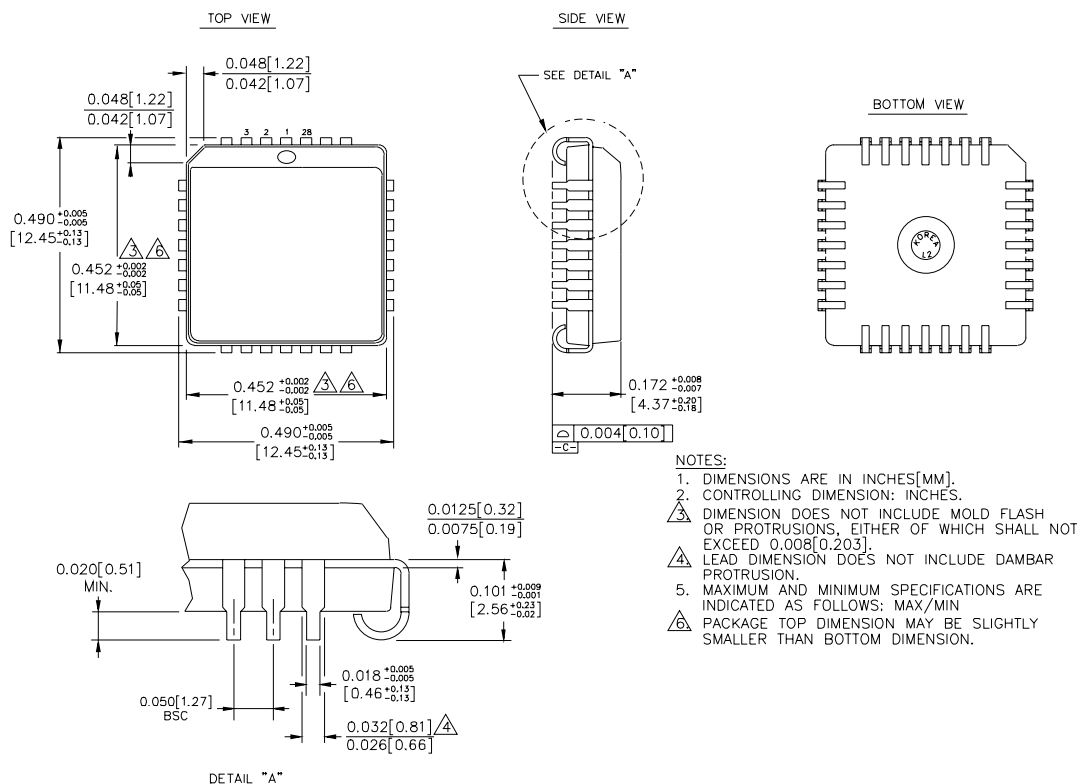
1. DIMENSIONS ARE IN INCHES[MM].

△ THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.

3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



Rev. 03