



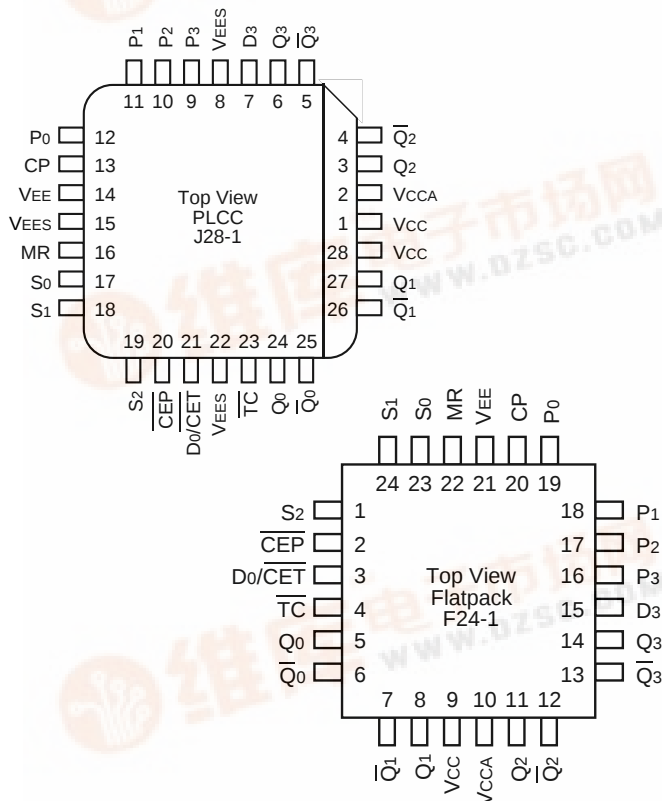
4-STAGE COUNTER/ SHIFT REGISTER

SY100S336

FEATURES

- Max. shift frequency of 700MHz
- Clock to Q delay max. of 1100ps
- IEE min. of -170mA
- Internal 75K Ω input pull-down resistors
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- 50% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

PIN CONFIGURATIONS



DESCRIPTION

The SY100S336 functions either as a modulo-16 up/down counter or as a 4-bit bidirectional shift register and is designed for use in high-performance ECL systems. Three Select inputs (S_n) are provided for determining the mode of operation. The Function Table lists the available modes of operation. In order to allow cascading for multistage counters, two Count Enable controls ($\overline{\text{CEP}}$, $\overline{\text{CET}}$) are provided. The $\overline{\text{CET}}$ input also functions as the Serial Data input (S₀) for a shift-up operation, while the D₃ input serves as the Serial Data input for the shift-down operation.

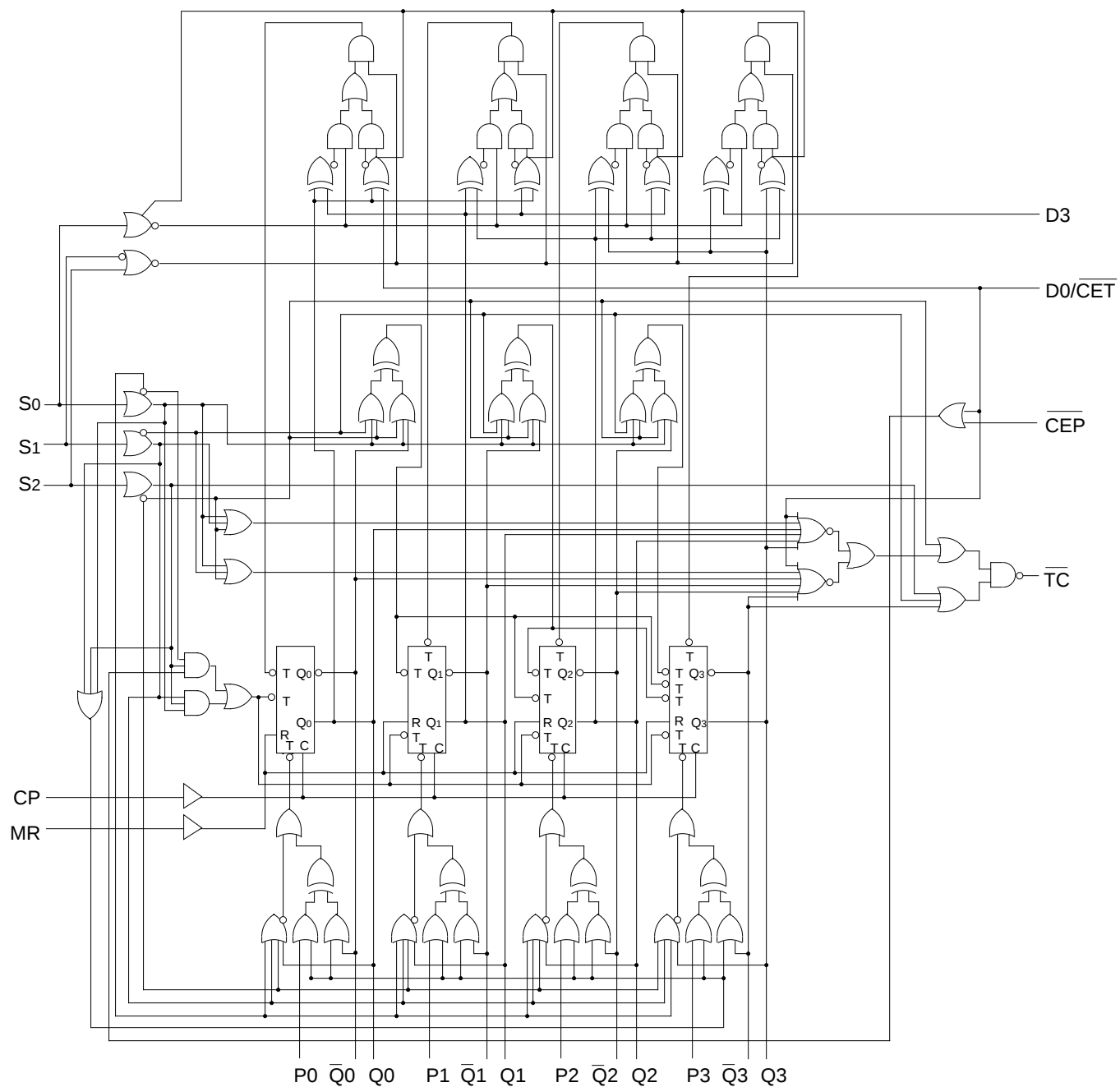
When the device is in the counting mode, the Terminal Count ($\overline{\text{TC}}$) goes to a logical LOW when the count reaches 15 for count-up or reaches 0 for count-down. When in the shift mode, the $\overline{\text{TC}}$ output simply repeats the Q₃ output.

The flexibility provided by the $\overline{\text{TC}}$ /Q₃ output and the D₀/ $\overline{\text{CET}}$ input allows these signals to be interconnected from one stage to the next higher stage for multistage counting or shift-up operations. The individual Presets (P_n) allow initialization of the counter by entering data in parallel to preset the counter. A logic HIGH on the Master Reset (MR) overrides all other inputs and asynchronously clears the flip-flops. An additional synchronous Clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 75K Ω pull-down resistors.

PIN NAMES

Pin	Function
CP	Clock Pulse Input
$\overline{\text{CEP}}$	Count Enable Parallel Input (Active LOW)
D ₀ / $\overline{\text{CET}}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S ₀ — S ₂	Select Inputs
MR	Master Reset Input
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs
P ₀ — P ₃	Preset Inputs
D ₃	Serial Data Input
$\overline{\text{TC}}$	Terminal Count Output
Q ₀ — Q ₃	Data Outputs
$\overline{\text{Q}}_0$ — $\overline{\text{Q}}_3$	Complementary Data Outputs

BLOCK DIAGRAM



TRUTH TABLE⁽¹⁾

Inputs								Outputs					
MR	S ₂	S ₁	S ₀	$\overline{\text{CEP}}$	$\text{D}_0/\overline{\text{CET}}$	D ₃	CP	Q ₀	Q ₁	Q ₂	Q ₃	$\overline{\text{TC}}$	Mode
L	L	L	L	X	X	X	u	P ₀	P ₁	P ₂	P ₃	L	Preset (Parallel Load)
L	L	L	H	X	X	X	u	$\overline{\text{Q}}_0$	$\overline{\text{Q}}_1$	$\overline{\text{Q}}_2$	$\overline{\text{Q}}_3$	L	Invert
L	L	H	L	X	X	X	u	Q ₁	Q ₂	Q ₃	D ₃	D ₃	Shift Left
L	L	H	H	X	X	X	u	D ₀	Q ₀	Q ₁	Q ₂	Q ₃ *	Shift Right
L	H	L	L	L	L	X	u	(Q ₀₋₃) minus 1				①	Count Down
L	H	L	L	H	L	X	X	Q ₀	Q ₁	Q ₂	Q ₃	①	Count Down with $\overline{\text{CEP}}$ Not Active
L	H	L	L	X	H	X	X	Q ₀	Q ₁	Q ₂	Q ₃	H	Count Down with $\overline{\text{CET}}$ Not Active
L	H	L	H	X	X	X	u	L	L	L	L	H	Clear
L	H	H	L	L	L	X	u	(Q ₀₋₃) plus 1				≠	Count Up
L	H	H	L	H	L	X	X	Q ₀	Q ₁	Q ₂	Q ₃	≠	Count Up with $\overline{\text{CEP}}$ Not Active
L	H	H	L	X	H	X	X	Q ₀	Q ₁	Q ₂	Q ₃	H	Count Up with $\overline{\text{CET}}$ Not Active
L	H	H	H	X	X	X	X	Q ₀	Q ₁	Q ₂	Q ₃	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	L	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

NOTE:

1. H = High Voltage Level

L = Low Voltage Level

X = Don't Care

u = LOW-to-HIGH Transition

① = L if Q₀ – Q₃ = LLLLH if Q₀ – Q₃ ≠ LLLL≠ = L if Q₀ – Q₃ = HHHHH if Q₀ – Q₃ ≠ HHHH* Before the clock, $\overline{\text{TC}}$ is Q₃; after the clock, $\overline{\text{TC}}$ is Q₂**DC ELECTRICAL CHARACTERISTICS**V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current, All Inputs	—	—	200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	–170	–145	–90	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
fshift	Shift Frequency700	—	700	—	700	—	MHz		
tPLH tPHL	Propagation Delay CP to Q_n , $\bar{Q}_n$	450	1200	450	1200	450	1200	ps	
tPLH tPHL	Propagation Delay CP to $\bar{TC}$	600	1900	600	1900	600	1900	ps	
tPLH tPHL	Propagation Delay MR to Q_n , $\bar{Q}_n$	500	1400	500	1400	500	1400	ps	
tPLH tPHL	Propagation Delay MR to $\bar{TC}$	600	1900	600	1900	600	1900	ps	
tPLH tPHL	Propagation Delay $D_0/\bar{CET}$ to $\bar{TC}$	400	1200	400	1200	400	1200	ps	
tPLH tPHL	Propagation Delay S_n to $\bar{TC}$	1500	2600	1500	2600	1500	2600	ps	
tTLH tTHL	Transition Time300 20% to 80%, 80% to 20%	900	300	900	300	900	ps		
ts	Set-up Time							ps	
	D_3	800	—	800	—	800	—		
	P_n	800	—	800	—	800	—		
	$D_0/\bar{CET}$ to $\bar{CEP}$	700	—	700	—	700	—		
	S_n	2000	—	2000	—	2000	—		
	MR (Release Time)	900	—	900	—	900	—		
th	Hold Time							ps	
	D_3	200	—	200	—	200	—		
	P_n	200	—	200	—	200	—		
	$D_0/\bar{CET}$ to $\bar{CEP}$	200	—	200	—	200	—		
	S_n	-600	—	-600	—	-600	—		
t _{pw} (H)	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps	

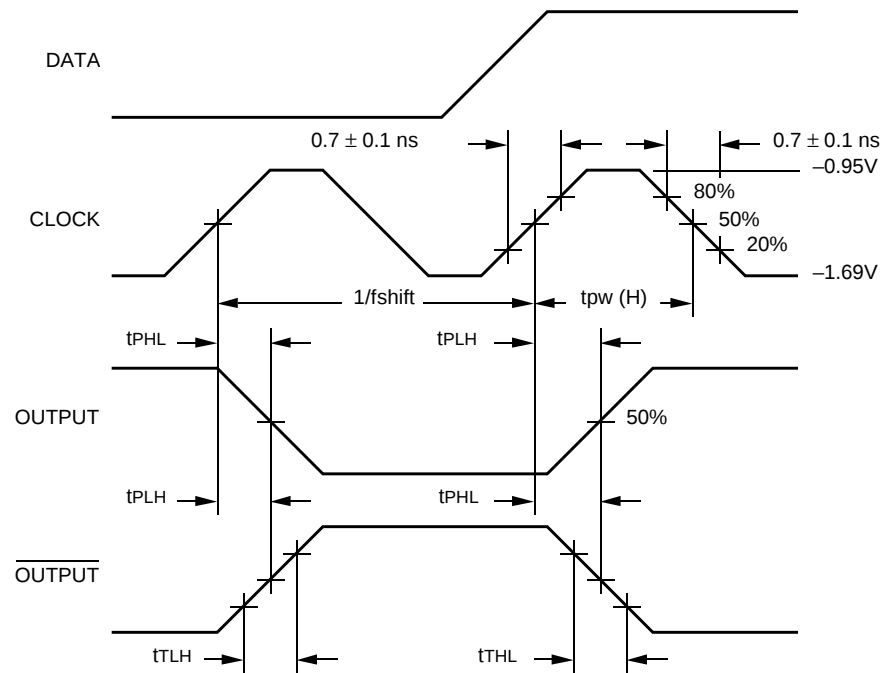
AC ELECTRICAL CHARACTERISTICS

PLCC

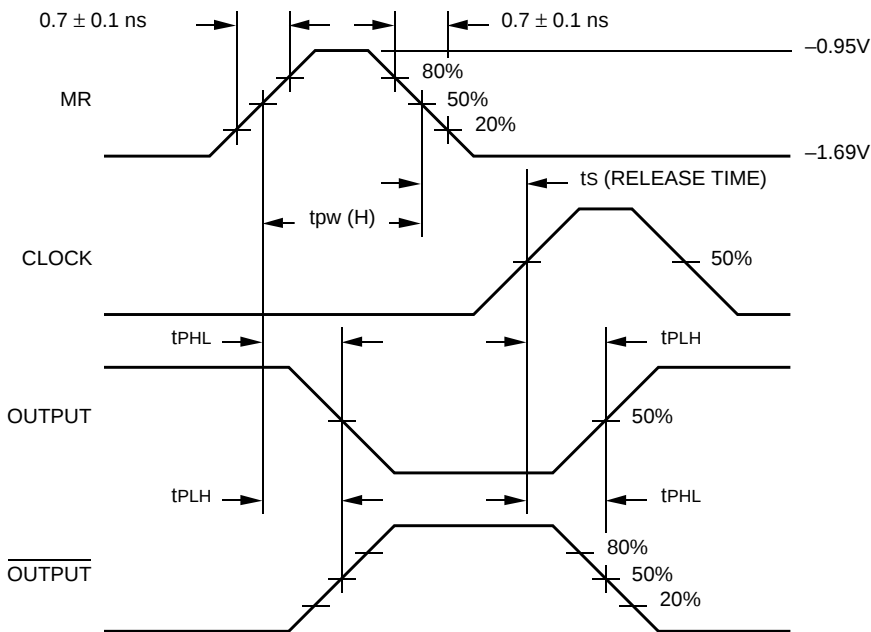
$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
fshift	Shift Frequency	—	700	—	700	—	—	MHz	
tPLH tPHL	Propagation Delay CP to Q_n , $\bar{Q}_n$	450	1100	450	1100	450	1100	ps	
tPLH tPHL	Propagation Delay CP to $\bar{T}C$	600	1800	600	1800	600	1800	ps	
tPLH tPHL	Propagation Delay MR to Q_n , $\bar{Q}_n$	500	1300	500	1300	500	1300	ps	
tPLH tPHL	Propagation Delay MR to $\bar{T}C$	600	1800	600	1800	600	1800	ps	
tPLH tPHL	Propagation Delay $D_0/\bar{C}ET$ to $\bar{T}C$	400	1100	400	1100	400	1100	ps	
tPLH tPHL	Propagation Delay S_n to $\bar{T}C$	1500	2500	1500	2500	1500	2500	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts	Set-up Time							ps	
	D_3	800	—	800	—	800	—		
	P_n	800	—	800	—	800	—		
	$D_0/\bar{C}ET$ to $\bar{C}EP$	700	—	700	—	700	—		
	S_n	2000	—	2000	—	2000	—		
	MR (Release Time)	900	—	900	—	900	—		
th	Hold Time							ps	
	D_3	200	—	200	—	200	—		
	P_n	200	—	200	—	200	—		
	$D_0/\bar{C}ET$ to $\bar{C}EP$	200	—	200	—	200	—		
	S_n	-600	—	-600	—	-600	—		
t _{pw} (H)	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps	

TIMING DIAGRAMS

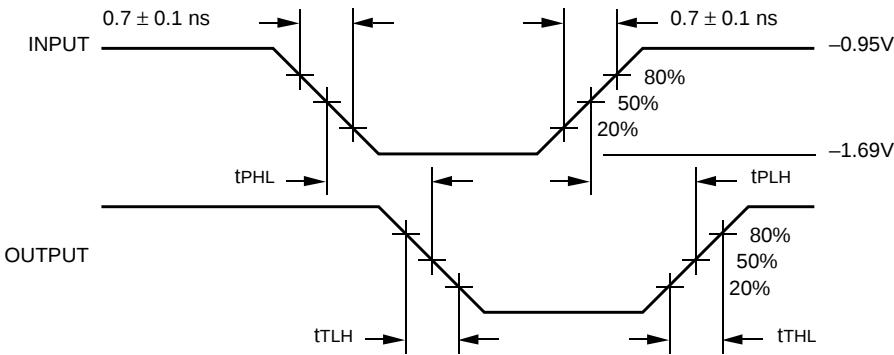


Propagation Delay (Clock) and Transition Times

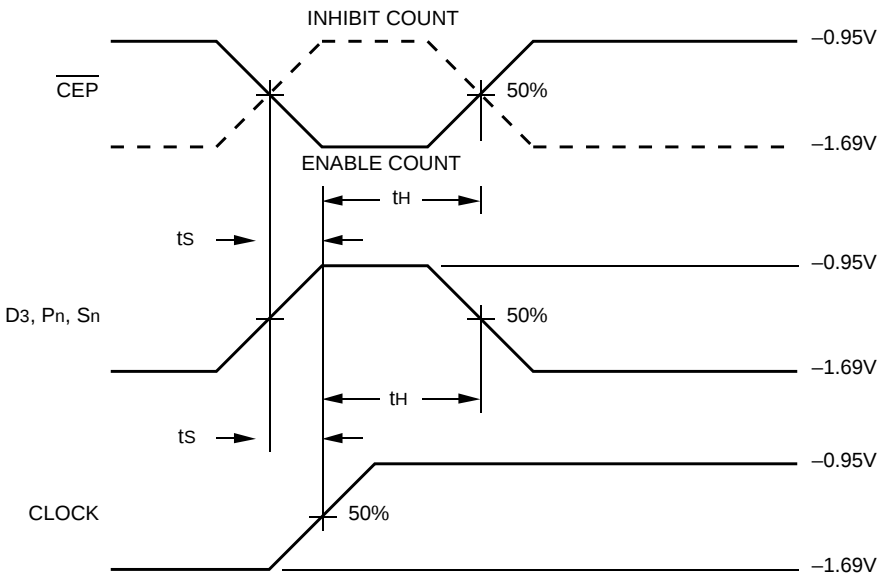


Propagation Delay (Reset)

TIMING DIAGRAMS



Propagation Delay (Serial Data, Selects)



Set-up and Hold Time

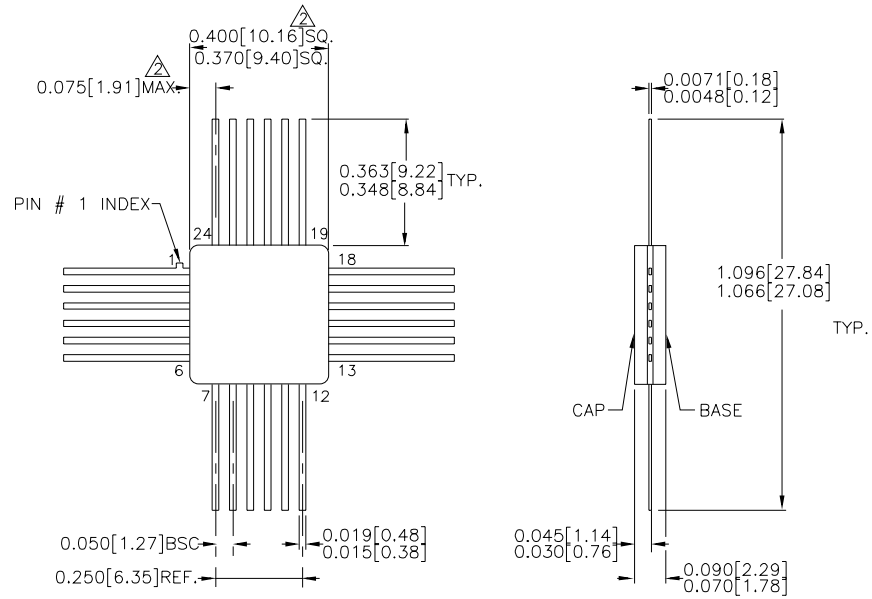
NOTES:

- 1. $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$.
- 2. t_s is the minimum time before the transition of the clock that information must be present at the data input.
- 3. t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S336FC	F24-1	Commercial
SY100S336JC	J28-1	Commercial
SY100S336JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)



NOTES:

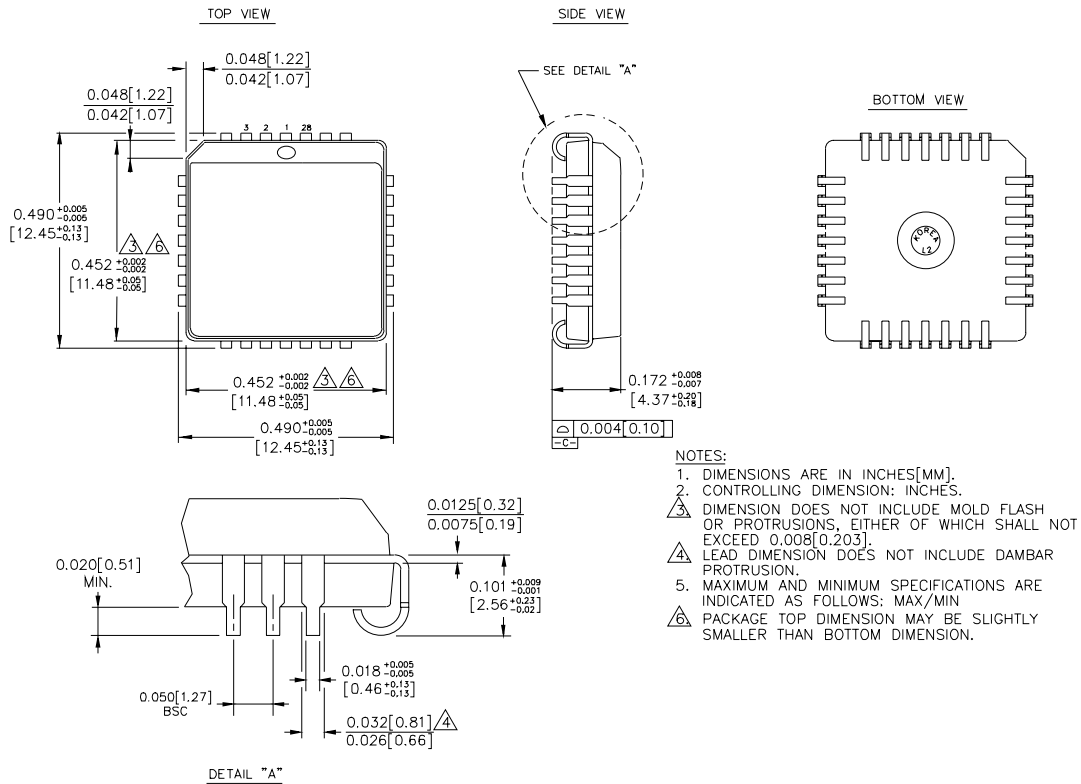
1. DIMENSIONS ARE IN INCHES[MM].

2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.

3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



Rev. 03