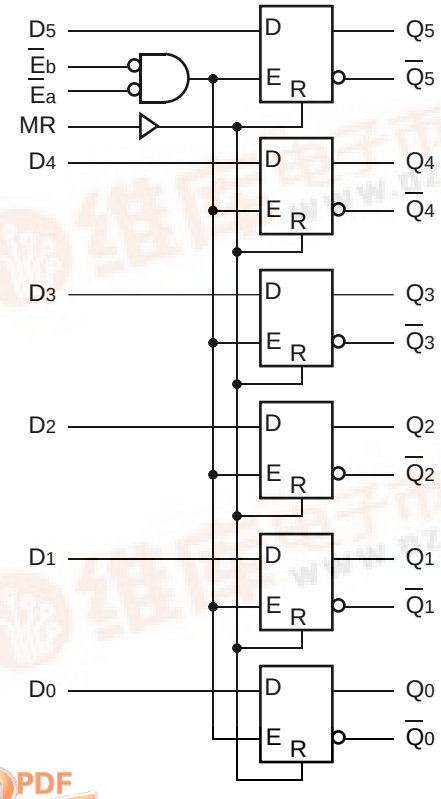
FEATURES

- Max. transparent propagation delay of 900ps
- Min. Master Reset and Enable pulse widths of 100ps
- IEE min. of –98mA
- Industry standard 100K ECL levels
- Extended supply voltage option: VEE = –4.2V to –5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- More than 40% faster than Fairchild
- Approximately 30% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

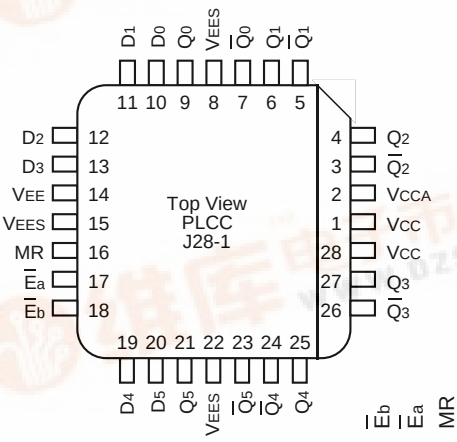
DESCRIPTION

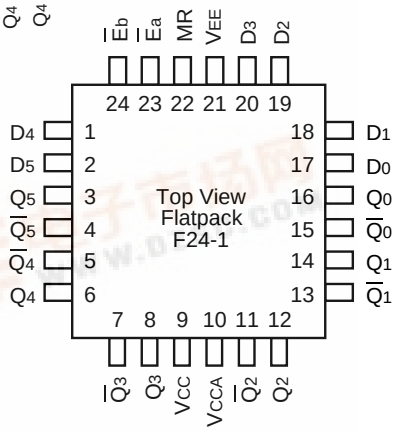
The SY100S350 offers six high-speed D-Latches with both true and complement outputs, and is performance compatible for use with high-performance ECL systems. When both enable signals ($\overline{E}_a$ and $\overline{E}_b$) are at a logic LOW, the latches are transparent and the input signals(D_0–D_5) appear at the outputs (Q_0–Q_5) after a propagation delay. If either or both of the enable signals are at a logic HIGH, then the latches store the last valid data present on its inputs before $\overline{E}_a$ or $\overline{E}_b$ went to a logic HIGH. The Master Reset (MR) overrides all other input signals and takes the outputs to a logic LOW state. All inputs have 75KΩ pull-down resistors.

BLOCK DIAGRAM



PIN CONFIGURATIONS





PIN NAMES

Pin	Function
D_0 — D_5	Data Inputs
$\overline{E}_a$, $\overline{E}_b$	Common Enable Inputs (Active LOW)
MR	Asynchronous Master Reset Input
Q_0 — Q_5	Data Outputs
$\overline{Q}_0$ — $\overline{Q}_5$	Complementary Data Outputs
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

TRUTH TABLE[1]

Each Latch

Inputs				Outputs		Operating Mode
D_n	$\overline{E}_a$	$\overline{E}_b$	MR	Q_n	$\overline{Q}_n$	
H	L	L	L	H	L	Latch
L	L	L	L	L	H	
X	X	H	L	Latched[2]	Latched[2]	
X	H	X	L	Latched[2]	Latched[2]	
X	X	X	H	L	H	Asynchronous

NOTES:

1. H = HIGH State
   L = LOW State
   X = Don't Care
2. Retains data that is present before $\overline{E}$ positive transition.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current				µA	V_{IN} = V_{IH} (Max.)
	MR	—	—	250		
	Dn	—	—	250		
	$\overline{E}$a, $\overline{E}$b	—	—	250		
I_{EE}	Power Supply Current	–98	–78	–49	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

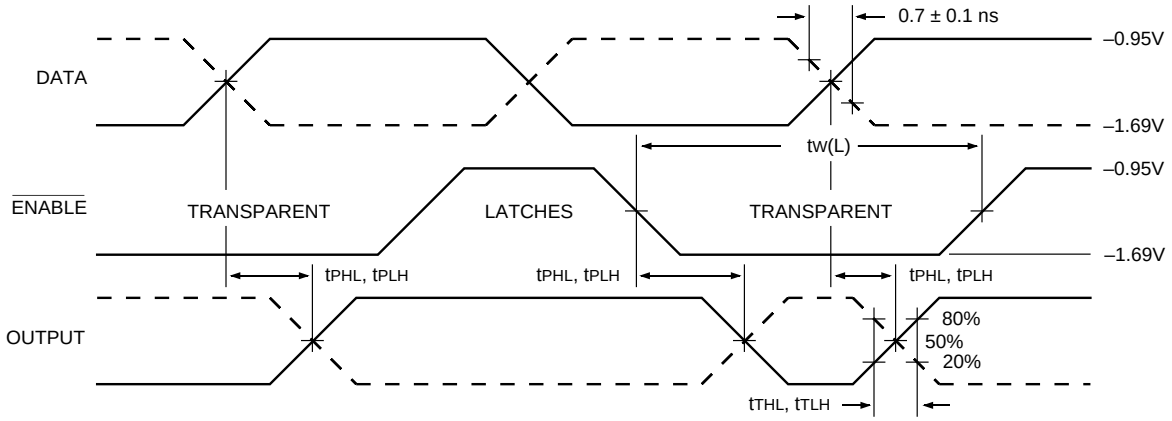
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	300	1000	300	1000	300	1000	ps	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	300	1100	300	1100	300	1100	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	300	1250	300	1250	300	1250	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_S	Set-up Time, D_n to $\overline{E}_n$	500	—	500	—	500	—	ps	
t_H	Hold Time, D_n to $\overline{E}_n$	500	—	500	—	500	—	ps	
t_r	Release Time, MR to $\overline{E}_n$	1000	—	1000	—	1000	—	ps	
t_{PW} (L)	Pulse Width, $\overline{E}_a$, $\overline{E}_b$	1000	—	1000	—	1000	—	ps	
t_{PW} (H)	Pulse Width, MR	1000	—	1000	—	1000	—	ps	

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	300	900	300	900	300	900	ps	
t_{PLH} t_{PHL}	Propagation Delay E_a, E_b to Output	300	1000	300	1000	300	1000	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	300	1200	300	1200	300	1200	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_S	Set-up Time, D_n to E_n	500	—	500	—	500	—	ps	
t_H	Hold Time, D_n to $\overline{E}_n$	500	—	500	—	500	—	ps	
t_r	Release Time, MR to $\overline{E}_n$	1000	—	1000	—	1000	—	ps	
t_{PW} (L)	Pulse Width, E_a, E_b	1000	—	1000	—	1000	—	ps	
t_{PW} (H)	Pulse Width, MR	1000	—	1000	—	1000	—	ps	

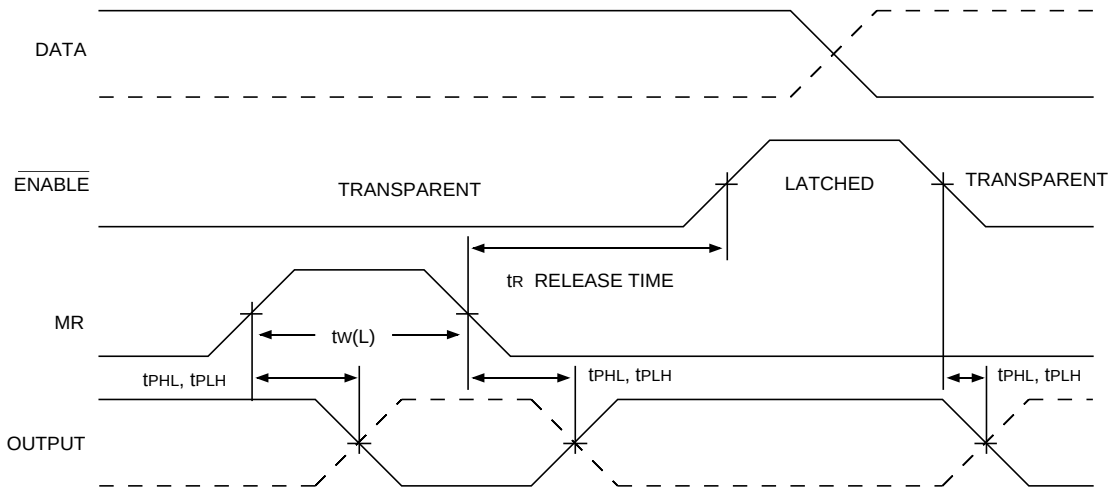
TIMING DIAGRAMS



Enable Timing

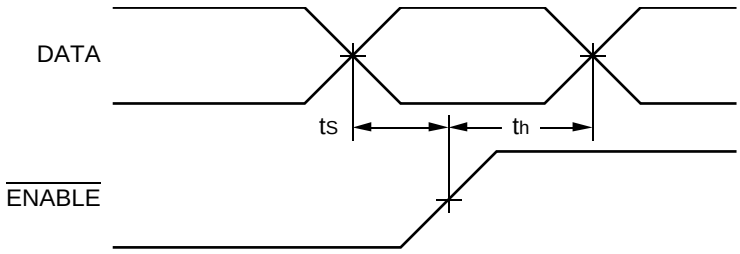
NOTE:

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND



Reset Timing

TIMING DIAGRAMS



Data Set-up and Hold Times

NOTES:

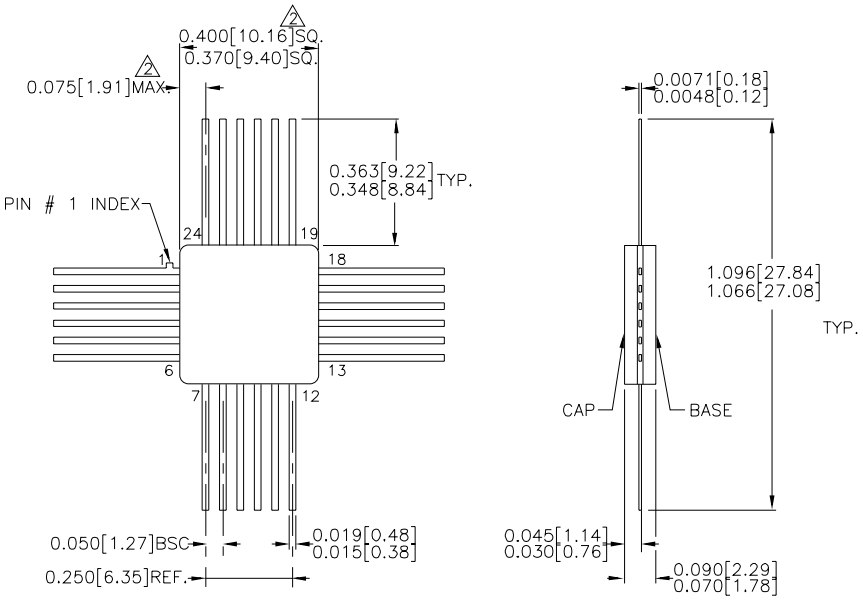
t_S is the minimum time before the transition of the clock that information must be present at the data input.

t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S350FC	F24-1	Commercial
SY100S350JC	J28-1	Commercial
SY100S350JCTR	J28-1	Commercial

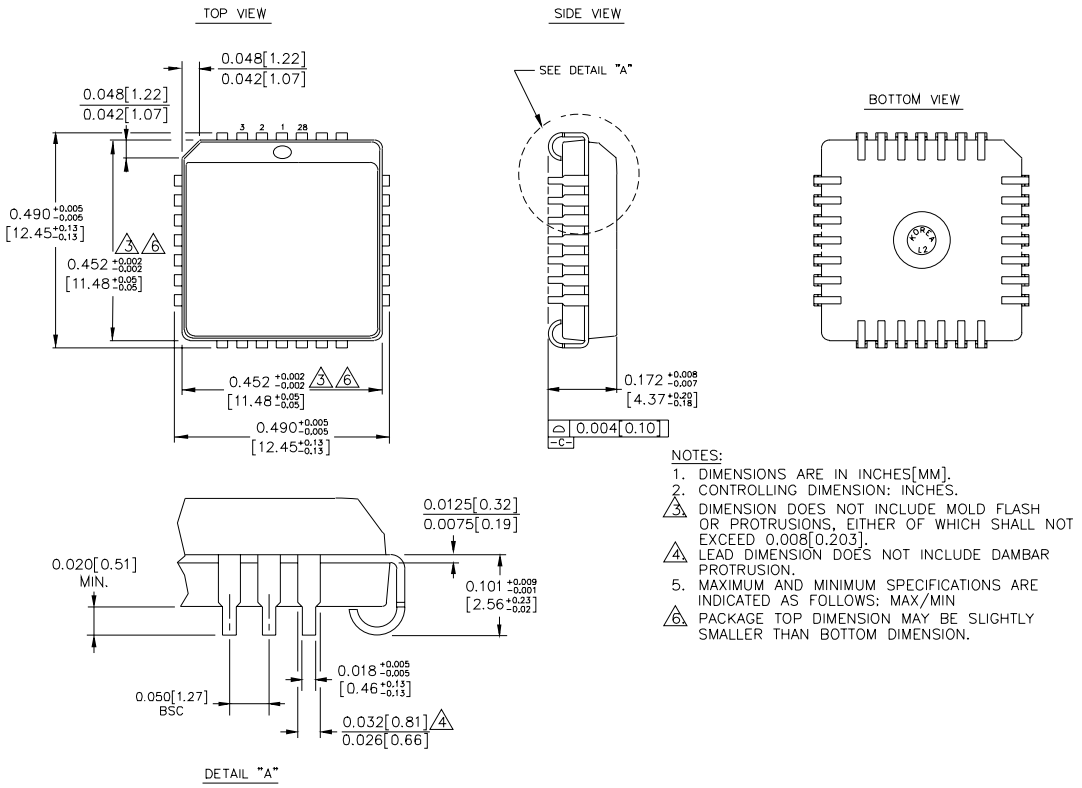
24 LEAD CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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