



QUAD MULTIPLEXER/LATCH

SY100S355

FEATURES

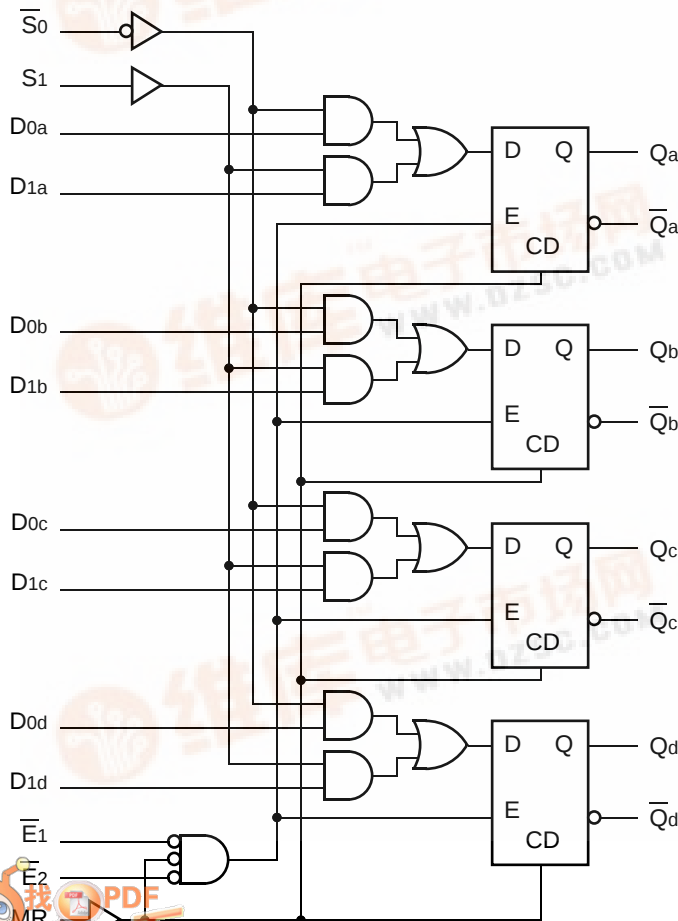
- Max. propagation delay of 1100ps
- Max. enable to output delay of 1400ps
- IEE min. of -80mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 50% faster than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPAC and 28-pin PLCC packages

DESCRIPTION

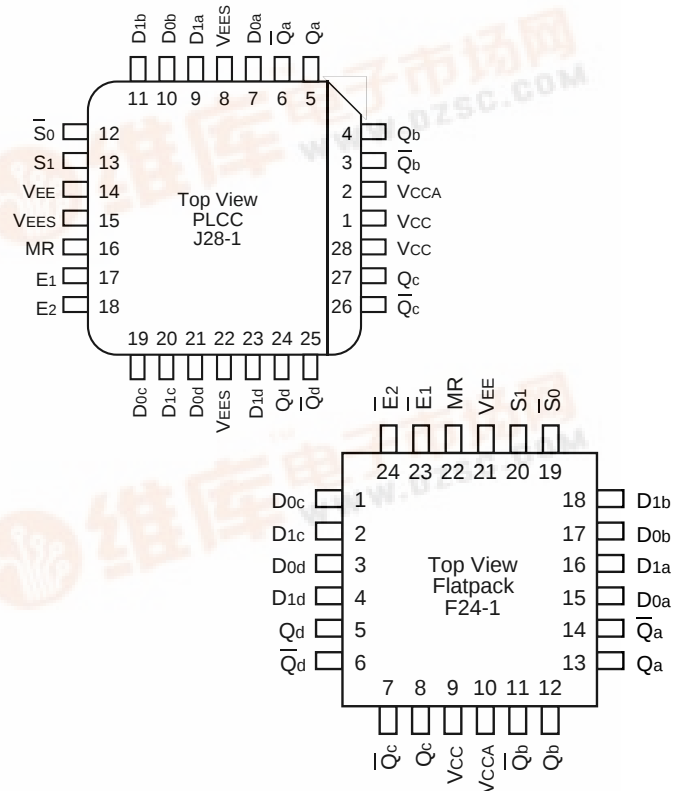
The SY100S355 offers four transparent latches with differential outputs and is designed for use in high-performance ECL systems. The Select inputs ($\bar{S}_0$, S_1) select one of the two sources of input data (D_0 or D_1) to the latch. The Select inputs can also force the outputs to a logic LOW when the latch is in the transparent mode. The latches are in the transparent mode when both Enables ($\bar{E}_1$, $\bar{E}_2$) are at a logic LOW state. In the transparent mode, the Select inputs can pass an input logic HIGH from D_0 or D_1 to the output.

If the Select inputs are tied together, then input data from either D_0 or D_1 is always passed through. A rising edge on either Enable input will latch the outputs with the most recent data at the latch inputs being stored. The Master Reset (MR) input overrides all other inputs and takes the Q outputs to a logic LOW. The inputs on this device have 75KΩ pull-down resistors.

BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

Pin	Function
$\bar{E}_1 - \bar{E}_2$	Enable Inputs (Active LOW)
$\bar{S}_0, S_1$	Select Inputs
MR	Master Reset
Dna – Dnd	Data Inputs
Qa – Qd	Data Outputs
$\bar{Q}_a - \bar{Q}_d$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

TRUTH TABLE⁽¹⁾

Inputs							Outputs	
MR	$\bar{E}_1$	$\bar{E}_2$	S1	$\bar{S}_0$	D1x	D0x	$\bar{Q}_x$	Qx
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched	Latched
L	X	H	X	X	X	X	Latched	Latched

NOTE:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current	—	—	—	μA	$V_{IN} = V_{IH} (Max.)$
	$\bar{S}_0, S_1$	—	—	220		
	$\bar{E}_1, \bar{E}_2$	—	—	350		
	Dna, Dnd	—	—	340		
	MR	—	—	430		
I _{EE}	Power Supply Current	–80	–57	–40	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

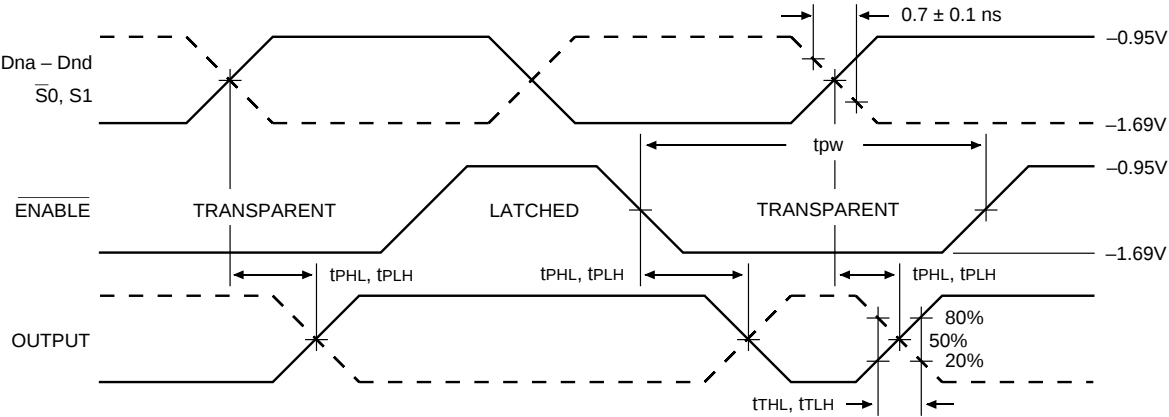
Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay Dna – Dnd to Output (Transparent Mode)	300	1200	300	1200	300	1200	ps	
tPLH tPHL	Propagation Delay S0, S1 to Output (Transparent Mode)	300	1500	300	1500	300	1500	ps	
tPLH tPHL	Propagation Delay E1, E2 to Output	300	1500	300	1500	300	1500	ps	
tPLH tPHL	Propagation Delay MR to Output	300	1200	300	1200	300	1200	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts	Set-up Time Dna – Dnd S0, S1 MR (Release Time)	700	—	700	—	700	—	ps	
		1200	—	1200	—	1200	—		
		1000	—	1000	—	1000	—		
th	Hold Time Dna – Dnd S0, S1	400	—	400	—	400	—	ps	
		400	—	400	—	400	—		
tpw (L)	Pulse Width LOW, E1, E2	1000	—	1000	—	1000	—	ps	
tpw (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps	

PLCC

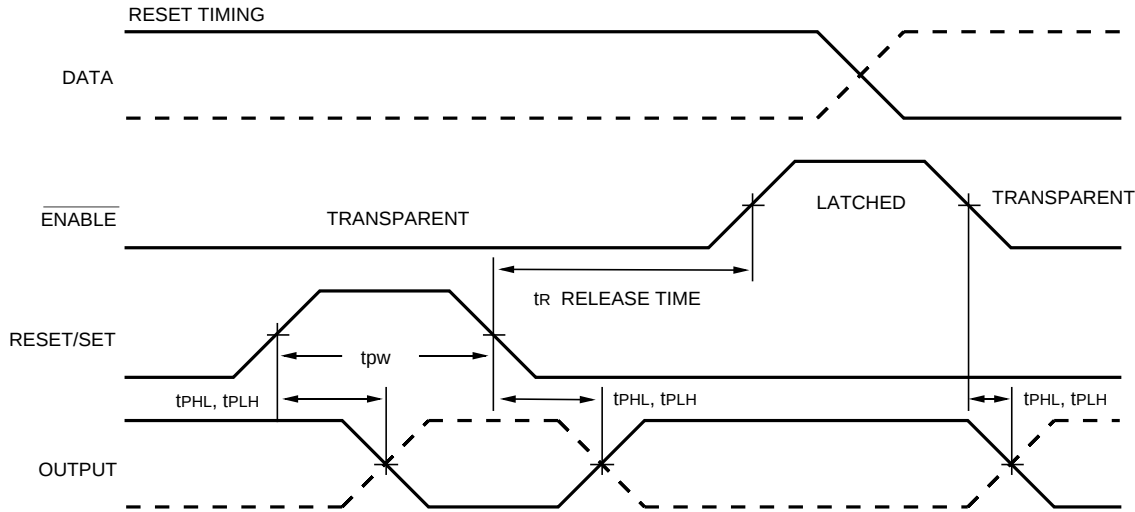
VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay Dna – Dnd to Output (Transparent Mode)	300	1100	300	1100	300	1100	ps	
tPLH tPHL	Propagation Delay S0, S1 to Output (Transparent Mode)	300	1400	300	1400	300	1400	ps	
tPLH tPHL	Propagation Delay E1, E2 to Output	300	1400	300	1400	300	1400	ps	
tPLH tPHL	Propagation Delay MR to Output	300	1100	300	1100	300	1100	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts	Set-up Time Dna – Dnd S0, S1 MR (Release Time)	700	—	700	—	700	—	ps	
		1200	—	1200	—	1200	—		
		1000	—	1000	—	1000	—		
th	Hold Time Dna – Dnd S0, S1	300	—	300	—	300	—	ps	
		300	—	300	—	300	—		
tpw (L)	Pulse Width LOW, E1, E2	1000	—	1000	—	1000	—	ps	
tpw (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps	

TIMING DIAGRAMS

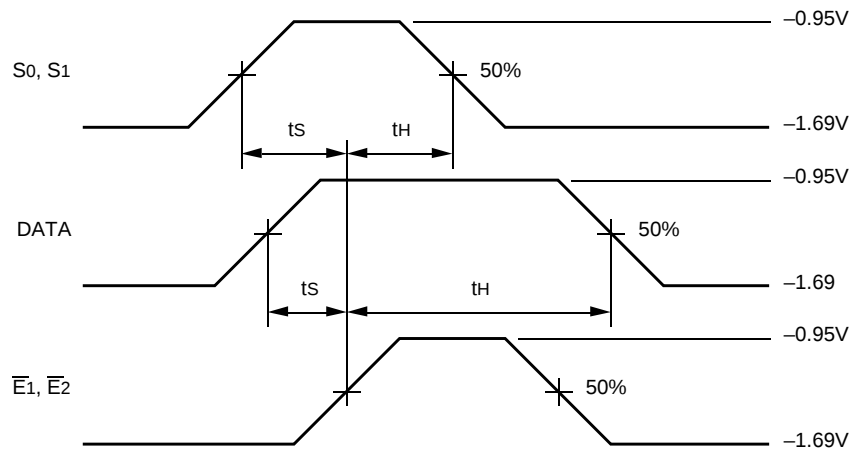


Enable Timing



Reset Timing

TIMING DIAGRAMS



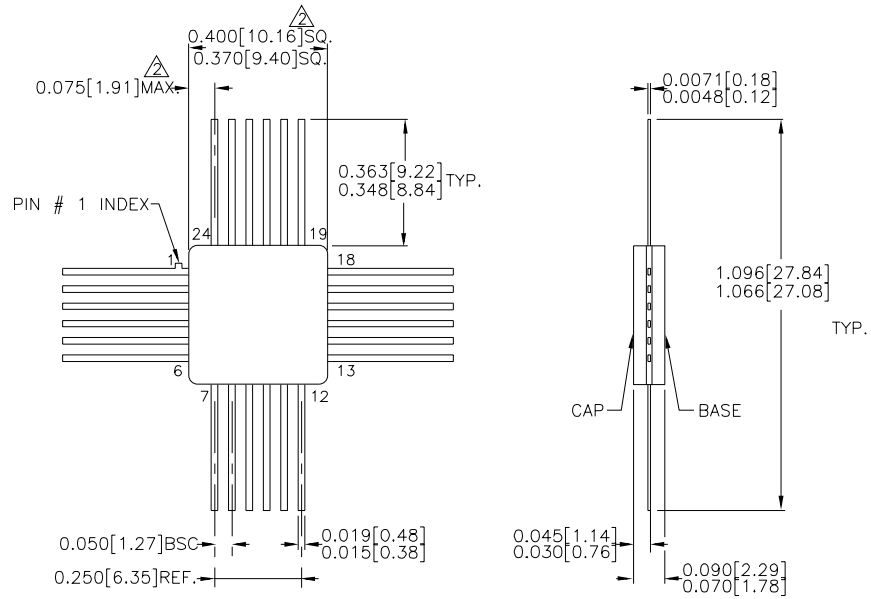
Data Set-up and Hold Times

- NOTES:**
- 1. $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$
 - 2. t_s is the minimum time before the transition of the clock that information must be present at the data input.
 - 3. t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S355FC	F24-1	Commercial
SY100S355JC	J28-1	Commercial
SY100S355JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)



NOTES:

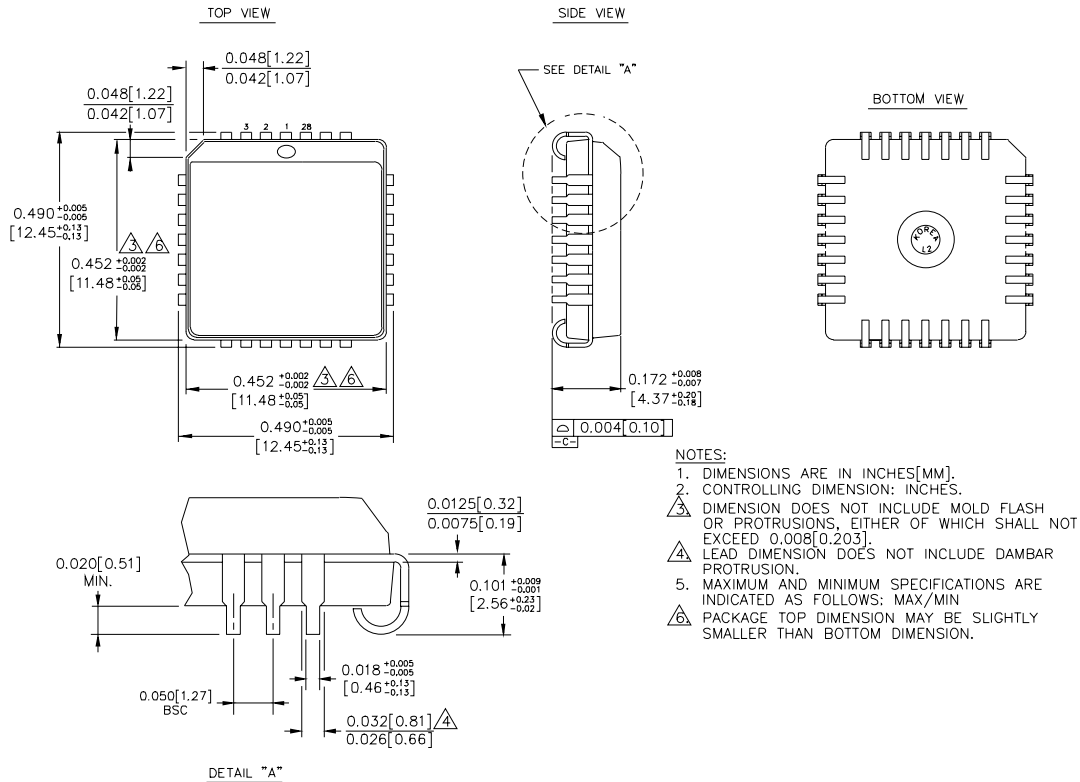
1. DIMENSIONS ARE IN INCHES[MM].

△ THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.

3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



Rev. 03