



QUAD 4-INPUT OR/NOR GATE

SY10E101
SY100E101

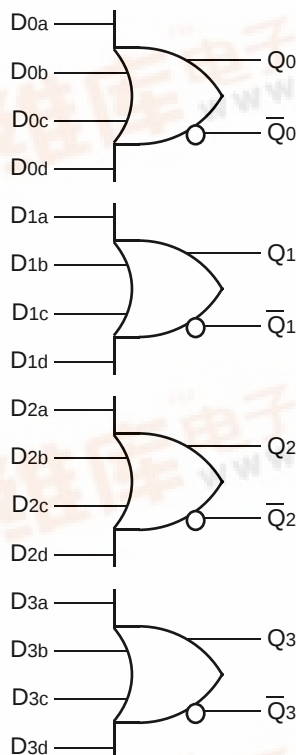
FEATURES

- 500ps max. propagation delay
- Extended 100E VEE range of -4.2V to -5.5V
- True and complementary outputs
- Fully compatible with industry standard 10KH, 100K I/O levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E101
- Available in 28-pin PLCC package

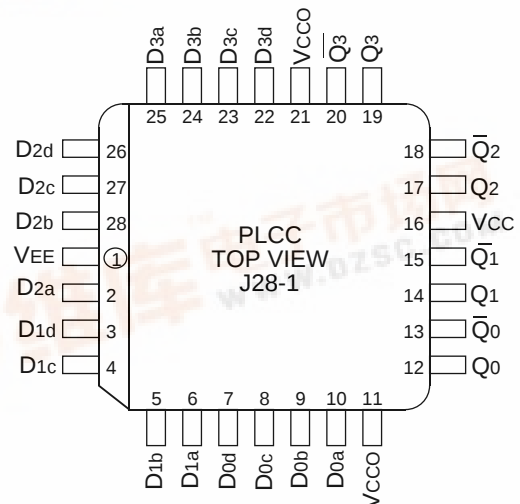
DESCRIPTION

The SY10/100E101 are quad 4-input OR/NOR gates designed for use in new, high-performance ECL systems. The E101 features both true and complementary outputs.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
Dna, Dnb, Dnc, Dnd	Data Inputs
Q0-Q3	True Outputs
$\bar{Q}0-\bar{Q}3$	Inverting Outputs
Vcco	Vcc to Output

LOGIC EQUATION

$$Q_n = D_{na} + D_{nb} + D_{nc} + D_{nd}$$

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}(\text{Min.})$ to $V_{EE}(\text{Max.})$; $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA
I_{EE}	Power Supply Current													mA
	10EL	—	30	36	—	30	36	—	30	36	—	30	36	
	100EL	—	30	36	—	30	36	—	30	36	—	35	42	

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}(\text{Min.})$ to $V_{EE}(\text{Max.})$; $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	150	—	550	200	350	500	200	350	500	200	350	500	ps
t_{skew}	Within-Device Skew ⁽¹⁾	—	50	—	—	50	—	—	50	—	—	50	—	ps
	Within-Gate Skew ⁽²⁾	—	25	—	—	25	—	—	25	—	—	25	—	ps
t_r t_f	Rise/Fall Time 20% to 80%	275	—	625	300	380	575	300	380	575	300	380	575	ps

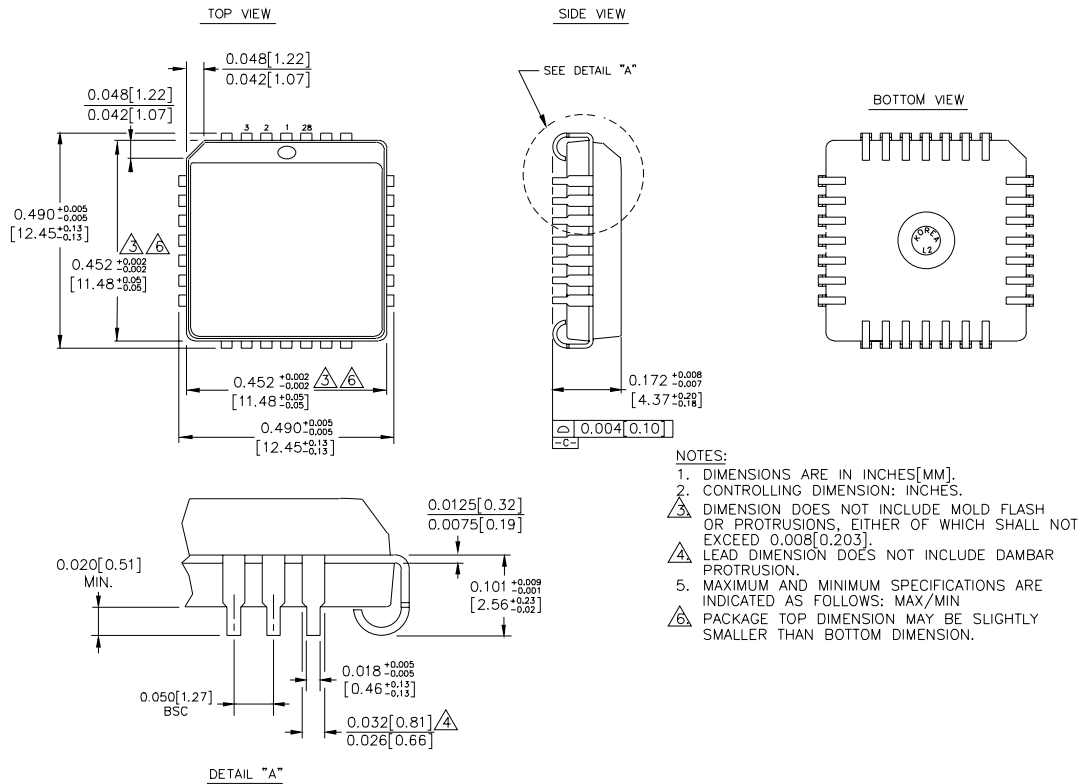
NOTES:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the variation in propagation delays through a single gate when driven from its different inputs.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E101JC	J28-1	Commercial
SY10E101JCTR	J28-1	Commercial
SY100E101JC	J28-1	Commercial
SY100E101JCTR	J28-1	Commercial

Ordering Code	Package Type	Operating Range
SY10E101JI	J28-1	Industrial
SY10E101JITR	J28-1	Industrial
SY100E101JI	J28-1	Industrial
SY100E101JITR	J28-1	Industrial

28 LEAD PLCC (J28-1)

Rev. 03