FEATURES

- 9-bit latch
- Extended 100E V_{EE} range of –4.2V to –5.5V
- Parity detection/generation
- 800ps max. D to Output
- Reset
- Internal 75KΩ input pull-down resistors
- Fully compatible with Motorola MC10E/100E175
- Available in 28-pin PLCC package

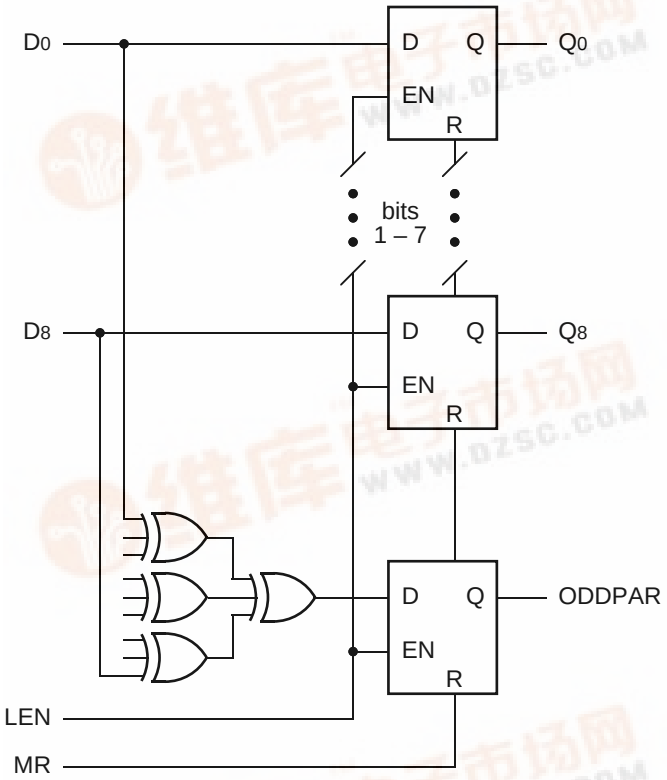
DESCRIPTION

The SY10/100E175 are 9-bit latches. They also feature a tenth latched output (ODDPAR) which is formed as the odd parity of the nine data inputs (ODDPAR is HIGH if an odd number of the inputs are HIGH).

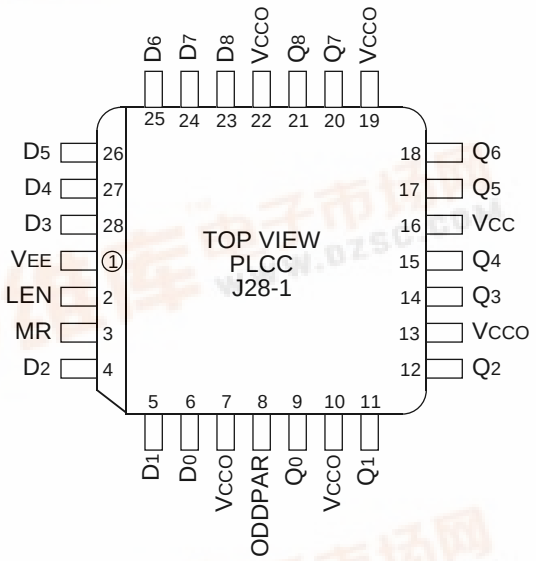
The E175 can also be used to generate byte parity by using D_8 as the parity-type select (L = even parity, H = odd parity) and using ODDPAR as the byte parity output.

The LEN pin latches the data when asserted with a logical high and makes the latch transparent when placed at a logic low level.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0 – D_8	Data Inputs
LEN	Latch Enable
MR	Master Reset
Q_0 – Q_8	Data Outputs
ODDPAR	Parity Output
V_{CCO}	V_{CC} to Output

TRUTH TABLE

D	LEN	MR	Q	ODDPAR
H	L	L	H	H if odd no. of D_n HIGH
L	L	L	L	H if odd no. of D_n HIGH
X	H	L	Q_0	Q_0
X	X	H	L	L

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	110	132	—	110	132	—	110	132		
	100E	—	110	132	—	110	132	—	127	152		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D to Q	450	600	800	450	600	800	450	600	800		
	D to ODDPAR	850	1150	1450	850	1150	1450	850	1150	1450		
	LEN to Q	525	700	900	525	700	900	525	700	900		
	LEN to ODDPAR	525	700	900	525	700	900	525	700	900		
	MR to Q (t_{PHL})	525	700	900	525	700	900	525	700	900		
	MR to ODDPAR (t_{PHL})	525	700	900	525	700	900	525	700	900		
t_S	Set-up Time										ps	—
	D (Q)	275	100	—	275	—	—	275	—	—		
	D (ODDPAR)	900	700	—	900	—	—	900	—	—		
t_H	Hold Time										ps	—
	D (Q)	175	–100	—	175	—	—	175	—	—		
	D (ODDPAR)	–300	–700	—	–300	—	—	–300	—	—		
t_{RR}	Reset Recovery Time	850	600	—	850	600	—	850	600	—	ps	—
t_{skew}	Within-Device Skew										ps	1
	LEN, MR	—	75	—	—	75	—	—	75	—		
	D to Q	—	75	—	—	75	—	—	75	—		
	D to ODDPAR	—	200	—	—	200	—	—	200	—		
t_r	Rise/Fall Times	300	500	800	300	500	800	300	500	800	ps	—
t_f	20–80%											

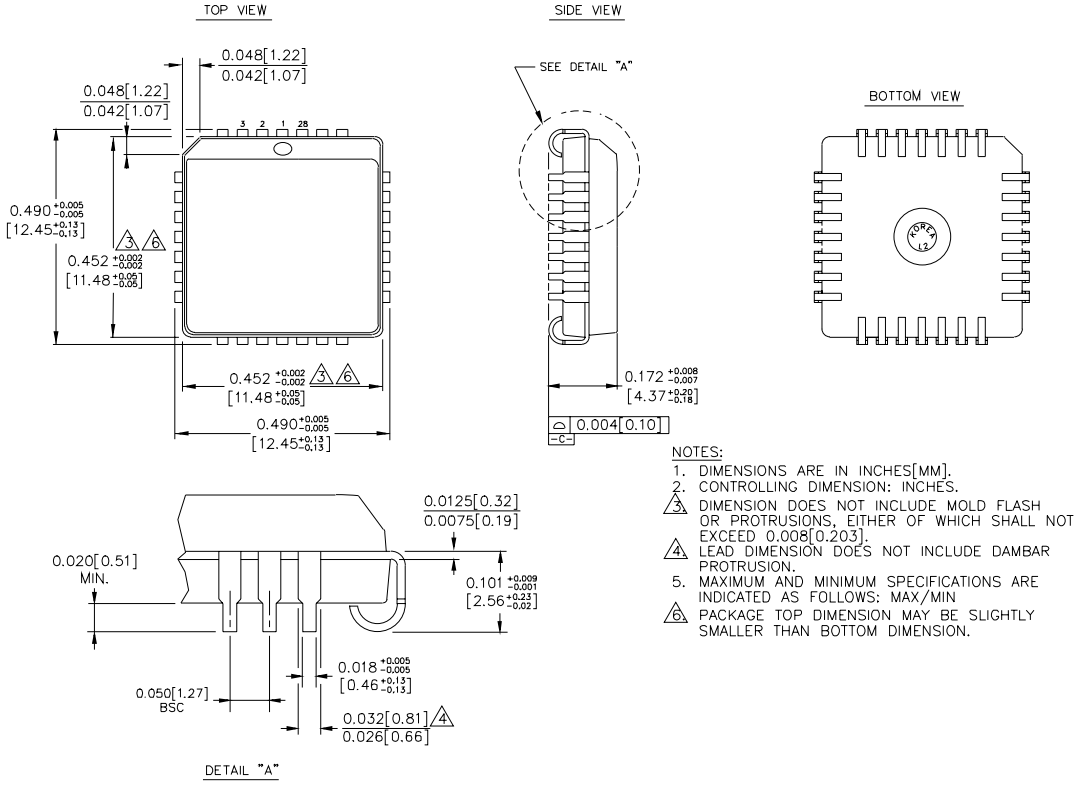
NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E175JC	J28-1	Commercial
SY10E175JCTR	J28-1	Commercial
SY100E175JC	J28-1	Commercial
SY100E175JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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