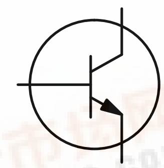
MJE18204
MJF18204

Designer's™ Data Sheet

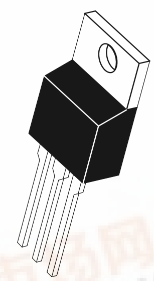
SWITCHMODE™ NPN Bipolar Power Transistor for Electronic Light Ballast and Switching Power Supply Applications

POWER TRANSISTORS
5 AMPERES
1200 VOLTS
35 and 75 WATTS

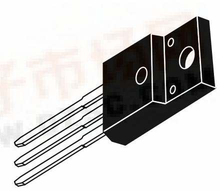


The MJE/MJF18204 have an application specific state–of–the–art die dedicated to the electronic ballast ("light ballast") and power supply applications.

- Improved Global Efficiency Due to Low Base Drive Requirements:
  - — High and Flat DC Current Gain h_{FE}
  - — Fast Switching
  - — No Coil Required in Base Circuit for Fast Turn–Off (No Current Tail)
- Full Characterization at 125°C
- Motorola "6 SIGMA" Philosophy Provides Tight and Reproducible Parametric Distributions
- Two Package Choices: Standard TO–220 or Isolated TO–220



CASE 221A–06
TO–220AB



CASE 221D–02
TO–220 FULLPACK

MAXIMUM RATINGS

Rating	Symbol	MJE18204	MJF18204	Unit
Collector–Emitter Voltage	V_{CEO}	600		Vdc
Collector–Base Voltage	V_{CBO}	1200		Vdc
Collector–Emitter Voltage	V_{CES}	1200		Vdc
Emitter–Base Voltage	V_{EBO}	10		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5 10		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4		Adc
RMS Isolation Voltage (2) (for 1 sec, R.H. ≤ 30%) T_C = 25°C — Per Figure 22 Per Figure 23 Per Figure 24	V_{ISOL1} V_{ISOL2} V_{ISOL3}		4500 3500 1500	Volts
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	35 0.28	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18204	MJF18204	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	3.55 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Voltage (I_C = 1 mA, I_B = 0)		V_{CEO}	600	660		Vdc
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH) (I_C = 200 mA, L = 25 mH, R = 2 Ω)		 $V_{CEO(sus)}$ $V_{CER(sus)}$	 550 600	 630 700		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA, I_E = 0)		V_{CBO}	1200	1300		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA, I_C = 0)		V_{EBO}	10	12.9		Vdc
Collector Cutoff Current (V_{CE} = 600 V, I_B = 0) (V_{CE} = 550 V, I_B = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CEO}			200 2000	µAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0) (V_{CE} = 1000 V, V_{BE} = 0)	@ T_C = 25°C @ T_C = 125°C @ T_C = 125°C	I_{CES}			100 500 100	µAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}			100	µAdc
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	µAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.1 Adc) (I_C = 2 Adc, I_B = 0.4 Adc)		$V_{BE(sat)}$		 0.83 0.92	 1.1 1.25	Vdc
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.1 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.3 0.7	1 1.25	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.3 0.8	0.6 1.25	
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	18	 23	35	—
(I_C = 1 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 8	 13	22	
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		5 4	8 6		—
(I_C = 5 mAdc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		10	25 33		—
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}			200	pF
Input Capacitance (V_{EB} = 8 Vdc)		C_{ib}			2000	pF

DYNAMIC SATURATION VOLTAGE

Characteristic	Conditions			Symbol	Min	Typ	Max	Unit
Dynamic Saturation Voltage: Determined 1 µs and 3 µs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 2 Adc I_{B1} = 660 mAdc V_{CC} = 300 V	@ 3 µs	@ T_C = 25°C	$V_{CE(dsat)}$		2.5		V
			@ T_C = 125°C			7.5		
	I_C = 2 Adc I_{B1} = 0.4 Adc V_{CC} = 300 V	@ 3 µs	@ T_C = 25°C			7		
			@ T_C = 125°C			15		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)							
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		105	175	ns
Turn–off Time		@ T_C = 25°C	t_{off}		1.75	2.5	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		95	200	ns
Turn–off Time		@ T_C = 25°C	t_{off}		3.5	4.5	μs
Turn–on Time	I_C = 0.7 Adc, I_{B1} = 50 mAdc I_{B2} = 0.4 Adc V_{CC} = 125 Vdc PW = 70 μs	@ T_C = 25°C	t_d		70	150	ns
			t_r		210	400	ns
Turn–off Time		@ T_C = 25°C	t_s		0.9	1.2	μs
			t_f		275	450	ns
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 1 Adc I_{B1} = 0.1 Adc I_{B2} = 0.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		110 95	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.35 1.9	2	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		150 115	250	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 1 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		120 180	200	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.9 2.35	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		190 180	300	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc	@ T_C = 25°C	t_f		185	300	ns
Storage Time		@ T_C = 25°C	t_s		4	5	μs
Crossover Time		@ T_C = 25°C	t_c		350	500	ns

TYPICAL STATIC CHARACTERISTICS

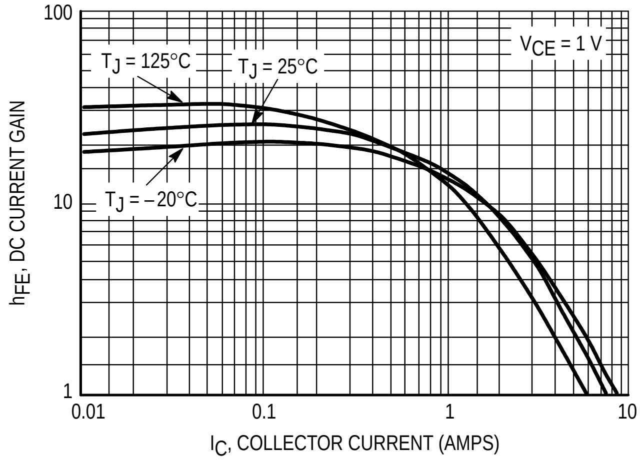


Figure 1. DC Current Gain @ 1 Volt

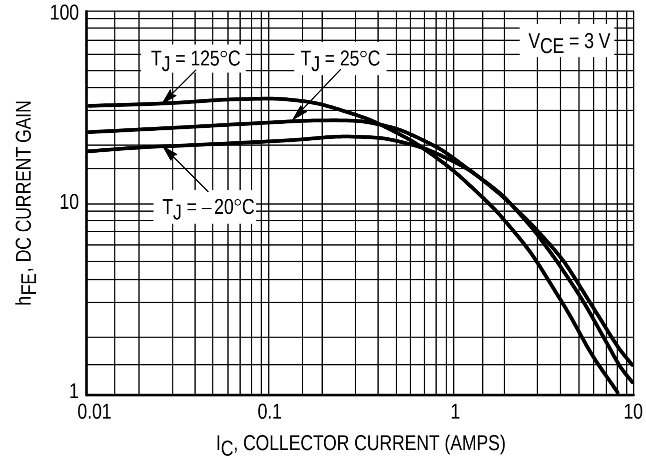


Figure 2. DC Current Gain @ 3 Volts

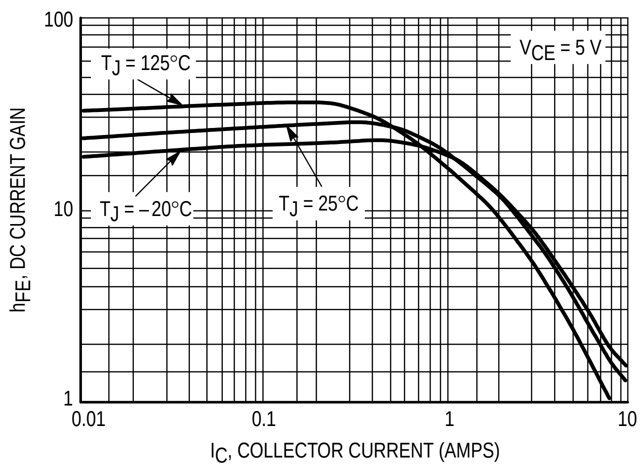


Figure 3. DC Current Gain @ 5 Volts

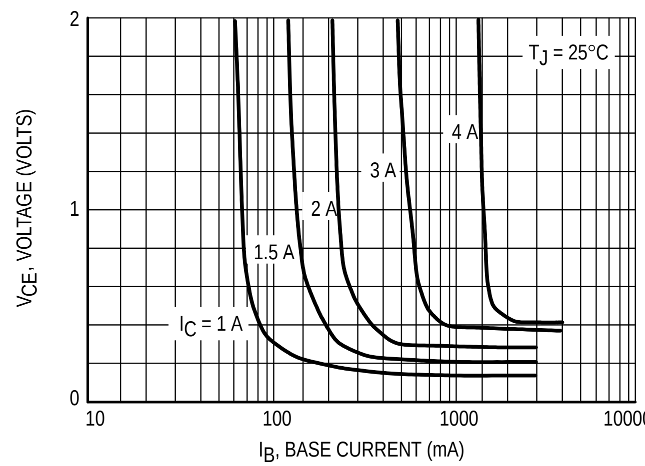


Figure 4. Collector Saturation Region

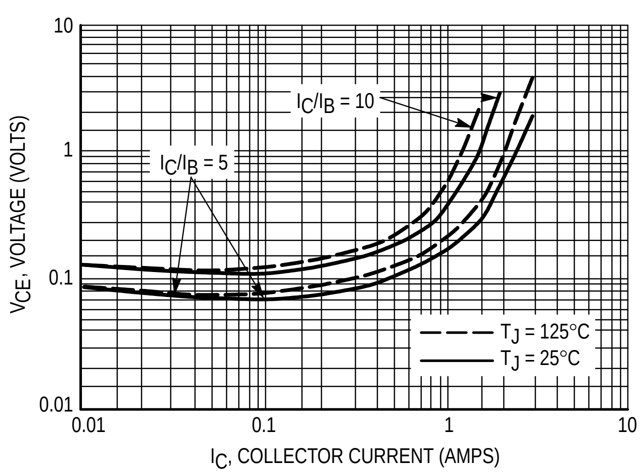


Figure 5. Collector–Emitter Saturation Voltage

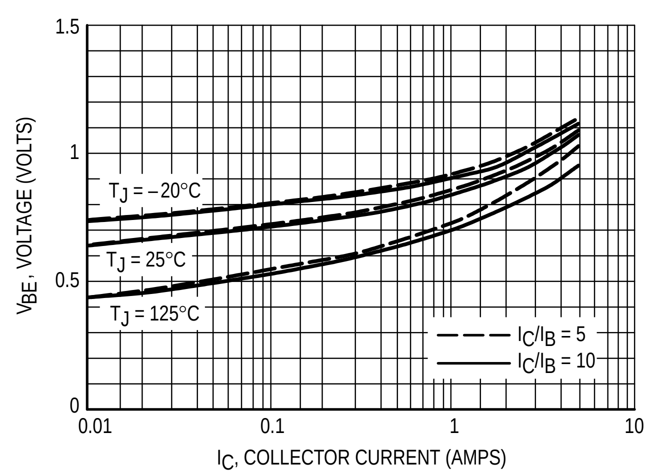


Figure 6. Base–Emitter Saturation Region

TYPICAL STATIC CHARACTERISTICS

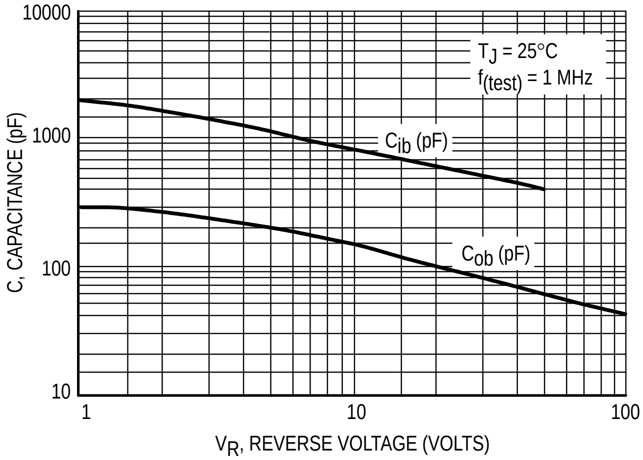


Figure 7. Capacitance

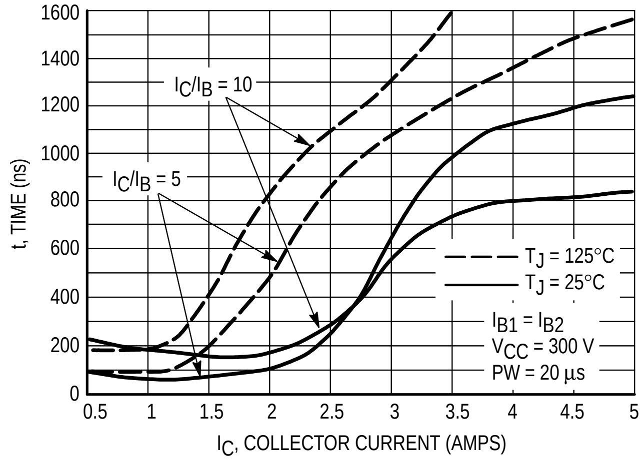


Figure 8. Resistive Switching, t_{on}

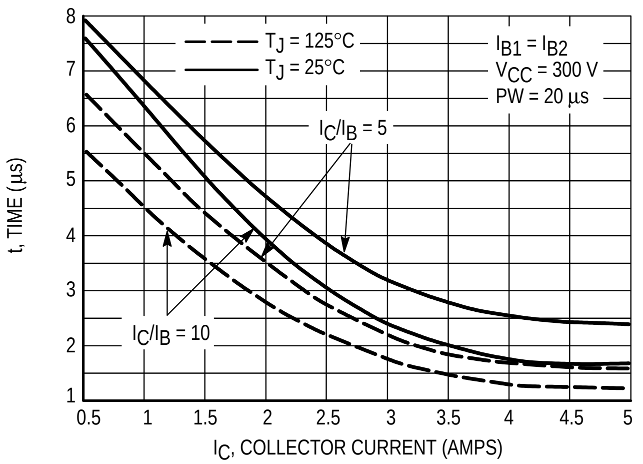


Figure 9. Resistive Switching, t_{off}

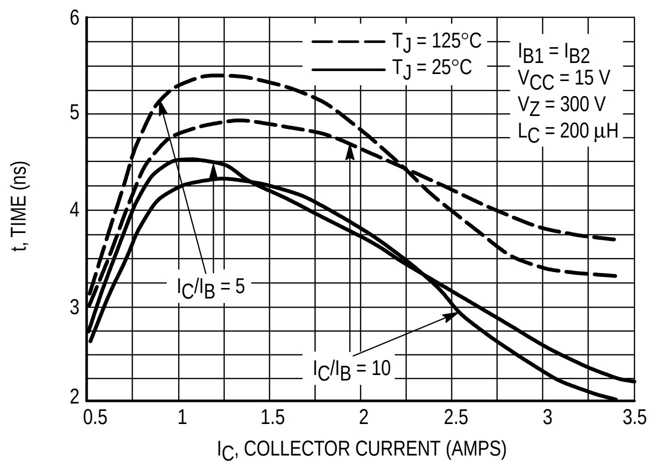


Figure 10. Inductive Storage Time, t_{si}

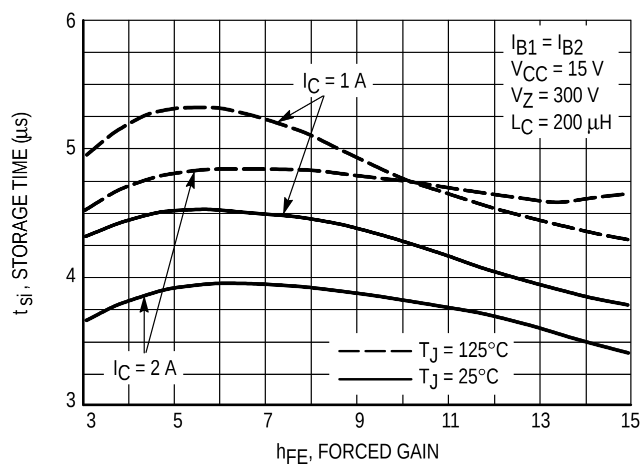


Figure 11. Inductive Storage Time, t_{si} (h_{FE})

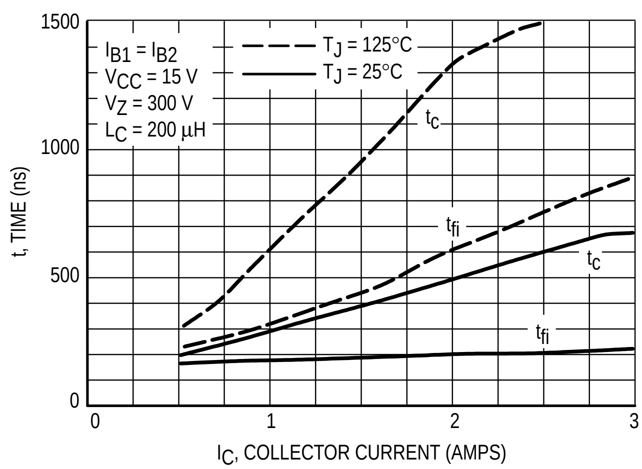


Figure 12. Inductive Switching,
t_c & t_{fi} @ $I_C/I_B = 5$

TYPICAL STATIC CHARACTERISTICS

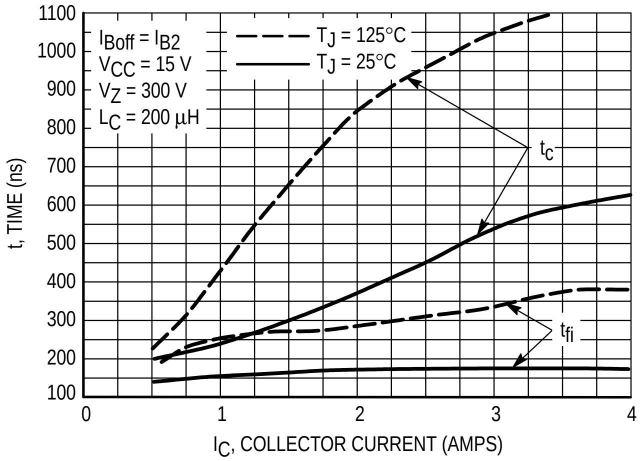


Figure 13. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 10

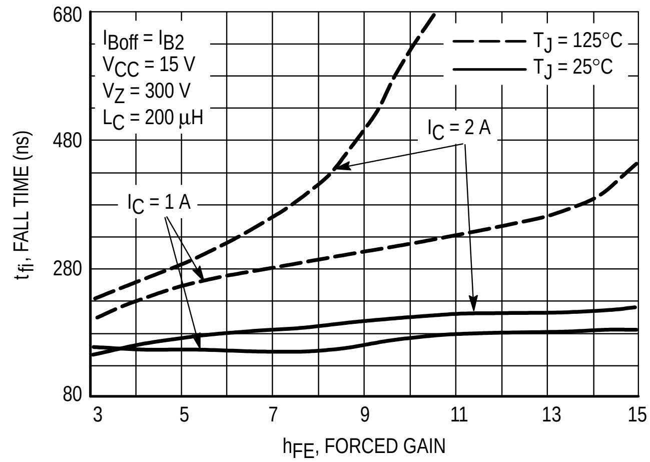


Figure 14. Inductive Fall Time

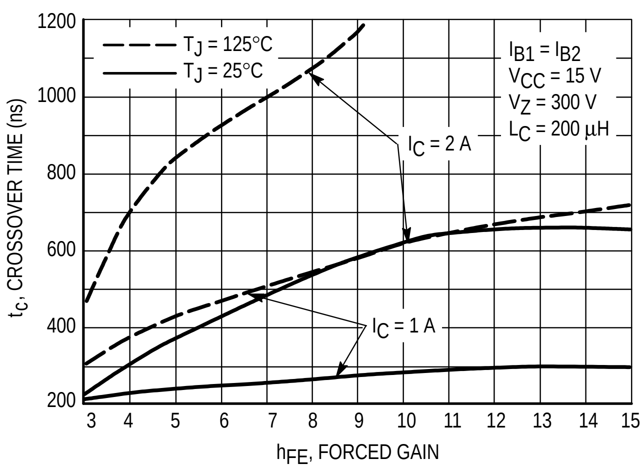


Figure 15. Inductive Crossover Time

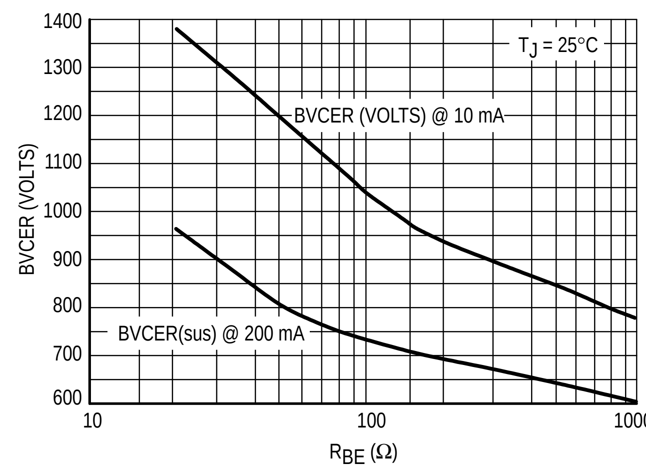


Figure 16. BVCER = f (R_{BE})

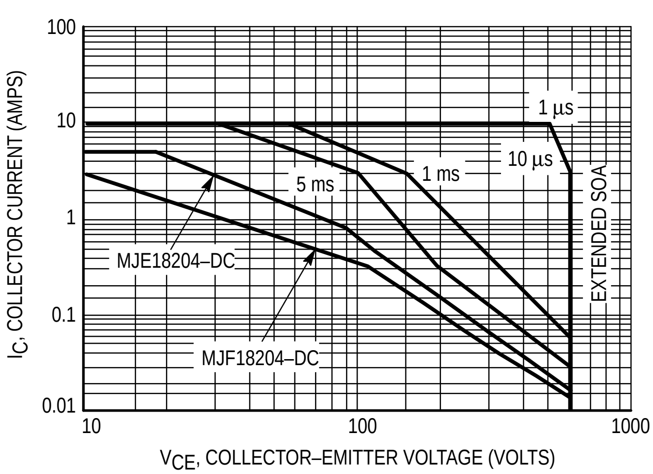


Figure 17. Forward Bias Safe Operating Area

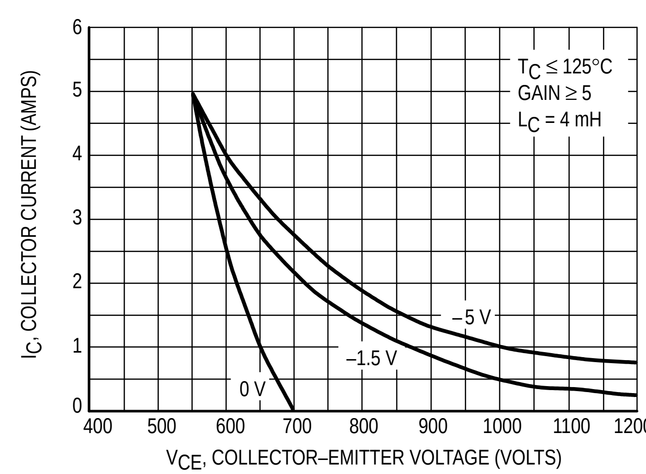


Figure 18. Reverse Bias Switching Safe Operating Area

TYPICAL STATIC CHARACTERISTICS

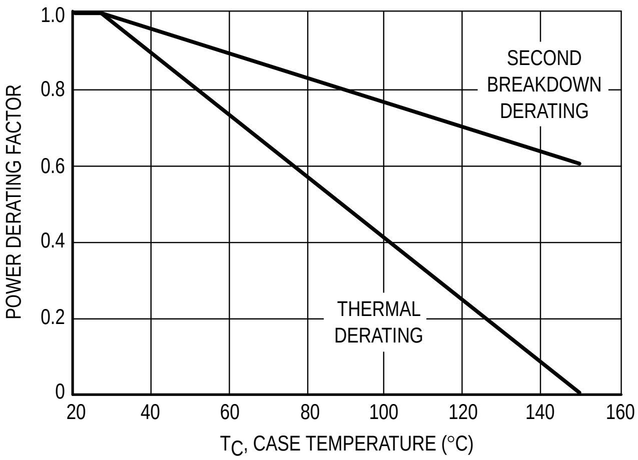


Figure 19. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 19 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

T_J(pk) may be calculated from the data in Figures 21 and 22. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse biased. The safe level is specified as a reverse–biased safe operating area (Figure 17). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL SWITCHING CHARACTERISTICS
($I_{B1} = I_{B2}$ FOR ALL CURVES)

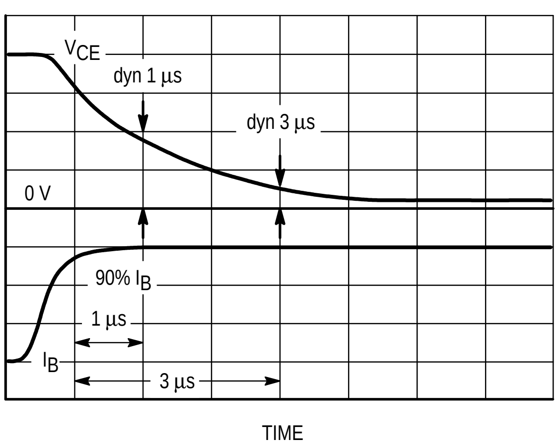


Figure 20. Dynamic Saturation Voltage Measurements

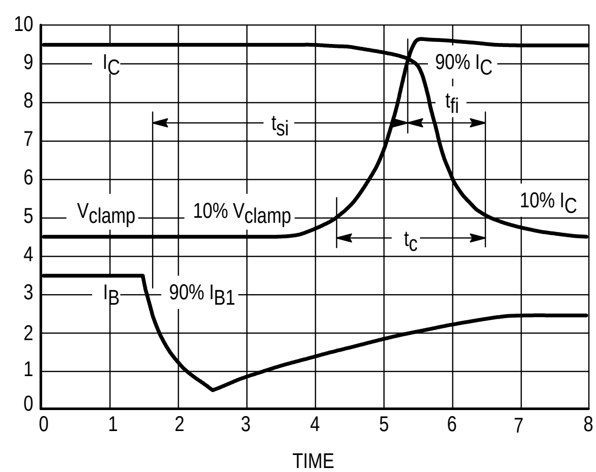
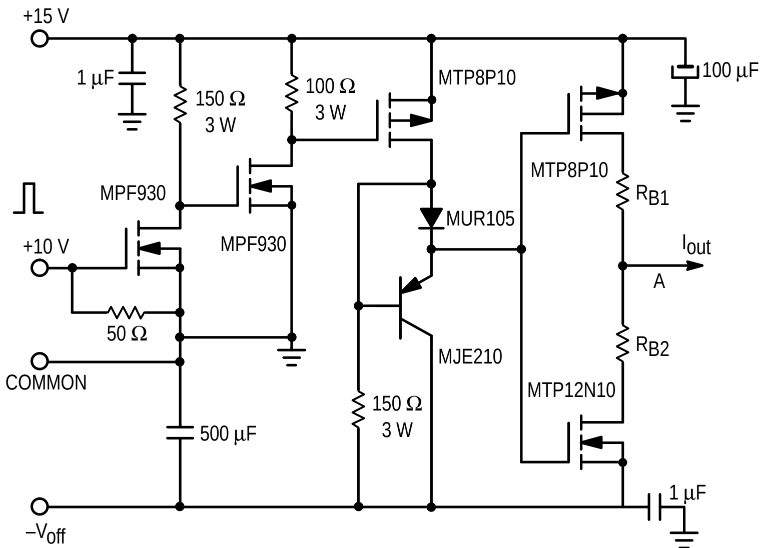
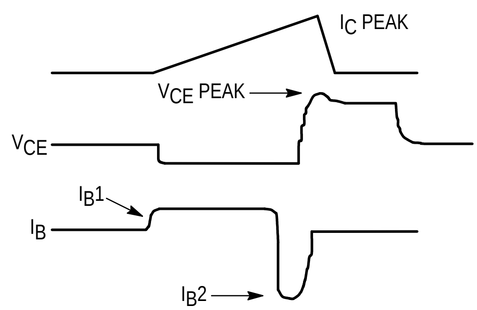


Figure 21. Inductive Switching Measurements

TYPICAL SWITCHING CHARACTERISTICS
($I_{B1} = I_{B2}$ FOR ALL CURVES)

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 µH	L = 500 µH
$R_{B2} = \infty$	$R_{B2} = 0$	$R_{B2} = 0$
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE
($I_{B1} = I_{B2}$ FOR ALL CURVES)

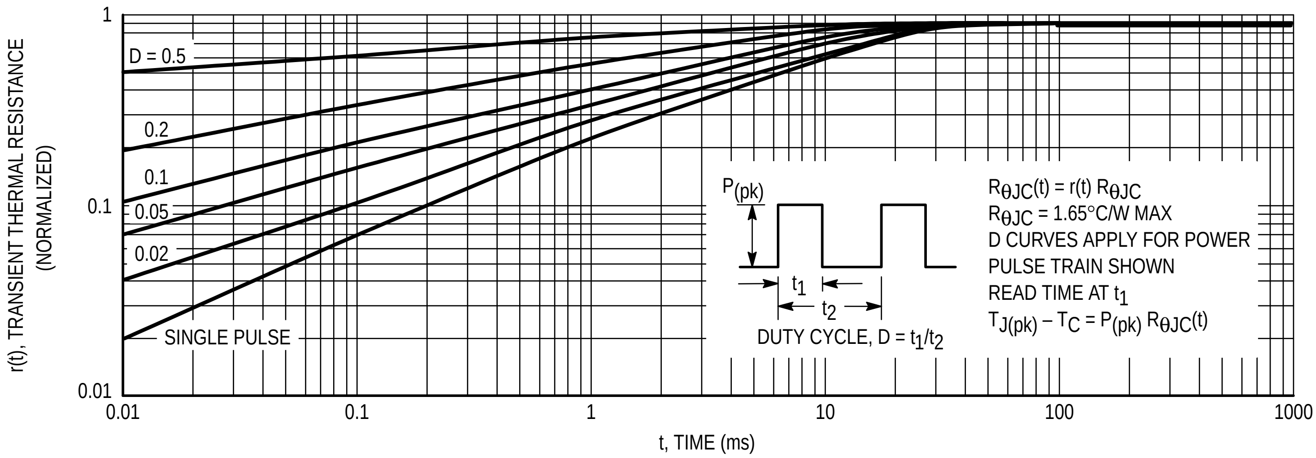


Figure 22. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18204

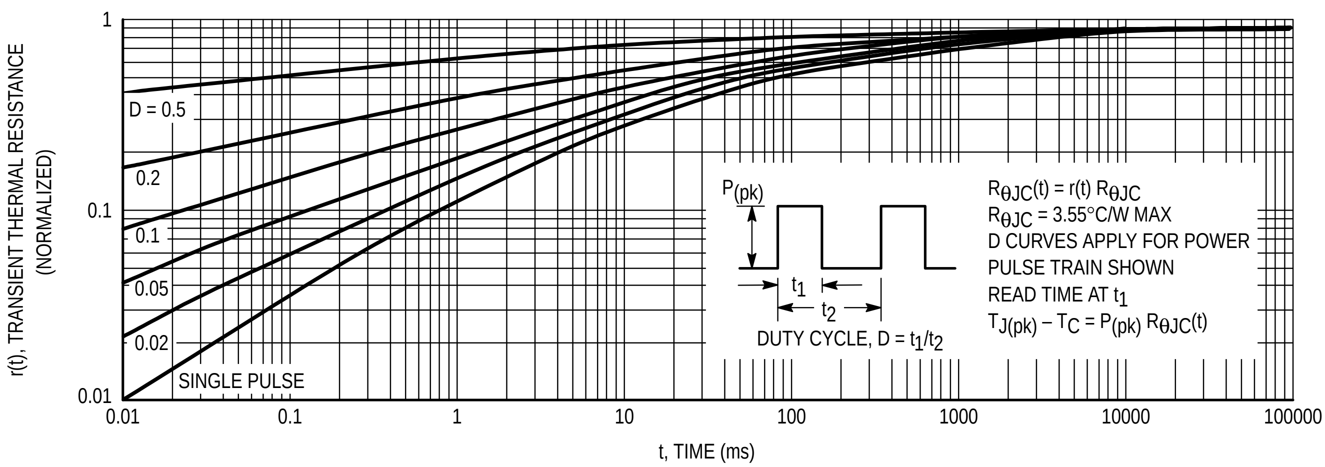


Figure 23. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJF18204

TEST CONDITIONS FOR ISOLATION TESTS*

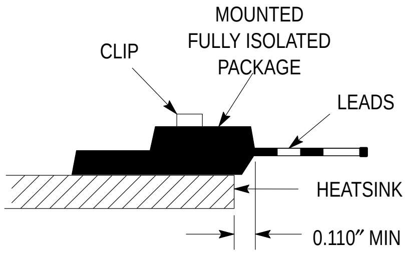


Figure 24. Screw or Clip Mounting Position for Isolation Test Number 1

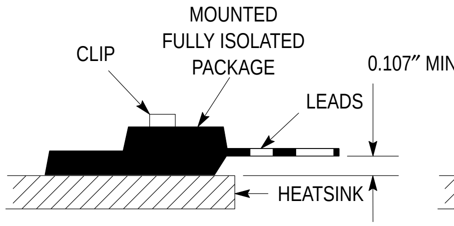


Figure 25. Clip Mounting Position for Isolation Test Number 2

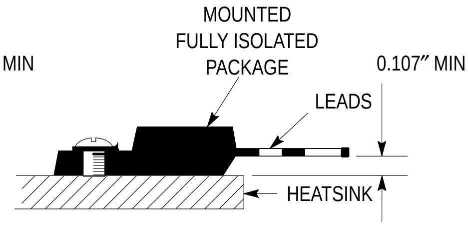


Figure 26. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

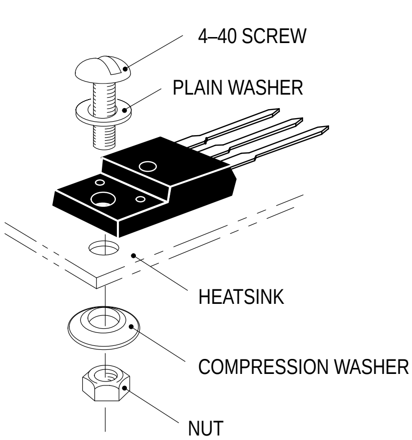


Figure 27a. Screw–Mounted

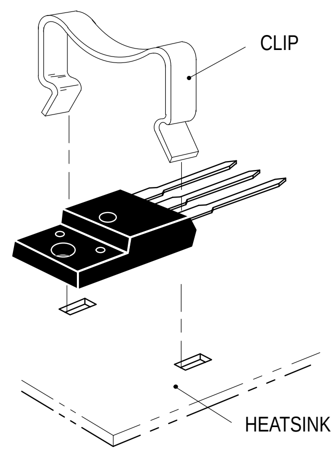


Figure 27b. Clip–Mounted

Figure 27. Typical Mounting Techniques for Isolated Package

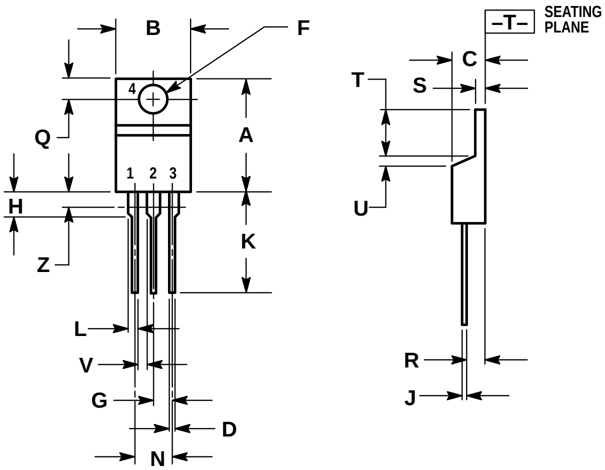
Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

PACKAGE DIMENSIONS

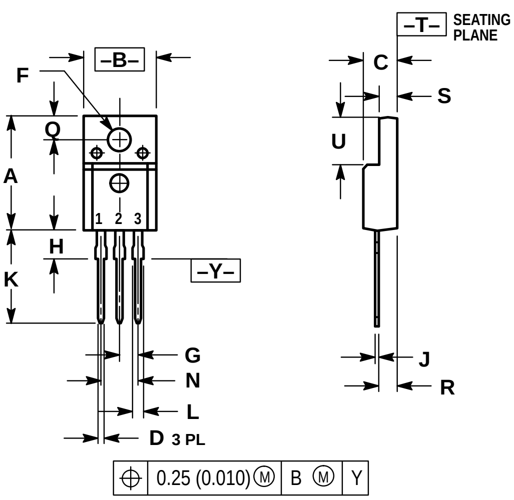


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A–06
TO–220AB
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

CASE 221D–02
(ISOLATED TO–220 TYPE)
UL RECOGNIZED: FILE #E69369
ISSUE D

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