

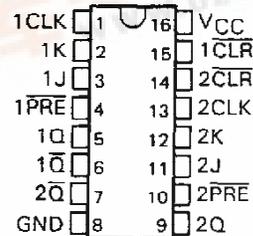
SDLS011

**SN54LS112A, SN54S112, SN74LS112A, SN74S112A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET AND CLEAR**

D2661, APRIL 1982—REVISED MARCH 1988

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54LS112A, SN54S112 . . . J OR W PACKAGE  
 SN74LS112A, SN74S112A . . . D OR N PACKAGE  
 (TOP VIEW)

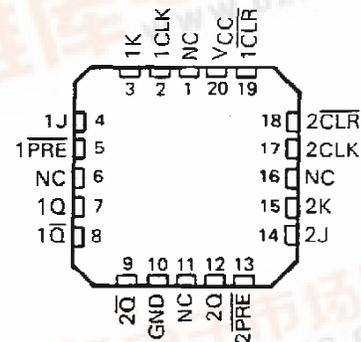


**description**

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

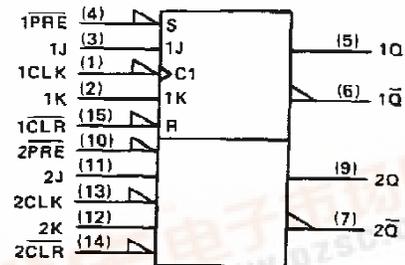
The SN54LS112A and SN54S112 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS112A and SN74S112A are characterized for operation from 0°C to 70°C.

SN54LS112A, SN54S112 . . . FK PACKAGE  
 (TOP VIEW)



NC—No internal connection

**logic symbol†**



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

FUNCTION TABLE (each flip-flop)

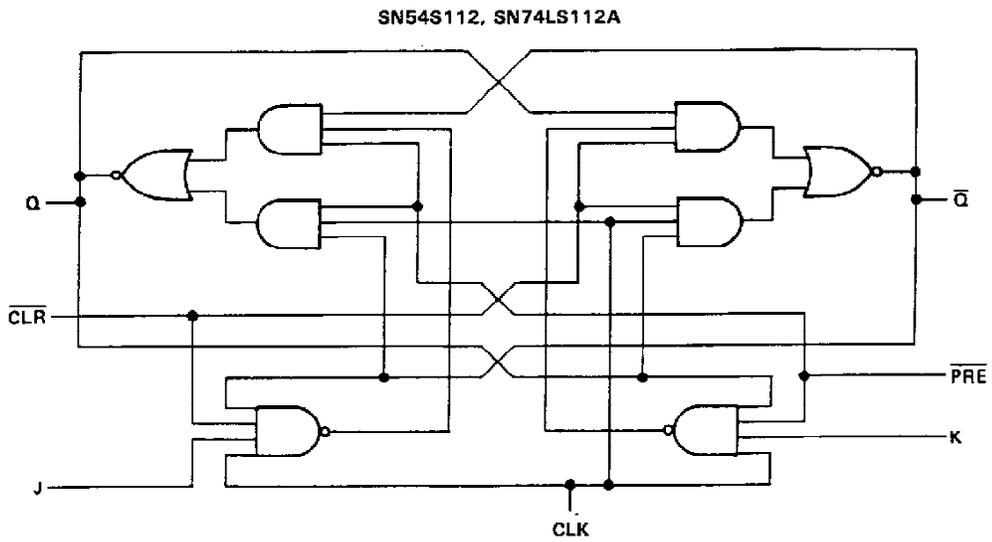
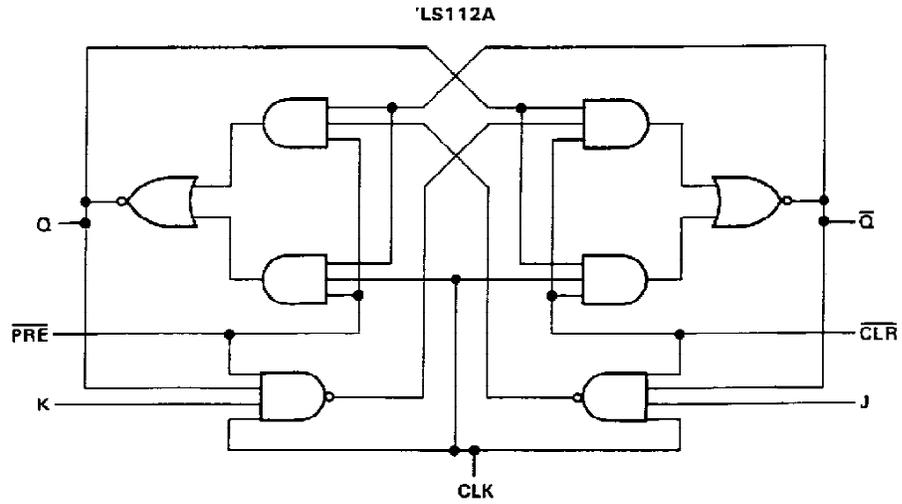
INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q-bar
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q <sub>0</sub>	Q <sub>0</sub> -bar
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q <sub>0</sub>	Q <sub>0</sub> -bar

† The output levels in this configuration are not guaranteed to meet the minimum levels for V<sub>OH</sub> if the lows at preset and clear are near V<sub>IL</sub> minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.



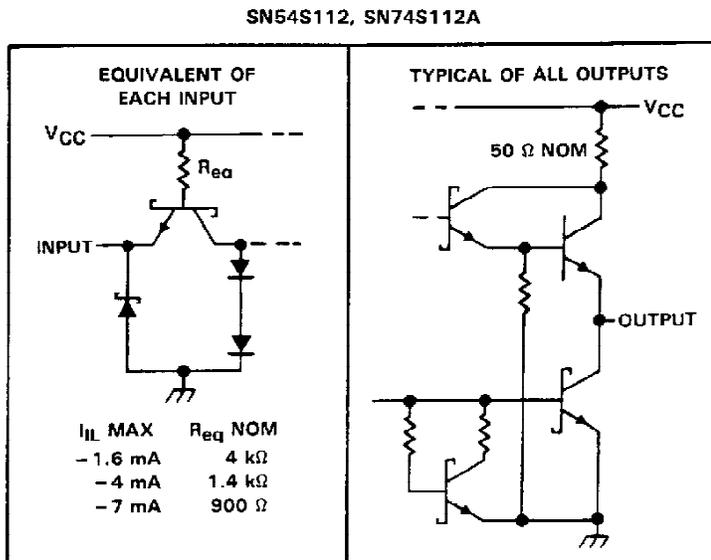
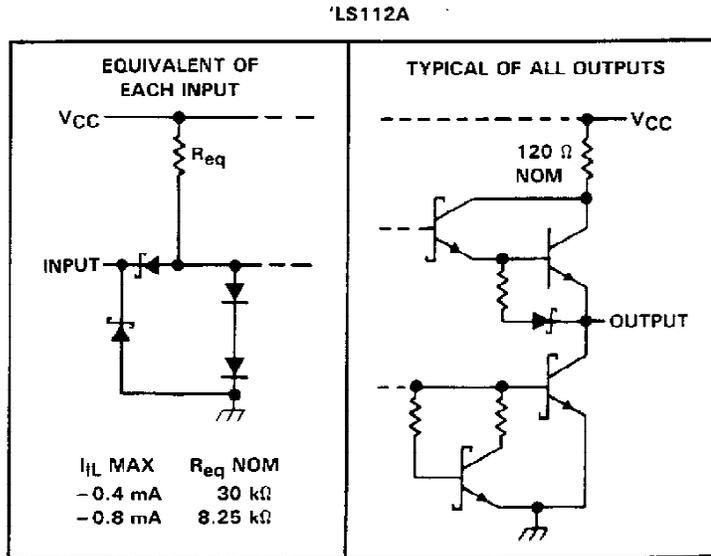
**SN54LS112A, SN54S112, SN74LS112A, SN74S112A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET AND CLEAR**

logic diagrams (positive logic)



**SN54LS112A, SN54S112, SN74LS112A, SN74S112A  
DUAL J-K NEGATIVE-EDGE-TRIGGERED  
FLIP-FLOPS WITH PRESET AND CLEAR**

schematics of inputs and outputs



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: 'LS112A	7 V
SN54LS112, SN74LS112A	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

**SN54LS112A, SN74LS112A  
DUAL J-K NEGATIVE-EDGE-TRIGGERED  
FLIP-FLOPS WITH PRESET AND CLEAR**

**recommended operating conditions**

		SN54LS112A			SN74LS112A			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
V <sub>IH</sub>	High-level input voltage	2			2			V		
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V		
I <sub>OH</sub>	High-level output current			-0.4			-0.4	mA		
I <sub>OL</sub>	Low-level output current			4			8	mA		
f <sub>clock</sub>	Clock frequency	0		30	0		30	MHz		
t <sub>w</sub>	Pulse duration	CLK high		20			20	ns		
		PRE or CLR low		25			25			
t <sub>su</sub>	Set up time-before CLK↓	Data high or low		20			20	ns		
		CLR inactive		25			25			
		PRE inactive		20			20			
t <sub>h</sub>	Hold time-data after CLK↓			0			0	ns		
T <sub>A</sub>	Operating free-air temperature			-55		125		0	70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†	SN54LS112A			SN74LS112A			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V <sub>IK</sub>		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V	
V <sub>OH</sub>		V <sub>CC</sub> = MIN, I <sub>OH</sub> = -0.4 mA, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	2.5	3.4		2.7	3.4		V	
V <sub>OL</sub>		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 4 mA, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V		0.25	0.4		0.25	0.4	V	
		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 8 mA, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V					0.35	0.5		
I <sub>I</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1			0.1	mA	
	CLR or PRE				0.3			0.3		
	CLK				0.4			0.4		
I <sub>IH</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			20	μA	
	CLR or PRE				60			60		
	CLK				80			80		
I <sub>IL</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4			-0.4	mA	
	All other				-0.8			-0.8		
I <sub>OS</sub> §		V <sub>CC</sub> = MAX, see Note 2	-20		-100			-20	-100	mA
I <sub>CC</sub> (Total)		V <sub>CC</sub> = MAX, see Note 3		4	6		4	6	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTES: 2. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

3. With all outputs open, I<sub>CC</sub> is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

**SN54LS112A, SN74LS112A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET AND CLEAR**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\max}$			$R_L = 2\text{ k}\Omega$ , $C_L = 15\text{ pF}$	30	45		MHz
$t_{PLH}$	CLR, PRE or CLK	Q or $\bar{Q}$			15	20	ns
$t_{PHL}$					15	20	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

**SN54S112, SN74S112A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET AND CLEAR**

**recommended operating conditions**

		SN54S112			SN74S112A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage	0.8			0.8			V
$I_{OH}$	High-level output current	-1			-1			mA
$I_{OL}$	Low-level output current	20			20			mA
$t_w$	Pulse duration	CLK high	6		6		ns	
		CLK low	6.5		6.5			
		PRE or CLR low	8		8			
$t_{su}$	Set up time-before CLK↓	7		7		ns		
$t_h$	Hold time-data after CLK↓	0		0		ns		
$T_A$	Operating free-air temperature	-55	125		0	70		°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†		SN54S112			SN74S112A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$		$V_{CC} = \text{MIN.}, I_I = -18 \text{ mA}$		-1.2			-1.2			V
$V_{OH}$		$V_{CC} = \text{MIN.}, V_{IH} = 2 \text{ V.}, V_{IL} = \text{MAX.}, I_{OH} = -1 \text{ mA}$		2.5	3.4		2.7	3.4		V
$V_{OL}$		$V_{CC} = \text{MIN.}, V_{IH} = 2 \text{ V.}, V_{IL} = 0.8 \text{ V.}, I_{OL} = 20 \text{ mA}$		0.5			0.5			V
$I_I$		$V_{CC} = \text{MAX.}, V_I = 5.5 \text{ V}$		1			1			mA
$I_{IH}$	J or K	$V_{CC} = \text{MAX.}, V_I = 2.7 \text{ V}$		50			50			$\mu\text{A}$
	All other			100			100			
$I_{IL}$	J or K	$V_{CC} = \text{MAX.}, V_I = 0.5 \text{ V}$		-1.6			-1.6			mA
	CLR‡			-7			-7			
	PRE‡			-7			-7			
	CLK			-4			-4			
$I_{OS}^\ddagger$		$V_{CC} = \text{MAX.}$		-40	-100		-40	-100		mA
$I_{CC}^\#$		$V_{CC} = \text{MAX.},$ see Note 3		15 25			15 25			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Clear is tested with preset high and preset is tested with clear high.

¶ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

# Values are average per flip-flop.

NOTE 3: With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

**SN54S112, SN74S112A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET AND CLEAR**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$			$R_L = 280\ \Omega, \quad C_L = 15\ \text{pF}$	80	125		MHz
$t_{PLH}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$		4	7		ns
$t_{PHL}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK high)	$\overline{\text{Q}}$ or Q		5	7		ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK low)			5	7		
$t_{PLH}$	CLK	Q or $\overline{\text{Q}}$		4	7		ns
$t_{PHL}$				5	7	ns	

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
JM38510/07102BEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
JM38510/07102BFA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30103B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30103BEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
JM38510/30103BFA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SN54LS112AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54S112J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN74LS112AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS112ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS112ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS112ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS112AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS112AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS112ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS112ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS112ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S112AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74S112ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S112ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S112AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S112AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S112ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S112ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S112ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54LS112AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS112AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS112AW	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S112FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S112J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S112W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

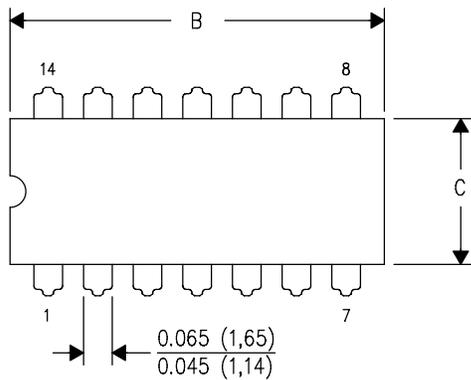
**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

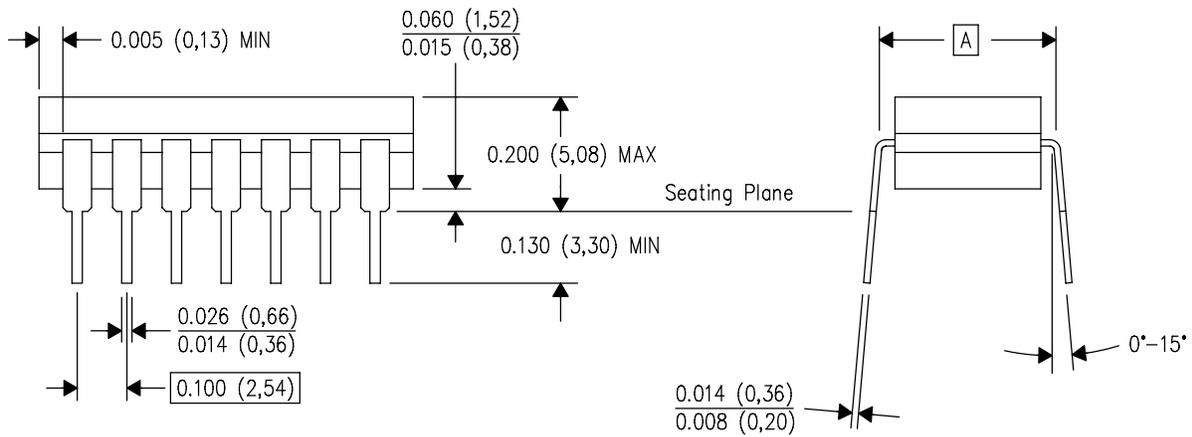
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



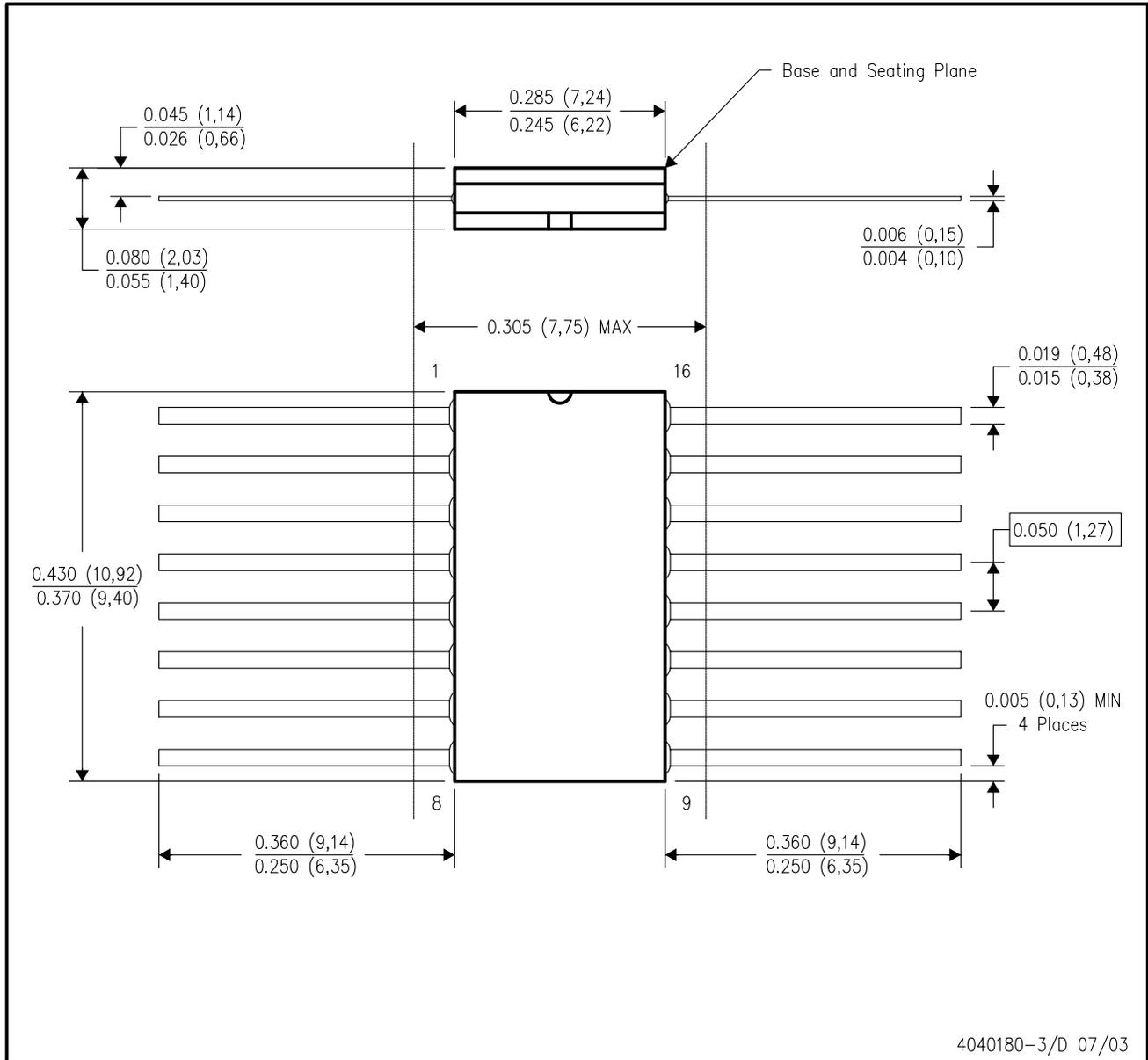
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# MECHANICAL DATA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/D 07/03

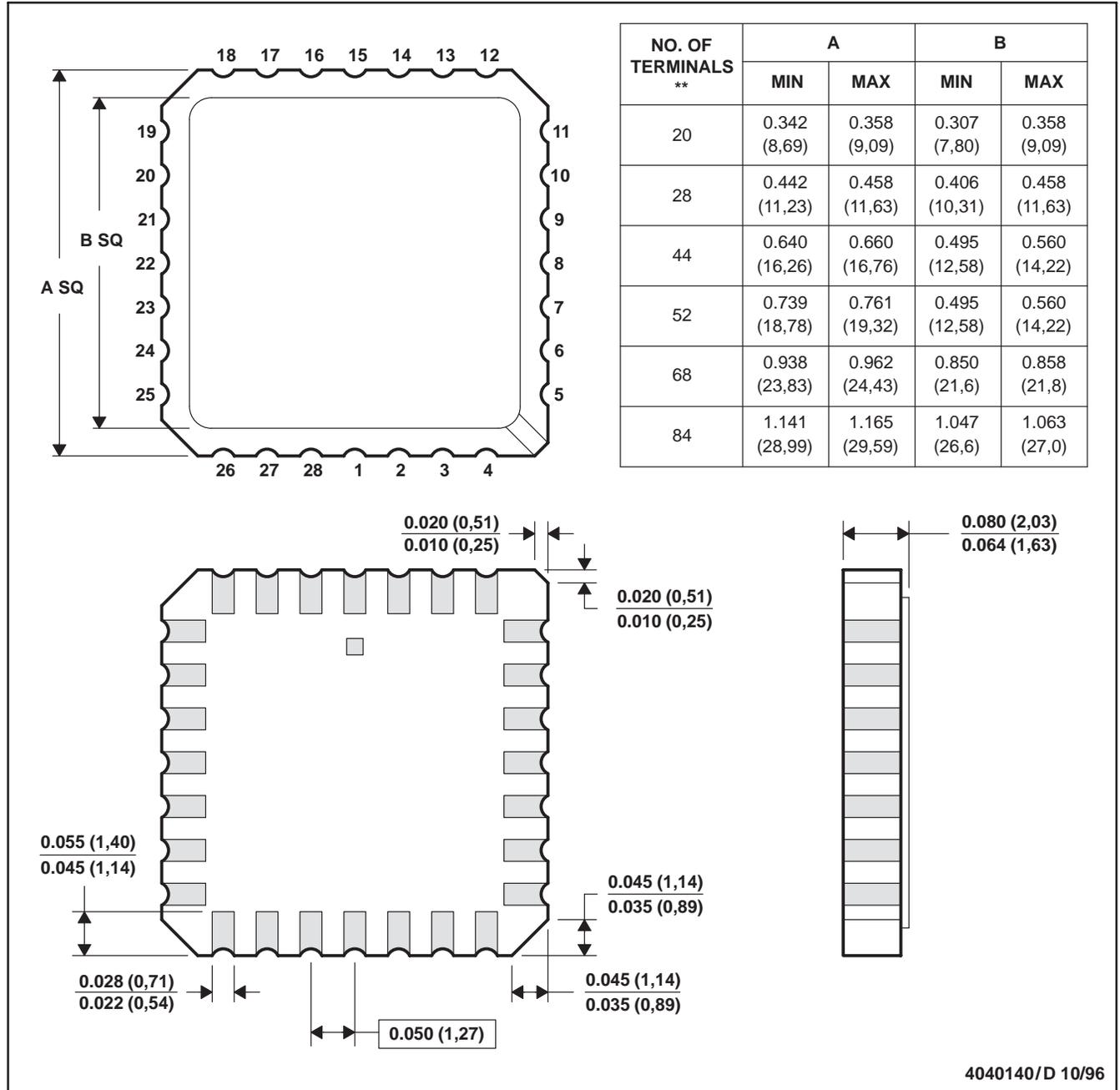
# MECHANICAL DATA

MLCC006B – OCTOBER 1996

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

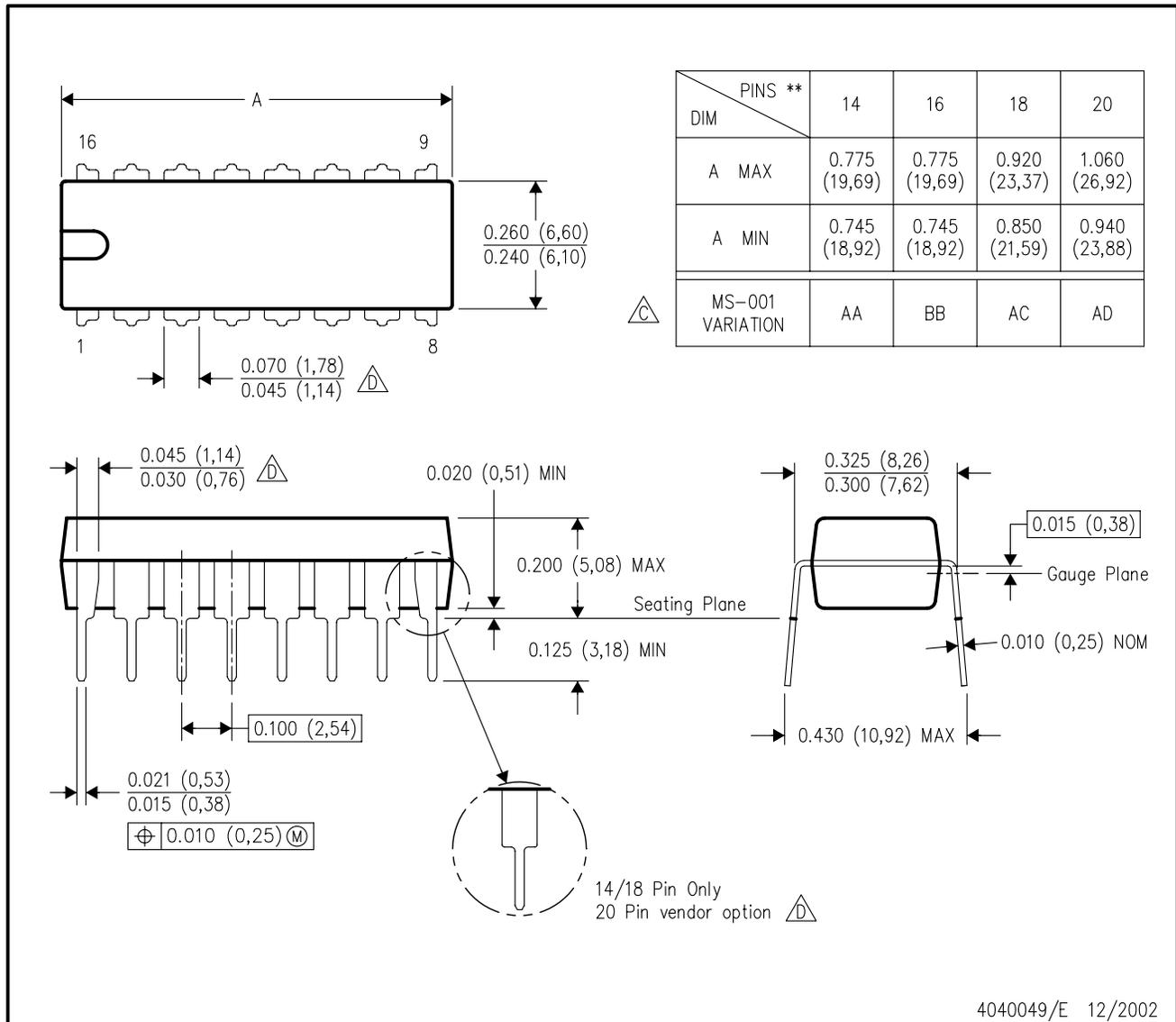
4040140/D 10/96

# MECHANICAL DATA

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE

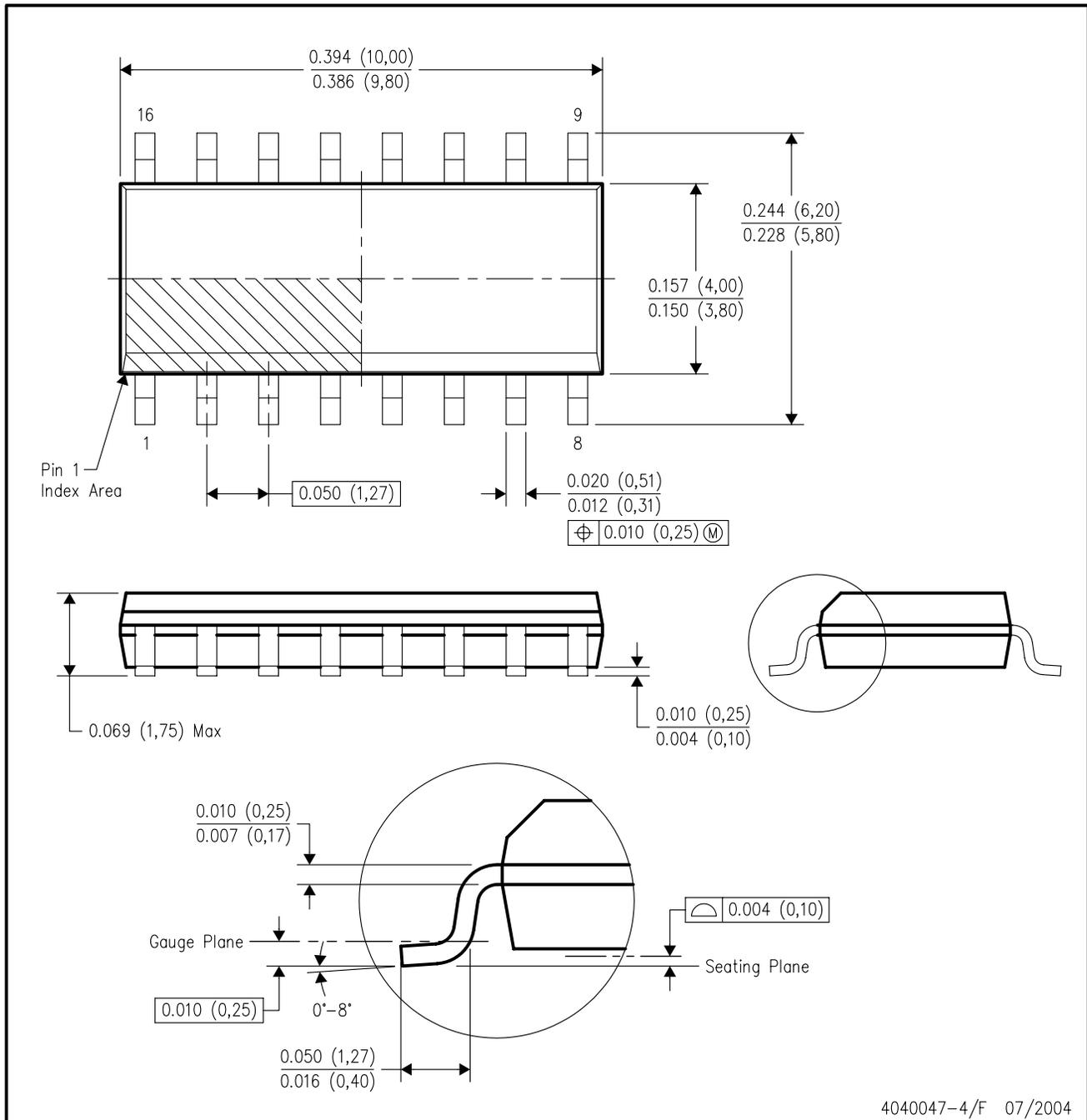


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# MECHANICAL DATA

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

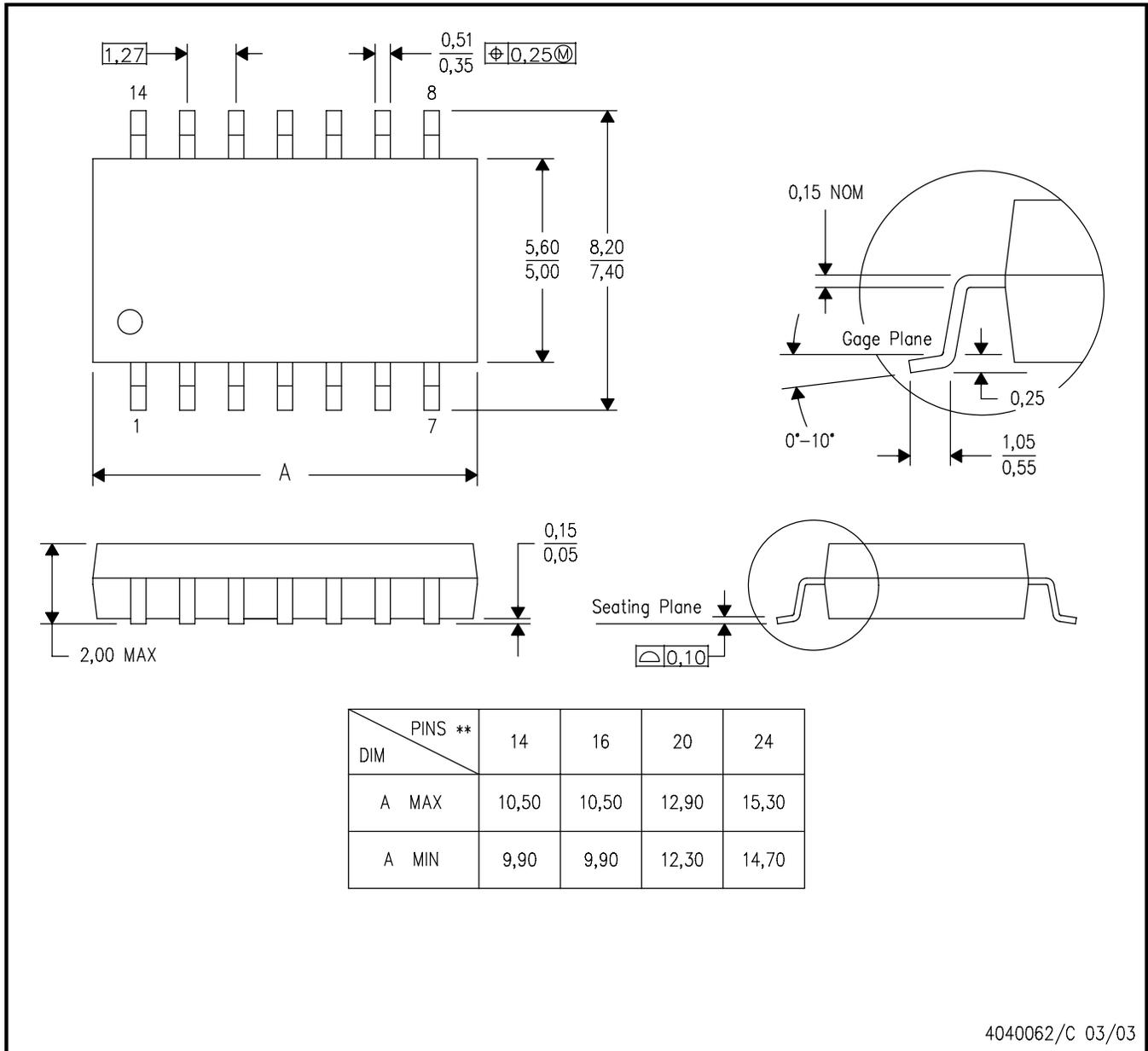
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-012 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265