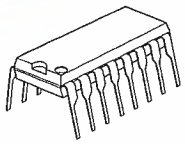
8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

■ GENERAL DESCRIPTION

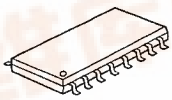
NJMDAC-08C series are 8-bit monolithic multiplying digital to analog converters with very highspeed performance. Open collector output provides dual complementary current outputs increasing versatility in application.

Adjustable threshold logic input voltage through V_{LC} pin, can be connected to various type of digital IC products.

■ PACKAGE OUTLINE



NJMDAC-08DC

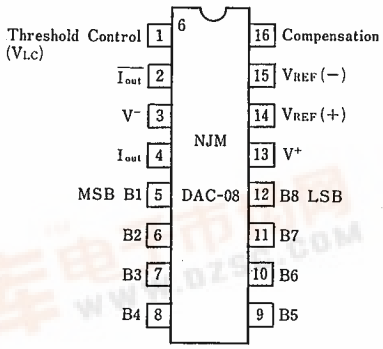


NJMDAC-08MC

■ FEATURES

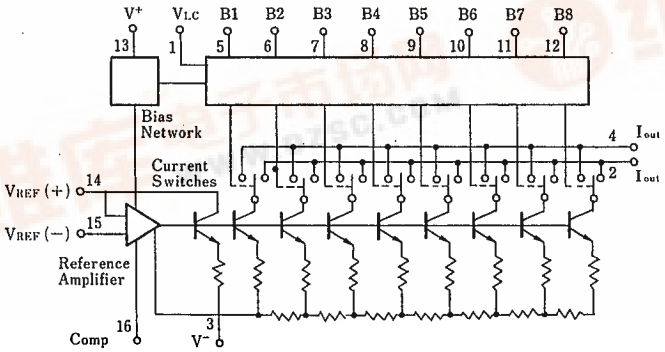
- Resolution (8bit)
- Settling Time (85ns)
- Linearity Error (±0.1%FS MAX (NJM DAC-08H))
- Full Scale Current Temperature Drift (50ppm/℃ MAX (NJM DAC-08H/E))
- Wide Operating Voltage (±5V～±18V)
- Wide Output Voltage Range (−10V～+18V)
- Wide Range Adjustable Threshold Logic Input (−10V～+13.5V(V^+/V =±15V))
- Multiplying operations can be performed
- Package Outline DIP16, DMP16
- Bipolar Technology

■ PIN CONFIGURATION



NJMDAC-08DC
NJMDAC-08MC

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply voltage	$V^+ - V^-$	36	V
Logic Input Voltage Range	V_I	$V^- \sim V^- + 36$	V
Threshold Control Input Voltage	V_{LC}	$V^- \sim V^+$	V
Analog Current Outputs	Io	4.2	mA
Reference Input Voltage Range	V_{REF}	$V^- \sim V^+$	V
Reference Input Differential Voltage	$V_{REF(+)} - V_{REF(-)}$	±18	V
Reference Input Current	I_{REF}	5.0	mA
Power Dissipation	P_D	(DIP16) 500	mW
		(DMP16) 300	mW
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=±15V, I_{REF}=2.0mA, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution			8	8	8	Bit
Monotonicity			8	8	8	Bit
Nonlinearity	NL				±0.39	%FS
*1 Settling Time	ts	To ±1/2LSB,all bits switched ON or OFF		85	150	ns
*1 Propagation Delay	t_{PLH} t_{PHL}	All bits switched		35	60	ns
*1 Full Scale Temperature Coefficient	TCI_{FS}			±10	±80	ppm/℃
Output Voltage Compliance	V_{OC}	ΔI_{FS}<1/2 LSB R_{OUT}>20 MΩ typ.	−10		+18	V
Full Scale Current	I_{FS4}	V_{REF}=10.000V R_{14}, R_{15}=5.000kΩ	1.94	1.99	2.04	mA
Full Scale Symmetry	I_{FSS}	$I_{FS4}-I_{FS2}$		±2.0	±16.0	μA
Zero Scale Current	I_{ZS}			0.2	4.0	μA
Output Current Range	I_{OR1}	V_{REF}=15 V, V^-=10 V $R_{14,15}$ 15.000 kΩ	2.1			mA
	I_{OR2}	V_{REF}=25 V, V^-=12 V $R_{14,15}$ 15.000 kΩ	4.2			mA
Logic Input Level "0"	V_{IL}	V_{LC}=0 V			0.8	V
〃 "1"	V_{IH}	V_{LC}=0 V	2.0			V
Logic Input Current "0"	I_{IL}	V_{LC}=0 V, V_{IN}=−10 V~+0.8 V		−2.0	−10	μA
"1"	I_{IH}	V_{LC}=0 V, V_{IN}=2 V~18 V		0.002	10	μA
Logic Input Swing	V_{IS}		−10		+18	V
Logic Threshold Range	V_{TH2}	———	−10		+13.5	V
Reference Bias Current	I_{IS}			−1.0	−3.0	μA
*1 Reference Input Slew Rate	dI/dt		4.0	8.0		mA/μs
*2 Power Supply Sensitivity	$PSSI_{FS}$	V^-=4.5V~18V, I_{REF}=1.0mA		±0.0003	±0.01	%/%
	$PSSI_{FS}$	V^-=−4.5V~18V, I_{REF}=1.0mA		±0.002	±0.01	
*3 Operating Current	I^+	$V^\pm$=±5 V, I_{REF}=1.0 mA		2.3	3.8	mA
	I^-	〃		−4.3	−5.8	
	I^+	V^+=5 V, V^-=−15 V		2.4	3.8	
	I^-	〃		−6.4	−7.8	
	I^+	———		2.5	3.8	
	I^-	———		−6.5	−7.8	

*1 Guaranteed by design

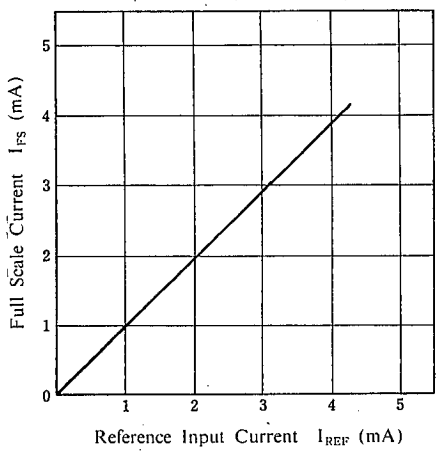
*2 Caluculation formula $PSSI_{FS}=\left(\frac{|\Delta I_{FS}|}{I_{FS}}\times 100\right)\div\left(\frac{18-4.5}{15}\right)\times 100$

*3 Caluculation formula $P_D=I^+\times(V^+-V^-)+2I_{REF}\times|V^-|$

■ TYPICAL CHARACTERISTICS

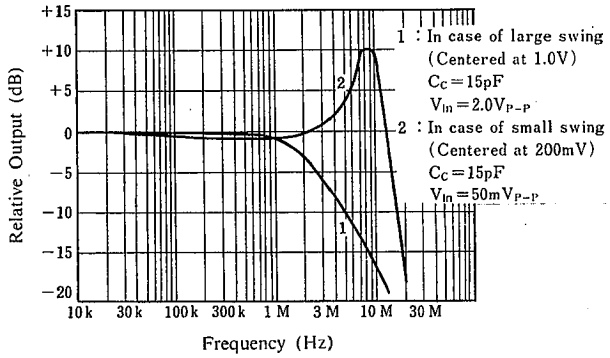
Full Scale Current vs. Reference Input Current

(All bits on, $V^- = -15V$)

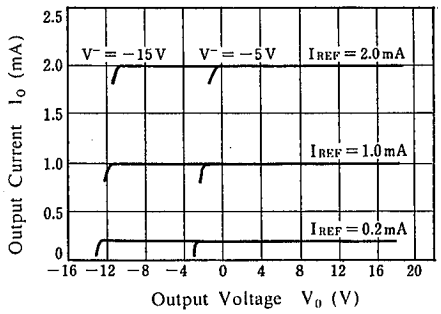


Reference Input Frequency Respons

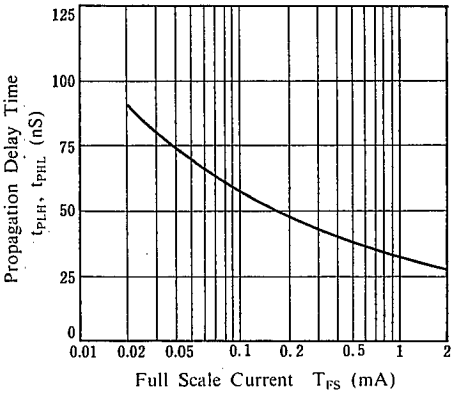
($R_{14}=R_{15}=1k\Omega$, $R_L=100\Omega$, ALL BITS "ON")



Output Current vs. Output Voltage

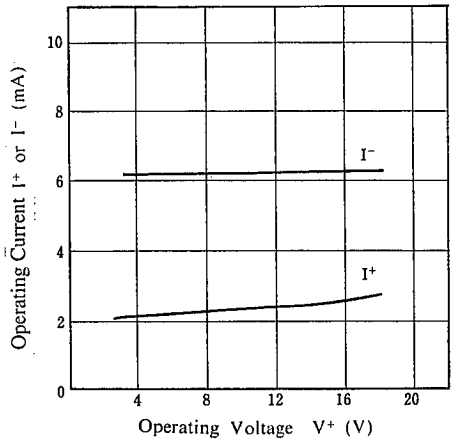


Propagation Delay Time vs. Full Scale Current



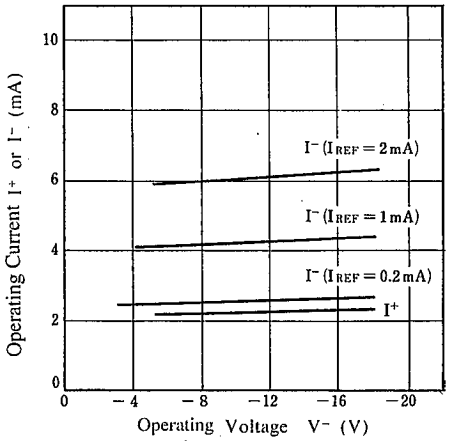
Operating Current vs. Operating Voltage

(ALL BITS "HIGH", OR "LOW")



Operating Current vs. Operating Voltage

(BITS MAY BE "HIGH" OR "LOW")



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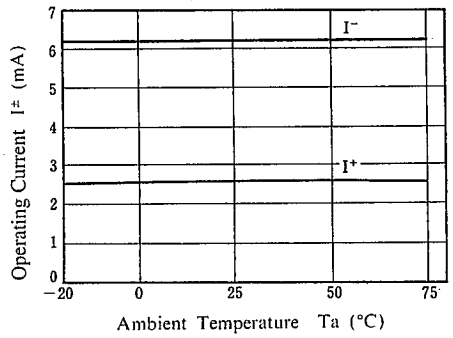
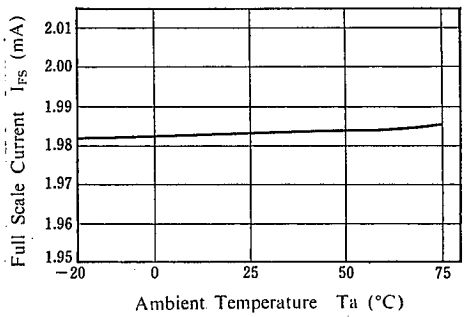
■ TYPICAL CHARACTERISTICS

Operating Current vs. Ambient Temperature

(I_{REF}=2mA)

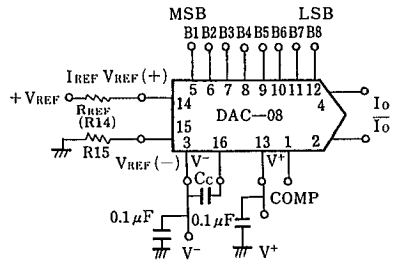


Full Scale Current vs. Ambient Temperature

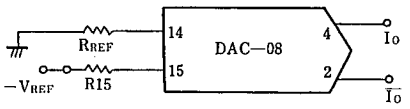


■ TYPICAL APPLICATION

① Connecting Reference Voltage

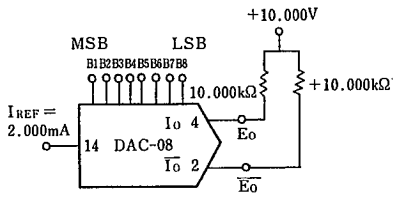


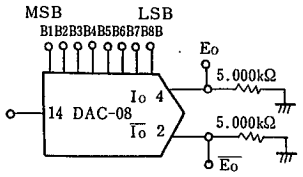
① Positive Reference Voltage
Minimum Compensation Capacitance
$C_C = R_{REF}(k\Omega) \times 15(pF)$



② Negative Reference Voltage
Recommended C_C Value
(When V_{REF} is DC)

② Connecting Output Circuit





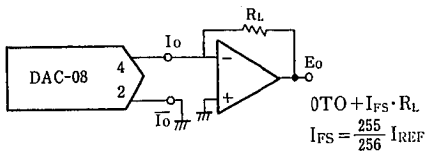
	B1	B2	B3	B4	B5	B6	B7	B8	Eo	$\overline{Eo}$
POS FULL RANGE	1	1	1	1	1	1	1	1	− 9.920	÷10.000
POS FULL RANGE−LSB	1	1	1	1	1	1	1	0	− 9.840	÷ 9.920
ZERO SCALE÷LSB	1	0	0	0	0	0	0	1	− 0.050	÷ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	÷ 0.050
ZERO SCALE−LSB	0	1	1	1	1	1	1	1	÷ 0.080	0.000
NEG FULL SCALE÷LSB	0	0	0	0	0	0	0	1	÷ 9.920	− 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	÷10.000	− 9.920

(1) Basic Bipolar Output Operation

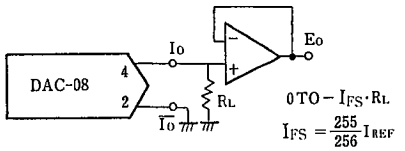
	B1	B2	B3	B4	B5	B6	B7	B8	I_{mA}	$\overline{I_{mA}}$	Eo	$\overline{Eo}$
FULL RANGE	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	−0.000
HALF SCALE÷LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
HALF SCALE−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
ZERO SCALE÷LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	−0.000	−9.950

(2) Basic Unipolar Negative Operation

③ Connecting Output Buffer Amp.

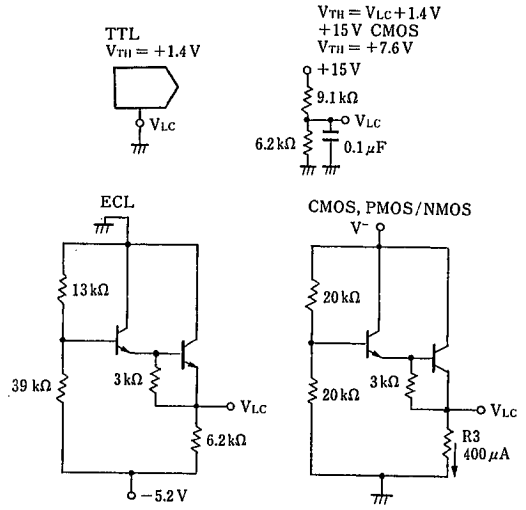


(1) Positive Low Impedance Output Operation



(2) Negative Low Impedance Output Operation

④ Connecting to various type logic IC products



V_{TH} temperature compensation is considered in the above circuit

MEMO