

# KS0741

128 SEG / 129 COM DRIVER & CONTROLLER FOR 4 GRAY SCALE STN LCD

February 8, 2000.

Ver. 1.2

Prepared by: Hyung-Suk, Kim

[highndry@samsung.co.kr](mailto:highndry@samsung.co.kr)

Contents in this document are subject to change without notice. No part of this document may be reproduced or transmitted in any form or by any means, electronic or mechanical, for any purpose, without the express written permission of LCD Driver IC Team.



| KS0741 Specification Revision History |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |               |
|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| Version                               | Content                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Date          |
| 0.0                                   | Preliminary specification (short form)                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | June 8, 1999  |
| 0.1                                   | Preliminary specification (full set)                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | July 14, 1999 |
| 0.2                                   | Added temporary pin number (page 5,6)                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | July 15, 1999 |
| 0.3                                   | Removed HPMB, CS2 pins<br>CS1B pin → CSB pin<br>VOL Max.: 0.3V <sub>DD</sub> → 0.2V <sub>DD</sub> , VOH Min.: 0.7V <sub>DD</sub> → 0.8V <sub>DD</sub> (page 59)                                                                                                                                                                                                                                                                                                                                         | July 30, 1999 |
| 0.4                                   | Removed CLS, OSCCK, OSC2 pins (page 7,8)<br>Read internal status: MF, DS ID is added, ADC is removed (Page 35, 39)<br>RESET flag: 0: display ON, 1: display OFF<br>→ 0: display OFF, 1: display ON (Page 39)                                                                                                                                                                                                                                                                                            | Aug. 12, 1999 |
| 0.5                                   | Changed input pin order, add RESETB pin (page 5)<br>Added VR, VEXT pin connection (page 8)<br>VR: When using internal resistors (INTRS = "H"), open this pin<br>VEXT: When using internal voltage regulator, connect to VDD, VSS or open this pin<br>Added test pin connection (page 9)<br>TEST1,TEST2: connect to "VDD"<br>TEST3,TEST4,TEST5: connect to "VSS"<br>Changed OSC resistance connection (page8, 23)<br>Between OSC1 and OSC2 → between OSC1 and VDD                                        | Aug. 30, 1999 |
| 0.6                                   | Removed TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 pins<br>Added COMS, COMS1 for ICON display.<br>Added ICON control register ON/OFF instruction.                                                                                                                                                                                                                                                                                                                                                         | Sep. 30, 1999 |
| 0.7                                   | Remove COMS, COMS1 for ICON display.<br>Remove ICON control register ON/OFF instruction.                                                                                                                                                                                                                                                                                                                                                                                                                | Oct. 4, 1999  |
| 1.0                                   | Added COMS, COMS1 for ICON display.<br>Added ICON control register ON/OFF instruction.<br>Modified bit settings for partial display command.<br>Relaxed VIH and VIL specifications.<br>Modified interface timing specs.                                                                                                                                                                                                                                                                                 | Jan. 18, 2000 |
| 1.1                                   | Added 6800-mode interface description for data latch with (page 14)<br>C2 CAP value : 0.1 to 0.47uF → 0.47 to 2.0uF (page 34)<br>Added Icon Mode Disabled to the Reset default list. (page 36)<br>Added description of the column address operation. (page 40)<br>Added that Display On/Off command has priority over Entire Display On/Off and Reverse Display On/Off. (page 44)<br>Added N-line inversion command description (page 47)<br>The lower limit of VOUT, V0 - V4 : +0.3V → -0.3V (page 60) | Jan. 24, 2000 |
| 1.2                                   | The upper limit of V1 - V4 : V0 → V0 + 0.3V (page 60)                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Feb. 8, 2000  |

# CONTENTS

|                                                |           |
|------------------------------------------------|-----------|
| <b>INTRODUCTION .....</b>                      | <b>1</b>  |
| <b>FEATURES .....</b>                          | <b>1</b>  |
| <b>BLOCK DIAGRAM .....</b>                     | <b>3</b>  |
| <b>PAD CONFIGURATION .....</b>                 | <b>4</b>  |
| <b>PAD Center Coordinates .....</b>            | <b>6</b>  |
| <b>PIN DESCRIPTION .....</b>                   | <b>6</b>  |
| POWER SUPPLY .....                             | 9         |
| LCD DRIVER SUPPLY .....                        | 9         |
| SYSTEM CONTROL .....                           | 10        |
| MICROPROCESSOR INTERFACE .....                 | 11        |
| LCD DRIVER OUTPUTS .....                       | 13        |
| <b>FUNCTIONAL DESCRIPTION.....</b>             | <b>14</b> |
| MICROPROCESSOR INTERFACE .....                 | 14        |
| DISPLAY DATA RAM (DDRAM) .....                 | 18        |
| LCD DISPLAY CIRCUITS.....                      | 21        |
| LCD DRIVER CIRCUIT .....                       | 26        |
| POWER SUPPLY CIRCUITS .....                    | 29        |
| REFERECE CIRCUIT EXAMPLES.....                 | 34        |
| RESET CIRCUIT .....                            | 36        |
| <b>INSTRUCTION DESCRIPTION.....</b>            | <b>37</b> |
| <b>SPECIFICATIONS.....</b>                     | <b>60</b> |
| ABSOLUTE MAXIMUM RATINGS .....                 | 60        |
| DC CHARACTERISTICS.....                        | 61        |
| AC CHARACTERISTICS .....                       | 64        |
| <b>REFERENCE APPLICATIONS.....</b>             | <b>68</b> |
| MICROPROCESSOR INTERFACE .....                 | 68        |
| CONNECTIONS BETWEEN KS0741 AND LCD PANEL ..... | 70        |



## INTRODUCTION

The KS0741 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. It contains 128 segment and 129 common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface(SPI) or 8-bit parallel display data and stores in an on-chip display data RAM of 128 x 129 x 2 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

## FEATURES

### 4-level (White, Light Gray, Dark Gray, Black) Gray Scale Display with PWM and FRC Methods

| DDRAM data [2n: 2n+1] | 00    | 01         | 10        | 11   |
|-----------------------|-------|------------|-----------|------|
| Gray scale            | White | Light gray | Dark gray | Dark |

(Accessible column address, n = 0, 1, 2, ....., 125, 126, 127)

### Driver Output Circuits

- 128 segment outputs / 129 common outputs

### Applicable Duty Ratios

| Duty ratio                                                  | Applicable LCD bias | Maximum display area |
|-------------------------------------------------------------|---------------------|----------------------|
| 1/16 ~ 1/128 (ICON disabled)<br>1/17 ~ 1/129 (ICON enabled) | 1/5 to 1/12         | 129 × 128            |

- Various partial display
- Partial window moving & data scrolling

### On-chip Display Data RAM

- Capacity:  $129 \times 128 \times 2 = 33,024$ bits
- Bit data "1": a dot of display is illuminated.
- Bit data "0": a dot of display is not illuminated.

### Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- SPI (serial peripheral interface) available (only write operation)

### On-chip Low Power Analog Circuit

- On-chip oscillator circuit
- Voltage converter (x3, x4, x5 or x6)
- Voltage regulator (temperature coefficient: -0.05%/°C, or external input)
- On-chip electronic contrast control function (64 steps)
- Voltage follower (LCD bias : 1/5 to 1/12)

### Operating Voltage Range

- Supply voltage (V<sub>DD</sub>): 1.8 to 3.3V
- LCD driving voltage (V<sub>LCD</sub> = V<sub>O</sub> - V<sub>SS</sub>): 4.0 to 15.0 V

**Low Power Consumption**

- TBD  $\mu$ A Max. (operation)
- TBD  $\mu$ A Max. (sleep mode)

**Package Type**

- Slim chip for TCP

## BLOCK DIAGRAM

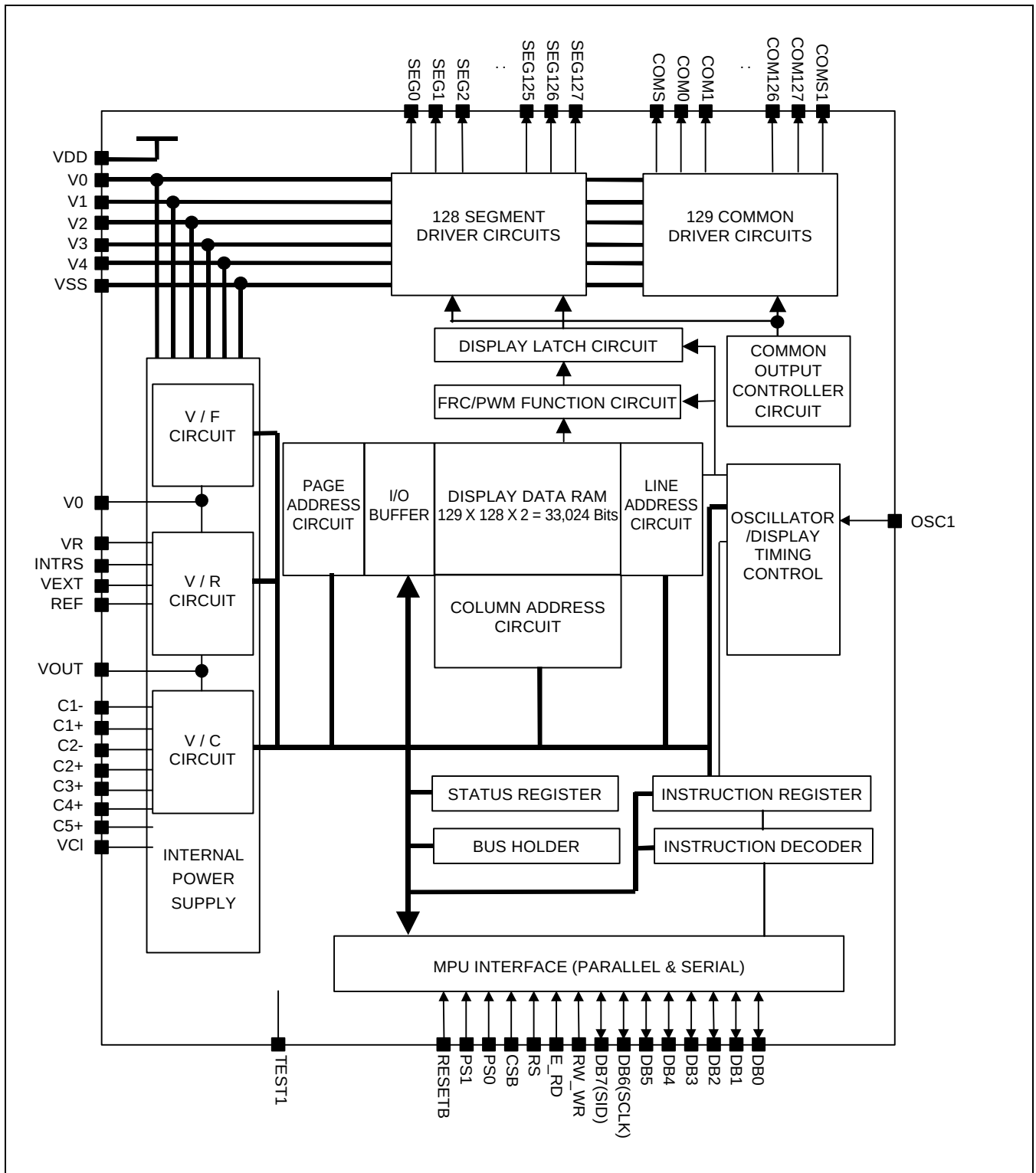


Figure 1. Block Diagram

PAD CONFIGURATION

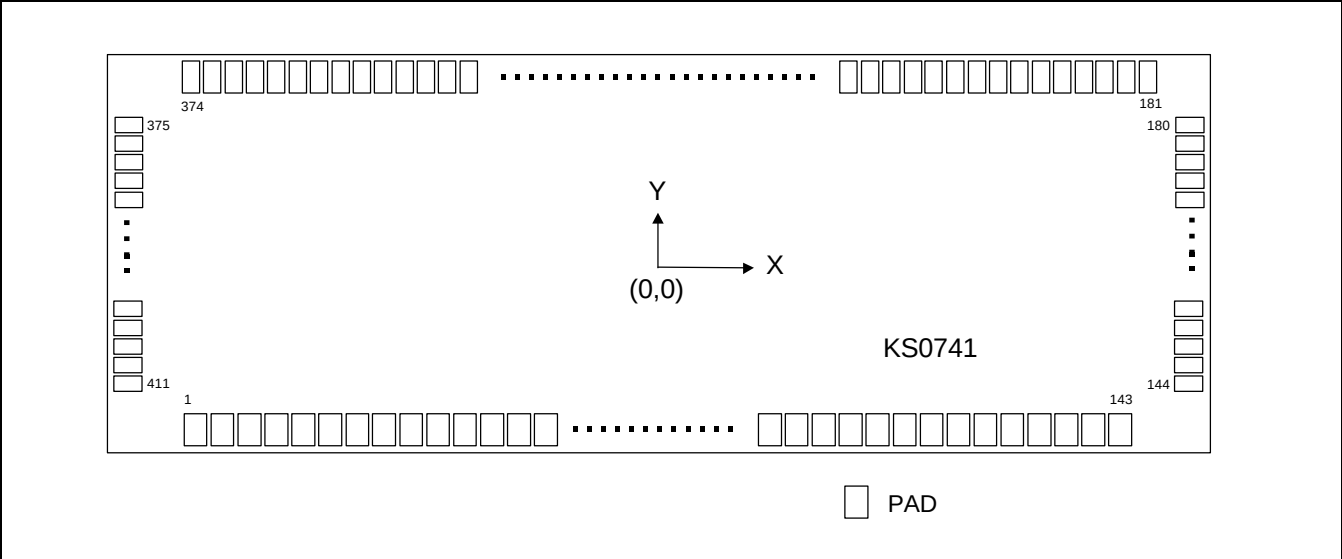


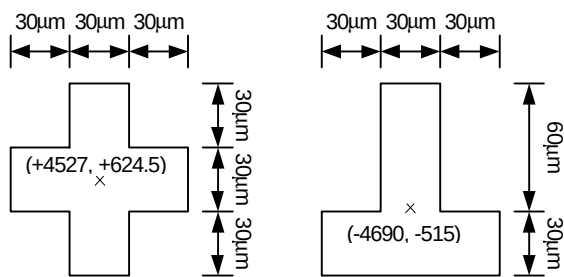
Figure 2. KS0741 Chip Configuration

Table 1. KS0741 Pad Dimensions

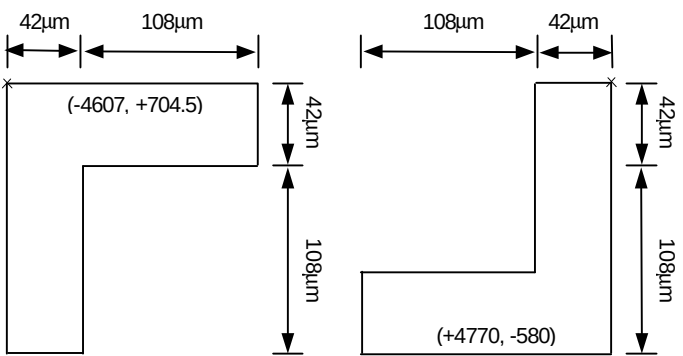
|                                      | PAD NO.                             | SIZE                   |          | UNIT |    |
|--------------------------------------|-------------------------------------|------------------------|----------|------|----|
|                                      |                                     | X                      | Y        |      |    |
| Chip Size                            | -                                   | 10580                  | 2520     | S-   |    |
| Pad Pitch                            | 1 ~ 143                             | 70                     |          |      |    |
|                                      | 144 ~ 178<br>183 ~ 372<br>377 ~ 411 | 52                     |          |      |    |
|                                      | 179 ~ 182<br>373 ~ 376              | 80                     |          |      |    |
|                                      | Bumped pad size                     | 1 ~ 143                | 42       |      | 92 |
|                                      |                                     | 145 ~ 178<br>377 ~ 410 | 70       |      | 34 |
| 183 ~ 372                            |                                     | 34                     | 70       |      |    |
| 144<br>179 ~ 180<br>375 ~ 376<br>411 |                                     | 70                     | 62       |      |    |
| 181 ~ 182<br>373 ~ 374               |                                     | 62                     | 70       |      |    |
| Bumped pad height                    |                                     | ALL PAD                | 14 (TYP) |      |    |



COG Align Key Coordinate



ILB Align Key Coordinate



## PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit:  $\mu\text{m}$ ]

| NO. | Name  | X     | Y     | NO. | Name   | X     | Y     | NO. | Name  | X    | Y     | NO. | Name  | X    | Y    |
|-----|-------|-------|-------|-----|--------|-------|-------|-----|-------|------|-------|-----|-------|------|------|
| 1   | DUMMY | -4970 | -1145 | 51  | DUMMY  | -1470 | -1145 | 101 | C3+   | 2030 | -1145 | 151 | COM57 | 5166 | -586 |
| 2   | DUMMY | -4900 | -1145 | 52  | DUMMY  | -1400 | -1145 | 102 | C3+   | 2100 | -1145 | 152 | COM56 | 5166 | -534 |
| 3   | DUMMY | -4830 | -1145 | 53  | DUMMY  | -1330 | -1145 | 103 | C1-   | 2170 | -1145 | 153 | COM55 | 5166 | -482 |
| 4   | DUMMY | -4760 | -1145 | 54  | DUMMY  | -1260 | -1145 | 104 | C1-   | 2240 | -1145 | 154 | COM54 | 5166 | -430 |
| 5   | DUMMY | -4690 | -1145 | 55  | DUMMY  | -1190 | -1145 | 105 | C1+   | 2310 | -1145 | 155 | COM53 | 5166 | -378 |
| 6   | DUMMY | -4620 | -1145 | 56  | DUMMY  | -1120 | -1145 | 106 | C1+   | 2380 | -1145 | 156 | COM52 | 5166 | -326 |
| 7   | DUMMY | -4550 | -1145 | 57  | DUMMY  | -1050 | -1145 | 107 | C2+   | 2450 | -1145 | 157 | COM51 | 5166 | -274 |
| 8   | DUMMY | -4480 | -1145 | 58  | DUMMY  | -980  | -1145 | 108 | C2+   | 2520 | -1145 | 158 | COM50 | 5166 | -222 |
| 9   | DUMMY | -4410 | -1145 | 59  | VDD    | -910  | -1145 | 109 | C2-   | 2590 | -1145 | 159 | COM49 | 5166 | -170 |
| 10  | DUMMY | -4340 | -1145 | 60  | TEST1  | -840  | -1145 | 110 | C2-   | 2660 | -1145 | 160 | COM48 | 5166 | -118 |
| 11  | DUMMY | -4270 | -1145 | 61  | VSS    | -770  | -1145 | 111 | C4+   | 2730 | -1145 | 161 | COM47 | 5166 | -66  |
| 12  | DUMMY | -4200 | -1145 | 62  | PS0    | -700  | -1145 | 112 | C4+   | 2800 | -1145 | 162 | COM46 | 5166 | -14  |
| 13  | DUMMY | -4130 | -1145 | 63  | VDD    | -630  | -1145 | 113 | VDD   | 2870 | -1145 | 163 | COM45 | 5166 | 38   |
| 14  | DUMMY | -4060 | -1145 | 64  | PS1    | -560  | -1145 | 114 | VDD   | 2940 | -1145 | 164 | COM44 | 5166 | 90   |
| 15  | DUMMY | -3990 | -1145 | 65  | VSS    | -490  | -1145 | 115 | REF   | 3010 | -1145 | 165 | COM43 | 5166 | 142  |
| 16  | DUMMY | -3920 | -1145 | 66  | CSB    | -420  | -1145 | 116 | VSS   | 3080 | -1145 | 166 | COM42 | 5166 | 194  |
| 17  | DUMMY | -3850 | -1145 | 67  | RESETB | -350  | -1145 | 117 | VEXT  | 3150 | -1145 | 167 | COM41 | 5166 | 246  |
| 18  | DUMMY | -3780 | -1145 | 68  | VDD    | -280  | -1145 | 118 | VDD   | 3220 | -1145 | 168 | COM40 | 5166 | 298  |
| 19  | DUMMY | -3710 | -1145 | 69  | RS     | -210  | -1145 | 119 | INTRS | 3290 | -1145 | 169 | COM39 | 5166 | 350  |
| 20  | DUMMY | -3640 | -1145 | 70  | RW WR  | -140  | -1145 | 120 | VSS   | 3360 | -1145 | 170 | COM38 | 5166 | 402  |
| 21  | DUMMY | -3570 | -1145 | 71  | VSS    | -70   | -1145 | 121 | VSS   | 3430 | -1145 | 171 | COM37 | 5166 | 454  |
| 22  | DUMMY | -3500 | -1145 | 72  | E RD   | 0     | -1145 | 122 | V4    | 3500 | -1145 | 172 | COM36 | 5166 | 506  |
| 23  | DUMMY | -3430 | -1145 | 73  | VDD    | 70    | -1145 | 123 | V4    | 3570 | -1145 | 173 | COM35 | 5166 | 558  |
| 24  | DUMMY | -3360 | -1145 | 74  | DB0    | 140   | -1145 | 124 | V3    | 3640 | -1145 | 174 | COM34 | 5166 | 610  |
| 25  | DUMMY | -3290 | -1145 | 75  | DB1    | 210   | -1145 | 125 | V3    | 3710 | -1145 | 175 | COM33 | 5166 | 662  |
| 26  | DUMMY | -3220 | -1145 | 76  | DB2    | 280   | -1145 | 126 | V2    | 3780 | -1145 | 176 | COM32 | 5166 | 714  |
| 27  | DUMMY | -3150 | -1145 | 77  | DB3    | 350   | -1145 | 127 | V2    | 3850 | -1145 | 177 | COM31 | 5166 | 766  |
| 28  | DUMMY | -3080 | -1145 | 78  | DB4    | 420   | -1145 | 128 | V1    | 3920 | -1145 | 178 | COM30 | 5166 | 818  |
| 29  | DUMMY | -3010 | -1145 | 79  | DB5    | 490   | -1145 | 129 | V1    | 3990 | -1145 | 179 | DUMMY | 5166 | 884  |
| 30  | DUMMY | -2940 | -1145 | 80  | DB6    | 560   | -1145 | 130 | V0    | 4060 | -1145 | 180 | DUMMY | 5166 | 964  |
| 31  | DUMMY | -2870 | -1145 | 81  | DB7    | 630   | -1145 | 131 | V0    | 4130 | -1145 | 181 | DUMMY | 5060 | 1136 |
| 32  | DUMMY | -2800 | -1145 | 82  | VDD    | 700   | -1145 | 132 | VR    | 4200 | -1145 | 182 | DUMMY | 4980 | 1136 |
| 33  | DUMMY | -2730 | -1145 | 83  | VDD    | 770   | -1145 | 133 | VR    | 4270 | -1145 | 183 | COM29 | 4914 | 1136 |
| 34  | DUMMY | -2660 | -1145 | 84  | VDD    | 840   | -1145 | 134 | VSS   | 4340 | -1145 | 184 | COM28 | 4862 | 1136 |
| 35  | DUMMY | -2590 | -1145 | 85  | VDD    | 910   | -1145 | 135 | VSS   | 4410 | -1145 | 185 | COM27 | 4810 | 1136 |
| 36  | DUMMY | -2520 | -1145 | 86  | VDD    | 980   | -1145 | 136 | VDD   | 4480 | -1145 | 186 | COM26 | 4758 | 1136 |
| 37  | DUMMY | -2450 | -1145 | 87  | VDD    | 1050  | -1145 | 137 | OSC1  | 4550 | -1145 | 187 | COM25 | 4706 | 1136 |
| 38  | DUMMY | -2380 | -1145 | 88  | VCI    | 1120  | -1145 | 138 | DUMMY | 4620 | -1145 | 188 | COM24 | 4654 | 1136 |
| 39  | DUMMY | -2310 | -1145 | 89  | VCI    | 1190  | -1145 | 139 | DUMMY | 4690 | -1145 | 189 | COM23 | 4602 | 1136 |
| 40  | DUMMY | -2240 | -1145 | 90  | VSS    | 1260  | -1145 | 140 | DUMMY | 4760 | -1145 | 190 | COM22 | 4550 | 1136 |
| 41  | DUMMY | -2170 | -1145 | 91  | VSS    | 1330  | -1145 | 141 | DUMMY | 4830 | -1145 | 191 | COM21 | 4498 | 1136 |
| 42  | DUMMY | -2100 | -1145 | 92  | VSS    | 1400  | -1145 | 142 | DUMMY | 4900 | -1145 | 192 | COM20 | 4446 | 1136 |
| 43  | DUMMY | -2030 | -1145 | 93  | VSS    | 1470  | -1145 | 143 | DUMMY | 4970 | -1145 | 193 | COM19 | 4394 | 1136 |
| 44  | DUMMY | -1960 | -1145 | 94  | VSS    | 1540  | -1145 | 144 | DUMMY | 5166 | -964  | 194 | COM18 | 4342 | 1136 |
| 45  | DUMMY | -1890 | -1145 | 95  | VSS    | 1610  | -1145 | 145 | COM63 | 5166 | -898  | 195 | COM17 | 4290 | 1136 |
| 46  | DUMMY | -1820 | -1145 | 96  | VSS    | 1680  | -1145 | 146 | COM62 | 5166 | -846  | 196 | COM16 | 4238 | 1136 |
| 47  | DUMMY | -1750 | -1145 | 97  | VOUT   | 1750  | -1145 | 147 | COM61 | 5166 | -794  | 197 | COM15 | 4186 | 1136 |
| 48  | DUMMY | -1680 | -1145 | 98  | VOUT   | 1820  | -1145 | 148 | COM60 | 5166 | -742  | 198 | COM14 | 4134 | 1136 |
| 49  | DUMMY | -1610 | -1145 | 99  | C5+    | 1890  | -1145 | 149 | COM59 | 5166 | -690  | 199 | COM13 | 4082 | 1136 |
| 50  | DUMMY | -1540 | -1145 | 100 | C5+    | 1960  | -1145 | 150 | COM58 | 5166 | -638  | 200 | COM12 | 4030 | 1136 |

Table 2. PAD Center Coordinates (Continued)

[unit: mm]

| NO. | Name  | X    | Y    | NO. | Name  | X     | Y    | NO. | Name   | X     | Y    | NO. | Name   | X     | Y    |
|-----|-------|------|------|-----|-------|-------|------|-----|--------|-------|------|-----|--------|-------|------|
| 201 | COM11 | 3978 | 1136 | 251 | SEG37 | 1378  | 1136 | 301 | SEG87  | -1222 | 1136 | 351 | COM73  | -3822 | 1136 |
| 202 | COM10 | 3926 | 1136 | 252 | SEG38 | 1326  | 1136 | 302 | SEG88  | -1274 | 1136 | 352 | COM74  | -3874 | 1136 |
| 203 | COM9  | 3874 | 1136 | 253 | SEG39 | 1274  | 1136 | 303 | SEG89  | -1326 | 1136 | 353 | COM75  | -3926 | 1136 |
| 204 | COM8  | 3822 | 1136 | 254 | SEG40 | 1222  | 1136 | 304 | SEG90  | -1378 | 1136 | 354 | COM76  | -3978 | 1136 |
| 205 | COM7  | 3770 | 1136 | 255 | SEG41 | 1170  | 1136 | 305 | SEG91  | -1430 | 1136 | 355 | COM77  | -4030 | 1136 |
| 206 | COM6  | 3718 | 1136 | 256 | SEG42 | 1118  | 1136 | 306 | SEG92  | -1482 | 1136 | 356 | COM78  | -4082 | 1136 |
| 207 | COM5  | 3666 | 1136 | 257 | SEG43 | 1066  | 1136 | 307 | SEG93  | -1534 | 1136 | 357 | COM79  | -4134 | 1136 |
| 208 | COM4  | 3614 | 1136 | 258 | SEG44 | 1014  | 1136 | 308 | SEG94  | -1586 | 1136 | 358 | COM80  | -4186 | 1136 |
| 209 | COM3  | 3562 | 1136 | 259 | SEG45 | 962   | 1136 | 309 | SEG95  | -1638 | 1136 | 359 | COM81  | -4238 | 1136 |
| 210 | COM2  | 3510 | 1136 | 260 | SEG46 | 910   | 1136 | 310 | SEG96  | -1690 | 1136 | 360 | COM82  | -4290 | 1136 |
| 211 | COM1  | 3458 | 1136 | 261 | SEG47 | 858   | 1136 | 311 | SEG97  | -1742 | 1136 | 361 | COM83  | -4342 | 1136 |
| 212 | COM0  | 3406 | 1136 | 262 | SEG48 | 806   | 1136 | 312 | SEG98  | -1794 | 1136 | 362 | COM84  | -4394 | 1136 |
| 213 | COMS  | 3354 | 1136 | 263 | SEG49 | 754   | 1136 | 313 | SEG99  | -1846 | 1136 | 363 | COM85  | -4446 | 1136 |
| 214 | SEG0  | 3302 | 1136 | 264 | SEG50 | 702   | 1136 | 314 | SEG100 | -1898 | 1136 | 364 | COM86  | -4498 | 1136 |
| 215 | SEG1  | 3250 | 1136 | 265 | SEG51 | 650   | 1136 | 315 | SEG101 | -1950 | 1136 | 365 | COM87  | -4550 | 1136 |
| 216 | SEG2  | 3198 | 1136 | 266 | SEG52 | 598   | 1136 | 316 | SEG102 | -2002 | 1136 | 366 | COM88  | -4602 | 1136 |
| 217 | SEG3  | 3146 | 1136 | 267 | SEG53 | 546   | 1136 | 317 | SEG103 | -2054 | 1136 | 367 | COM89  | -4654 | 1136 |
| 218 | SEG4  | 3094 | 1136 | 268 | SEG54 | 494   | 1136 | 318 | SEG104 | -2106 | 1136 | 368 | COM90  | -4706 | 1136 |
| 219 | SEG5  | 3042 | 1136 | 269 | SEG55 | 442   | 1136 | 319 | SEG105 | -2158 | 1136 | 369 | COM91  | -4758 | 1136 |
| 220 | SEG6  | 2990 | 1136 | 270 | SEG56 | 390   | 1136 | 320 | SEG106 | -2210 | 1136 | 370 | COM92  | -4810 | 1136 |
| 221 | SEG7  | 2938 | 1136 | 271 | SEG57 | 338   | 1136 | 321 | SEG107 | -2262 | 1136 | 371 | COM93  | -4862 | 1136 |
| 222 | SEG8  | 2886 | 1136 | 272 | SEG58 | 286   | 1136 | 322 | SEG108 | -2314 | 1136 | 372 | COM94  | -4914 | 1136 |
| 223 | SEG9  | 2834 | 1136 | 273 | SEG59 | 234   | 1136 | 323 | SEG109 | -2366 | 1136 | 373 | DUMMY  | -4980 | 1136 |
| 224 | SEG10 | 2782 | 1136 | 274 | SEG60 | 182   | 1136 | 324 | SEG110 | -2418 | 1136 | 374 | DUMMY  | -5060 | 1136 |
| 225 | SEG11 | 2730 | 1136 | 275 | SEG61 | 130   | 1136 | 325 | SEG111 | -2470 | 1136 | 375 | DUMMY  | -5166 | 964  |
| 226 | SEG12 | 2678 | 1136 | 276 | SEG62 | 78    | 1136 | 326 | SEG112 | -2522 | 1136 | 376 | DUMMY  | -5166 | 884  |
| 227 | SEG13 | 2626 | 1136 | 277 | SEG63 | 26    | 1136 | 327 | SEG113 | -2574 | 1136 | 377 | COM95  | -5166 | 818  |
| 228 | SEG14 | 2574 | 1136 | 278 | SEG64 | -26   | 1136 | 328 | SEG114 | -2626 | 1136 | 378 | COM96  | -5166 | 766  |
| 229 | SEG15 | 2522 | 1136 | 279 | SEG65 | -78   | 1136 | 329 | SEG115 | -2678 | 1136 | 379 | COM97  | -5166 | 714  |
| 230 | SEG16 | 2470 | 1136 | 280 | SEG66 | -130  | 1136 | 330 | SEG116 | -2730 | 1136 | 380 | COM98  | -5166 | 662  |
| 231 | SEG17 | 2418 | 1136 | 281 | SEG67 | -182  | 1136 | 331 | SEG117 | -2782 | 1136 | 381 | COM99  | -5166 | 610  |
| 232 | SEG18 | 2366 | 1136 | 282 | SEG68 | -234  | 1136 | 332 | SEG118 | -2834 | 1136 | 382 | COM100 | -5166 | 558  |
| 233 | SEG19 | 2314 | 1136 | 283 | SEG69 | -286  | 1136 | 333 | SEG119 | -2886 | 1136 | 383 | COM101 | -5166 | 506  |
| 234 | SEG20 | 2262 | 1136 | 284 | SEG70 | -338  | 1136 | 334 | SEG120 | -2938 | 1136 | 384 | COM102 | -5166 | 454  |
| 235 | SEG21 | 2210 | 1136 | 285 | SEG71 | -390  | 1136 | 335 | SEG121 | -2990 | 1136 | 385 | COM103 | -5166 | 402  |
| 236 | SEG22 | 2158 | 1136 | 286 | SEG72 | -442  | 1136 | 336 | SEG122 | -3042 | 1136 | 386 | COM104 | -5166 | 350  |
| 237 | SEG23 | 2106 | 1136 | 287 | SEG73 | -494  | 1136 | 337 | SEG123 | -3094 | 1136 | 387 | COM105 | -5166 | 298  |
| 238 | SEG24 | 2054 | 1136 | 288 | SEG74 | -546  | 1136 | 338 | SEG124 | -3146 | 1136 | 388 | COM106 | -5166 | 246  |
| 239 | SEG25 | 2002 | 1136 | 289 | SEG75 | -598  | 1136 | 339 | SEG125 | -3198 | 1136 | 389 | COM107 | -5166 | 194  |
| 240 | SEG26 | 1950 | 1136 | 290 | SEG76 | -650  | 1136 | 340 | SEG126 | -3250 | 1136 | 390 | COM108 | -5166 | 142  |
| 241 | SEG27 | 1898 | 1136 | 291 | SEG77 | -702  | 1136 | 341 | SEG127 | -3302 | 1136 | 391 | COM109 | -5166 | 90   |
| 242 | SEG28 | 1846 | 1136 | 292 | SEG78 | -754  | 1136 | 342 | COM64  | -3354 | 1136 | 392 | COM110 | -5166 | 38   |
| 243 | SEG29 | 1794 | 1136 | 293 | SEG79 | -806  | 1136 | 343 | COM65  | -3406 | 1136 | 393 | COM111 | -5166 | -14  |
| 244 | SEG30 | 1742 | 1136 | 294 | SEG80 | -858  | 1136 | 344 | COM66  | -3458 | 1136 | 394 | COM112 | -5166 | -66  |
| 245 | SEG31 | 1690 | 1136 | 295 | SEG81 | -910  | 1136 | 345 | COM67  | -3510 | 1136 | 395 | COM113 | -5166 | -118 |
| 246 | SEG32 | 1638 | 1136 | 296 | SEG82 | -962  | 1136 | 346 | COM68  | -3562 | 1136 | 396 | COM114 | -5166 | -170 |
| 247 | SEG33 | 1586 | 1136 | 297 | SEG83 | -1014 | 1136 | 347 | COM69  | -3614 | 1136 | 397 | COM115 | -5166 | -222 |
| 248 | SEG34 | 1534 | 1136 | 298 | SEG84 | -1066 | 1136 | 348 | COM70  | -3666 | 1136 | 398 | COM116 | -5166 | -274 |
| 249 | SEG35 | 1482 | 1136 | 299 | SEG85 | -1118 | 1136 | 349 | COM71  | -3718 | 1136 | 399 | COM117 | -5166 | -326 |
| 250 | SEG36 | 1430 | 1136 | 300 | SEG86 | -1170 | 1136 | 350 | COM72  | -3770 | 1136 | 400 | COM118 | -5166 | -378 |



## PIN DESCRIPTION

### POWER SUPPLY

**Table 3. Power Supply Pin Description**

| Name                       | I/O            | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |            |  |  |          |    |    |    |    |          |                |                |            |            |
|----------------------------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------|--|--|----------|----|----|----|----|----------|----------------|----------------|------------|------------|
| VDD                        | Supply         | Power supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |            |            |  |  |          |    |    |    |    |          |                |                |            |            |
| VSS                        | Supply         | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |            |  |  |          |    |    |    |    |          |                |                |            |            |
| V0<br>V1<br>V2<br>V3<br>V4 | I/O            | <div>LCD driver supply voltages<br/>The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.<br/>Voltages should have the following relationship;<br/><math>V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS</math><br/>When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.</div> <table><tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr><tr><td>1/N bias</td><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr></table> <div>NOTE: N = 5 to 12</div> |            |            |  |  | LCD bias | V1 | V2 | V3 | V4 | 1/N bias | (N-1) / N x V0 | (N-2) / N x V0 | (2/N) x V0 | (1/N) x V0 |
| LCD bias                   | V1             | V2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | V3         | V4         |  |  |          |    |    |    |    |          |                |                |            |            |
| 1/N bias                   | (N-1) / N x V0 | (N-2) / N x V0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | (2/N) x V0 | (1/N) x V0 |  |  |          |    |    |    |    |          |                |                |            |            |

### LCD DRIVER SUPPLY

**Table 4. LCD Driver Supply Pin Description**

| Name | I/O | Description                                                                                                                                                                                              |
|------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C1-  | O   | Capacitor 1 negative connection pin for voltage converter                                                                                                                                                |
| C1+  | O   | Capacitor 1 positive connection pin for voltage converter                                                                                                                                                |
| C2-  | O   | Capacitor 2 negative connection pin for voltage converter                                                                                                                                                |
| C2+  | O   | Capacitor 2 positive connection pin for voltage converter                                                                                                                                                |
| C3+  | O   | Capacitor 3 positive connection pin for voltage converter                                                                                                                                                |
| C4+  | O   | Capacitor 4 positive connection pin for voltage converter                                                                                                                                                |
| C5+  | O   | Capacitor 5 positive connection pin for voltage converter                                                                                                                                                |
| VOUT | I/O | Voltage converter input / output pin                                                                                                                                                                     |
| VCI  | I   | Voltage converter input voltage pin                                                                                                                                                                      |
| VR   | I   | <p>V0 voltage adjustment pin<br/>It is valid only when on-chip resistors are not used (INTRS = "L")<br/>When using internal resistors (INTRS = "H"), open this pin</p>                                   |
| REF  | I   | <p>Selects the external VREF voltage via the VEXT pin<br/>– REF = "H": using the internal VREF<br/>– REF = "L": using the external VREF</p>                                                              |
| VEXT | I   | <p>Externally input reference voltage (VREF) for the internal voltage regulator<br/>It is valid only when REF is "L"<br/>When using internal voltage regulator, connect to VDD, VSS or open this pin</p> |
| OSC1 | I   | When using internal clock oscillator, connect a resistor between OSC1 and VDD.                                                                                                                           |

## SYSTEM CONTROL

Table 5. System Control Pin Description

| Name  | I/O | Description                                                                                                                                                                                                                                          |
|-------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INTRS | I   | Internal resistor select pin<br>This pin selects the resistors for adjusting V0 voltage level<br>– INTRS = "H": use the internal resistors.<br>– INTRS = "L": use the external resistors<br>VR pin and external resistive divider control V0 voltage |
| TEST1 | O   | Test pins<br>Don't use this pin.<br>– TEST1: Open this pin.                                                                                                                                                                                          |

## MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pin Description

| Name   | I/O | Description                                                                                                                                                                                                                                                                     |                |                    |                                                                                                          |               |              |
|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|--------------------|----------------------------------------------------------------------------------------------------------|---------------|--------------|
| RESETB | I   | Reset input pin<br>When RESETB is “L”, initialization is executed.                                                                                                                                                                                                              |                |                    |                                                                                                          |               |              |
| PS0    | I   | Parallel / Serial data input select input                                                                                                                                                                                                                                       |                |                    |                                                                                                          |               |              |
|        |     | PS0                                                                                                                                                                                                                                                                             | Interface mode | Data / instruction | Data                                                                                                     | Read / Write  | Serial clock |
|        |     | H                                                                                                                                                                                                                                                                               | Parallel       | RS                 | DB0 to DB7                                                                                               | E_RD<br>RW_WR | -            |
|        |     | L                                                                                                                                                                                                                                                                               | Serial         | RS or None         | SID (DB7)                                                                                                | Write only    | SCLK (DB6)   |
|        |     | *NOTE: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either “H” or “L”.                                                                                                             |                |                    |                                                                                                          |               |              |
| PS1    | I   | Microprocessor interface select input pin<br>– PS0 = “H” , PS1 = “H”: 6800-series parallel MPU interface<br>– PS0 = “H” , PS1 = “L”: 8080-series parallel MPU interface<br>– PS0 = “L” , PS1 = “H”: 4 pin-SPI MPU interface<br>– PS0 = “L” , PS1 = “L”: 3 pin-SPI MPU interface |                |                    |                                                                                                          |               |              |
| CSB    | I   | Chip select input pins<br>Data/instruction I/O is enabled only when CSB is “L”. When chip select is non-active, DB0 to DB7 may be high impedance.                                                                                                                               |                |                    |                                                                                                          |               |              |
| RS     | I   | Register select input pin<br>– RS = “H”: DB0 to DB7 are display data<br>– RS = “L”: DB0 to DB7 are control data                                                                                                                                                                 |                |                    |                                                                                                          |               |              |
| RW_WR  | I   | Read / Write execution control pin                                                                                                                                                                                                                                              |                |                    |                                                                                                          |               |              |
|        |     | C68                                                                                                                                                                                                                                                                             | MPU type       | RW_WR              | Description                                                                                              |               |              |
|        |     | H                                                                                                                                                                                                                                                                               | 6800-series    | RW                 | Read / Write control input pin<br>– RW = “H” : read<br>– RW = “L” : write                                |               |              |
|        |     | L                                                                                                                                                                                                                                                                               | 8080-series    | /WR                | Write enable clock input pin<br>The data on DB0 to DB7 are latched at the rising edge of the /WR signal. |               |              |
|        |     |                                                                                                                                                                                                                                                                                 |                |                    |                                                                                                          |               |              |

Table 7. Microprocessor Interface Pin Description (Continued)

| Name       | I/O | Description                                                                                                                                                                                                                                                                                                               |             |      |                                                                                                                                                                                         |
|------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E_RD       | I   | Read / Write execution control pin                                                                                                                                                                                                                                                                                        |             |      |                                                                                                                                                                                         |
|            |     | PS1                                                                                                                                                                                                                                                                                                                       | MPU Type    | E_RD | Description                                                                                                                                                                             |
|            |     | H                                                                                                                                                                                                                                                                                                                         | 6800-series | E    | Read / Write control input pin<br>– RW = "H": When E is "H", DB0 to DB7 are in an output status.<br>– RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal. |
|            |     | L                                                                                                                                                                                                                                                                                                                         | 8080-series | /RD  | Read enable clock input pin<br>When /RD is "L", DB0 to DB7 are in an output status.                                                                                                     |
|            |     |                                                                                                                                                                                                                                                                                                                           |             |      |                                                                                                                                                                                         |
| DB0 to DB7 | I/O | 8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS0 = "L");<br>– DB0 to DB5: high impedance<br>– DB6: serial input clock (SCLK)<br>– DB7: serial input data (SID)<br>When chip select is not active, DB0 to DB7 may be high impedance. |             |      |                                                                                                                                                                                         |



## LCD DRIVER OUTPUTS

Table 8. LCD Driver Output Pin Description

| Name                 | I/O | Description                                                                                                            |              |                               |                 |
|----------------------|-----|------------------------------------------------------------------------------------------------------------------------|--------------|-------------------------------|-----------------|
| SEG0<br>to<br>SEG127 | O   | LCD segment driver outputs<br>The display data and the M signal control the output voltage of segment driver.          |              |                               |                 |
|                      |     | Display data                                                                                                           | M (Internal) | Segment driver output voltage |                 |
|                      |     |                                                                                                                        |              | Normal display                | Reverse display |
|                      |     | H                                                                                                                      | H            | V0                            | V2              |
|                      |     | H                                                                                                                      | L            | VSS                           | V3              |
|                      |     | L                                                                                                                      | H            | V2                            | V0              |
|                      |     | L                                                                                                                      | L            | V3                            | VSS             |
|                      |     | Power save mode                                                                                                        |              | VSS                           | VSS             |
|                      |     |                                                                                                                        |              |                               |                 |
| COM0<br>to<br>COM127 | O   | LCD common driver outputs<br>The internal scanning data and M signal control the output voltage of common driver.      |              |                               |                 |
|                      |     | Scan data                                                                                                              | M (Internal) | Common driver output voltage  |                 |
|                      |     | H                                                                                                                      | H            | VSS                           |                 |
|                      |     | H                                                                                                                      | L            | V0                            |                 |
|                      |     | L                                                                                                                      | H            | V1                            |                 |
|                      |     | L                                                                                                                      | L            | V4                            |                 |
|                      |     | Power save mode                                                                                                        |              | VSS                           |                 |
|                      |     |                                                                                                                        |              |                               |                 |
| COMS<br>(COMS1)      | O   | Common output for the icons<br>The output signals of two pins are same. When not used, these pins should be left open. |              |                               |                 |

NOTE: **DUMMY** – These pins should be opened (floated).

## FUNCTIONAL DESCRIPTION

### MICROPROCESSOR INTERFACE

#### Chip Select Input

There is CSB pin for chip selection. The KS0741 can interface with an MPU when CSB is "L". When these pins are set to any other combination, RS, E\_RD, and RW\_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

#### Parallel / Serial Interface

KS0741 has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 9.

**Table 9. Parallel / Serial Interface Mode**

| Type     | PS1 | CSB | PS0 | Interface mode       |
|----------|-----|-----|-----|----------------------|
| Parallel | H   | CSB | H   | 6800-series MPU mode |
|          | L   |     |     | 8080-series MPU mode |
| Serial   | H   | CSB | L   | 4-pin SPI mode       |
|          | L   |     |     | 3-pin SPI mode       |

#### Parallel Interface (PS0 = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in table 10. The type of data transfer is determined by signals at RS, E\_RD and RW\_WR as shown in table 11.

**Table 10. Microprocessor Selection for Parallel Interface**

| PS1 | CSB | RS | E_RD | RW_WR | DB0 to DB7 | MPU bus     |
|-----|-----|----|------|-------|------------|-------------|
| H   | CSB | RS | E    | RW    | DB0 to DB7 | 6800-series |
| L   | CSB | RS | /RD  | /WR   | DB0 to DB7 | 8080-series |

**Table 11. Parallel Data Transfer**

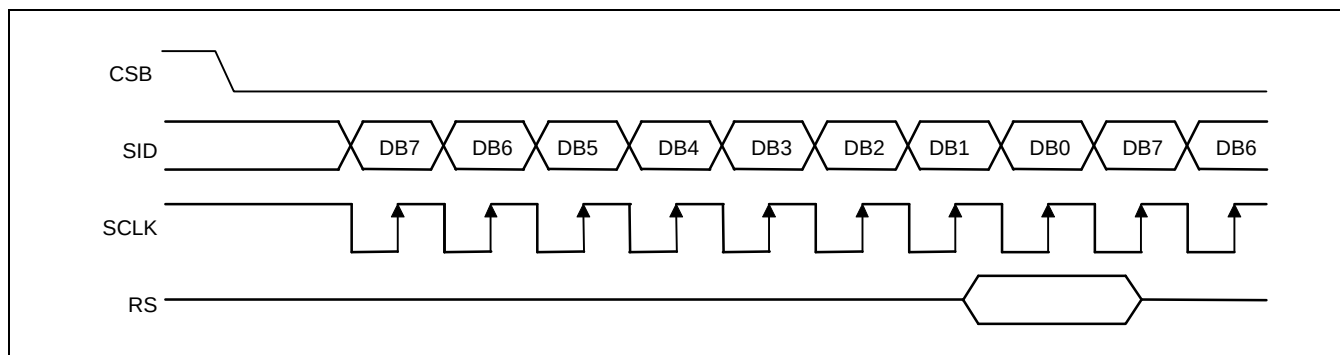
| Common | 6800-series |            | 8080-series |             | Description                               |
|--------|-------------|------------|-------------|-------------|-------------------------------------------|
| RS     | E_RD (E)    | RW_WR (RW) | E_RD (/RD)  | RW_WR (/WR) |                                           |
| H      | H           | H          | L           | H           | Display data read out                     |
| H      | H           | L          | H           | L           | Display data write                        |
| L      | H           | H          | L           | H           | Register status read                      |
| L      | H           | L          | H           | L           | Writes to internal register (instruction) |

NOTE: When E\_RD pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at RS, RW\_WR as in case of 6800-series mode.

**Serial Interface (PS0 = "L")**

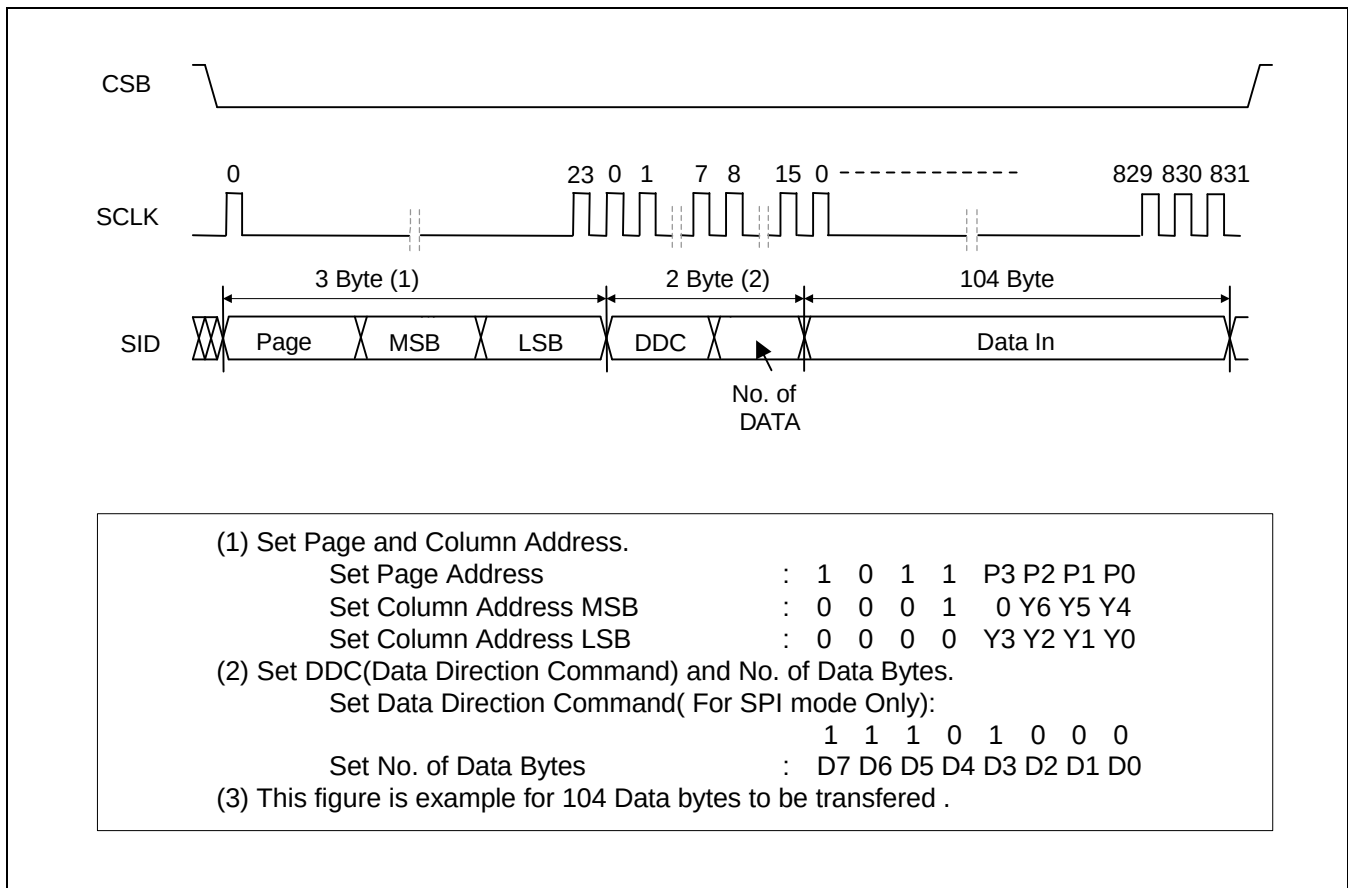
When the KS0741 is active(CSB="L"), serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select(RS) Pin, based on the setting of PS1. When the RS pin is used (PS1 = "H"), data is display data when RS is high, and command data when RS is low. When RS is not used (PS1 = "L"), the LCD Driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data Direction command(11101000) to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are send, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.

| Serial Mode    | PS0 | PS1 | CSB | RS       |
|----------------|-----|-----|-----|----------|
| 4-Pin SPI mode | L   | H   | CSB | Used     |
| 3-Pin SPI mode | L   | L   | CSB | Not used |

**4-pin SPI mode (PS0 = "L" , PS1 = "H")****Figure 3. 4-pin SPI Timing (RS is used)**

### 3-pin SPI mode (PS0 = "L" , PS1 = "L")

To write data to the DDRAM, send Data Direction Command in 3-pin SPI mode. Data is latched at the rising edge of SCLK. And the DDRAM column address pointer will be increased by one automatically.



**Figure 4. 3-pin SPI Timing (RS is not used)**

This command is used in 3-pin SPI mode only. It will be two continuous commands, the first byte controls the data direction and informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is stopped in transmitting, it is not valid data. New data will be transferred serially with most significant bit first.

NOTE: In spite of transmission of data, if CSB will be disable, state terminates abnormally. Next state is initialized.

### Busy Flag

The Busy Flag indicates whether the KS0741 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

## Data Transfer

The KS0741 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 5. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 6. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

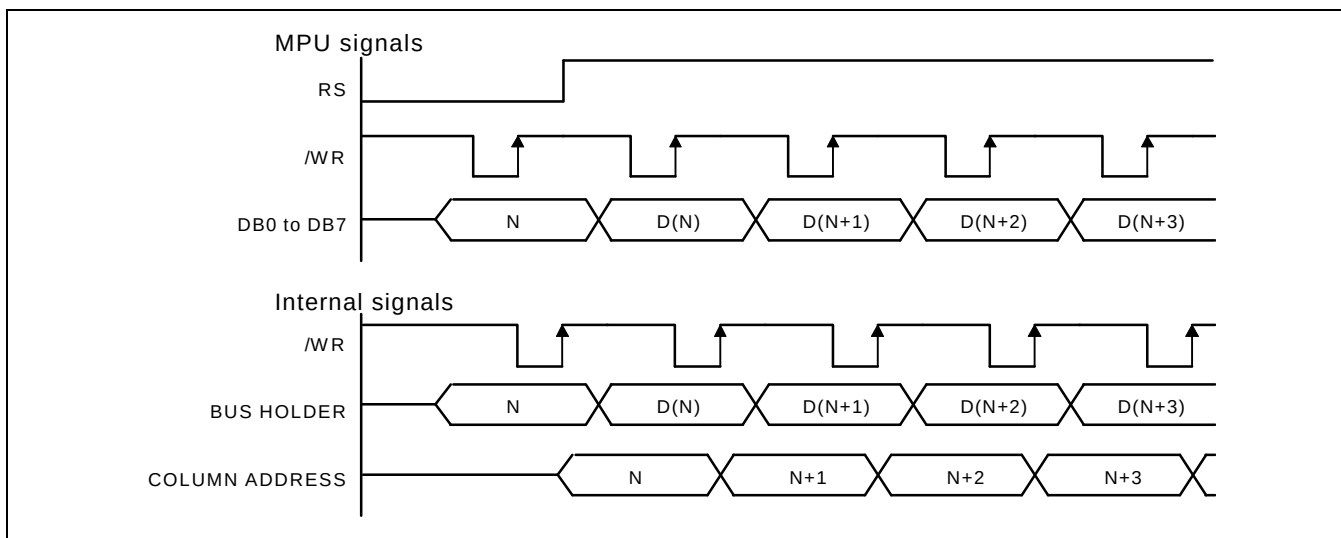


Figure 5. Write Timing

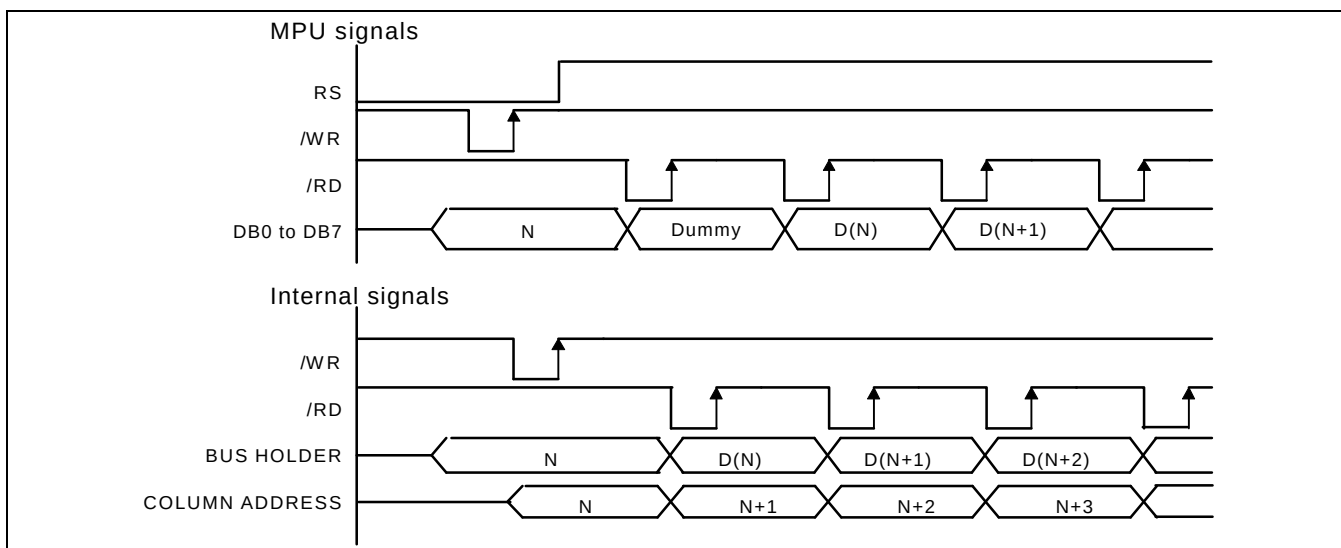


Figure 6. Read Timing

## DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 129-row (17 page by 8 bits) by 128-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 129 rows are divided into 16 pages of 8 lines and the 17th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

### Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 8. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid.

### Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 8. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128-bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

### Column Address Circuit

Column Address Circuit has a 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure 8. When set Column Address MSB / LSB instruction is issued, 7-bit [Y7:Y1] are set and lowest bit, Y0 is set to "0". Since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 7EH. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the column address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following figure 7.

| SEG output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | SEG 0     |           | SEG 1     |           | SEG 2     |           | SEG 3     |           | ... .. | SEG 124   |           | SEG 125   |           | SEG 126   |           | SEG 127   |           |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|--------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Column address [Y7:Y1]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 00H       |           | 01H       |           | 02H       |           | 03H       |           | ... .. | 7CH       |           | 7DH       |           | 7EH       |           | 7FH       |           |
| Internal column address [Y7:Y0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 00<br>HEX | 01<br>HEX | 02<br>HEX | 03<br>HEX | 04<br>HEX | 05<br>HEX | 06<br>HEX | 07<br>HEX | ... .. | F8<br>HEX | F9<br>HEX | FA<br>HEX | FB<br>HEX | FC<br>HEX | FD<br>HEX | FE<br>HEX | FF<br>HEX |
| Display data (ADC = 0)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1         | 1         | 1         | 0         | 0         | 0         | 0         | 1         | ... .. | 1         | 0         | 1         | 1         | 0         | 0         | 0         | 1         |
| LCD panel display                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |           |           |           |           |           |           |           |           | ... .. |           |           |           |           |           |           |           |           |
| <div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div></div> |           |           |           |           |           |           |           |           |        |           |           |           |           |           |           |           |           |
| Display data (ADC = 1)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0         | 1         | 0         | 0         | 1         | 1         | 1         | 0         | ... .. | 0         | 1         | 0         | 0         | 1         | 0         | 1         | 1         |
| LCD panel display                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |           |           |           |           |           |           |           |           | ... .. |           |           |           |           |           |           |           |           |

Figure 7. The Relationship between the Column Address and The Segment Outputs

### Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

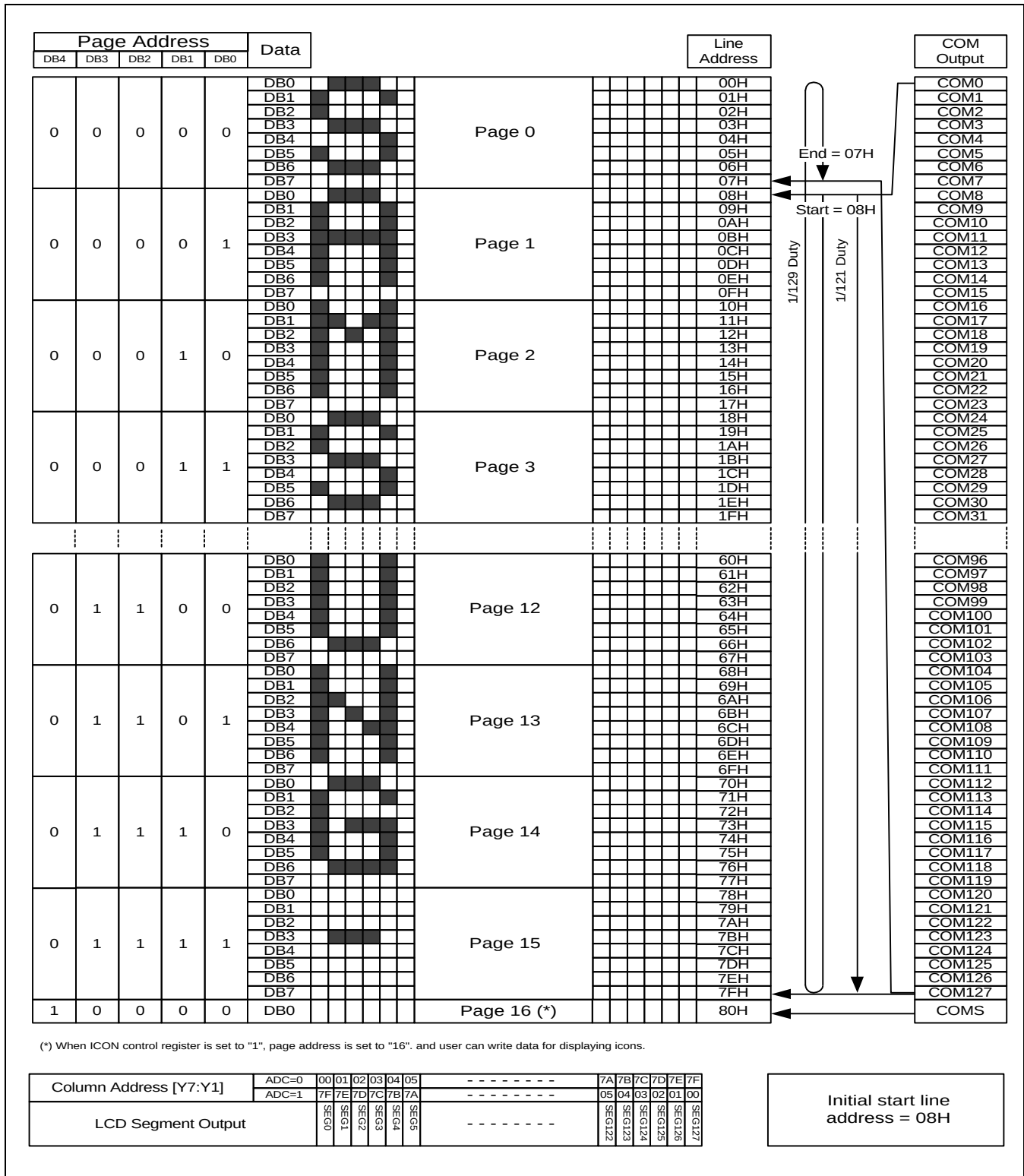


Figure 8. Display Data RAM Map



## LCD DISPLAY CIRCUITS

### FRC (Frame Rate Control) and PWM (Pulse Width Modulation) Function Circuit

The KS0741 incorporates an FRC function and a PWM function circuit to display a 4-level gray scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective value of applied voltage. The KS0741 provides four 4-bit palette-registers to assign the desired gray level. These registers are set by the instructions and the RESETB.

#### – Gray Scale Table of 4 FRC (Frame Rate Control)

| Gray scale level | MSB (DB7 to DB4) | LSB (DB3 to DB0) |
|------------------|------------------|------------------|
| White            | 2nd FR (FR2)     | 1st FR (FR1)     |
|                  | 4th FR (FR4)     | 3rd FR (FR3)     |
| Light gray       | 2nd FR (FR2)     | 1st FR (FR1)     |
|                  | 4th FR (FR4)     | 3rd FR (FR3)     |
| Dark gray        | 2nd FR (FR2)     | 1st FR (FR1)     |
|                  | 4th FR (FR4)     | 3rd FR (FR3)     |
| Black            | 2nd FR (FR2)     | 1st FR (FR1)     |
|                  | 4th FR (FR4)     | 3rd FR (FR3)     |

#### – Gray Scale Table of 3 FRC (Frame Rate Control)

| Gray scale level | MSB (DB7 to DB4) | LSB (DB3 to DB0) |
|------------------|------------------|------------------|
| White            | 2nd FR (FR2)     | 1st FR (FR1)     |
|                  | × × × ×          | 3rd FR (FR3)     |
| Light gray       | 2nd FR (FR2)     | 1st FR (FR1)     |
|                  | × × × ×          | 3rd FR (FR3)     |
| Dark gray        | 2nd FR (FR2)     | 1st FR (FR1)     |
|                  | × × × ×          | 3rd FR (FR3)     |
| Black            | 2nd FR (FR2)     | 1st FR (FR1)     |
|                  | × × × ×          | 3rd FR (FR3)     |

## – Gray Scale Table of 15 PWM (Pulse Width Modulation)

| Dec | Hex | 4-bits | PWM (on width) | Note     |
|-----|-----|--------|----------------|----------|
| 0   | 00  | 0000   | 0 (0/15)       | Brighter |
| 1   | 01  | 0001   | 1/15           | ↑        |
| 2   | 02  | 0010   | 2/15           |          |
| 3   | 03  | 0011   | 3/15           |          |
| 4   | 04  | 0100   | 4/15           |          |
| 5   | 05  | 0101   | 5/15           |          |
| 6   | 06  | 0110   | 6/15           |          |
| 7   | 07  | 0111   | 7/15           |          |
| 8   | 08  | 1000   | 8/15           |          |
| 9   | 09  | 1001   | 9/15           |          |
| 10  | 0A  | 1010   | 10/15          |          |
| 11  | 0B  | 1011   | 11/15          |          |
| 12  | 0C  | 1100   | 12/15          |          |
| 13  | 0D  | 1101   | 13/15          | ↓        |
| 14  | 0E  | 1110   | 14/15          |          |
| 15  | 0F  | 1111   | 1 (15/15)      | Darker   |

## – Gray Scale Table of 12 PWM (Pulse Width Modulation)

| Dec | Hex | 4-bits | PWM (on width) | Note                                            |
|-----|-----|--------|----------------|-------------------------------------------------|
| 0   | 00  | 0000   | 0 (0/12)       | Brighter                                        |
| 1   | 01  | 0001   | 1/12           | ↑                                               |
| 2   | 02  | 0010   | 2/12           |                                                 |
| 3   | 03  | 0011   | 3/12           |                                                 |
| 4   | 04  | 0100   | 4/12           |                                                 |
| 5   | 05  | 0101   | 5/12           |                                                 |
| 6   | 06  | 0110   | 6/12           |                                                 |
| 7   | 07  | 0111   | 7/12           |                                                 |
| 8   | 08  | 1000   | 8/12           |                                                 |
| 9   | 09  | 1001   | 9/12           |                                                 |
| 10  | 0A  | 1010   | 10/12          |                                                 |
| 11  | 0B  | 1011   | 11/12          | ↓                                               |
| 12  | 0C  | 1100   | 1 (12/12)      |                                                 |
| 13  | 0D  | 1101   | 0/12           |                                                 |
| 14  | 0E  | 1110   | 0/12           |                                                 |
| 15  | 0F  | 1111   | 0/12           | This area is selected to OFF level (0/12 level) |
|     |     |        |                |                                                 |

– Gray Scale Table of 9 PWM (Pulse Width Modulation)

| Dec | Hex | 4-bits | PWM (on width) | Note                                           |
|-----|-----|--------|----------------|------------------------------------------------|
| 0   | 00  | 0000   | 0 (0/9)        | Brighter                                       |
| 1   | 01  | 0001   | 1/9            | ▲                                              |
| 2   | 02  | 0010   | 2/9            |                                                |
| 3   | 03  | 0011   | 3/9            |                                                |
| 4   | 04  | 0100   | 4/9            |                                                |
| 5   | 05  | 0101   | 5/9            |                                                |
| 6   | 06  | 0110   | 6/9            |                                                |
| 7   | 07  | 0111   | 7/9            |                                                |
| 8   | 08  | 1000   | 8/9            | ▼                                              |
| 9   | 09  | 1001   | 1 (9/9)        | Darker                                         |
| 10  | 0A  | 1010   | 0/9            | This area is selected to OFF level (0/9 level) |
| 11  | 0B  | 1011   | 0/9            |                                                |
| 12  | 0C  | 1100   | 0/9            |                                                |
| 13  | 0D  | 1101   | 0/9            |                                                |
| 14  | 0E  | 1110   | 0/9            |                                                |
| 15  | 0F  | 1111   | 0/9            |                                                |

## Oscillator

This is on-chip Oscillator with external resistor. Its frequency is controlled by external resistor between OSC1 and VDD. This oscillator signal is used in the voltage converter and display timing generation circuit.

## Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL(internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 128-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 9.

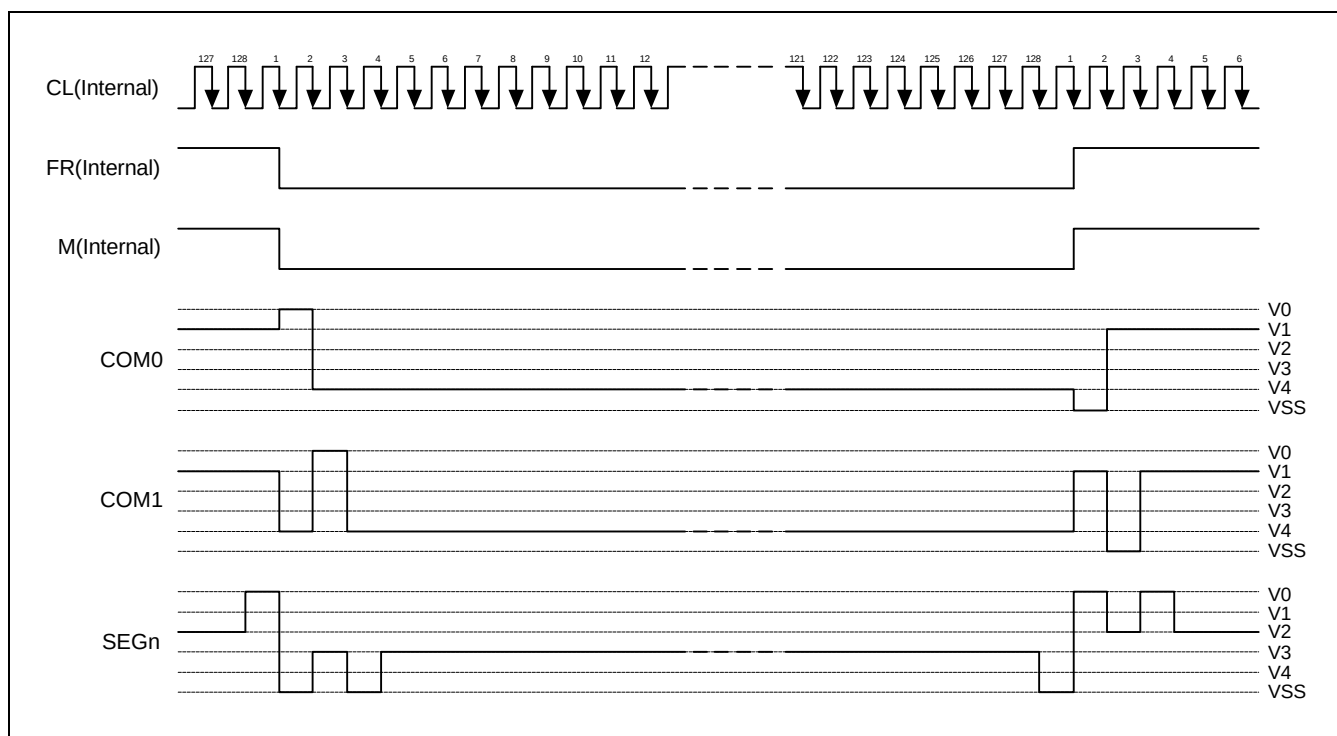


Figure 9. 2-frame AC Driving Waveform (Duty Ratio = 1/128)

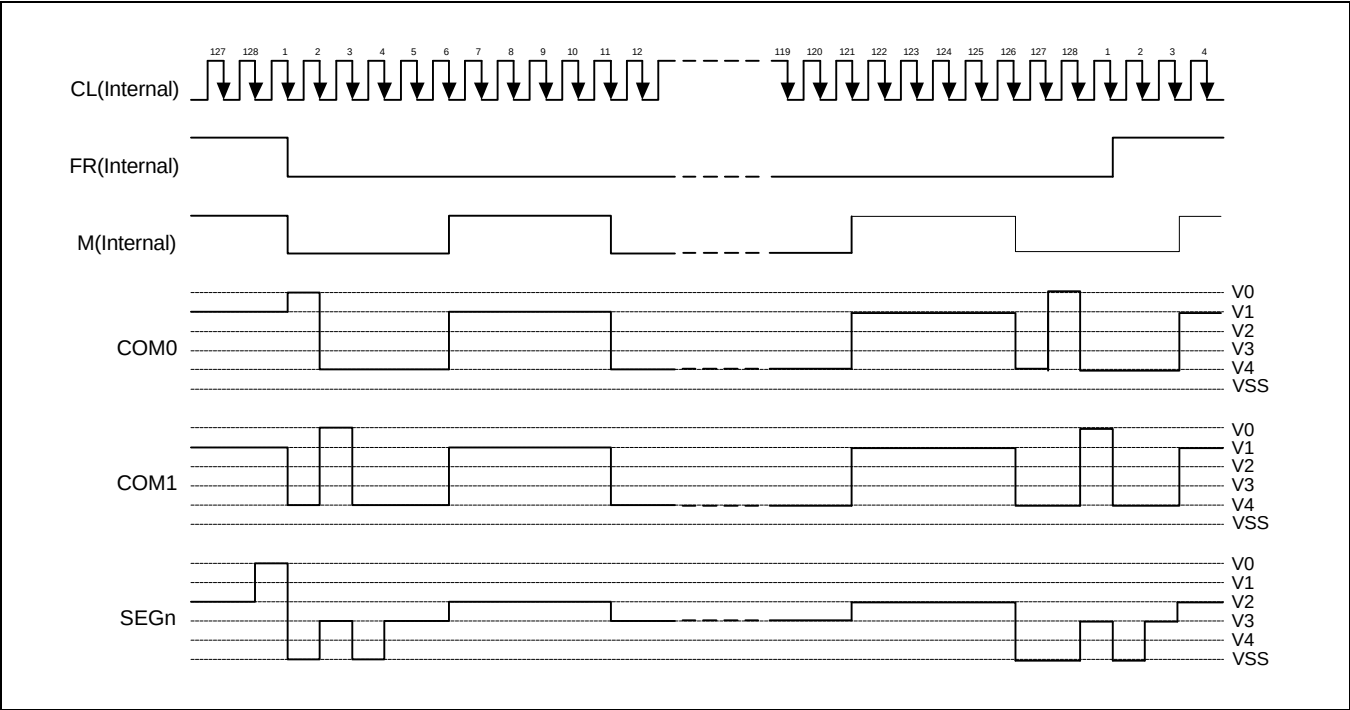


Figure 10. N-Line Inversion Driving Waveform (N = 5, Duty Ratio = 1/128)

## LCD DRIVER CIRCUIT

This driver circuit is configured by 129-channel common drivers and 128-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.

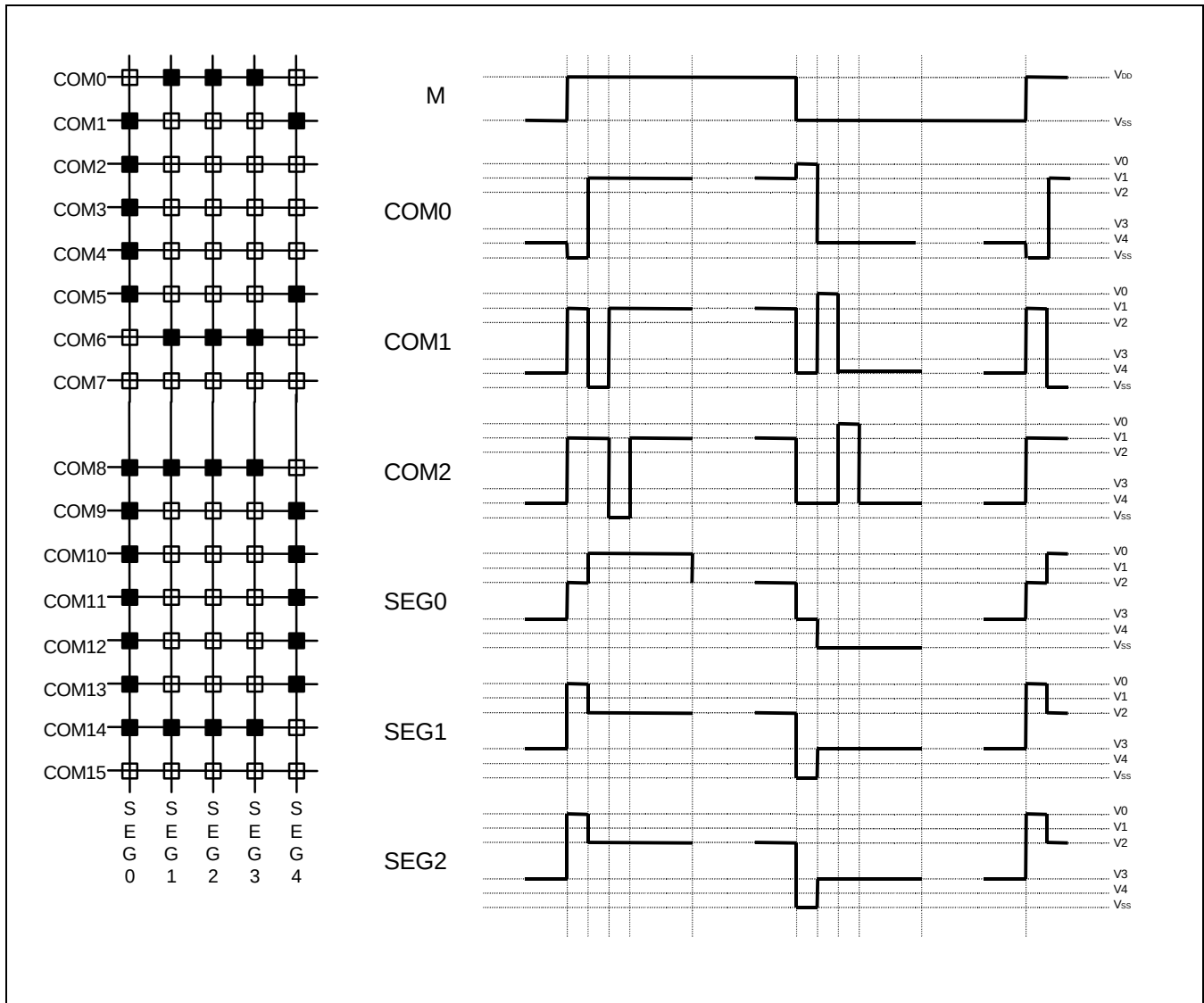


Figure 11. Segment and Common Timing

## Partial Display on LCD

The KS0741 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages

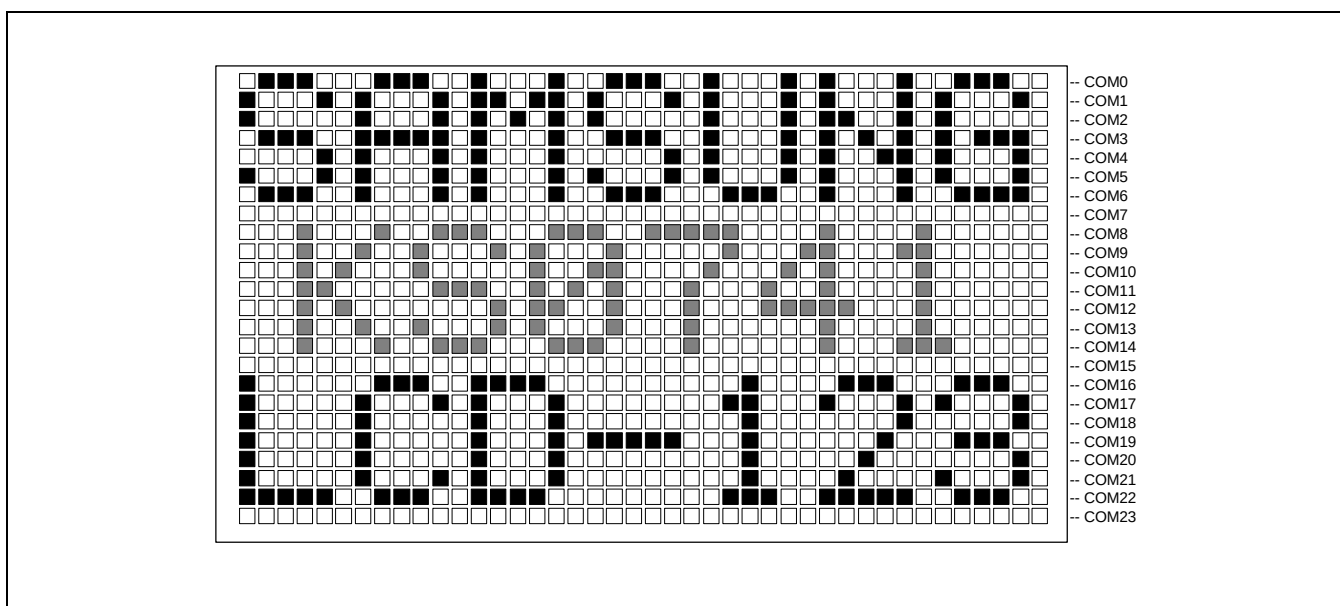


Figure 12. Reference Example for Partial Display

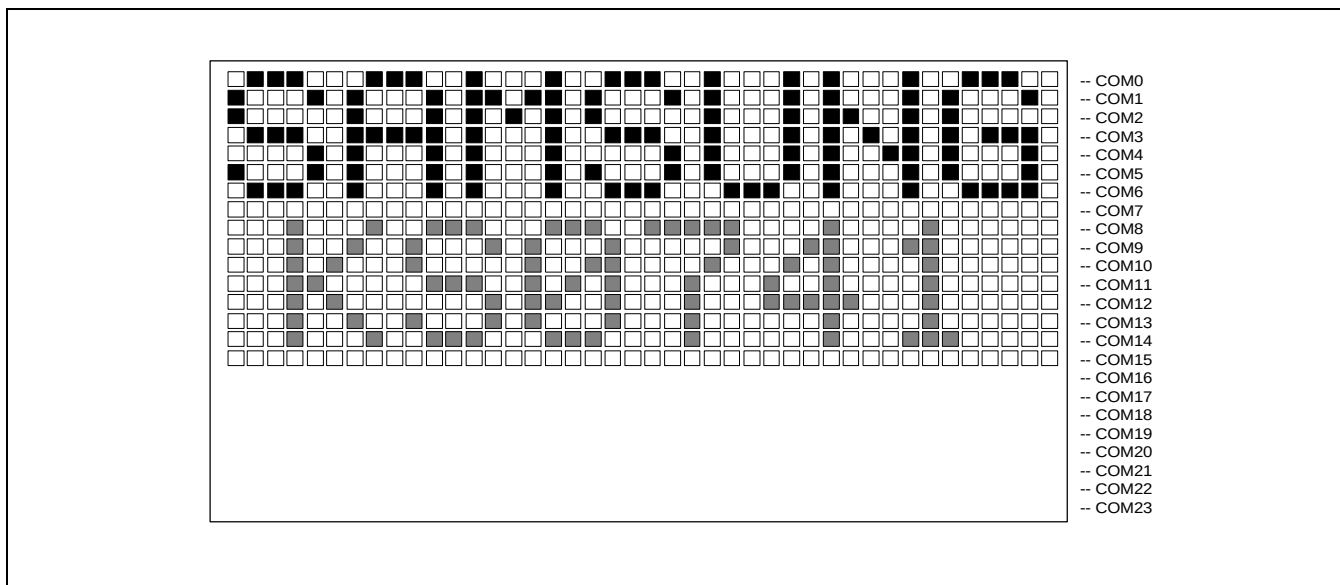


Figure 13. Partial Display (Partial Display Duty = 16, Initial COM0 = 0)

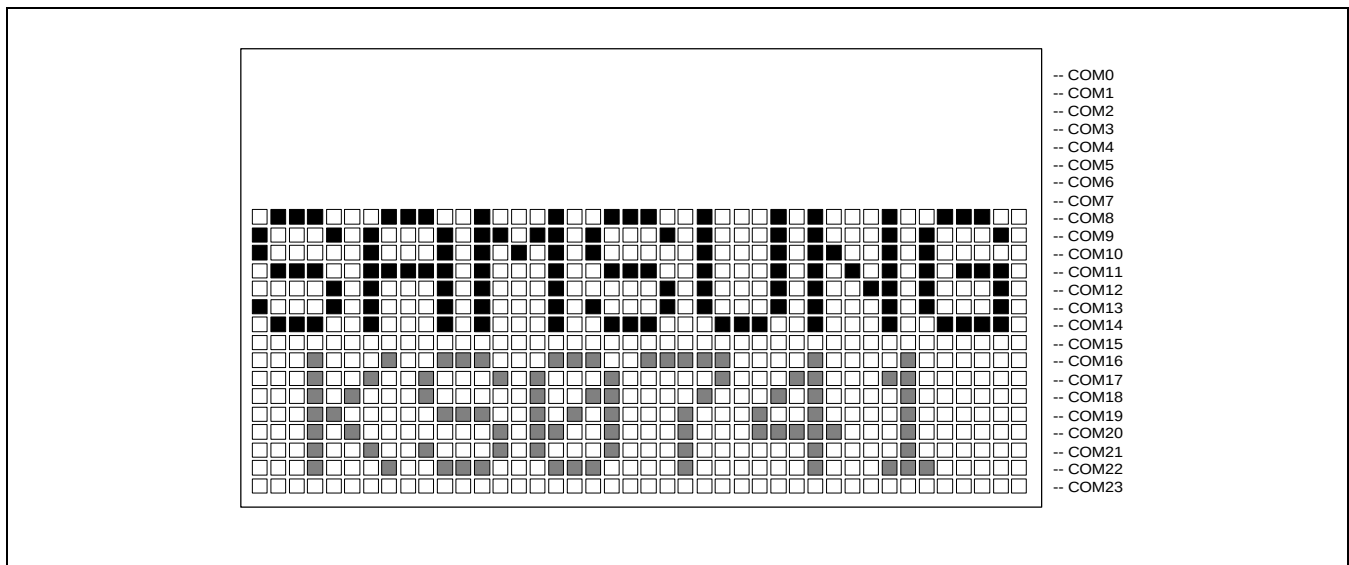


Figure 14. Moving Display (Partial Display Duty = 16, Initial COM0 = 8)



## POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 12 shows the referenced combinations in using Power Supply circuits.

**Table 12. Recommended Power Supply Combinations**

| User setup                                                                 | Power control<br>(VC VR VF) | V/C<br>circuits | V/R<br>circuits | V/F<br>circuits | VOUT           | V0             | V1 to V4       |
|----------------------------------------------------------------------------|-----------------------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|
| Only the internal power supply circuits are used                           | 1 1 1                       | ON              | ON              | ON              | Open           | Open           | Open           |
| Only the voltage regulator circuits and voltage follower circuits are used | 0 1 1                       | OFF             | ON              | ON              | External input | Open           | Open           |
| Only the voltage follower circuits are used                                | 0 0 1                       | OFF             | OFF             | ON              | Open           | External input | Open           |
| Only the external power supply circuits are used                           | 0 0 0                       | OFF             | OFF             | OFF             | Open           | External input | External input |

### Voltage Converter Circuits

These circuits boost up the electric potential between VCI and Vss to 3, 4, 5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by "Set DC-DC Step-up" instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

[C1 = 1.0 to 4.7 mF]

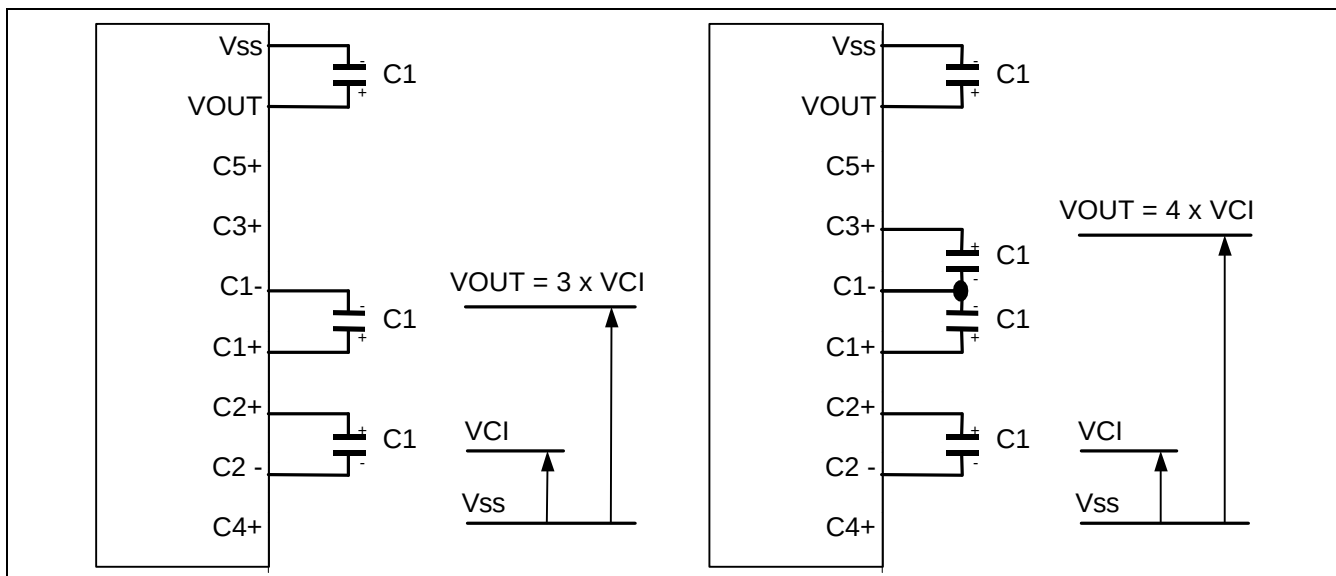


Figure 15. Three Times Boosting Circuit

Figure 16. Four Times Boosting Circuit

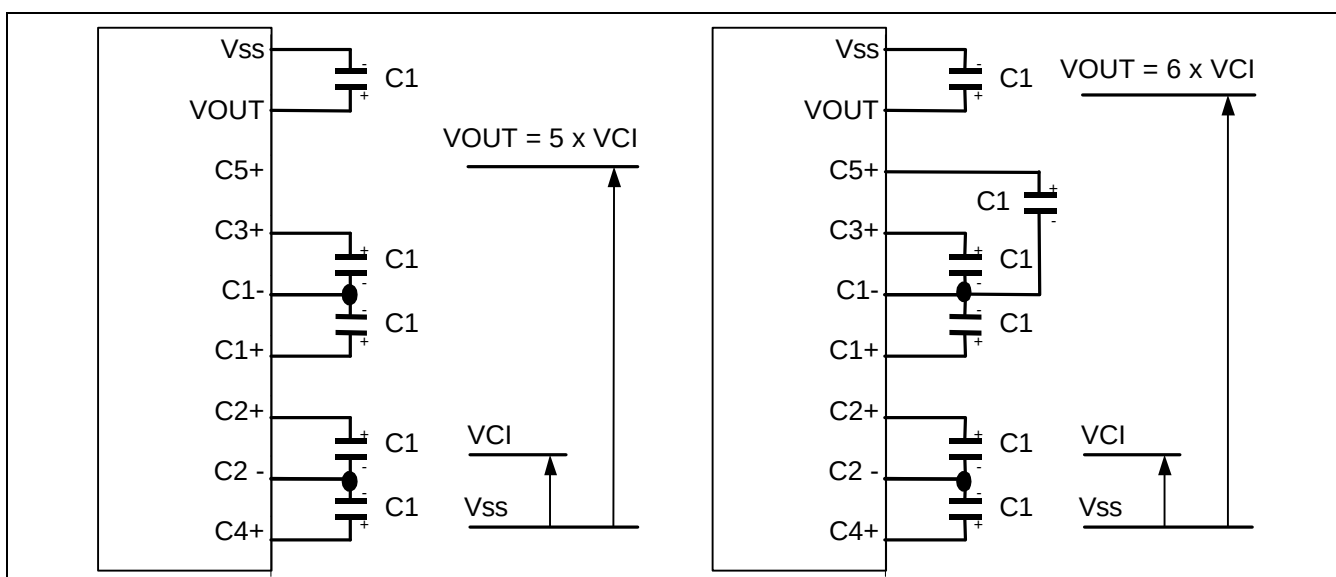


Figure 17. Five Times Boosting Circuit

Figure 18. Six Times Boosting Circuit

### Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage,  $V_0$ , by adjusting resistors,  $R_a$  and  $R_b$ , within the range of  $|V_0| < |V_{OUT}|$ . Because  $V_{OUT}$  is the operating voltage of operational-amplifier circuits shown in figure 19, it is necessary to be applied internally or externally.

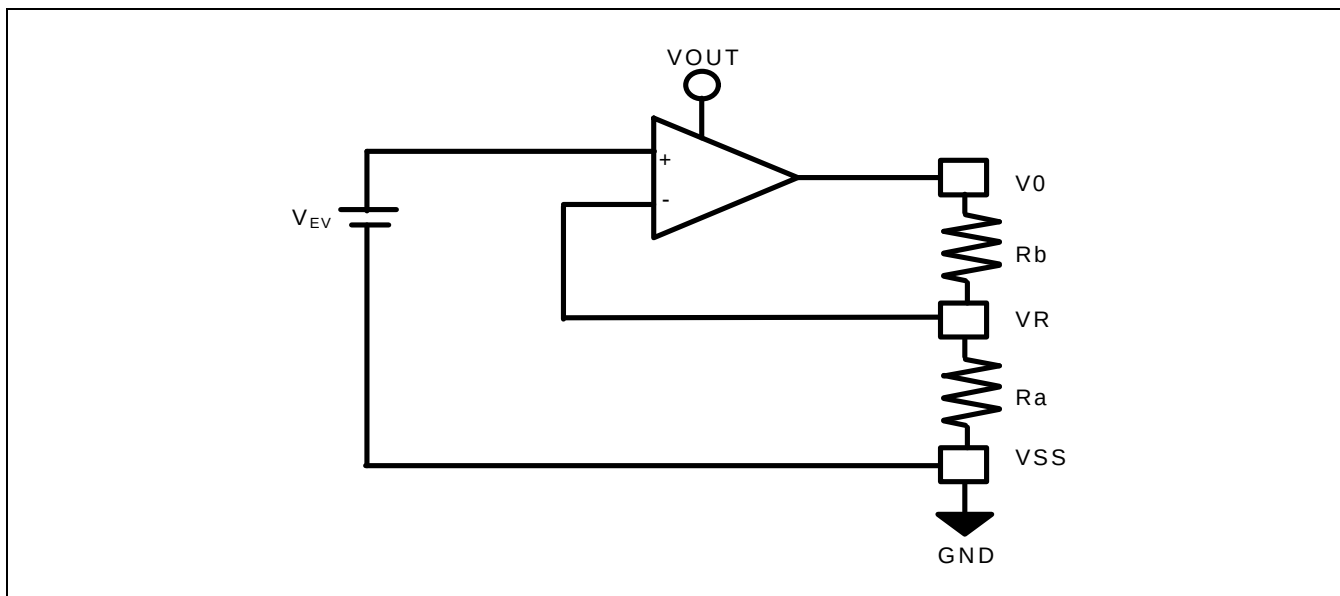
For the Eq. 1, we determine  $V_0$  by  $R_a$ ,  $R_b$  and  $V_{EV}$ . The  $R_a$  and  $R_b$  are connected internally or externally by INTR pin. And  $V_{EV}$  called the voltage of electronic volume is determined by Eq. 2, where the parameter  $\alpha$  is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63.  $V_{REF}$  voltage at  $T_a = 25^\circ\text{C}$  is shown in Table 13.

$$V_0 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV} \quad [\text{V}] \quad \text{----- (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{210}\right) \times V_{REF} \quad [\text{V}] \quad \text{----- (Eq. 2)}$$

**Table 13 .  $V_{REF}$  Voltage at  $T_a = 25^\circ\text{C}$**

| REF | Temp. coefficient         | $V_{REF} [\text{V}]$ |
|-----|---------------------------|----------------------|
| 1   | -0.05% / $^\circ\text{C}$ | 2.1                  |
| 0   | External input            | $V_{EXT}$            |



**Figure 19. Internal Voltage Regulator Circuit**

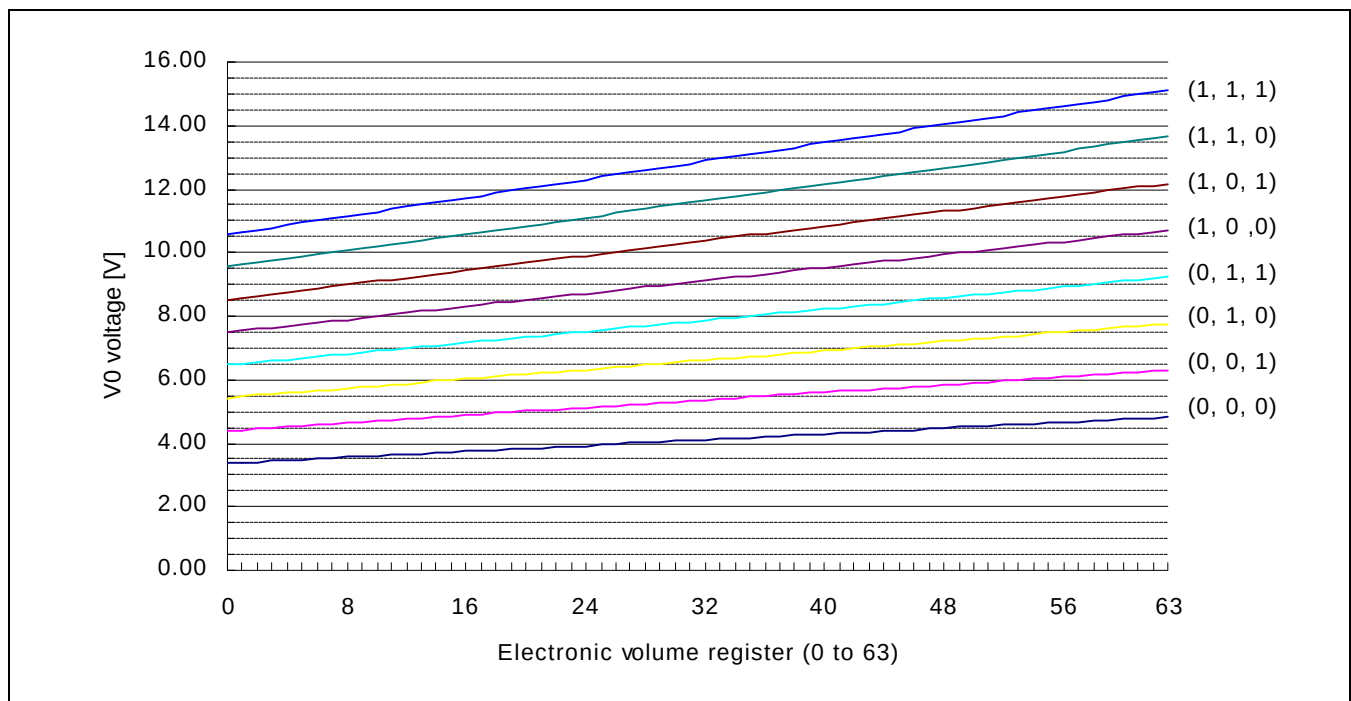
### In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is "H", resistor Ra is connected internally between VR pin and Vss, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

**Table 14. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)**

|               | 3-bit data settings (R2 R1 R0) |       |       |       |       |       |       |       |
|---------------|--------------------------------|-------|-------|-------|-------|-------|-------|-------|
|               | 0 0 0                          | 0 0 1 | 0 1 0 | 0 1 1 | 1 0 0 | 1 0 1 | 1 1 0 | 1 1 1 |
| 1 + (Rb / Ra) | 2.3                            | 3.0   | 3.7   | 4.4   | 5.1   | 5.8   | 6.5   | 7.2   |

Figure 20 Shows V0 voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.



**Figure 20. Electronic Volume Level (Temp. Coefficient = -0.05% / °C)**

### In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$10 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV} \quad [V] \text{ ----- (Eq. 3)}$$

From Eq. 1

$$V_{EV} = \left(1 - \frac{(63 - 32)}{210}\right) \times 2.1 = 1.79 \quad [V] \text{ ----- (Eq. 4)}$$

From requirement 3.

$$\frac{10}{R_a + R_b} = 1 \quad [\mu A] \text{ ----- (Eq. 5)}$$

From equations Eq. 3, 4 and 5

$$R_a = 1.79 \quad [M\Omega]$$

$$R_b = 8.21 \quad [M\Omega]$$

Table 15 Shows the Range of V0 depending on the above Requirements.

**Table 15. The Range of V0**

|    | Electronic volume level |       |       |       |       |
|----|-------------------------|-------|-------|-------|-------|
|    | 0                       | ..... | 32    | ..... | 63    |
| V0 | 8.21                    | ..... | 10.00 | ..... | 11.73 |

### Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 16 shows the relationship between V1 to V4 level and each duty ratio.

**Table 16. The Relationship Between V1 to V4 Level and Each Duty Ratio**

| LCD bias | V1           | V2           | V3       | V4       | Remarks     |
|----------|--------------|--------------|----------|----------|-------------|
| 1/N      | (N-1)/N x V0 | (N-2)/N x V0 | 2/N x V0 | 1/N x V0 | N = 5 to 12 |

## REFERENCE CIRCUIT EXAMPLES

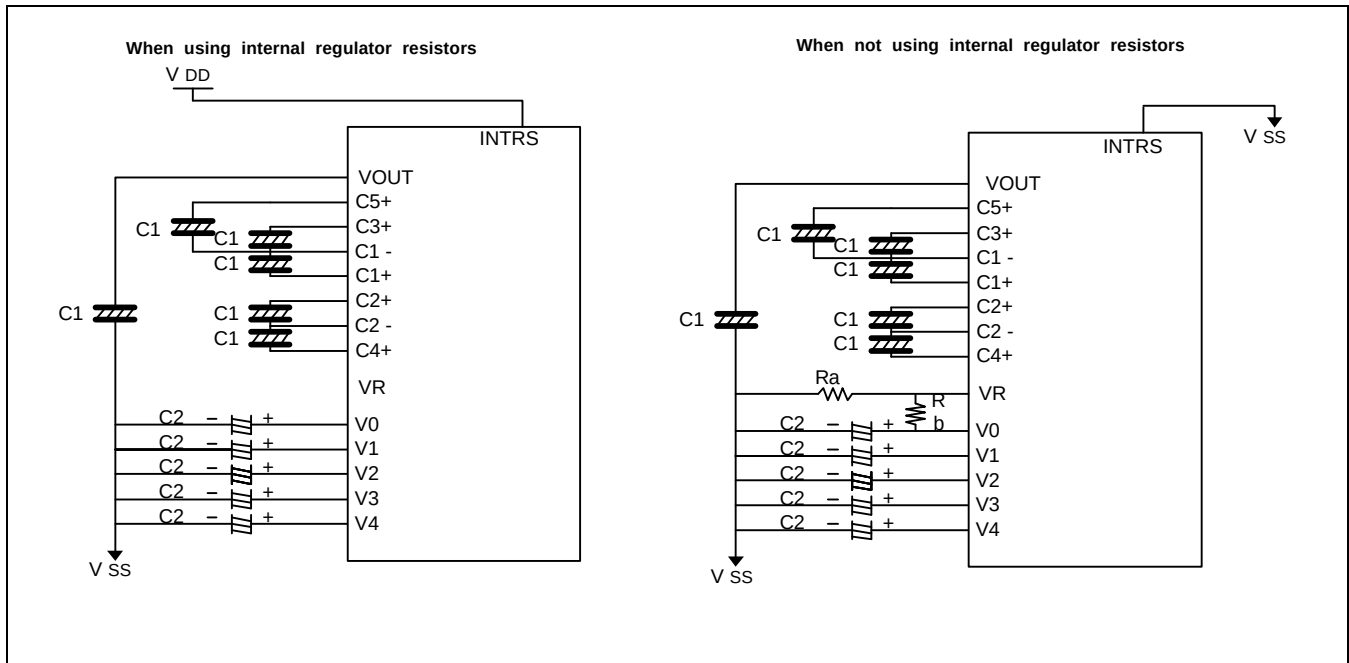
[C1 = 1.0 to 4.7  $\mu$ F, C2 = 0.47 to 2.0  $\mu$ F]

Figure 21. When Using all LCD Power Circuits (6-Time V/C: ON, V/R: ON, V/F: ON)

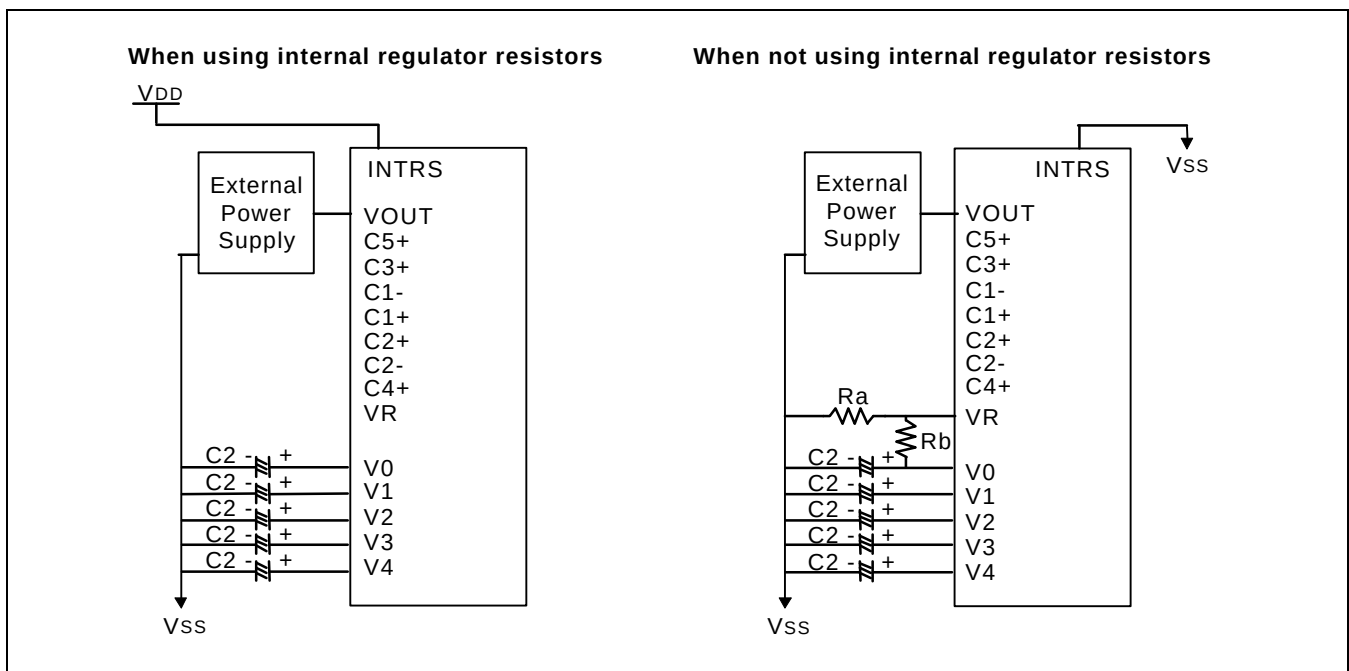
[C2 = 0.47 to 2.0  $\mu$ F]

Figure 22. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

[C2 = 0.47 to 2.0 [μF]]

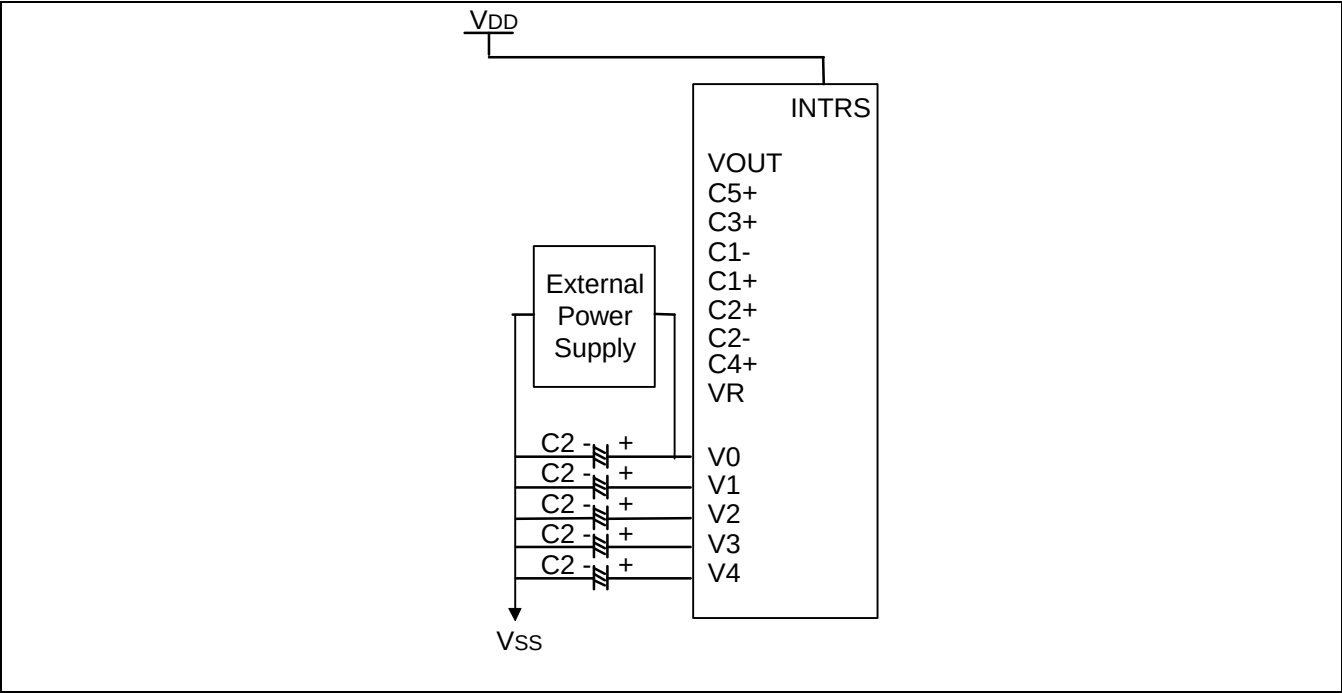


Figure 23. When Using some LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: ON)

[C2 = 0.47 to 2.0 [μF]]

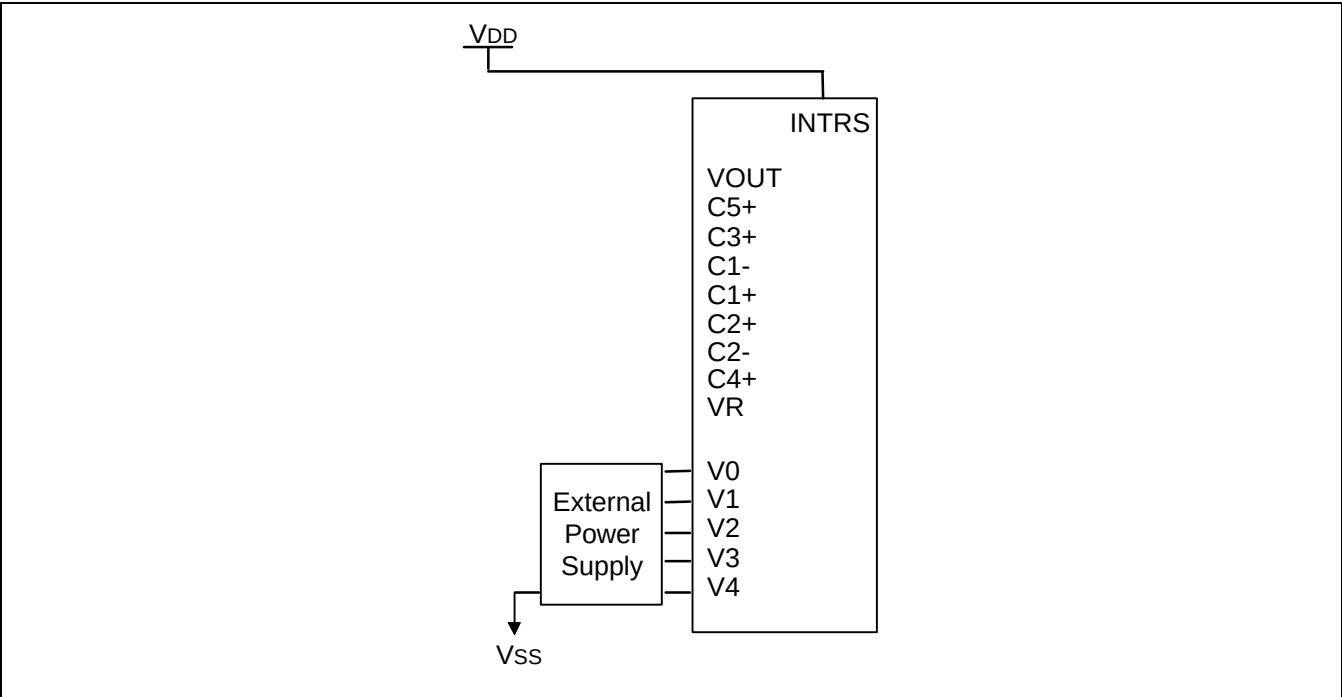


Figure 24. When Not Using any Internal LCD Power Supply Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

## RESET CIRCUIT

Setting RESETB to "L" or Reset instruction can initialize internal function.  
When RESETB becomes "L", following procedure is occurred.

Page address: 0  
Column address: 0  
Read-modify-write: OFF  
Display ON / OFF: OFF  
Initial display line: 0 (first)  
Initial COM0 register: 0 (COM0)  
Partial display duty ratio: 1/128  
Reverse display ON / OFF: OFF (normal)  
N-line inversion register: 0 (disable)  
Entire Display ON/OFF: OFF  
ICON Control register ON/OFF: OFF (ICON disable)  
Power control register (VC, VR, VF) = (0, 0, 0)  
DC-DC converter circuit = (0, 0)  
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)  
Contrast Level: 32  
LCD bias ratio: 1/12  
COM Scan Direction: 0  
ADC Select: 0  
Oscillator: OFF  
Power Save Mode: Release  
Display Data Length register: 0 (for SPI mode)  
White mode set: OFF  
White palette register (WG3, WG2, WG1, WG0) = (0, 0, 0, 0)  
Light gray mode set: OFF  
Light gray palette register (LG3, LG2, LG1, LG0) = (0, 0, 0, 0)  
Dark gray mode set: OFF  
Dark gray palette register (DG3, DG2, DG1, DG0) = (1, 1, 1, 1)  
Black mode set: OFF  
Black palette register (BG3, BG2, BG1, BG0) = (1, 1, 1, 1)  
FRC, PWM mode: 4FRC, 9PWM

When RESET instruction is issued, following procedure is occurred.

Page address: 0  
Column address: 0  
Read-modify-write: OFF  
Initial display line: 0 (First)  
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)  
Contrast Level: 32  
Display Data Length register: 0 (for SPI mode)  
White mode set: OFF  
White palette register (WG3, WG2, WG1, WG0) = (0, 0, 0, 0)  
Light gray mode set: OFF  
Light gray palette register (LG3, LG2, LG1, LG0) = (0, 0, 0, 0)  
Dark gray mode set: OFF  
Dark gray palette register (DG3, DG2, DG1, DG0) = (1, 1, 1, 1)  
Black mode set: OFF  
Black palette register (BG3, BG2, BG1, BG0) = (1, 1, 1, 1)  
FRC, PWM mode: 4FRC, 9PWM

While RESETB is "L" or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.



## INSTRUCTION DESCRIPTION

Table 17. Instruction Table

× : Don't care

| Instruction                       | RS | RW | DB7        | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0  | Description                                                                          |
|-----------------------------------|----|----|------------|-----|-----|-----|-----|-----|-----|------|--------------------------------------------------------------------------------------|
| Read display data                 | 1  | 1  | Read data  |     |     |     |     |     |     |      | Read data from DDRAM                                                                 |
| Write display data                | 1  | 0  | Write data |     |     |     |     |     |     |      | Write data into DDRAM                                                                |
| Read status                       | 0  | 1  | BUSY       | ON  | RES | MF2 | MF1 | MF0 | DS1 | DS0  | Read the internal status                                                             |
| ICON control register ON/OFF      | 0  | 0  | 1          | 0   | 1   | 0   | 0   | 0   | 1   | ICON | ICON=0: ICON disable (default)<br>ICON=1: ICON enable & set the page address to 16   |
| Set page address                  | 0  | 0  | 1          | 0   | 1   | 1   | P3  | P2  | P1  | P0   | Set page address                                                                     |
| Set column address MSB            | 0  | 0  | 0          | 0   | 0   | 1   | 0   | Y7  | Y6  | Y5   | Set column address MSB                                                               |
| Set column address LSB            | 0  | 0  | 0          | 0   | 0   | 0   | Y4  | Y3  | Y2  | Y1   | Set column address LSB                                                               |
| Set modify-read                   | 0  | 0  | 1          | 1   | 1   | 0   | 0   | 0   | 0   | 0    | Set modify-read mode                                                                 |
| Reset modify-read                 | 0  | 0  | 1          | 1   | 1   | 0   | 1   | 1   | 1   | 0    | release modify-read mode                                                             |
| Display ON/OFF                    | 0  | 0  | 1          | 0   | 1   | 0   | 1   | 1   | 1   | D    | D=0: display OFF<br>D=1: display ON                                                  |
| Set initial display line register | 0  | 0  | 0          | 1   | 0   | 0   | 0   | 0   | ×   | ×    | 2-byte instruction to specify the initial display line to realize vertical scrolling |
|                                   | 0  | 0  | ×          | S6  | S5  | S4  | S3  | S2  | S1  | S0   |                                                                                      |
| Set initial COM0 register         | 0  | 0  | 0          | 1   | 0   | 0   | 0   | 1   | ×   | ×    | 2-byte instruction to specify the initial COM0 to realize window scrolling           |
|                                   | 0  | 0  | ×          | C6  | C5  | C4  | C3  | C2  | C1  | C0   |                                                                                      |
| Set partial display duty ratio    | 0  | 0  | 0          | 1   | 0   | 0   | 1   | 0   | ×   | ×    | 2-byte instruction to set partial display duty ratio                                 |
|                                   | 0  | 0  | D7         | D6  | D5  | D4  | D3  | D2  | D1  | D0   |                                                                                      |
| Set N-line inversion              | 0  | 0  | 0          | 1   | 0   | 0   | 1   | 1   | ×   | ×    | 2-byte instruction to set N-line inversion register                                  |
|                                   | 0  | 0  | ×          | ×   | ×   | N4  | N3  | N2  | N1  | N0   |                                                                                      |
| Release N-line inversion          | 0  | 0  | 1          | 1   | 1   | 0   | 0   | 1   | 0   | 0    | Release N-line Inversion mode                                                        |
| Reverse display ON/OFF            | 0  | 0  | 1          | 0   | 1   | 0   | 0   | 1   | 1   | REV  | REV=0: normal display,<br>REV=1: reverse display                                     |
| Entire display ON/OFF             | 0  | 0  | 1          | 0   | 1   | 0   | 0   | 1   | 0   | EON  | EON=0: normal display.<br>EON=1: entire display ON                                   |

Table 17. Instruction Table (Continued)

× : Don't care

| Instruction                                   | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Description                                                                         |
|-----------------------------------------------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-------------------------------------------------------------------------------------|
| Power control                                 | 0  | 0  | 0   | 0   | 1   | 0   | 1   | VC  | VR  | VF  | Control power circuit operation                                                     |
| Select DC-DC step-up                          | 0  | 0  | 0   | 1   | 1   | 0   | 0   | 1   | DC1 | DC0 | Select the step-up of the internal voltage converter                                |
| Select regulator resistor                     | 0  | 0  | 0   | 0   | 1   | 0   | 0   | R2  | R1  | R0  | Select internal resistance ratio of the regulator resistor                          |
| Set electronic volume register                | 0  | 0  | 1   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 2-byte instruction to specify the Reference voltage                                 |
|                                               | 0  | 0  | ×   | ×   | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |                                                                                     |
| Select LCD bias                               | 0  | 0  | 0   | 1   | 0   | 1   | 0   | B2  | B1  | B0  | Select LCD bias                                                                     |
| SHL select                                    | 0  | 0  | 1   | 1   | 0   | 0   | SHL | ×   | ×   | ×   | COM bi-directional selection<br>SHL=0: normal direction<br>SHL=1: reverse direction |
| ADC select                                    | 0  | 0  | 1   | 0   | 1   | 0   | 0   | 0   | 0   | ADC | SEG bi-directional selection<br>ADC=0: normal direction<br>ADC=1: reverse direction |
| Oscillator on start                           | 0  | 0  | 1   | 0   | 1   | 0   | 1   | 0   | 1   | 1   | Start the built-in oscillator                                                       |
| Set power save mode                           | 0  | 0  | 1   | 0   | 1   | 0   | 1   | 0   | 0   | P   | P=0: normal mode<br>P=1: sleep mode                                                 |
| Release power save mode                       | 0  | 0  | 1   | 1   | 1   | 0   | 0   | 0   | 0   | 1   | Release power save mode                                                             |
| Reset                                         | 0  | 0  | 1   | 1   | 1   | 0   | 0   | 0   | 1   | 0   | Initialize the internal functions                                                   |
| Set data direction & display data length(DDL) | ×  | ×  | 1   | 1   | 1   | 0   | 1   | 0   | 0   | 0   | 2-byte instruction to specify the number of data bytes.<br>(SPI Mode)               |
|                                               | ×  | ×  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |                                                                                     |
| NOP                                           | 0  | 0  | 1   | 1   | 1   | 0   | 0   | 0   | 1   | 1   | <u>No operation</u>                                                                 |
| Test Instruction                              | 0  | 0  | 1   | 1   | 1   | 1   | ×   | ×   | ×   | ×   | <u>Don't use this instruction.</u>                                                  |

Table 17. Instruction Table (Continued)

| Instruction                                                                     | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1  | DB0  | Description                                                                        |
|---------------------------------------------------------------------------------|----|----|-----|-----|-----|-----|-----|-----|------|------|------------------------------------------------------------------------------------|
| Set FRC and PWM mode                                                            | 0  | 0  | 1   | 0   | 0   | 1   | 0   | FRC | PWM1 | PWM0 | FRC(1:3FRC, 0:4FRC)<br>PWM1 PWM0<br>0 0 9PWM<br>0 1 9PWM<br>1 0 12PWM<br>1 1 15PWM |
| Set white mode and 1 <sup>st</sup> /2 <sup>nd</sup> frame, set pulse width      | 0  | 0  | 1   | 0   | 0   | 0   | 1   | 0   | 0    | 0    | Set white mode and 1 <sup>st</sup> /2 <sup>nd</sup> frame                          |
|                                                                                 | 0  | 0  | WB3 | WB2 | WB1 | WB0 | WA3 | WA2 | WA1  | WA0  |                                                                                    |
| Set white mode and 3 <sup>rd</sup> /4 <sup>th</sup> frame, set pulse width      | 0  | 0  | 1   | 0   | 0   | 0   | 1   | 0   | 0    | 1    | Set white mode and 3 <sup>rd</sup> /4 <sup>th</sup> frame                          |
|                                                                                 | 0  | 0  | WD3 | WD2 | WD1 | WD0 | WC3 | WC2 | WC1  | WC0  |                                                                                    |
| Set light gray mode and 1 <sup>st</sup> /2 <sup>nd</sup> frame, set pulse width | 0  | 0  | 1   | 0   | 0   | 0   | 1   | 0   | 1    | 0    | Set light gray mode and 1 <sup>st</sup> /2 <sup>nd</sup> frame                     |
|                                                                                 | 0  | 0  | LB3 | LB2 | LB1 | LB0 | LA3 | LA2 | LA1  | LA0  |                                                                                    |
| Set light gray mode and 3 <sup>rd</sup> /4 <sup>th</sup> frame, set pulse width | 0  | 0  | 1   | 0   | 0   | 0   | 1   | 0   | 1    | 1    | Set light gray mode and 3 <sup>rd</sup> /4 <sup>th</sup> frame                     |
|                                                                                 | 0  | 0  | LD3 | LD2 | LD1 | LD0 | LC3 | LC2 | LC1  | LC0  |                                                                                    |
| Set dark gray mode and 1 <sup>st</sup> /2 <sup>nd</sup> frame, set pulse width  | 0  | 0  | 1   | 0   | 0   | 0   | 1   | 1   | 0    | 0    | Set dark gray mode and 1 <sup>st</sup> /2 <sup>nd</sup> frame                      |
|                                                                                 | 0  | 0  | DB3 | DB2 | DB1 | DB0 | DA3 | DA2 | DA1  | DA0  |                                                                                    |
| Set dark gray mode and 3 <sup>rd</sup> /4 <sup>th</sup> frame, set pulse width  | 0  | 0  | 1   | 0   | 0   | 0   | 1   | 1   | 0    | 1    | Set dark gray mode and 3 <sup>rd</sup> /4 <sup>th</sup> frame                      |
|                                                                                 | 0  | 0  | DD3 | DD2 | DD1 | DD0 | DC3 | DC2 | DC1  | DC0  |                                                                                    |
| Set black mode and 1 <sup>st</sup> /2 <sup>nd</sup> frame, set pulse width      | 0  | 0  | 1   | 0   | 0   | 0   | 1   | 1   | 1    | 0    | Set black mode and 1 <sup>st</sup> /2 <sup>nd</sup> frame                          |
|                                                                                 | 0  | 0  | BB3 | BB2 | BB1 | BB0 | BA3 | BA2 | BA1  | BA0  |                                                                                    |
| Set black mode and 3 <sup>rd</sup> /4 <sup>th</sup> frame, set pulse width      | 0  | 0  | 1   | 0   | 0   | 0   | 1   | 1   | 1    | 1    | Set black mode and 3 <sup>rd</sup> /4 <sup>th</sup> frame                          |
|                                                                                 | 0  | 0  | BD3 | BD2 | BD1 | BD0 | BC3 | BC2 | BC1  | BC0  |                                                                                    |

### Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

| RS | RW | DB7       | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----------|-----|-----|-----|-----|-----|-----|-----|
| 1  | 1  | Read data |     |     |     |     |     |     |     |

### Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written

| RS | RW | DB7        | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|------------|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0  | Write data |     |     |     |     |     |     |     |

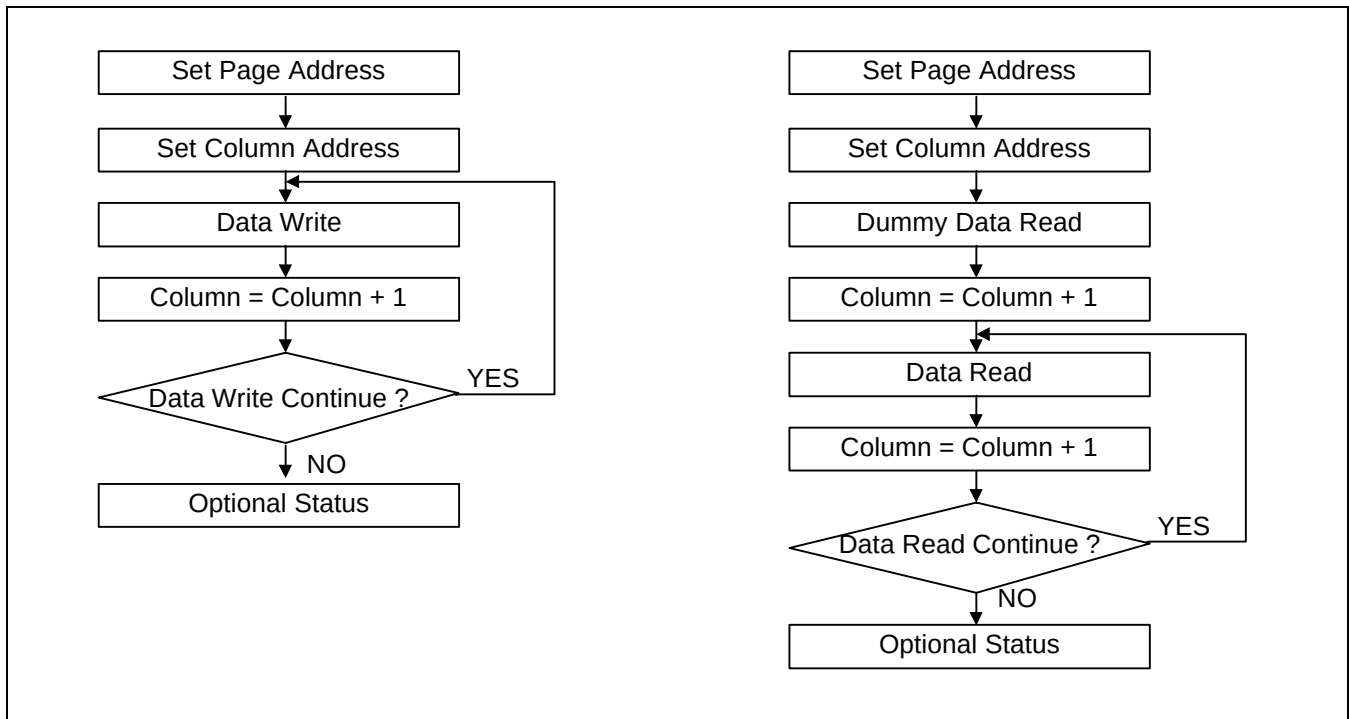


Figure 25. Sequence for Writing Display Data

Figure 26. Sequence for Reading Display Data

**Read Status**

Indicates the internal status of the KS0741

| RS | RW | DB7  | DB6    | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|------|--------|-----|-----|-----|-----|-----|-----|
| 0  | 1  | BUSY | ON/OFF | RES | MF2 | MF1 | MF0 | DS1 | DS0 |

| Flag     | Description                                                                                                                                       |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| BUSY     | The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low.<br>0: chip is active, 1: chip is being busy |
| ON / OFF | Indicates display ON / OFF status<br>0: display OFF, 1: display ON                                                                                |
| RESET    | Indicates the initialization is in progress by RESET signal.<br>0: chip is active, 1: chip is being reset                                         |
| MF       | Manufacturer ID, MF2 MF1 MF0 = [0 0 0]                                                                                                            |
| DS       | Display size ID, DS1 DS0 = [1 0]                                                                                                                  |

**ICON control register ON/OFF**

This instruction makes ICON enable or disable. By default, ICON display is disabled (ICON= 0). When ICON control register is set to "1", ICON display is enabled and page address is set to "16". Then user can write data for icons. It is impossible to set the page address to "16" by Set Page Address instruction. Therefore, when writing data for icons, ICON control register ON instruction would be used to set the page address to "16". When ICON control register is set to "0", ICON display is disabled.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0  |
|----|----|-----|-----|-----|-----|-----|-----|-----|------|
| 0  | 0  | 1   | 0   | 1   | 0   | 0   | 0   | 1   | ICON |

ICON=0: ICON disable (default)

ICON=1: ICON enable & set the page address to 16

**Set Page Address**

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status. Set Page Address instruction can not be used to set the page address to "16". Use ICON control register ON/OFF instruction to set the page address to "16".

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 1   | P3  | P2  | P1  | P0  |

| P3 | P2 | P1 | P0 | Page |
|----|----|----|----|------|
| 0  | 0  | 0  | 0  | 0    |
| 0  | 0  | 0  | 1  | 1    |
| :  | :  | :  | :  | :    |
| 1  | 1  | 1  | 0  | 14   |
| 1  | 1  | 1  | 1  | 15   |

**Set Column Address**

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

**Set Column Address MSB**

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 0   | 0   | 1   | 0   | Y7  | Y6  | Y5  |

**Set Column Address LSB**

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 0   | 0   | 0   | Y4  | Y3  | Y2  | Y1  |

| Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Column address [Y7:Y1] |
|----|----|----|----|----|----|----|------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1                      |
| :  | :  | :  | :  | :  | :  | :  | :                      |
| 1  | 1  | 1  | 1  | 1  | 1  | 0  | 126                    |
| 1  | 1  | 1  | 1  | 1  | 1  | 1  | 127                    |

### Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-Read instruction.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 1   | 0   | 0   | 0   | 0   | 0   |

### Reset Modify-Read

This instruction cancels the Modify-Read mode, and makes the column address return to its initial value just before the set Modify-Read instruction is started.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 1   | 0   | 1   | 1   | 1   | 0   |

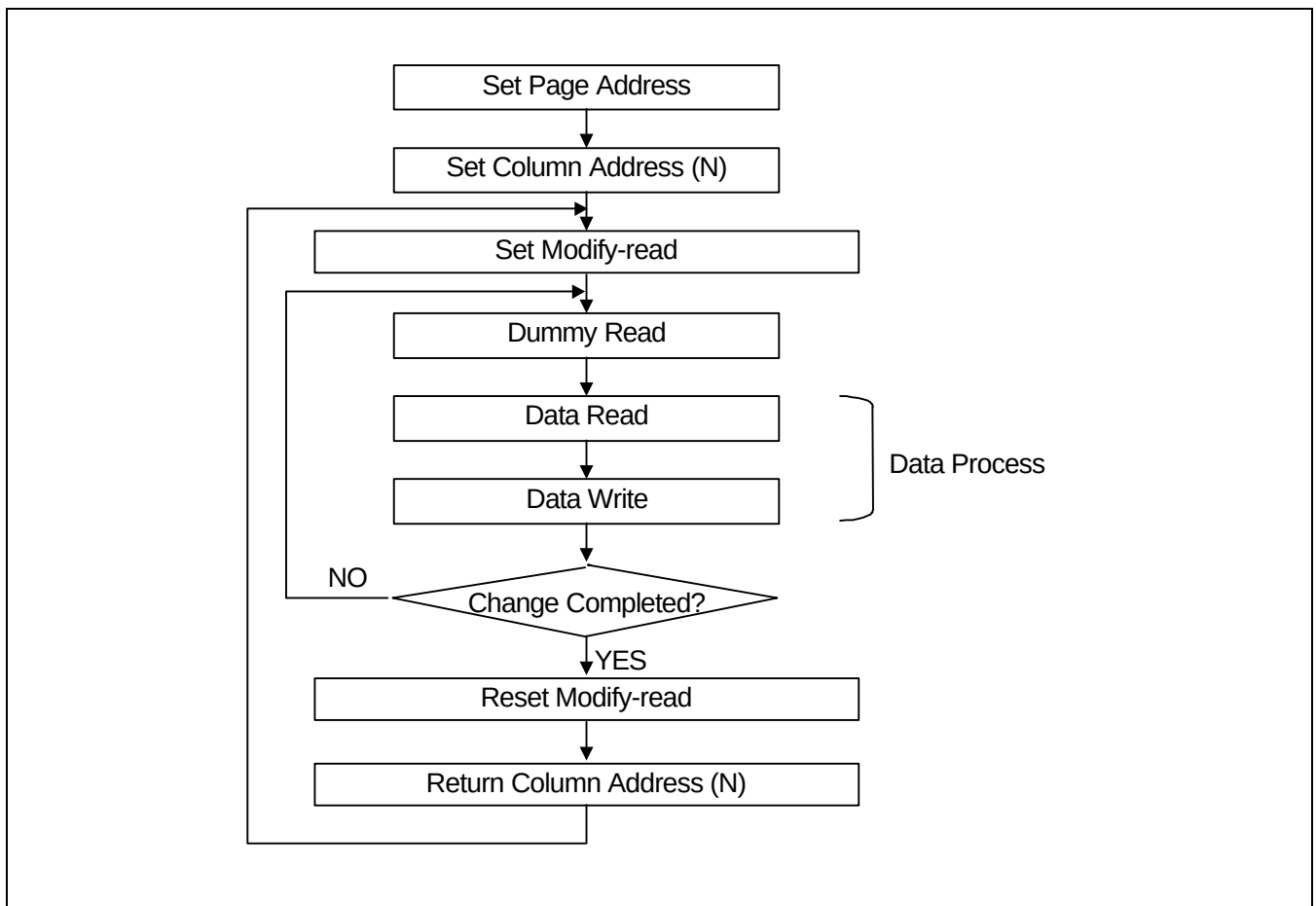


Figure 27. Sequence for Cursor Display

**Display ON / OFF**

Turns the display ON or OFF.

This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 0   | 1   | 1   | 1   | DON |

DON = 1: display ON

DON = 0: display OFF

**Set Initial Display Line Register**

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row(COM0) of LCD panel.

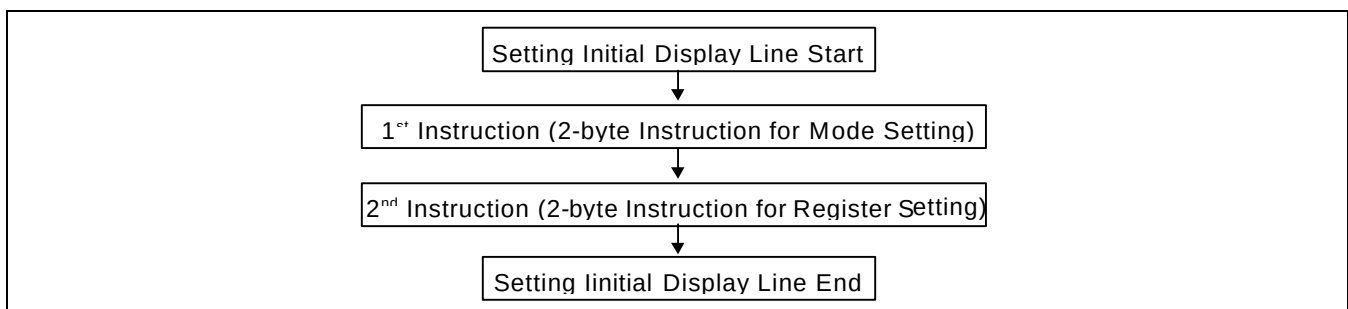
**The 1<sup>st</sup> Instruction**

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 1   | 0   | 0   | 0   | 0   | ×   | ×   |

**The 2<sup>nd</sup> Instruction**

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | ×   | S6  | S5  | S4  | S3  | S2  | S1  | S0  |

| S6 | S5 | S4 | S3 | S2 | S1 | S0 | Line address |
|----|----|----|----|----|----|----|--------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1            |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 2            |
| 0  | 0  | 0  | 0  | 0  | 1  | 1  | 3            |
| :  | :  | :  | :  | :  | :  | :  | :            |
| 1  | 1  | 1  | 1  | 1  | 0  | 0  | 124          |
| 1  | 1  | 1  | 1  | 1  | 0  | 1  | 125          |
| 1  | 1  | 1  | 1  | 1  | 1  | 0  | 126          |
| 1  | 1  | 1  | 1  | 1  | 1  | 1  | 127          |



**Figure 28. The Sequence for Setting the Initial Display Line**



### Set Initial COM0 Register

Sets the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

#### The 1<sup>st</sup> Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 1   | 0   | 0   | 0   | 1   | ×   | ×   |

#### The 2<sup>nd</sup> Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | ×   | C6  | C5  | C4  | C3  | C2  | C1  | C0  |

| C6 | C5 | C4 | C3 | C2 | C1 | C0 | Initial COM0 |
|----|----|----|----|----|----|----|--------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | COM0         |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | COM1         |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | COM2         |
| 0  | 0  | 0  | 0  | 0  | 1  | 1  | COM3         |
| :  | :  | :  | :  | :  | :  | :  | :            |
| 1  | 1  | 1  | 1  | 1  | 0  | 0  | COM124       |
| 1  | 1  | 1  | 1  | 1  | 0  | 1  | COM125       |
| 1  | 1  | 1  | 1  | 1  | 1  | 0  | COM126       |
| 1  | 1  | 1  | 1  | 1  | 1  | 1  | COM127       |

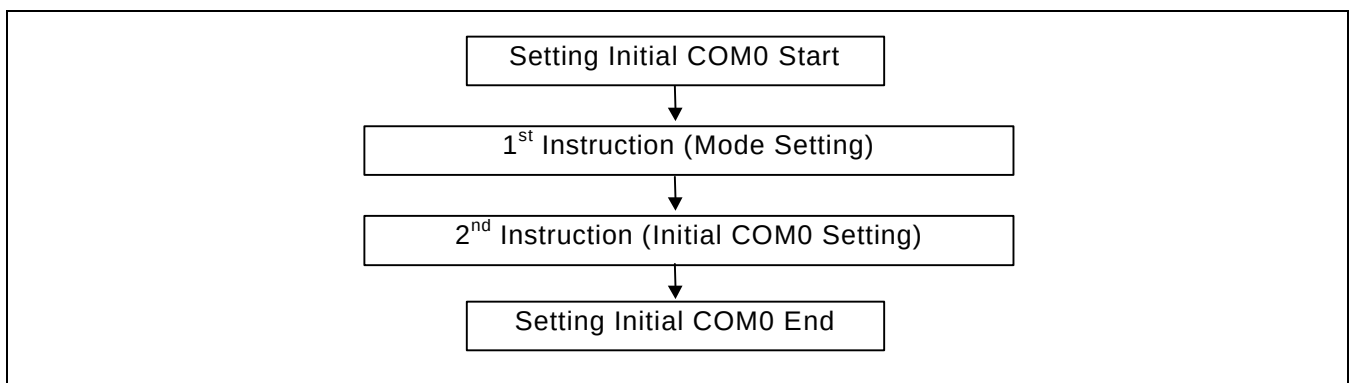


Figure 29. Sequence for Setting the Initial COM0

## Set Partial Display Duty Ratio

Sets the duty ratio within range of 16 to 128 (ICON disabled) or 17 to 129 (ICON enabled) to realize partial display by using the 2-byte instruction.

### The 1<sup>st</sup> Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 1   | 0   | 0   | 1   | 0   | ×   | ×   |

### The 2<sup>nd</sup> Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Selected partial duty ratio<br>(ICON disabled) | Selected partial duty ratio<br>(ICON enabled) |
|----|----|----|----|----|----|----|----|------------------------------------------------|-----------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | No operation                                   | No operation                                  |
| :  | :  | :  | :  | :  | :  | :  | :  |                                                |                                               |
| 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  |                                                |                                               |
| 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1/16                                           | 1/17                                          |
| 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 1/17                                           | 1/18                                          |
| :  | :  | :  | :  | :  | :  | :  | :  | :                                              | :                                             |
| 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1/127                                          | 1/128                                         |
| 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1/128                                          | 1/129                                         |
| 1  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | No operation                                   | No operation                                  |
| :  | :  | :  | :  | :  | :  | :  | :  |                                                |                                               |
| 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |                                                |                                               |

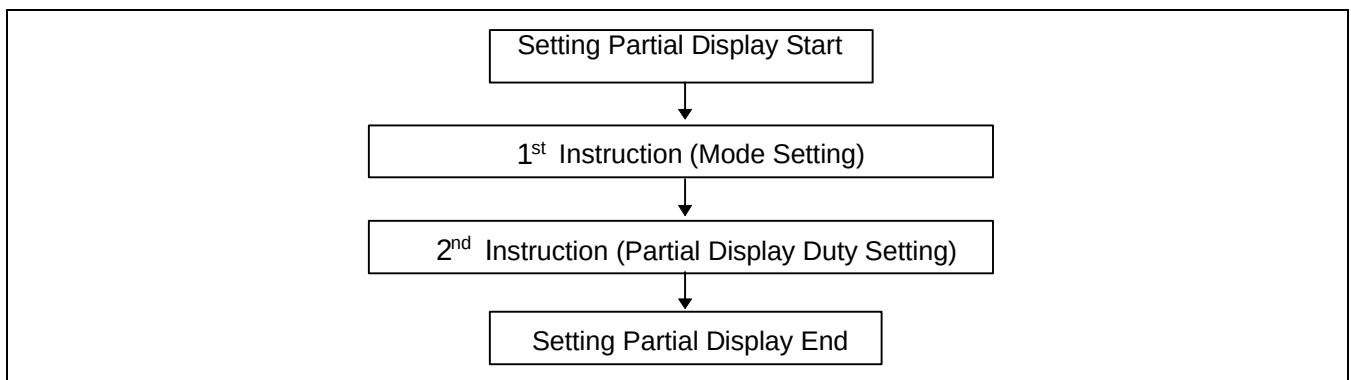


Figure 30. Sequence for Setting Partial Display

### Set N-line Inversion Register

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

The DC-bias problem could be occurred if K is even number. So, we recommend customers to set K to be odd number. K : D/N

D : The number of display duty ratio (D is selectable by customers)

N : N for N-line inversion (N is selectable by customers).

#### The 1<sup>st</sup> Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 1   | 0   | 0   | 1   | 1   | ×   | ×   |

#### The 2<sup>nd</sup> Instruction

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | ×   | ×   | ×   | N4  | N3  | N2  | N1  | N0  |

| N4 | N3 | N2 | N1 | N0 | Selected n-line inversion          |
|----|----|----|----|----|------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0-line inversion (frame inversion) |
| 0  | 0  | 0  | 0  | 1  | 3-line inversion                   |
| 0  | 0  | 0  | 1  | 0  | 4-line inversion                   |
| 0  | 0  | 0  | 1  | 1  | 5-line inversion                   |
| :  | :  | :  | :  | :  | :                                  |
| 1  | 1  | 1  | 0  | 1  | 31-line inversion                  |
| 1  | 1  | 1  | 1  | 0  | 32-line inversion                  |
| 1  | 1  | 1  | 1  | 1  | 33-line inversion                  |

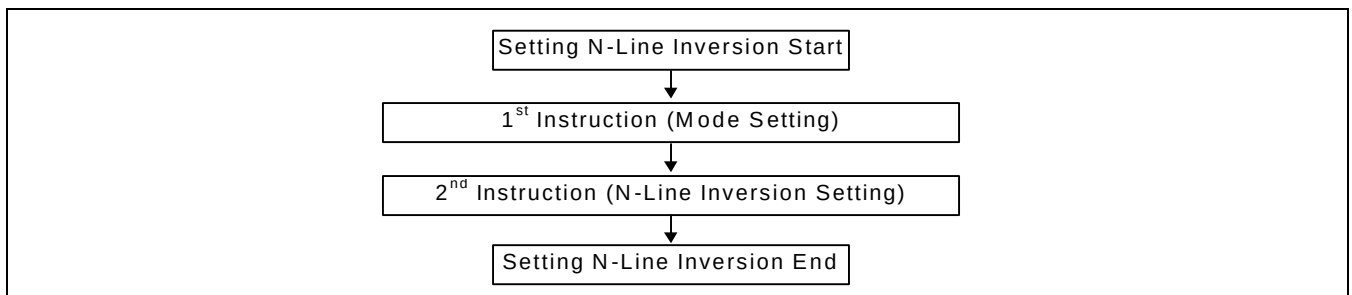


Figure 31. Sequence for N-line Inversion

### Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 1   | 0   | 0   | 1   | 0   | 0   |

**Reverse Display ON / OFF**

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 0   | 0   | 1   | 1   | REV |

| REV         | DDRAM data = "00"<br>– White | DDRAM data = "01"<br>– Light gray | DDRAM data = "10"<br>– Dark gray | DDRAM data = "11"<br>– Dark |
|-------------|------------------------------|-----------------------------------|----------------------------------|-----------------------------|
| 0 (normal)  | White ("00")                 | Light gray ("01")                 | Dark gray ("10")                 | Dark ("11")                 |
| 1 (reverse) | Dark ("11")                  | Dark gray ("10")                  | Light gray ("01")                | White ("00")                |

**Entire Display ON / OFF**

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 0   | 0   | 1   | 0   | EON |

| EON        | DDRAM data = "00"<br>– White | DDRAM data = "01"<br>– Light gray | DDRAM data = "10"<br>– Dark gray | DDRAM data = "11"<br>– Dark |
|------------|------------------------------|-----------------------------------|----------------------------------|-----------------------------|
| 0 (normal) | White ("00")                 | Light gray ("01")                 | Dark gray ("10")                 | Dark ("11")                 |
| 1 (entire) | Dark ("11")                  | Dark ("11")                       | Dark ("11")                      | Dark ("11")                 |

**Power Control**

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 0   | 1   | 0   | 1   | VC  | VR  | VF  |

| VC     | VR     | VF     | Status of internal power supply circuits                                              |
|--------|--------|--------|---------------------------------------------------------------------------------------|
| 0<br>1 |        |        | Internal voltage converter circuit is OFF<br>Internal voltage converter circuit is ON |
|        | 0<br>1 |        | Internal voltage regulator circuit is OFF<br>Internal voltage regulator circuit is ON |
|        |        | 0<br>1 | Internal voltage follower circuit is OFF<br>Internal voltage follower circuit is ON   |

**Select DC-DC Step-up**

Selects one of 4 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 1   | 1   | 0   | 0   | 1   | DC1 | DC0 |

| DC1 | DC0 | Selected DC-DC converter circuit |
|-----|-----|----------------------------------|
| 0   | 0   | 3 times boosting circuit         |
| 0   | 1   | 4 times boosting circuit         |
| 1   | 0   | 5 times boosting circuit         |
| 1   | 1   | 6 times boosting circuit         |

**Select Regulator Resistor**

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 14.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 0   | 1   | 0   | 0   | R2  | R1  | R0  |

| R2 | R1 | R0 | 1+ (Rb / Ra) |
|----|----|----|--------------|
| 0  | 0  | 0  | 2.3          |
| 0  | 0  | 1  | 3.0          |
| 0  | 1  | 0  | 3.7          |
| 0  | 1  | 1  | 4.4          |
| 1  | 0  | 0  | 5.1          |
| 1  | 0  | 1  | 5.8          |
| 1  | 1  | 0  | 6.5          |
| 1  | 1  | 1  | 7.2          |

### Set Electronic Volume Register

Consist of 2-byte Instructions

The 1<sup>st</sup> instruction set Reference Voltage mode, the 2<sup>nd</sup> one updates the contents of reference voltage register. After second instruction, Reference Voltage mode is released.

#### The 1<sup>st</sup> Instruction: Set Reference Voltage Select Mode

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |

#### The 2<sup>nd</sup> Instruction: Set Reference Voltage Register

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | ×   | ×   | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |

| EV5 | EV4 | EV3 | EV2 | EV1 | EV0 | Reference voltage parameter (a) |
|-----|-----|-----|-----|-----|-----|---------------------------------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0                               |
| 0   | 0   | 0   | 0   | 0   | 1   | 1                               |
| :   | :   | :   | :   | :   | :   | :                               |
| :   | :   | :   | :   | :   | :   | :                               |
| 1   | 1   | 1   | 1   | 1   | 0   | 62                              |
| 1   | 1   | 1   | 1   | 1   | 1   | 63                              |

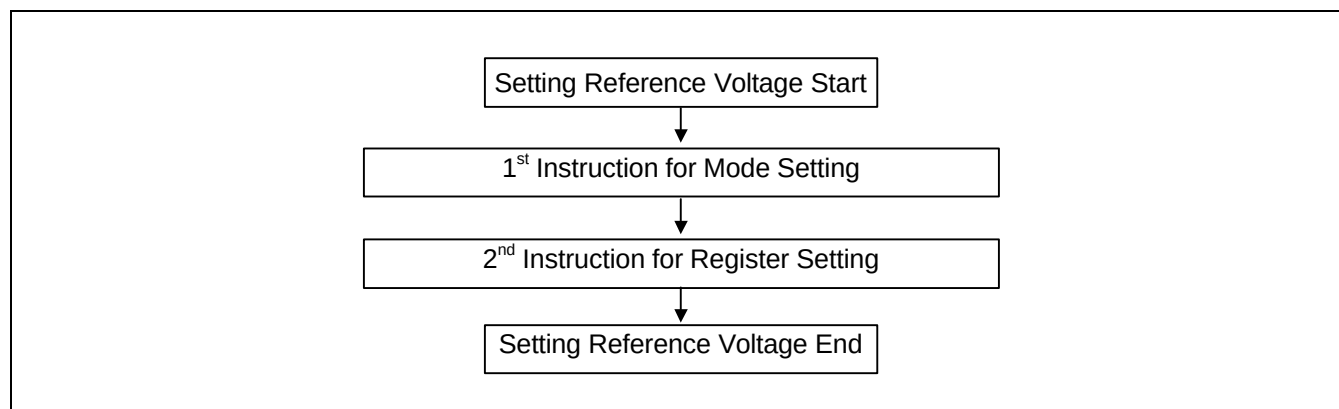


Figure 32. Sequence for Setting the Electronic Volume

**Select LCD Bias**

Selects LCD bias ratio of the voltage required for driving the LCD.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 1   | 0   | 1   | 0   | B2  | B1  | B0  |

| B2 | B1 | B0 | LCD bias |
|----|----|----|----------|
| 0  | 0  | 0  | 1/5      |
| 0  | 0  | 1  | 1/6      |
| 0  | 1  | 0  | 1/7      |
| 0  | 1  | 1  | 1/8      |
| 1  | 0  | 0  | 1/9      |
| 1  | 0  | 1  | 1/10     |
| 1  | 1  | 0  | 1/11     |
| 1  | 1  | 1  | 1/12     |

**SHL Select**

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 0   | 0   | SHL | ×   | ×   | ×   |

× : Don't care

SHL = 0: normal direction (COM0 → COM127)

SHL = 1: reverse direction (COM127 → COM0)

**ADC Select**

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 0   | 0   | 0   | 0   | ADC |

ADC = 0: normal direction (SEG0 → SEG127)

ADC = 1: reverse direction (SEG127 → SEG0)

**Oscillator ON Start**

This instruction enables the built-in oscillator circuit.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 0   | 1   | 0   | 1   | 1   |

**Power Save**

The KS0741 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

**Set Power Save Mode**

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 0   | 1   | 0   | 0   | P   |

P = 0: normal mode

P = 1: sleep mode

**Release Power Save Mode**

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 1   | 0   | 0   | 0   | 0   | 1   |

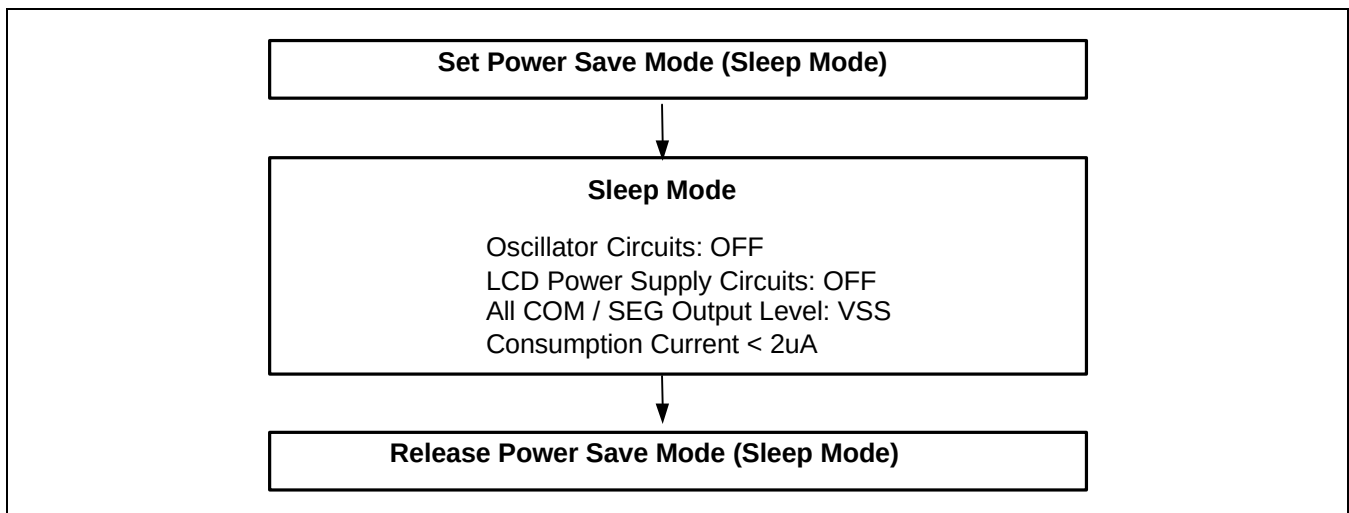


Figure 33. Power Save Routine



**Reset**

This instruction Resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 1   | 0   | 0   | 0   | 1   | 0   |

**Set Data Direction & Display Data Length (3-Pin SPI Mode)**

Consists of 2 bytes instruction.

This command is used in 3-Pin SPI mode only(PS0 = "L" and PS1 = "L"). It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When RS is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.

**The 1<sup>st</sup> Instruction: Set Data Direction (Only Write Mode)**

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| x  | x  | 1   | 1   | 1   | 0   | 1   | 0   | 0   | 0   |

**The 2<sup>nd</sup> Instruction: Set Display Data Length (DDL) Register**

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| x  | x  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Display Data Length |
|----|----|----|----|----|----|----|----|---------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1                   |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 2                   |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 3                   |
| :  | :  | :  | :  | :  | :  | :  | :  | :                   |
| 1  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 254                 |
| 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 255                 |
| 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 256                 |

**NOP**

No operation

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 1   | 0   | 0   | 0   | 1   | 1   |

**Test Instruction**

This instruction is for testing IC. Please do not use it.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 1   | 1   | ×   | ×   | ×   | ×   |

**Set PWM & FRC mode**

Selects 3/4 FRC and 9 / 12 / 15 PWM

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1  | DB0  |
|----|----|-----|-----|-----|-----|-----|-----|------|------|
| 0  | 0  | 1   | 0   | 0   | 1   | 0   | FRC | PWM1 | PWM0 |

| FRC | PWM1 | PWM0 | Status of PWM & FRC |
|-----|------|------|---------------------|
| 0   |      |      | 4FRC                |
| 1   |      |      | 3FRC                |
|     | 0    | 0    | 9PWM                |
|     | 0    | 1    | 9PWM                |
|     | 1    | 0    | 12PWM               |
|     | 1    | 1    | 15PWM               |

### Set Gray Scale Mode & Register

Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.

#### – Set Gray Scale Mode

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 0   | 0   | 1   | GM2 | GM1 | GM0 |

| GM2 | GM1 | GM0 | Description                                                                    |
|-----|-----|-----|--------------------------------------------------------------------------------|
| 0   | 0   | 0   | In case of setting white mode and 1 <sup>st</sup> / 2 <sup>nd</sup> frame      |
| 0   | 0   | 1   | In case of setting white mode and 3 <sup>rd</sup> / 4 <sup>th</sup> frame      |
| 0   | 1   | 0   | In case of setting light gray mode and 1 <sup>st</sup> / 2 <sup>nd</sup> frame |
| 0   | 1   | 1   | In case of setting light gray mode and 3 <sup>rd</sup> / 4 <sup>th</sup> frame |
| 1   | 0   | 0   | In case of setting dark gray mode and 1 <sup>st</sup> / 2 <sup>nd</sup> frame  |
| 1   | 0   | 1   | In case of setting dark gray mode and 3 <sup>rd</sup> / 4 <sup>th</sup> frame  |
| 1   | 1   | 0   | In case of setting black mode and 1 <sup>st</sup> / 2 <sup>nd</sup> frame      |
| 1   | 1   | 1   | In case of setting black mode and 3 <sup>rd</sup> / 4 <sup>th</sup> frame      |

#### – Set Gray Scale Register

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | GB3 | GB2 | GB1 | GB0 | GA3 | GA2 | GA1 | GA0 |
| 0  | 0  | GD3 | GD2 | GD1 | GD0 | GC3 | GC2 | GC1 | GC0 |

| GA3, GB3, GC3, GD3 | GA2, GB2, GC2, GD2 | GA1, GB1, GC1, GD1 | GA0, GB0, GC0, GD0 | Pulse width (9PWM) | Pulse width (12PWM) | Pulse width (15PWM) |
|--------------------|--------------------|--------------------|--------------------|--------------------|---------------------|---------------------|
| 0                  | 0                  | 0                  | 0                  | 0/9                | 0/12                | 0/15                |
| 0                  | 0                  | 0                  | 1                  | 1/9                | 1/12                | 1/15                |
| :                  | :                  | :                  | :                  | :                  | :                   | :                   |
| 1                  | 0                  | 0                  | 1                  | 9/9                | 9/12                | 9/15                |
| 1                  | 0                  | 1                  | 0                  | 0/9                | 10/12               | 10/15               |
| 1                  | 0                  | 1                  | 1                  | 0/9                | 11/12               | 11/15               |
| 1                  | 1                  | 0                  | 0                  | 0/9                | 12/12               | 12/15               |
| 1                  | 1                  | 0                  | 1                  | 0/9                | 0/12                | 13/15               |
| 1                  | 1                  | 1                  | 0                  | 0/9                | 0/12                | 14/15               |
| 1                  | 1                  | 1                  | 1                  | 0/9                | 0/12                | 15/15               |

\* GA3=WA3,LA3,DA3,BA3 GA2=WA2,LA2,DA2,BA2 GA1=WA1,LA1,DA1,BA1 GA0=WA0,LA0,DA0,BA0  
 GB3=WB3,LB3,DB3,BB3 GA2=WB2,LB2,DB2,BB2 GA1=WB1,LB1,DB1,BB1 GA0=WB0,LB0,DB0,BB0  
 GC3=WC3,LC3,DC3,BC3 GA2=WC2,LC2,DC2,BC2 GA1=WC1,LC1,DC1,BC1 GA0=WC0,LC0,DC0,BC0  
 GD3=WD3,LD3,DD3,BD3 GA2=WD2,LD2,DD2,BD2 GA1=WD1,LD1,DD1,BD1 GA0=WD0,LD0,DD0,BD0

## Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

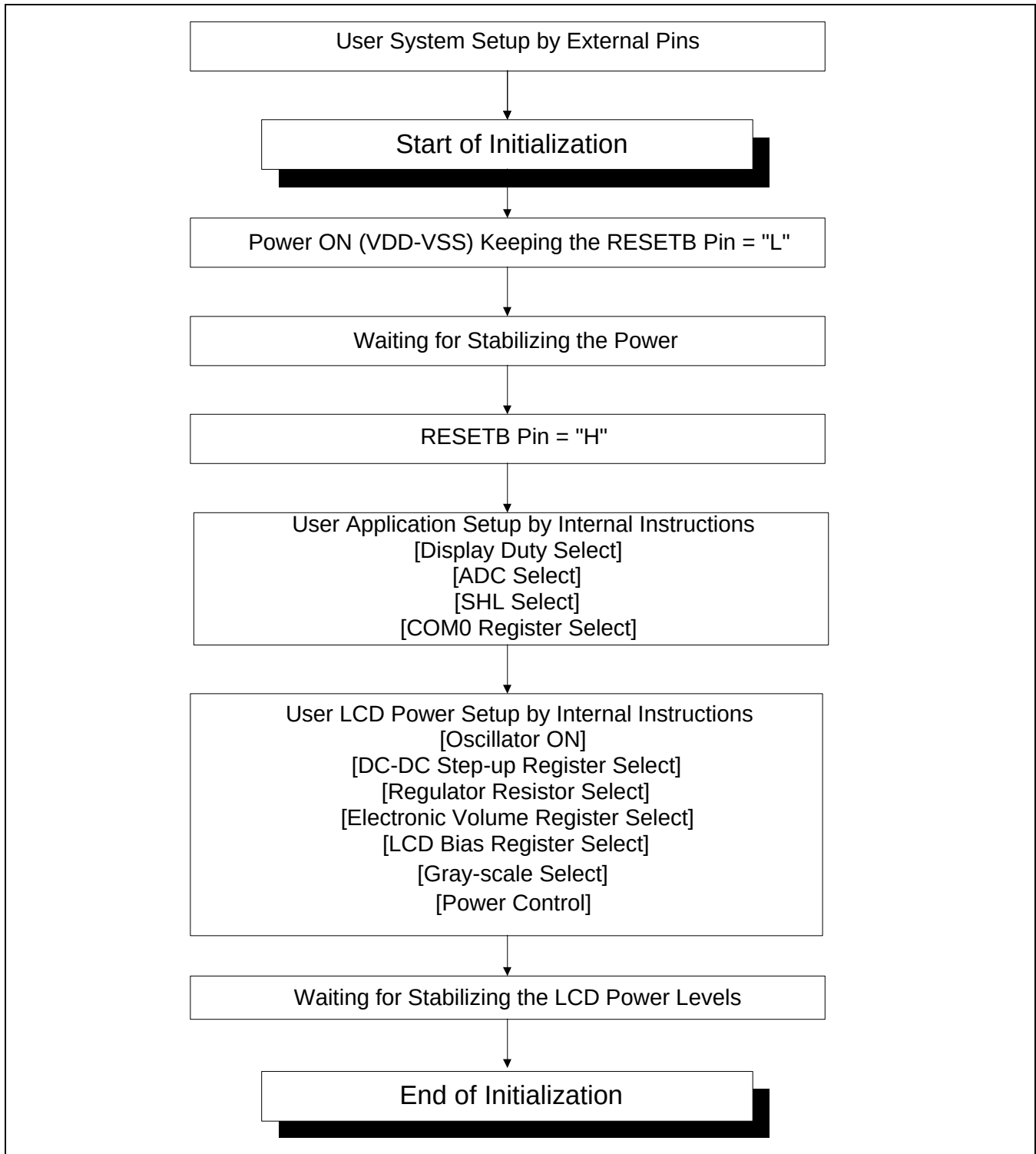
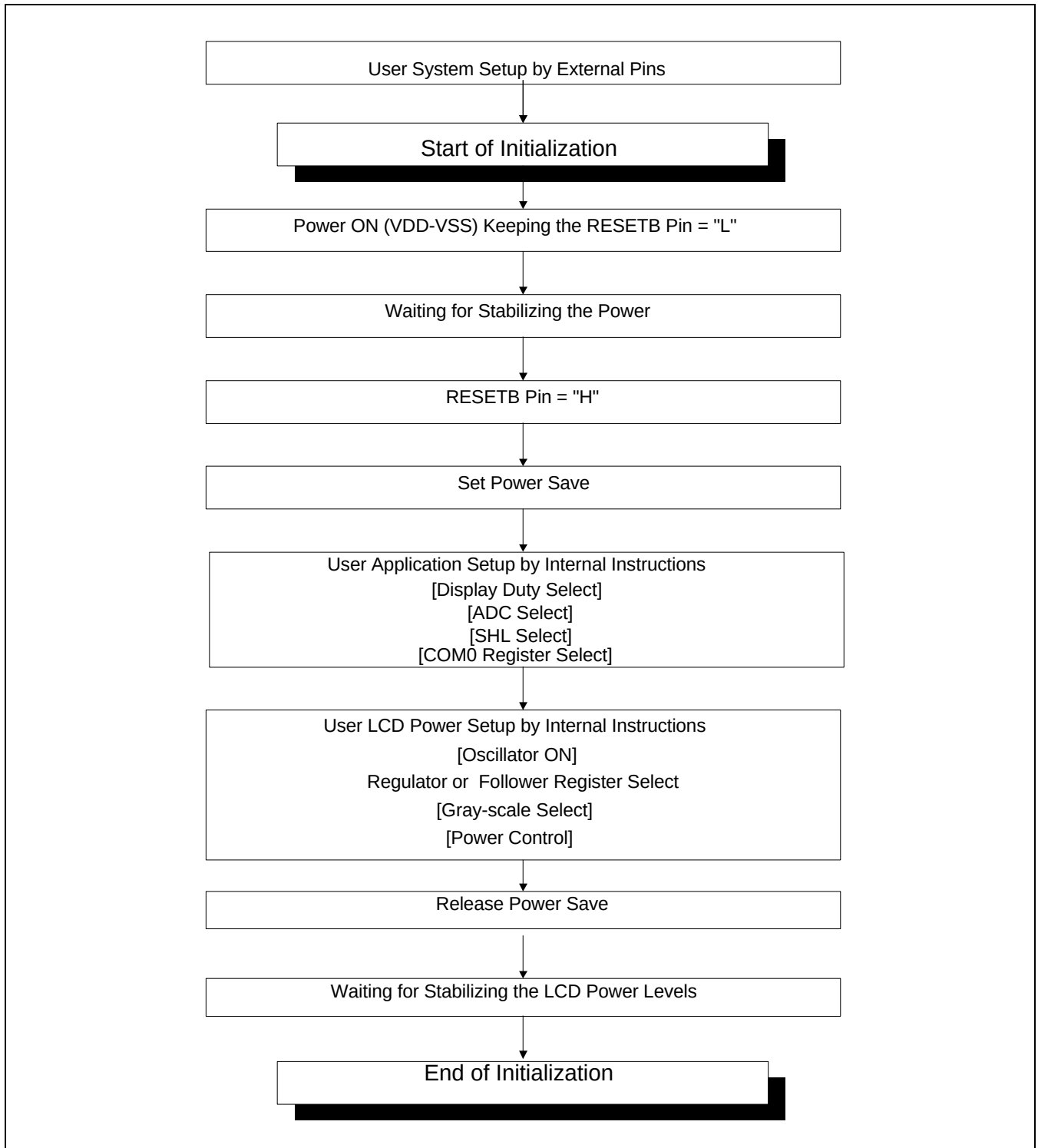


Figure 34. Initializing with the Built-in Power Supply Circuits

**Referential Instruction Setup Flow: Initializing without the built-in Power Supply Circuits****Figure 35. Initializing without the Built-in Power Supply Circuits**

## Referential Instruction Setup Flow: Data Displaying

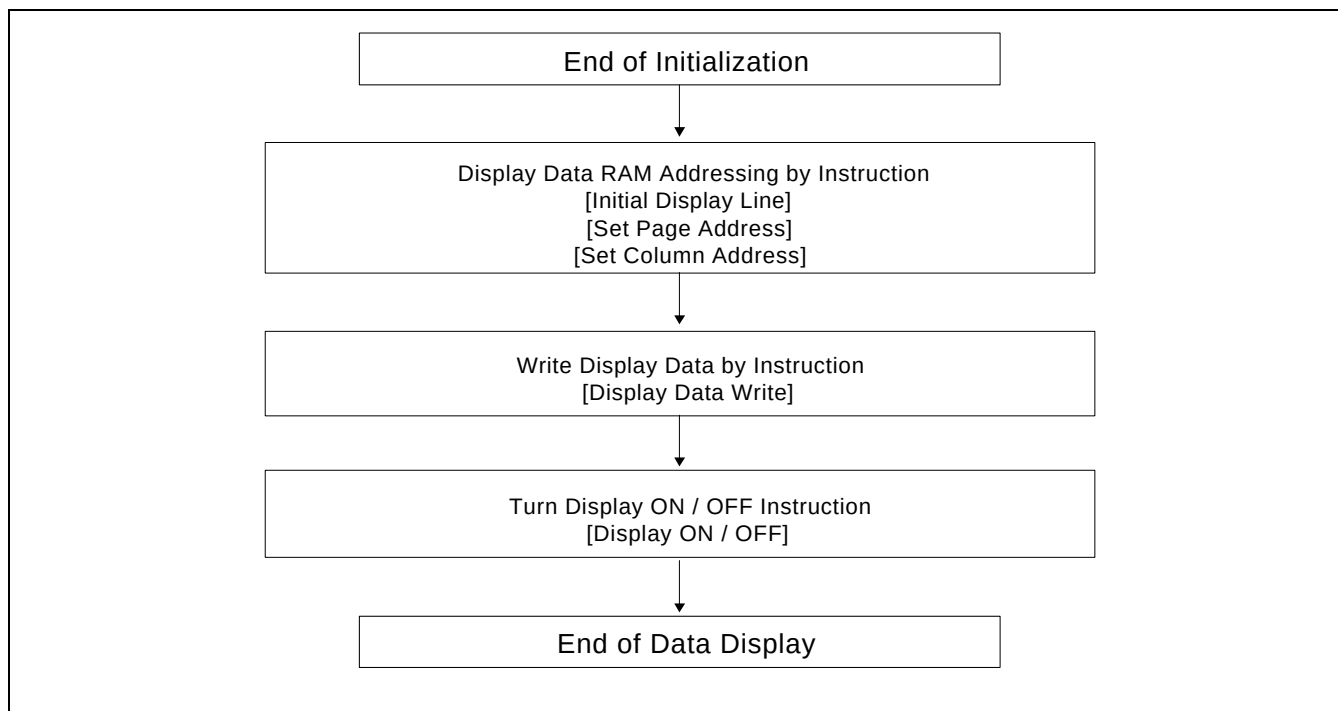


Figure 36. Data Displaying

## Referential Instruction Setup Flow: Power OFF

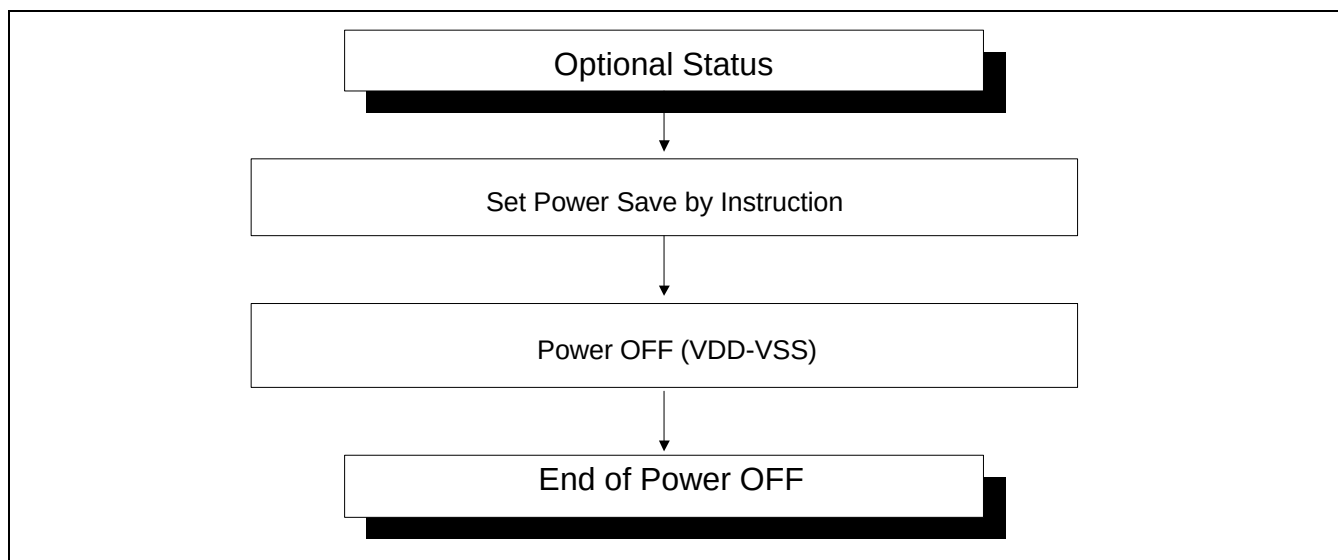
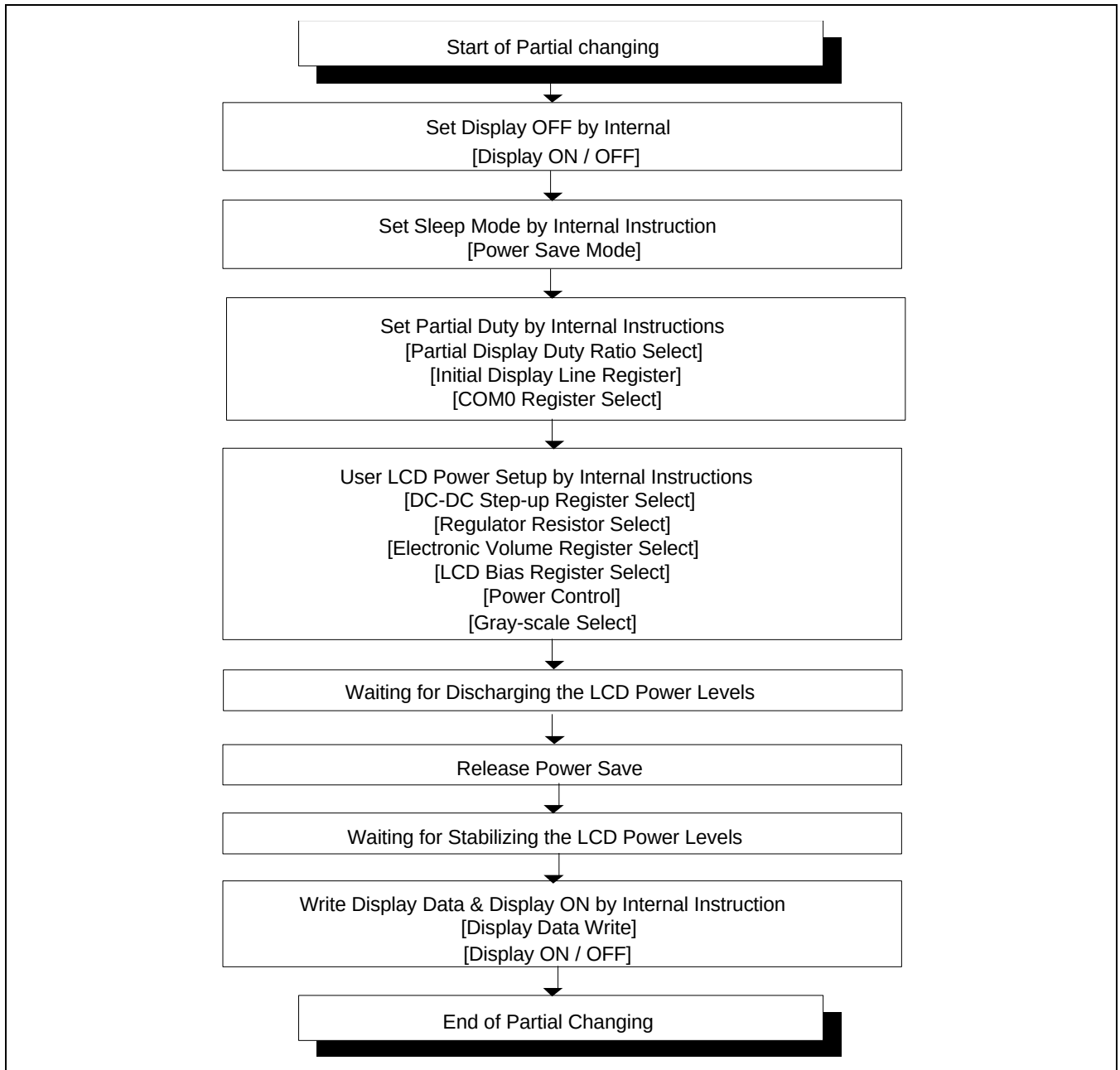


Figure 37. Power OFF

**Referential Instruction Setup Flow: Partial Duty Changing****Figure 38. Partial Duty Changing**

## SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Table 18. Absolute Maximum Ratings

(V<sub>SS</sub> = 0V)

| Parameter                   | Symbol                                                            | Rating                        | Unit |
|-----------------------------|-------------------------------------------------------------------|-------------------------------|------|
| Supply voltage range        | V <sub>DD</sub>                                                   | - 0.3 ~ + 7.0                 | V    |
|                             | V <sub>0</sub> , V <sub>OUT</sub>                                 | - 0.3 ~ + 17.0                | V    |
|                             | V <sub>1</sub> , V <sub>2</sub> , V <sub>3</sub> , V <sub>4</sub> | - 0.3 ~ V <sub>0</sub> + 0.3  | V    |
| External reference voltage  | V <sub>EXT</sub>                                                  | +0.3 ~ V <sub>DD</sub>        |      |
| Input voltage range         | V <sub>IN</sub>                                                   | - 0.3 ~ V <sub>DD</sub> + 0.3 | V    |
| Operating temperature range | T <sub>OPR</sub>                                                  | - 40 ~ + 85                   | °C   |
| Storage temperature range   | T <sub>STR</sub>                                                  | - 55 ~ + 125                  | °C   |

#### NOTES:

1. V<sub>DD</sub>, V<sub>0</sub>, V<sub>OUT</sub>, V<sub>1</sub> to V<sub>4</sub> and V<sub>EXT</sub> are based on V<sub>SS</sub> = 0V.
2. Voltages V<sub>0</sub> ≥ V<sub>1</sub> ≥ V<sub>2</sub> ≥ V<sub>3</sub> ≥ V<sub>4</sub> ≥ V<sub>SS</sub> must always be satisfied. (V<sub>LCD</sub> = V<sub>0</sub> - V<sub>SS</sub>)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently.  
It is desirable to use this LSI under electrical characteristic conditions during general operation.  
Otherwise, this LSI may malfunction or reduced LSI reliability may result.



## DC CHARACTERISTICS

Table 19. DC Characteristics

(V<sub>SS</sub> = 0V, V<sub>DD</sub> = 1.8 to 3.3V, T<sub>a</sub> = -40 to 85°C)

| Item                                   | Symbol           | Condition                                                  | Min.                     | Typ.               | Max.               | Unit | Pin used                                |
|----------------------------------------|------------------|------------------------------------------------------------|--------------------------|--------------------|--------------------|------|-----------------------------------------|
| Operating voltage (1)                  | V <sub>DD</sub>  |                                                            | 1.8                      | -                  | 3.3                | V    | V <sub>DD</sub> *1                      |
| Operating voltage (2)                  | V <sub>O</sub>   |                                                            | 4.0                      | -                  | 15.0               | V    | V <sub>O</sub> *2                       |
| Input voltage                          | High             | V <sub>IH</sub>                                            | 0.8V <sub>DD</sub>       | -                  | V <sub>DD</sub>    | V    | *3                                      |
|                                        | Low              | V <sub>IL</sub>                                            | V <sub>SS</sub>          | -                  | 0.2V <sub>DD</sub> |      |                                         |
| Output voltage                         | High             | V <sub>OH</sub>                                            | I <sub>OH</sub> = -0.5mA | 0.8V <sub>DD</sub> | V <sub>DD</sub>    | V    | *4                                      |
|                                        | Low              | V <sub>OL</sub>                                            | I <sub>OL</sub> = 0.5mA  | V <sub>SS</sub>    | 0.2V <sub>DD</sub> |      |                                         |
| Input leakage current                  | I <sub>IL</sub>  | V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>       | - 1.0                    | -                  | + 1.0              | μA   | *3                                      |
| Output leakage current                 | I <sub>OZ</sub>  | V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>       | - 3.0                    | -                  | + 3.0              | μA   | *5                                      |
| LCD driver ON resistance               | R <sub>ON</sub>  | T <sub>a</sub> = 25°C, V <sub>O</sub> = 8V                 | -                        | 2.0                | 3.0                | kΩ   | SEg <sub>n</sub><br>COM <sub>n</sub> *6 |
| Operating frequency                    | f <sub>FR</sub>  | T <sub>a</sub> = 25°C<br>1/128 Duty, 9 PWM<br>REXT = TBDkΩ | 70                       | 85                 | 100                | Hz   | *7                                      |
| Voltage converter<br>Input voltage     | V <sub>CI</sub>  | × 3                                                        | 1.8                      | -                  | 5.0                | V    | V <sub>CI</sub>                         |
|                                        |                  | × 4                                                        | 1.8                      | -                  | 3.75               |      |                                         |
|                                        |                  | × 5                                                        | 1.8                      | -                  | 3.0                |      |                                         |
|                                        |                  | × 6                                                        | 1.8                      | -                  | 2.5                |      |                                         |
| Voltage converter<br>output voltage    | V <sub>OUT</sub> | ×3 / ×4 / ×5 / ×6<br>voltage conversion<br>(no-load )      | 95                       | 99                 | -                  | %    | V <sub>OUT</sub>                        |
| Voltage regulator<br>operating voltage | V <sub>OUT</sub> |                                                            | 5.4                      | -                  | 15.0               | V    | V <sub>OUT</sub>                        |
| Voltage follower<br>operating voltage  | V <sub>O</sub>   |                                                            | 4.0                      | -                  | 15.0               | V    | V <sub>O</sub> *8                       |
| Reference voltage                      | V <sub>REF</sub> | T <sub>a</sub> = 25°C                                      | 2.04                     | 2.10               | 2.16               | V    | *9                                      |

**Dynamic Current Consumption (1) when An External Power Supply is used.****Table 20. Dynamic Current 1 (External Power)**(V<sub>DD</sub> = 3.0V, Ta = 25°C)

| Item                            | Symbol           | Condition                                                      | Min | Typ | Max | Unit | Pin used |
|---------------------------------|------------------|----------------------------------------------------------------|-----|-----|-----|------|----------|
| Dynamic current consumption (1) | I <sub>DD1</sub> | V0-Vss = 11.0V, duty = 1/128<br>(Display Off)                  | -   | -   | TBD | μA   | *10      |
|                                 |                  | V0-Vss = 11.0V, duty = 1/128<br>(Display On , Checker Pattern) | -   | -   | TBD | μA   | *10      |

**Dynamic Current Consumption (2) when The Internal Power Supply is ON****Table 21. Dynamic Current 2 (Internal Power)**(V<sub>DD</sub> = 3.0V, Ta = 25°C)

| Item                            | Symbol           | Condition                                                                                     | Min. | Typ. | Max. | Unit | Pin used |
|---------------------------------|------------------|-----------------------------------------------------------------------------------------------|------|------|------|------|----------|
| Dynamic current consumption (2) | I <sub>DD2</sub> | V0 - Vss = 12.0V, x5 boosting,<br>duty = 1/128, normal mode<br>(Display Off)                  | -    | -    | TBD  | μA   | *10      |
|                                 |                  | V0 - Vss = 12.0V, x5 boosting,<br>duty = 1/128, normal mode<br>(Display On , Checker Pattern) | -    | -    | TBD  | μA   | *10      |

**Current Consumption during Power Save Mode****Table 22. Power Save Mode Current**(V<sub>DD</sub> = 3.0V, Ta = 25°C)

| Item               | Symbol            | Condition    | Min. | Typ. | Max. | Unit | Pin used |
|--------------------|-------------------|--------------|------|------|------|------|----------|
| Sleep mode current | I <sub>DDs1</sub> | During sleep | -    | -    | TBD  | μA   | *10      |

**Table 23. The Relationship between Oscillation Frequency and Frame Frequency**

| Duty ratio | Item                               | f <sub>CL</sub>     | f <sub>osc</sub>              |
|------------|------------------------------------|---------------------|-------------------------------|
| 1/N        | On-chip oscillator circuit is used | f <sub>FR</sub> × N | f <sub>FR</sub> × PWM × 2 × N |

(f<sub>osc</sub>: oscillation frequency, f<sub>CL</sub>: display clock frequency, f<sub>FR</sub>: frame frequency, N = 16 to 129)

[\* Remark Solves]

- \*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
- \*2. In case of external power supply is applied.
- \*3. CSB, RS, DB0 to DB7, E\_RD, RW\_WR, RESETB, PS1, PS0, INTRs, HPMB and REF
- \*4. DB0 to DB7
- \*5. Applies when the DB0 to DB7 pins are in high impedance.
- \*6. Resistance value when -0.1[mA] is applied during the ON status of the output pin SEGn or COMn.  
 $R_{ON} [k\Omega] = \Delta V[V] / 0.1[mA]$  ( $\Delta V$  : voltage change when -0.1[mA] is applied in the ON status.)
- \*7. See Table 23 for the relationship between oscillation frequency and frame frequency.
- \*8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
- \*9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
- \*10. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.  
 The current consumption, when the built-in power supply circuit is ON or OFF.  
 The current flowing through voltage regulation resistors(Rb and Ra) is not included.  
 It does not include the current of the LCD panel capacity, wiring capacity, etc.

## AC CHARACTERISTICS

### Read / Write Characteristics (8080-series MPU)

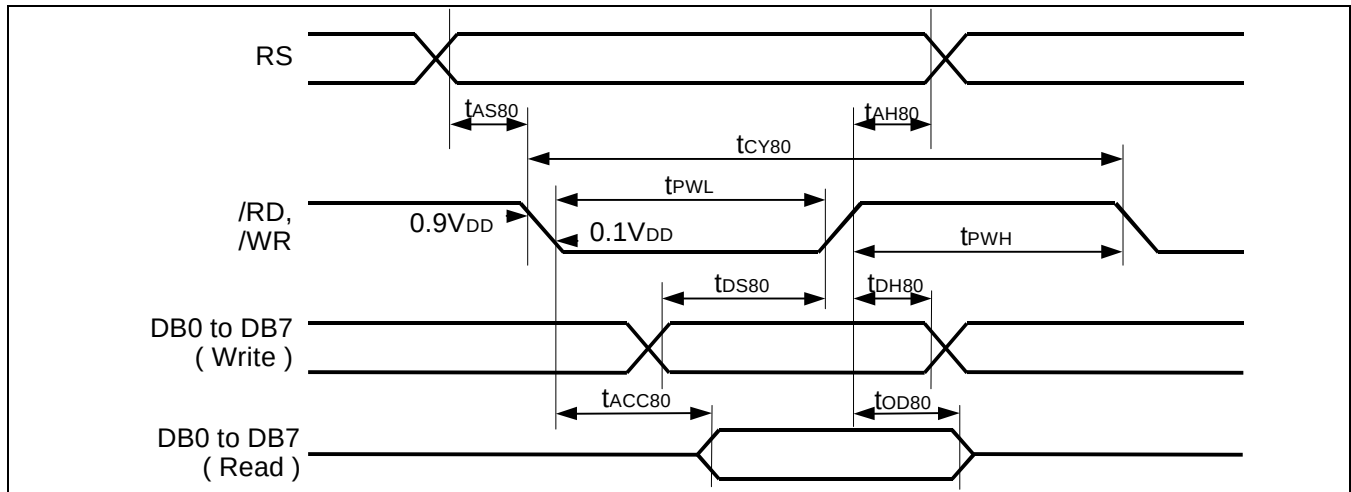


Figure 39. Read / Write Characteristics (8080-series MPU)

( $V_{DD} = 1.8V$ ,  $T_a = -40 \sim +85^{\circ}C$ )

| Item                | Signal           | Symbol      | Condition   | Min. | Max. | Unit |
|---------------------|------------------|-------------|-------------|------|------|------|
| Address setup time  | RS               | $t_{AS80}$  |             | 0    | 25   | ns   |
| Address hold time   |                  | $t_{AH80}$  |             | 0    | -    |      |
| System cycle time   |                  | $t_{CY80}$  |             | 330  | -    | ns   |
| Pulse width low     | /WR<br>/RD       | $t_{PWL}$   |             | 60   | -    | ns   |
| Pulse width high    |                  | $t_{PWH}$   |             | 60   | -    |      |
| Data setup time     | DB0<br>to<br>DB7 | $t_{DS80}$  | CL = 100 pF | 40   | -    | ns   |
| Data hold time      |                  | $t_{DH80}$  |             | 10   | -    |      |
| Read access time    |                  | $t_{ACC80}$ |             | 15   | -    | ns   |
| Output disable time |                  | $t_{OD80}$  |             | 10   | 50   |      |

( $V_{DD} = 2.7V$ ,  $T_a = -40 \sim +85^{\circ}C$ )

| Item                | Signal           | Symbol      | Condition   | Min. | Max. | Unit |
|---------------------|------------------|-------------|-------------|------|------|------|
| Address setup time  | RS               | $t_{AS80}$  |             | 0    | 25   | ns   |
| Address hold time   |                  | $t_{AH80}$  |             | 0    | -    |      |
| System cycle time   |                  | $t_{CY80}$  |             | 166  | -    | ns   |
| Pulse width low     | /WR<br>/RD       | $t_{PWL}$   |             | 50   | -    | ns   |
| Pulse width high    |                  | $t_{PWH}$   |             | 50   | -    |      |
| Data setup time     | DB0<br>to<br>DB7 | $t_{DS80}$  | CL = 100 pF | 30   | -    | ns   |
| Data hold time      |                  | $t_{DH80}$  |             | 5    | -    |      |
| Read access time    |                  | $t_{ACC80}$ |             | 15   | -    | ns   |
| Output disable time |                  | $t_{OD80}$  |             | 10   | 50   |      |

NOTE: \*1. The input signal rise time and fall time ( $t_r$ ,  $t_f$ ) is specified at 15 ns or less.  
 $(t_r + t_f) < (t_{CY80} - t_{PWLW} - t_{PWHW})$  for write,  $(t_r + t_f) < (t_{CY80} - t_{PWLW} - t_{PWHW})$  for read

## Read / Write Characteristics (6800-series Microprocessor)

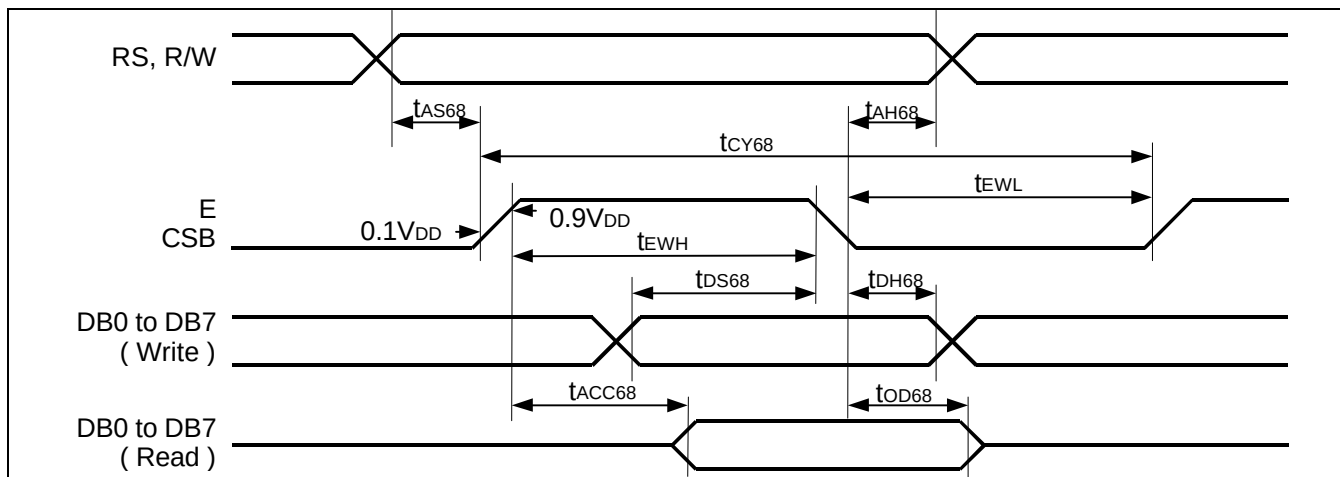


Figure 40. Read / Write Characteristics (6800-series Microprocessor)

(V<sub>DD</sub> = 1.8V, Ta = -40 ~ +85°C)

| Item                | Signal     | Symbol             | Condition               | Min. | Max. | Unit |
|---------------------|------------|--------------------|-------------------------|------|------|------|
| Address setup time  | RS         | t <sub>AS68</sub>  |                         | 0    | 25   | ns   |
| Address hold time   | RW         | t <sub>AH68</sub>  |                         | 0    | -    | ns   |
| System cycle time   |            | t <sub>CY68</sub>  |                         | 330  | -    | ns   |
| Enable width high   | E_RD       | t <sub>EWL</sub>   |                         | 60   | -    | ns   |
| Enable width low    | (E)        | t <sub>EWL</sub>   |                         | 60   | -    | ns   |
| Data setup time     | DB0 to DB7 | t <sub>DS68</sub>  |                         | 40   | -    | ns   |
| Data hold time      |            | t <sub>DH68</sub>  |                         | 10   | -    | ns   |
| Read access time    |            | t <sub>ACC68</sub> | C <sub>L</sub> = 100 pF | 15   | -    | ns   |
| Output disable time |            | t <sub>OD68</sub>  |                         | 10   | 50   | ns   |

(V<sub>DD</sub> = 2.7V, Ta = -40 ~ +85°C)

| Item                | Signal     | Symbol             | Condition               | Min. | Max. | Unit |
|---------------------|------------|--------------------|-------------------------|------|------|------|
| Address setup time  | RS         | t <sub>AS68</sub>  |                         | 0    | 25   | ns   |
| Address hold time   | RW         | t <sub>AH68</sub>  |                         | 0    | -    | ns   |
| System cycle time   |            | t <sub>CY68</sub>  |                         | 166  | -    | ns   |
| Enable width high   | E_RD       | t <sub>EWL</sub>   |                         | 50   | -    | ns   |
| Enable width low    | (E)        | t <sub>EWL</sub>   |                         | 50   | -    | ns   |
| Data setup time     | DB0 to DB7 | t <sub>DS68</sub>  |                         | 30   | -    | ns   |
| Data hold time      |            | t <sub>DH68</sub>  |                         | 5    | -    | ns   |
| Read access time    |            | t <sub>ACC68</sub> | C <sub>L</sub> = 100 pF | 15   | -    | ns   |
| Output disable time |            | t <sub>OD68</sub>  |                         | 10   | 50   | ns   |

NOTE: \*1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

(tr + tf) < (t<sub>CY68</sub> - t<sub>EWLH</sub> - t<sub>EWLW</sub>) for write, (tr + tf) < (t<sub>CY68</sub> - t<sub>EWHR</sub> - t<sub>EWLR</sub>) for read

## Serial Interface Characteristics

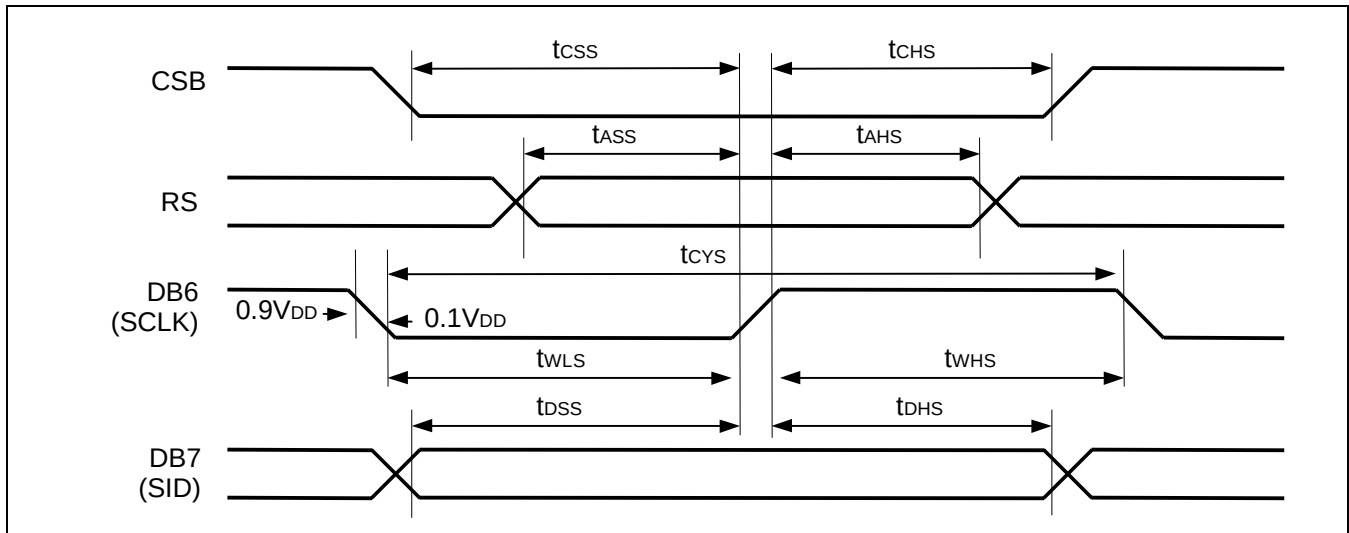


Figure 41. Serial Interface Characteristics

(V<sub>DD</sub> = 1.8V, Ta = -40 ~ +85°C)

| Item                                                                | Signal     | Symbol                              | Condition | Min.                  | Max.        | Unit |
|---------------------------------------------------------------------|------------|-------------------------------------|-----------|-----------------------|-------------|------|
| Serial clock cycle<br>SCLK high pulse width<br>SCLK low pulse width | DB6 (SCLK) | $t_{CYS}$<br>$t_{WHS}$<br>$t_{WLS}$ |           | 111<br>60<br>60       | -<br>-<br>- | ns   |
| Address setup time<br>Address hold time                             | RS         | $t_{ASS}$<br>$t_{AHS}$              |           | 60<br>60              | -<br>-      | ns   |
| Data setup time<br>Data hold time                                   | DB7 (SID)  | $t_{DSS}$<br>$t_{DHS}$              |           | 60<br>60              | -<br>-      | ns   |
| CSB setup time<br>CSB hold time                                     | CSB        | $t_{CSS}$<br>$t_{CHS}$              |           | 60<br>$1/2 * t_{CYS}$ | -<br>-      | ns   |

(V<sub>DD</sub> = 2.7V, Ta = -40 ~ +85°C)

| Item                                                                | Signal     | Symbol                              | Condition | Min.                  | Max.        | Unit |
|---------------------------------------------------------------------|------------|-------------------------------------|-----------|-----------------------|-------------|------|
| Serial clock cycle<br>SCLK high pulse width<br>SCLK low pulse width | DB6 (SCLK) | $t_{CYS}$<br>$t_{WHS}$<br>$t_{WLS}$ |           | 58.8<br>30<br>30      | -<br>-<br>- | ns   |
| Address setup time<br>Address hold time                             | RS         | $t_{ASS}$<br>$t_{AHS}$              |           | 30<br>30              | -<br>-      | ns   |
| Data setup time<br>Data hold time                                   | DB7 (SID)  | $t_{DSS}$<br>$t_{DHS}$              |           | 30<br>30              | -<br>-      | ns   |
| CSB setup time<br>CSB hold time                                     | CSB        | $t_{CSS}$<br>$t_{CHS}$              |           | 30<br>$1/2 * t_{CYS}$ | -<br>-      | ns   |

NOTE: \*1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

## Reset Input Timing

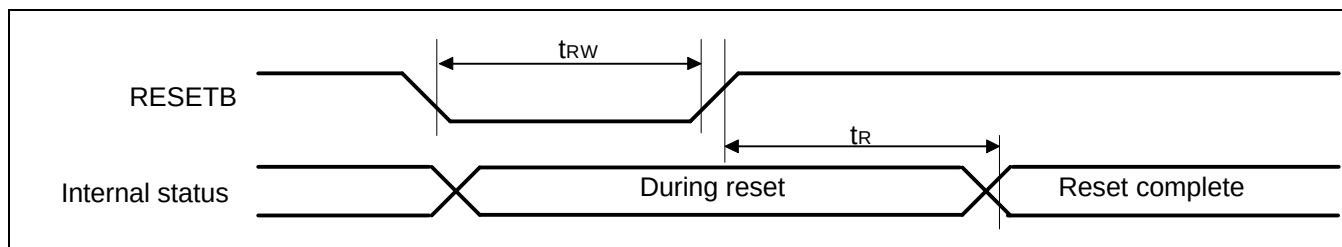


Figure 42. Reset Input Timing

(V<sub>DD</sub> = 1.8 ~ 3.3V, Ta = -40 ~ +85°C)

| Item                  | Signal | Symbol   | Condition | Min. | Max. | Unit |
|-----------------------|--------|----------|-----------|------|------|------|
| Reset low pulse width | RESETB | $t_{RW}$ |           | 1000 | -    | ns   |
| Reset time            | -      | $t_R$    |           | -    | 1000 | ns   |

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS0 = “H”, PS1 = “H”)

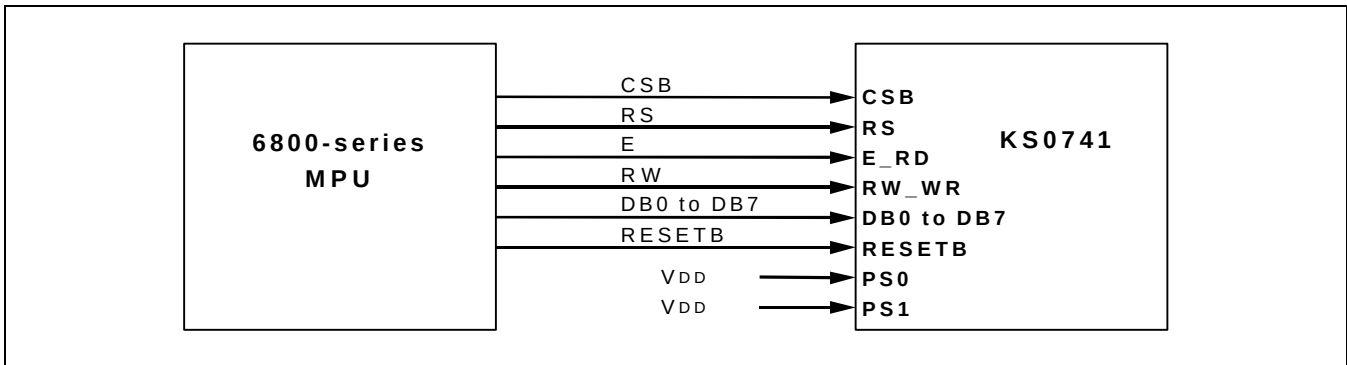


Figure 43. Interfacing with 6800-series (PS0 = “H”, C68 = “H”)

In Case of Interfacing with 8080-series (PS0 = “H”, PS1 = “L”)

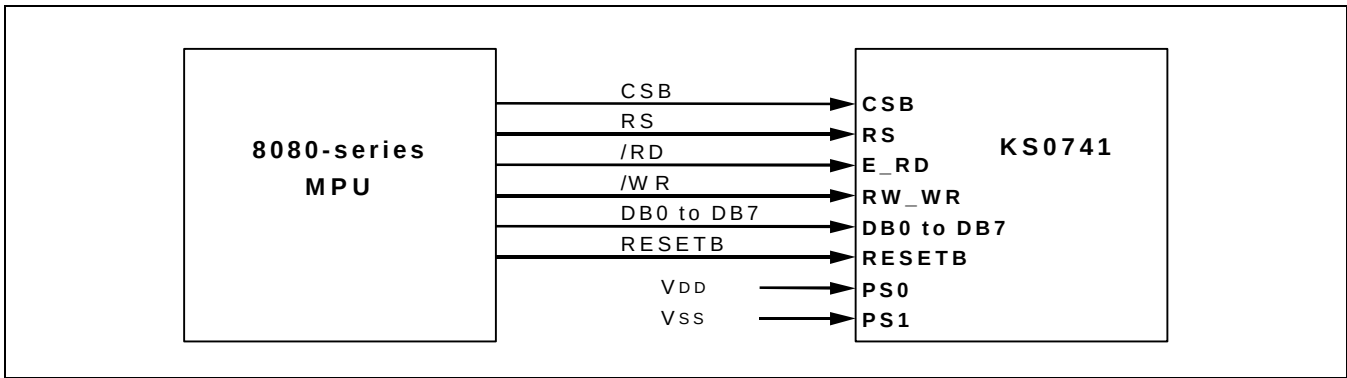


Figure 44. Interfacing with 8080-series (PS0 = “H”, C68 = “L”)



In Case of 4-pin SPI mode (PS0 = "L" , PS1 = "H" )

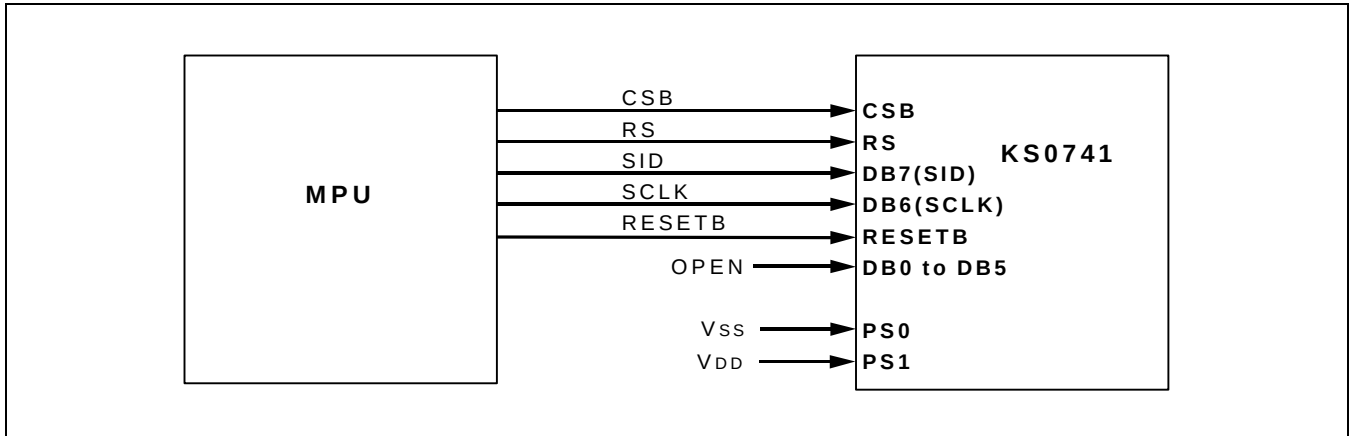


Figure 45. Serial Interface (PS0 = "L", PS1 = "H")

In Case of 3-pin SPI mode (PS0 = "L" , PS1 = "L" )

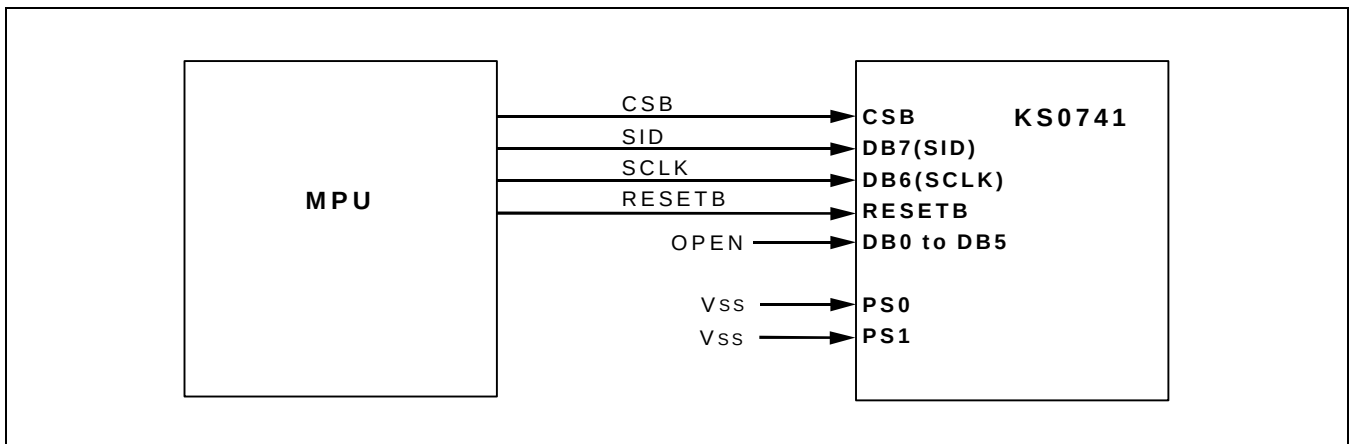


Figure 46. Serial Interface (PS0 = "L", PS1 = "L")

CONNECTIONS BETWEEN KS0741 AND LCD PANEL

Single Chip Configuration (1/129 Duty Configurations)

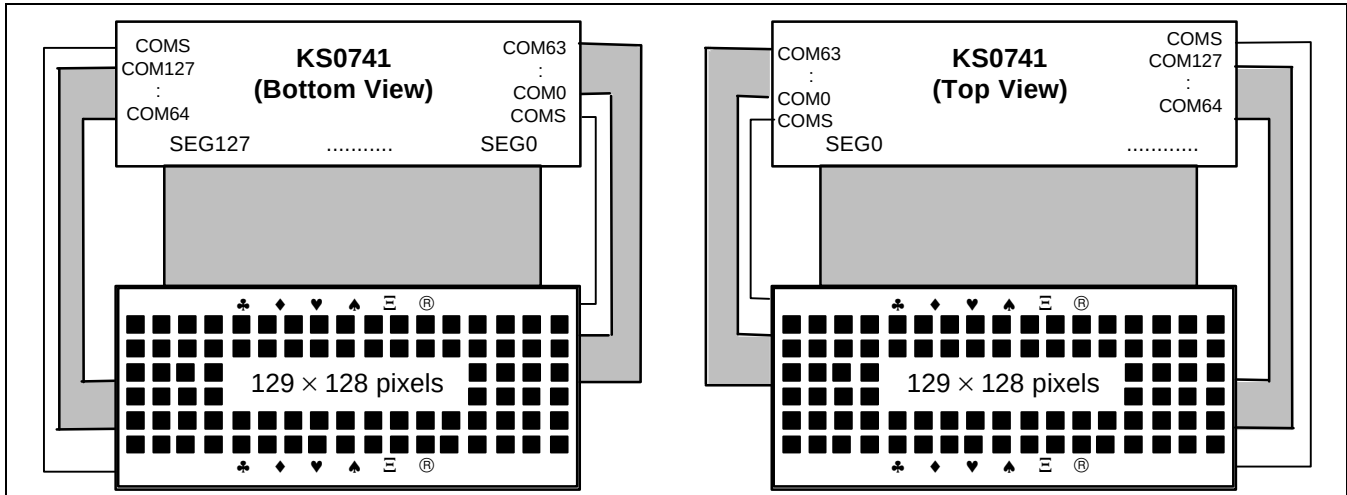


Figure 47. SHL = 0, ADC = 1

Figure 48. SHL = 0, ADC = 0

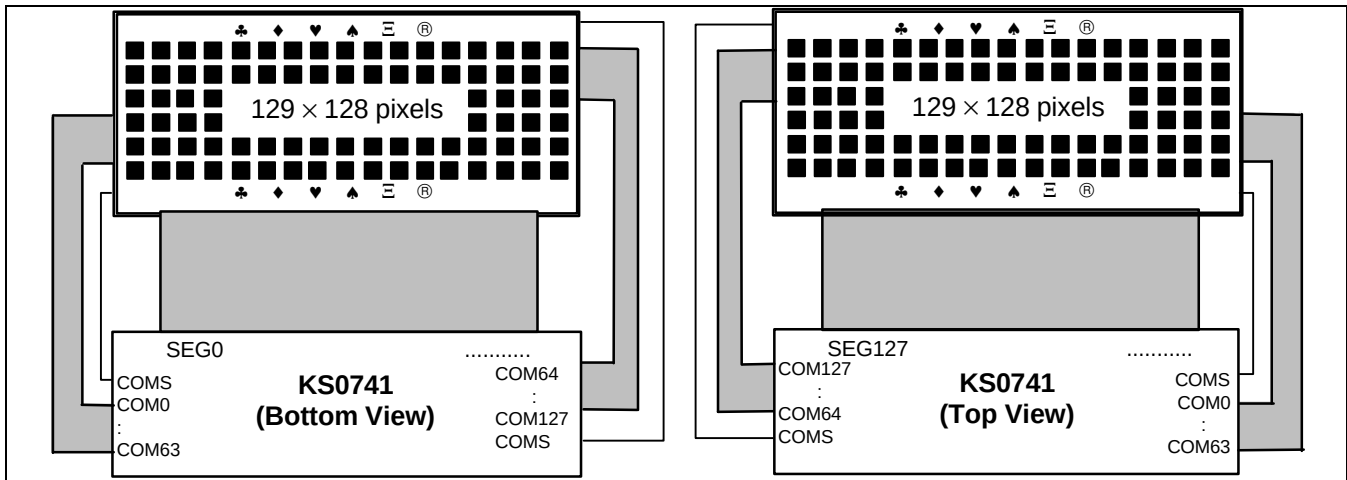


Figure 49. SHL = 1, ADC = 0

Figure 50. SHL = 1, ADC = 1