

## KT8554B/7B

## 1 CHIP CODECS

### INTRODUCTION

The KT8554B/7B are single-chip PCM encoders and decoders (PCM CODECS) and PCM line filters. These devices provide all the functions required to interface a full-duplex voice telephone circuit with a time-division-multiplex (TDM) system.

These devices are designed to perform the transmit encoding and receive decoding as well as the transmit and receive filtering functions in PCM system. They are intended to be used at the analog termination of a PCM line or trunk.

These devices provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signalling and supervision information.

### FEATURES

- Complete CODEC and filtering system
- Meets or exceeds AT&T D3/D4 and CCITT specifications  
 $\mu$ -Law : KT8554B, A-Law : KT8557B
- On-chip auto zero, sample and hold, and precision voltage references
- Low power dissipation : 60mW (operating)  
 3mW (standby)
- $\pm 5V$  operation
- TTL or CMOS compatible
- Automatic power down



### ORDERING INFORMATION

Device	Package	Operating Temperature
KT8554BJ KT8557BJ	16-CERDIP	- 25 ~ 125°C
KT8557BN KT8554BN	16-DIP-300A	- 25 ~ 70°C
KT8554BD KT8557BD	16-SOP-BD300 -SG	- 25 ~ 70°C

### PIN CONFIGURATION

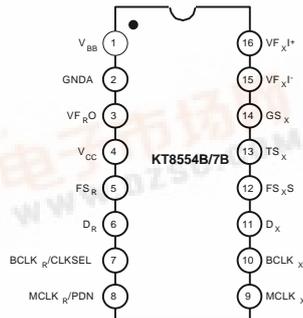


Fig. 1

SAMSUNG

ELECTRONICS

## PIN DESCRIPTION

Pin No	Symbol	Description
1	$V_{BB}$	$V_{BB} = -5V \pm 5\%$ .
2	GNDA	Analog ground.
3	$VF_{R}O$	Analog output of the receive power Amp.
4	$V_{CC}$	$V_{CC} = +5V \pm 5\%$ .
5	$FS_R$	Receive frame sync pulse. 8KHz pulse train.
6	$D_R$	PCM data input.
7	$BCLK_R / CLKSEL$	Logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in normal operation and $BCLK_x$ is used for both TX and RX directions. Alternately direct clock input available, vary from 64KHz to 2.048MHz.
8	$MCLK_R / PDN$	When $MCLK_R$ is connected continuously high, the device is powered down. Normally connected continuously low, $MCLK_x$ is selected for all DAC timing. Alternately direct 1.536MHz/1.544MHz or 2.048MHz clock input available.
9	$MCLK_x$	Must be 1.536MHz/1.544MHz or 2.048MHz.
10	$BCLK_x$	May be vary from 64KHz to 2.048MHz but $BCLK_x$ is externally tied with $MCLK_x$ in normal operation.
11	$D_x$	PCM data output.
12	$FS_x$	TX frame sync pulse. 8KHz pulse train.
13	$\overline{TS}_x$	Changed from high to low during the encoder timeslot. Open drain output.
14	$GS_x$	Analog output of the TX input amplifier. Used to set gain through external resistor.
15	$VF_xI^-$	Inverting input stage of the TX analog signal.
16	$VF_xI^+$	Non-inverting input stage of the TX analog signal.

## ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	$V_{CC}$	7	V
Negative Supply Voltage	$V_{BB}$	- 7	V
Voltage at Any Analog Input or Output	$V_{I(A)}$	$V_{CC} + 0.3$ to $V_{BB} - 0.3$	V
Voltage at Any Digital Input or Output	$V_{I(D)}$	$V_{CC} + 0.3$ to GNDA - 0.3	V
Operating Temperature Range	Ta	- 25 to + 125	°C
Storage Temperature Range	$T_{STG}$	- 65 to + 150	°C
Lead Temperature (Soldering, 10 secs)	$T_{LEAD}$	300	°C

**ELECTRICAL CHARACTERISTICS**

(Unless otherwise noted,  $V_{CC} = 5.0V \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ,  $G_NDA = 0V$ ,  $T_a = 0^\circ C$  to  $70^\circ C$  ; typical characteristics specified at  $V_{CC} = 5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_a = 25^\circ C$  ; all signals referenced to  $G_NDA$ ).

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Power Dissipation</b>						
Power-Down Current	$I_{CC(DOWN)}$	No Load		0.5	1.5	mA
Power-Down Current	$I_{BB(DOWN)}$	No Load		0.05	0.3	mA
Active Current	$I_{CC(A)}$	No Load		6.0	9.0	mA
Active Current	$I_{BB(A)}$	No Load		6.0	9.0	mA
<b>Digital Interface</b>						
Input Low Voltage	$V_{IL}$				0.6	V
Input High Voltage	$V_{IH}$		2.2			V
Input Low Current	$I_{IL}$	$G_NDA \leq V_{IN} \leq V_{IL}$ , all digital inputs	-10		10	$\mu A$
Input High Current	$I_{IH}$	$V_{IH} \leq V_{IN} \leq V_{CC}$	-10		10	$\mu A$
Output Low Voltage	$V_{OL}$	$D_X, I_L = 3.2mA$			0.4	V
		$SIG_R, I_L = 1.0mA$			0.4	V
		$\overline{T}S_X, I_L = 3.2mA, \text{open drain}$			0.4	V
Output High Voltage	$V_{OH}$	$D_X, I_H = -3.2mA$	2.4			V
		$SIG_R, I_H = -1.0mA$	2.4			V
Output Current in High Impedance State (TRI-STATE)	$I_{O(HZ)}$	$D_X, G_NDA \leq V_O \leq V_{CC}$	-10		10	$\mu A$
<b>Analog Interface with Receive Filter</b>						
Output Resistance	$R_O$	Pin $VF_R O$		1	3	$\Omega$
Load Resistance	$R_L$	$VF_R O = \pm 2.5V$	600			$\Omega$
Load Capacitance	$C_L$				500	pF
Output DC Offset Voltage	$V_{OO(RX)}$		-200		200	mV
<b>Analog Interface with Transmit input Amplifier</b>						
Input Leakage Current	$I_{LKG}$	$-2.5V \leq V_S \leq +2.5V, VF_X I + \text{ or } VF_X I -$	-200		200	nA
Input Resistance	$R_I$	$-2.5V \leq V_S \leq +2.5V, VF_X I + \text{ or } VF_X I -$	10			$M\Omega$
Output Resistance	$R_O$	Closed loop, unity gain		1	3	$\Omega$
Load Resistance	$R_L$	$GS_X$	10			$K\Omega$
Load Capacitance	$C_L$	$GS_X$			50	pF
Output Dynamic Range	$V_{OD(TX)}$	$GS_X, R_L \leq 10KW$	$\pm 2.8$			V
Voltage Gain	$G_V$	$VF_X I + \text{ to } GS_X$	5,000			V/V
Unity Gain Bandwidth	BW		1	2		MHz
Offset Voltage	$V_{IO(TX)}$		-20		20	mV
Common-Mode Voltage	$V_{CM(TX)}$	$CMRR_XA > 60dB$	-2.5		2.5	V
Common-Mode Rejection Ratio	CMRR	DC Test	60			dB
Power Supply Rejection Ratio	PSRR	DC Test	60			dB

**TIMING CHARACTERISTICS**

(Unless otherwise noted,  $V_{CC} = 5.0 \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ,  $GNDA = 0V$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ; typical characteristics specified at  $V_{CC} = 5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_a = 25^\circ\text{C}$ ; all signals referenced to  $GNDA$ .)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Frequency of Master Clocks	$f_{MCK}$	Depends on the device used and the $BCLK_R/CLKSEL$ Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
Rise Time of Bit Clock	$t_{R(BCK)}$	$t_{PB} = 488\text{ns}$			50	ns
Fall Time of Bit Clock	$t_{F(BCK)}$	$t_{PB} = 488\text{ns}$			50	ns
Holding Time from Bit Clock Low to Frame Sync	$t_{H(LFS)}$	Long frame only	0			ns
Holding Time from Bit Clock High to Frame Sync	$t_{H(HFS)}$	Short frame only	0			ns
Set-Up Time from Frame Sync to Bit Clock Low	$t_{SU(FBCL)}$	Long frame only	80			ns
Delay Time from $BCLK_X$ High to Data Valid	$t_{D(HDV)}$	Load = 150pF plus 2 LSTTL loads	0		180	ns
Delay Time to $\overline{TS}_X$ Low	$t_{D(TSXL)}$	Load = 150pF plus 2 LSTTL loads			140	ns
Delay Time from $BCLK_X$ Low to Data Output Disabled	$t_{D(LDD)}$		50		165	ns
Delay Time to Valid Data from $FS_X$ or $BCLK_X$ , Whichever Comes Later	$t_{D(VD)}$	$C_L = 0\text{pF}$ to $150\text{pF}$	20		165	ns
Set-Up Time from $D_R$ Valid to $BCLK_{R/X}$ Low	$t_{SU(DRBL)}$		50			ns
Hold Time from $BCLK_{R/X}$ Low to $D_R$ Invalid	$t_{H(BLDR)}$		50			ns
Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	$t_{SU(FBLS)}$	Short frame sync pulse (1 or 2 bit clock periods long) (Note1)	50			ns
Width of Master Clock High	$t_{W(MCKH)}$	$MCLK_X$ and $MCLK_R$	160			ns
Width of Master Clock Low	$t_{W(MCKL)}$	$MCLK_X$ and $MCLK_R$	160			ns
Rise Time of Master Clock	$t_{R(MCK)}$	$MCLK_X$ and $MCLK_R$			50	ns
Fall Time of Master Clock	$t_{F(MCK)}$	$MCLK_X$ and $MCLK_R$			50	ns
Set-Up Time from $BCLK_X$ High (and $FS_X$ In Long Frame Sync Mode) to $MCLK_X$ Falling Edge	$t_{SU(BHMF)}$	First bit clock after the leading edge of $FS_X$				
Period of Bit Clock	$t_{CK}$		485	488	15,725	ns
Width of Bit Clock High	$t_{W(BCKH)}$	$V_{IH} = 2.2V$	160			ns
Width of Bit Clock Low	$t_{W(BCKL)}$	$V_{IL} = 0.6V$	160			ns

TIMING CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Hold Time from BCLK <sub>X/R</sub> Low to FS <sub>X/R</sub> Low	$t_{H(BLFL)}$	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	100			ns
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS <sub>X</sub> or FS <sub>R</sub> )	$t_{H(3rd)}$	Long frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
Minimum Width of the Frame Sync Pulse (Low Level)	$t_{WFL}$	64K bit/s operating mode	160			ns

Note 1 : For short frame sync timing, FS<sub>X</sub> and FS<sub>R</sub> must go high while their respective bit clocks are high.

TIMING DIAGRAM

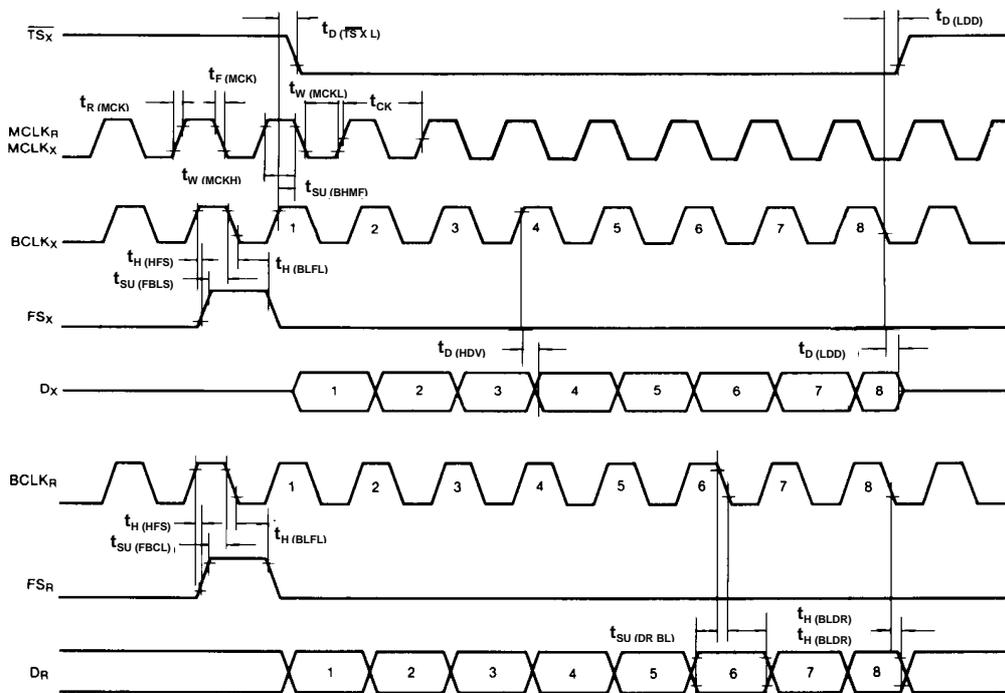


Fig. 2. Short Frame Sync Timing

TIMING DIAGRAM (Continued)

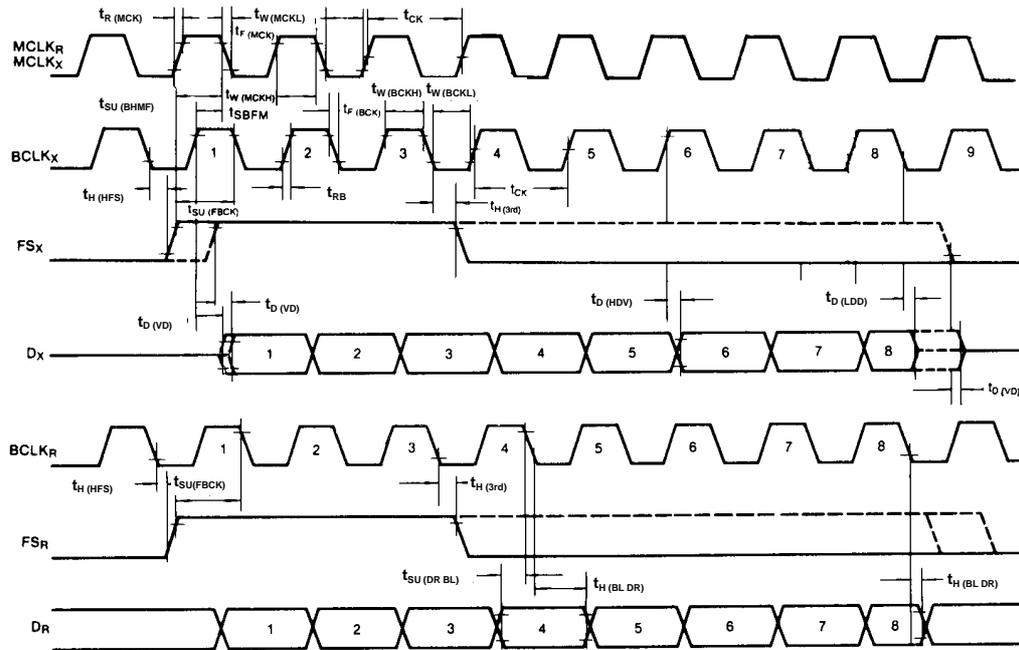


Fig. 3 Long Frame Sync Timing

**TRANSMISSION CHARACTERISTICS**

(Unless otherwise specified : Ta = 0°C to 70°C, V<sub>CC</sub> = 5V ±5%, V<sub>BB</sub> = -5V ±5%, G<sub>NDA</sub> = 0V, f = 1.02KHz, V<sub>IN</sub> = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Amplitude Respons</b>						
Receive Gain, Absolute	G <sub>V (ARX)</sub>	Ta = 25 °C, V <sub>CC</sub> = 5V, V <sub>BB</sub> = -5V Input = Digital code sequence for 0dBm0 signal at 1020Hz	-0.15		0.15	dB
Receive Gain, Relative to G <sub>V (ARX)</sub>	G <sub>V (RRX)</sub>	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	-0.15 -0.35 -0.7		0.15 0.05 0 -14	dB dB dB dB
Absolute Receive Gain Variation with Temperature	$\Delta G_{V (ARX)} / \Delta T$	Ta = 0°C to 70°C			±0.1	dB
Absolute Receive Gain Variation with Supply Voltage	$\Delta G_{V (ARX)} / \Delta V$	V <sub>CC</sub> = 5V ±5%, V <sub>BB</sub> = -5V ±5%			±0.05	dB
Receive Gain Variations with Level	$\Delta G_{V (RXL)}$	Sinusoidal test method ; reference input PCM code corresponds to an Ideally encoded -10dBm0 signal PCM level = -40dBm0 to +3dBm0 PCM level = -50dBm0 to -40dBm0 PCM level = -55dBm0 to -50dBm0	-0.2 -0.4 -1.2		0.2 0.4 1.2	dB dB dB
Receive Output Drive Level	V <sub>O (RX)</sub>	R <sub>L</sub> = 600Ω	-2.5		2.5	V
Absolute Levels	V <sub>AL</sub>	Nominal 0dBm0 level is 4dBm (600Ω) 0dBm0		1.2276		V <sub>rms</sub>
Max Overload Level	V <sub>OL (MAX)</sub>	Max overload level (3.17dBm0): KT8554B Max overload level (3.14dBm0): KT8557B		2.501		V <sub>PK</sub>
Transmit Gain, Absolute	G <sub>V (ATX)</sub>	Ta = 25 °C, V <sub>CC</sub> = 5V, V <sub>BB</sub> = -5V Input at GS <sub>x</sub> = 0dBm0 at 1020Hz	-0.15		0.15	dB
Transmit Gain, Relative to G <sub>V (ATX)</sub>	G <sub>V (RTX)</sub>	f = 16Hz f = 50Hz f = 60Hz f = 200Hz f = 300Hz - 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure response from 0Hz to 4000Hz	-1.8 -0.15 -0.35 -0.7		-40 -30 -26 -0.1 0.15 0.05 0 -14 -32	dB dB dB dB dB dB dB dB dB
Absolute Transmit Gain Variation with Temperature	$\Delta G_{V (ATX)} / \Delta T$	Ta = 0°C to 70°C			±0.1	dB
Absolute Transmit Gain Variation with Supply Voltage	$\Delta G_{V (ATX)} / \Delta V$	V <sub>CC</sub> = 5V ±5%, V <sub>BB</sub> = -5V ±5%			±0.05	dB
Transmit Gain Variations with Level	$\Delta G_{V (TXL)}$	Sinusoidal test method Reference level = - 10dBm0 VF <sub>x1</sub> + = - 40dBm0 to + 3dBm0 VF <sub>x1</sub> + = - 50dBm0 to - 40dBm0 VF <sub>x1</sub> + = - 55dBm0 to - 50dBm0	- 0.2 - 0.4 - 1.2		0.2 0.4 1.2	dB dB dB

## TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Envelope Delay Distortion with Frequency</b>						
Receive Delay, Absolute	$t_{D(ARX)}$	f = 1600Hz		180	200	$\mu$ s
Receive Delay, Relative to $t_{D(ARX)}$	$t_{D(RRX)}$	f = 500Hz - 1000Hz	-40	-25		$\mu$ s
		f = 1000Hz - 1600Hz	-30	-20		$\mu$ s
		f = 1600Hz - 2600Hz		70	90	$\mu$ s
		f = 2600Hz - 2800Hz		100	125	$\mu$ s
		f = 2800Hz - 3000Hz		145	175	$\mu$ s
Transmit Delay, Absolute	$t_{D(ATX)}$	f = 1600Hz		290	315	$\mu$ s
Transmit Delay, Relative to $t_{D(ATX)}$	$t_{D(RTX)}$	f = 500Hz - 600Hz		195	220	$\mu$ s
		f = 600Hz - 800Hz		120	145	$\mu$ s
		f = 800Hz - 1000Hz		50	75	$\mu$ s
		f = 1000Hz - 1600Hz		20	40	$\mu$ s
		f = 1600Hz - 2600Hz		55	75	$\mu$ s
		f = 2600Hz - 2800Hz		80	105	$\mu$ s
		f = 2800Hz - 3000Hz		130	155	$\mu$ s
<b>Noise</b>						
Receive Noise, C Message Weighted	$N_{RXC}$	PCM code equals alternating positive and negative zero, KT8554B		8	11	dBrnc0
Receive Noise, P Message Weighted	$N_{RXP}$	PCM code equals, positive zero, KT8557B		-82	-79	dBm0p
Transmit Noise, C Message Weighted	$N_{TXC}$	KT8554B		12	15	dBrnc0
Transmit Noise, P Message Weighted	$N_{TXP}$	KT8557B		74	-67	dBm0p
Noise, Single Frequency	$N_{SF}$	f = 0KHz to 100KHz, loop around measurement, $V_{F_xI} + = 0V_{rms}$			-53	dBm0
Positive Power Supply Rejection, Transmit	PSRR (PTX)	$V_{F_xI} + = 0V_{rms}$ $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0KHz - 50KHz	40			dB
Negative Power Supply Rejection, Transmit	PSRR (NTX)	$V_{F_xI} + = 0V_{rms}$ $V_{BB} = -5.0V_{DC} + 100mV_{rms}$ f = 0KHz - 50KHz	40			dB
Positive Power Supply Rejection, Receive	PSRR (PRX)	PCM code equals positive zero $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0Hz - 4000Hz f = 4KHz - 25KHz f = 25KHz - 50KHz	40 40 36			dB dB dB
Negative Power Supply Rejection, Receive	PSRR (NRX)	PCM code equals positive zero $V_{BB} = 5.0V_{DC} + 100mV_{rms}$ f = 0Hz - 4000Hz f = 4KHz - 25KHz f = 25KHz - 50KHz	40 40 36			dB dB dB

## TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	typ	Max	Unit
Spurious Out-of-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz - 3400Hz input PCM applied to $D_R$ . Measure individual image signals at $V_{F_xO}$ 4600Hz - 760Hz 7600Hz - 8400Hz 8400Hz - 100,000Hz			-32 -40 -32	dB dB dB
<b>Distortion</b>						
Signal to Total Distortion Transmit or Receive Half-Channel	THD <sub>TX</sub> THD <sub>RX</sub>	Sinusoidal test method Level = 3.0dBm0 = 0dBm0 to 30dBm0 = -40dBm0 XMT RCV = -55dBm0 XMT RCV	33 26 29 30 14 15			dBC dBC dBC dBC dBC dBC
Single Frequency Distortion, Transmit	THD <sub>SF(TX)</sub>				-46	dB
Single Frequency Distortion, Receive	THD <sub>SF(RX)</sub>				-46	dB
Intermodulation Distortion	THD <sub>IMD</sub>	Loop around measurement, $V_{F_xI} = -4dBm0$ to $-21dBm0$ , two frequencies in the range 300Hz - 3400Hz			-41	dB
<b>Crosstalk</b>						
Transmit to Receive Crosstalk, 0dBm0 Transmit Level	CT <sub>(TX-RX)</sub>	f = 300Hz - 3400Hz $D_R$ = Steady PCM code		-90	-75	dB
Receive to Transmit Crosstalk, 0dBm0 Receive Level	CT <sub>(RX-TX)</sub>	f = 300Hz - 3400Hz, $V_{F_xI} = 0V$		-90	-70 (Note1)	dB

Note 1. CT<sub>(RX-TX)</sub> is measured with a -40dBm0 activating signal applied at  $V_{F_xI} +$

ENCODING FORMAT AT  $D_x$  OUTPUT

	mLaw KT8554B	A-Law KT8557B
$V_{IN}$ (at $GS_x$ ) = + Full Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
$V_{IN}$ (at $GS_x$ ) = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
$V_{IN}$ (at $GS_x$ ) = - Full Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

APPLICATION CIRCUIT

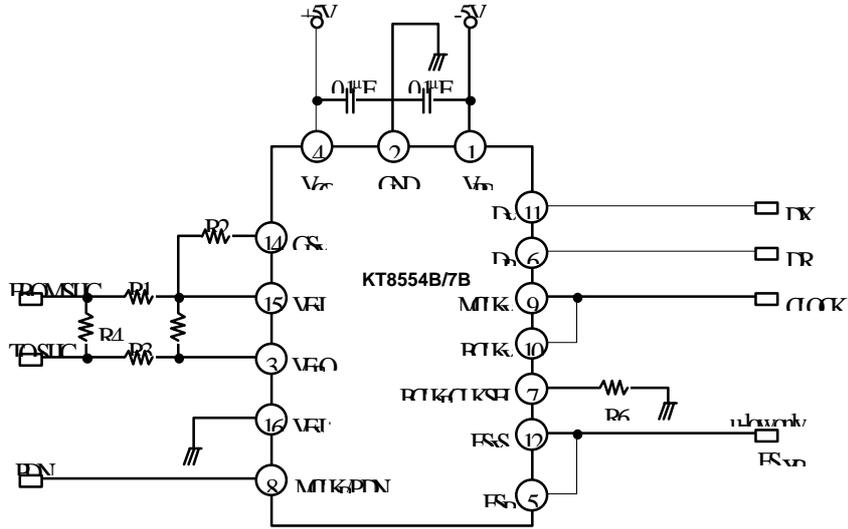


Fig. 4

NOTE 1 : Supposing Desired Line Termination Impedance  $R_L = 600\text{ohm}$

It is  $0\text{dBm} = 0.77459\text{Vrms}$

NOTE 2 :  $T_x\text{Gain } 20 \log (R_2/R_1)$ ,  $R_1 + R_2 < 100\text{Kohm}$ , or The Correspondence of 1-CHIP CODEC  $0\text{dBm } 0 = 4\text{dBm}$ .

SELECTION OF MASTER CLOCK FREQUENCY

BCLKR/CLKSEL	KT 8554	KT 8557
Clocked	1.536 / 1.544 MHz	2.048MHz
0	2.048 MHz	1.536 / 1.544 MHz
1 (or open)	1.536 / 1.544 MHz	2.048MHz