



No.2058A

CMOS LSI

LC5812

4-Bit Microcomputer
with Internal LCD Driver

The LC5812 series models are 4-bit, single-chip, high-performance microcomputers equipped with LCD drivers. They are produced by CMOS technology. Their numerous features include low-voltage operation and low current dissipation.

A 4 bit parallel-processing ALU, program memory (ROM), data memory (RAM), input and output ports, a timer, a clock generator, and LCD drivers, among other things, are integrated on a single chip.

A set of 134 instructions, including the operation and processing instructions executable in 4-bit units and various conditional branch instructions and LCD driver data transfer instructions form an easy-to-use and effective instruction system.

In HALT mode the user can readily implement the clock function during low-power dissipation. To minimize the current required, overall internal operation is stopped except for the oscillation and frequency divider circuits and the LCD drivers.

In HOLD mode the operation of the system clock oscillation is stopped so that the current dissipation becomes much less.

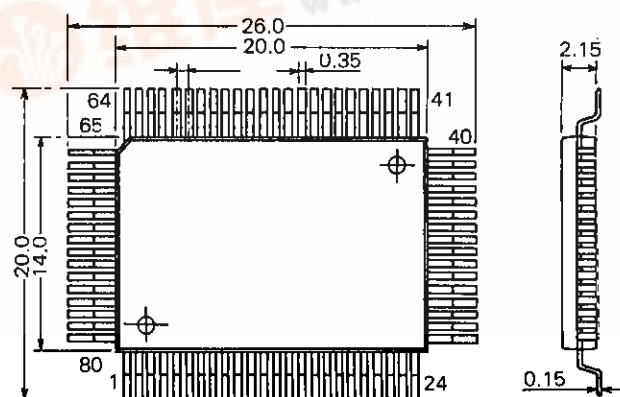
The LC5812 is very useful for controlling electronic tuners, cameras, and other portable devices at low voltage, with low power dissipation.

Features

- A wide supply voltage range

	Cycle time	Supply voltage range	Remarks
LC5812	122 μ s	$V_{SS2} = -2.0$ to $-3.6V$	32k crystal
LC5812H	122 μ s	$V_{SS2} = -2.0$ to $-5.0V$	32k crystal
	61 μ s	$V_{SS2} = -2.3$ to $-5.0V$	65k crystal
	40 μ s	$V_{SS2} = -3.5$ to $-5.0V$	400k ceramic resonator
	20 μ s	$V_{SS2} = -4.5$ to $-5.0V$	800k ceramic resonator

Package Dimensions 3044B
(unit: mm)



SANYO : QIP80A

○ Micro-level operating current

Only micro-level current is needed to operate the equipment if the HALT function is used efficiently. Although the exact current dissipation depends on the oscillation frequency (and the oscillator) and the program structure, a typical current requirement is about $5\mu\text{A}$ to run the clock program if the optimum technique is used to design the program.

○ Enhanced HALT/HOLD release and interrupt functions

- Five types of HALT/HOLD release functions and five types of interrupt functions
- External interrupt function (included in the above 5 interrupt functions)
- Up to 8 levels of subroutine nesting (common with interrupts)

○ Enhanced hardware for greater processing capability

- Built-in segment PLA circuit: Is able to join the LCD driver outputs to any patterns on the LCD panel without software.
- Built-in decimal up/down counter
- Built-in 8-bit programmable timer
- The entire RAM area can be used as a working area (bank switching).
- Built-in data pointer
- All instructions per step operation
- Built-in clock oscillator and frequency divider circuit

○ Various LCD output terminals for LCD panel drive (42 terminals)

LCD panel		Number of LCD segments
1/3 bias	1/3 duty	126 segments (max.)
1/2 bias	1/3 duty	126 segments (max.)
1/2 bias	1/2 duty	84 segments (max.)
Static		42 segments (max.)

○ The LCD panel drive output terminal can be switched to the general-purpose output terminal.

○ A number of input and output terminals are provided.

Input dedicated port:	2 ports/8 pins
Input/output port:	2 ports/8 pins
Output dedicated port:	1 port/4 pins

○ An initial reset terminal is provided.

○ Built-in oscillation circuit for system clock

Two kinds of oscillation circuits are available: one for the system clock and the other for clock oscillation.

○ Number of instructions: 134

○ ROM: 2,048 x 16 bits

○ RAM: 152 x 4 bits

○ Form of shipment: QIP80 (or chip)

Application Development Support System

An evaluation chip (LC5897) and special devices for the application development tool will be provided.

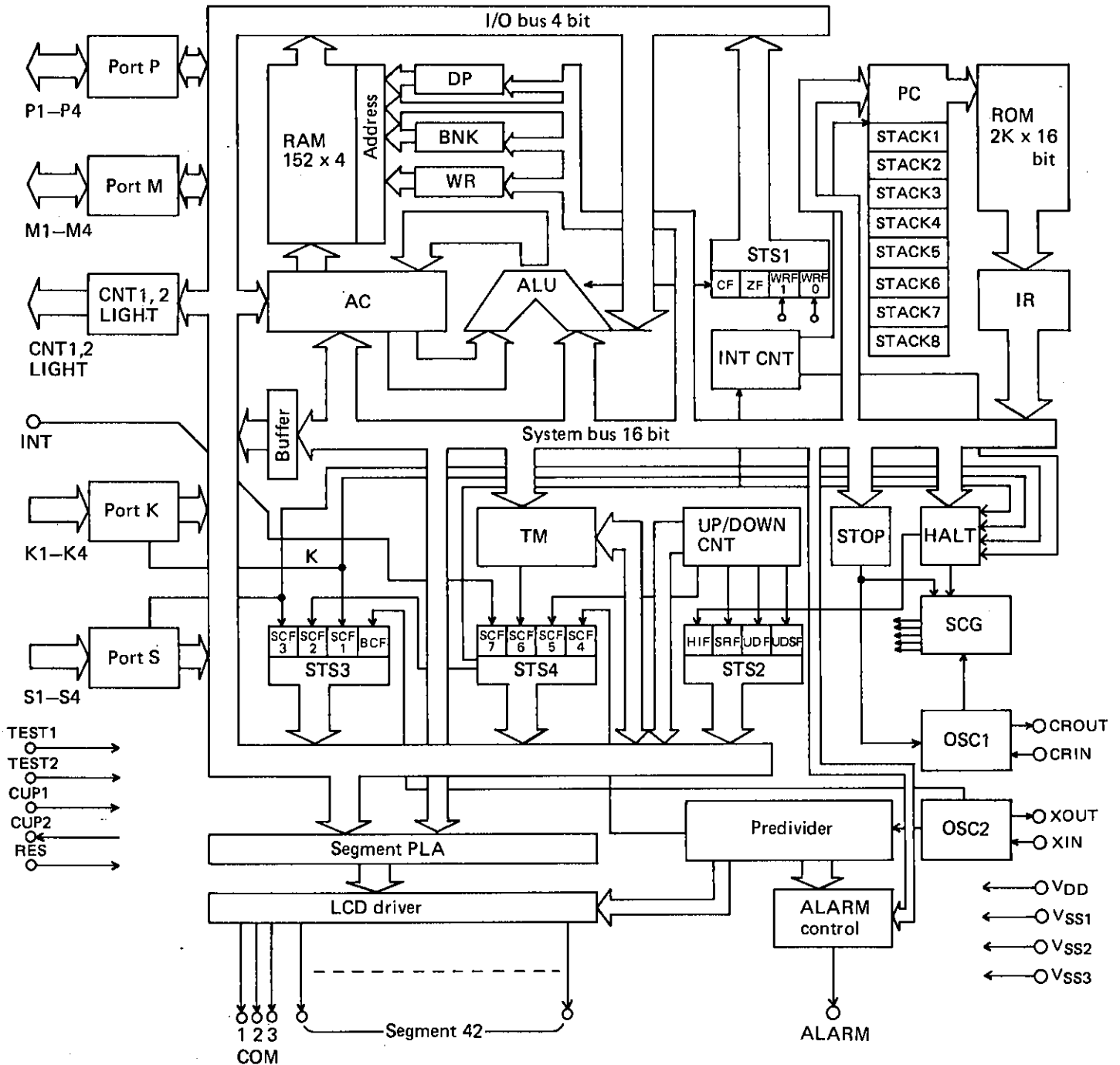
- SDS410 system
Enables the user to create an application development program in assembler language (edit-assembling).
- EVA510 + TB5812 + DCB1 + Application Evaluation Board + LC5897
Modification and debugging of the application development program are possible by connecting to the SDS410.
The EVA510 is identical with the EVA410 except that the control ROM has been replaced.
- TB5812 + DCB1 + Application Evaluation Board + LC5897
Load and evaluation is possible using the EPROM (2732) in which the data for the application development program is contained.

Note) The application evaluation board is created by the user.
Either LEDs or on LCD can be used as the display element.

Application Examples

- Portable equipment (camera control, various card controls, high-quality electric calculators and timers)
- Acoustic equipment (electronic control, electronic tuning, and clocks)
- Household electrical apparatus (remote control, and timer control)
- Telephone equipment (telephone control, and display control)

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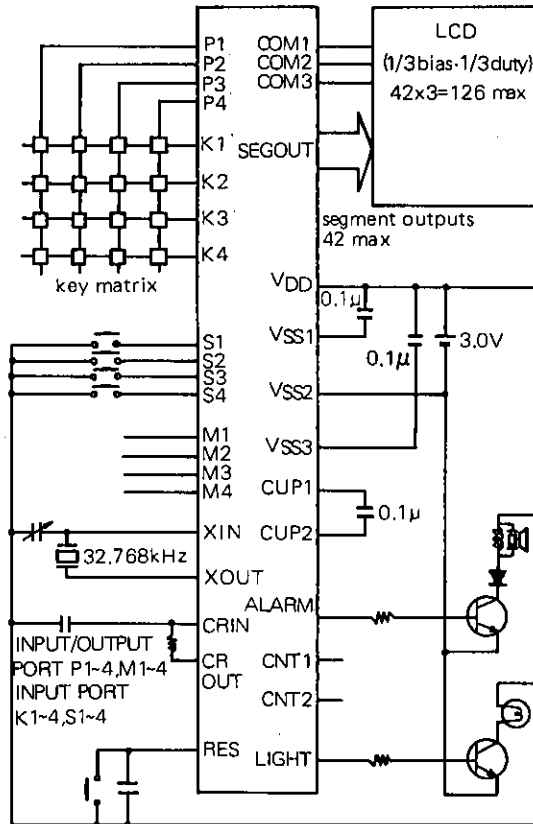


DP: Data pointer
 BNK: Bank register
 WR: Working register
 AC: Accumulator
 ALU: Arithmetic and logical unit
 INT: Interrupt control circuit
 PC: Program counter
 UP/DOWN CNT: Decimal up/down counter
 TM: Preset timer
 IR: Instruction register
 STOP: HOLD control circuit
 HALT: HALT control circuit
 SCG: System clock generator
 STS1: Status register 1
 STS2: Status register 2

STS3: Status register 3
 STS4: Status register 4
 CF: Carry flag
 ZF: Zero flag
 WRF0: Working flag 0
 WRF1: Working flag 1
 BCF: Test flag
 SCF1: S port flag
 SCF2: STS4 flag
 SCF3: K port flag
 SCF4: Divider overflow flag
 SCF5: UP/DOWN CNT overflow flag
 SCF6: Timer overflow flag
 SCF7: INT signal change flag
 ICF: Internal clock flag

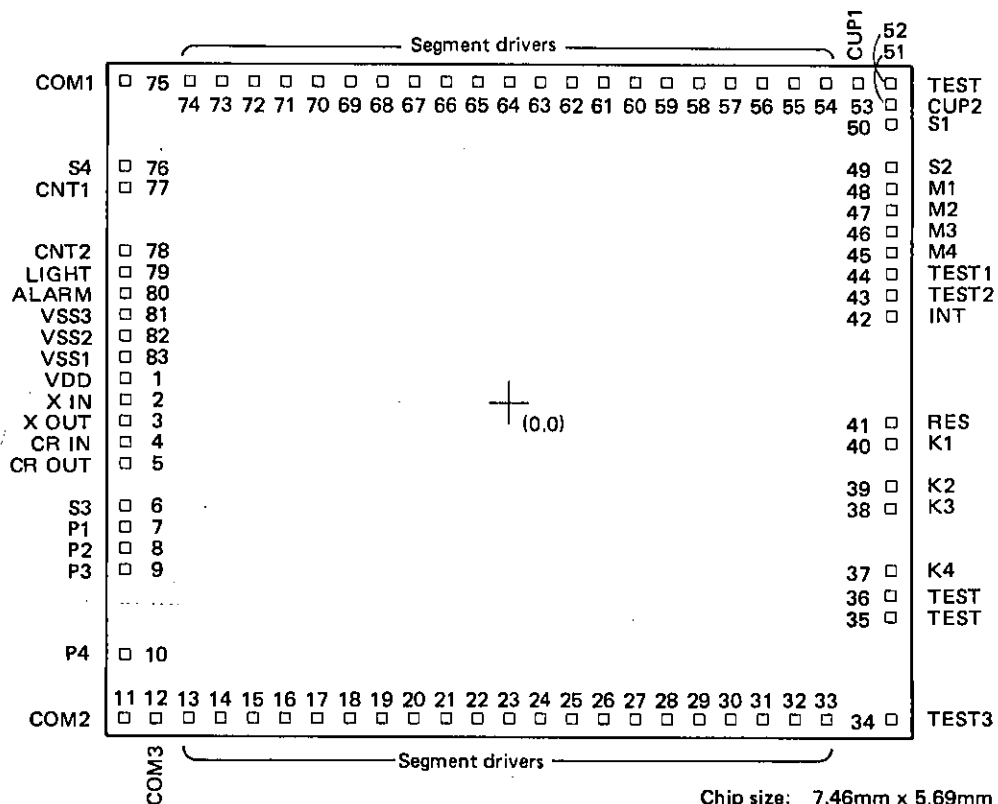
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Application Circuit – Example (1/3 bias – 1/3 duty)



Unit (capacitance: F)

Pad Arrangement of LSI Chip



Pin Layout

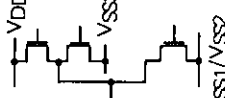
Pad name and coordinates

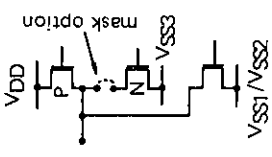
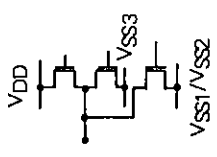
QIP80 pin arrangement					QIP80 pin arrangement				
	Pad No.	Pad name	X (um)	Y (um)		Pad No.	Pad name	X (um)	Y (um)
72	1	VDD	-3581	+214	32	43	TEST2	+3581	+878
73	2	XIN	"	+3	33	44	TEST1	"	+1105
74	3	XOUT	"	-176	34	45	M4	"	+1285
75	4	CRIN	"	-369	35	46	M3	"	+1465
76	5	CROUT	"	-549	36	47	M2	"	+1645
77	6	S3	"	-1048	37	48	M1	"	+1825
78	7	P1	"	-1228	38	49	S2	"	+2005
79	8	P2	"	-1408	39	50	S1	"	+2317
80	9	P3	"	-1588	40	51	CUP2	"	+2497
1	10	P4	"	-2380	—	52	TEST	"	+2696
2	11	COM2	"	-2696	41	53	CUP1	+3300	"
3	12	COM3	-3367	-2696	42	54	seg	+3059	"
4	13	seg	-2823	"	43	55	↑	+2764	"
5	14	↑	-2528	"	44	56	↑	+2469	"
6	15	↑	-2233	"	45	57	↑	+2174	"
7	16	↑	-1938	"	46	58	↑	+1878	"
8	17	↑	-1643	"	47	59	↑	+1583	"
9	18	↑	-1347	"	48	60	↑	+1288	"
10	19	↑	-1052	"	49	61	↑	+993	"
11	20	↑	-757	"	50	62	↑	+687	"
12	21	↑	-462	"	51	63	↑	+381	"
13	22	↑	-156	"	52	64	↑	+75	"
14	23	↑	+150	"	53	65	↑	-231	"
15	24	↑	+456	"	54	66	↑	-537	"
16	25	↑	+762	"	55	67	↑	-843	"
17	26	↑	+1068	"	56	68	↑	-1149	"
18	27	↑	+1374	"	57	69	↑	-1455	"
19	28	↑	+1680	"	58	70	↑	-1761	"
20	29	↑	+1986	"	59	71	↑	-2067	"
21	30	↑	+2292	"	60	72	↑	-2373	"
22	31	↑	+2598	"	61	73	↑	-2679	"
23	32	↑	+2904	"	62	74	seg	-2985	"
24	33	seg	+3210	"	63	75	COM1	-3581	"
25	34	TEST3	+3581	"	64	76	S4	"	+2101
—	35	TEST	"	-1795	65	77	CNT1	"	+1849
—	36	TEST	"	-1584	66	78	CNT2	"	+1298
26	37	K4	"	-1402	67	79	LIGHT	"	+1114
27	38	K3	"	-1049	68	80	ALARM	"	+934
28	39	K2	"	-868	69	81	VSS3	"	+754
29	40	K1	"	-515	70	82	VSS2	"	+574
30	41	RES	+3581	-335	71	83	VSS1	"	+394
31	42	INT	"	+698					

- The values (X, Y) indicate the coordinates of each pad center with the center of the chip as the origin.
- The TEST terminal should be open during normal operation.
- If the chip is used, the substrate must be tied to VDD.

Pin Description

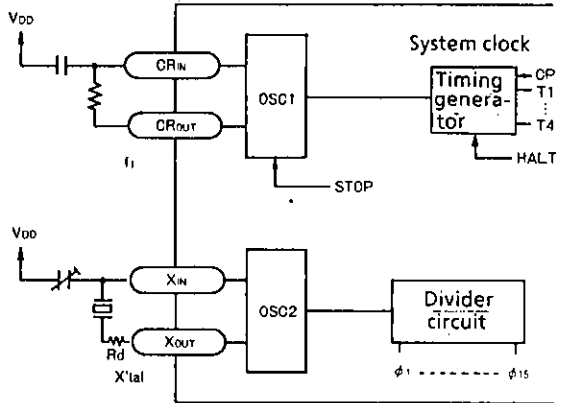
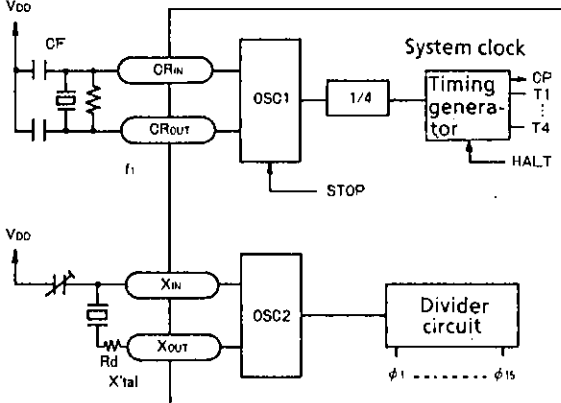
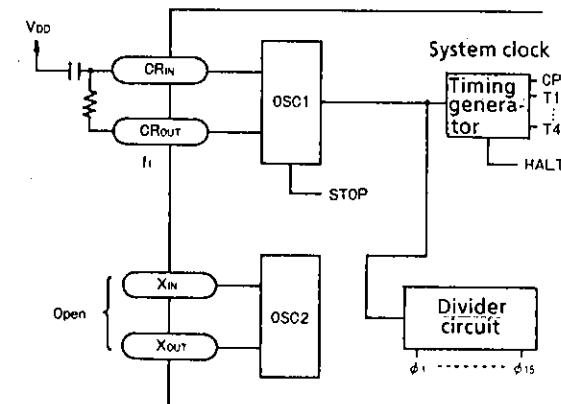
Terminal name	Input/Output	Circuit configuration	Function	Option	Status during reset
X IN	Input		Connects 32.768kHz or 65.536kHz crystal between X IN and X OUT for oscillation. Used for the timer reference clock and system clock. X OUT incorporates a 20pF capacitor to VDD.	(1) For 32K (2) For 65K *Option (2) is available only on the LC5812H.	
X OUT	Output				
S1 S2 S3 S4	Input		Input-dedicated port Has a 7ms or 32ms chatter removal circuit. By applying VDD to S1 through S4 simultaneously, the internal LSI devices are reset (mask option). (The chatter removal time is for the 32.768kHz option.)	(1) Selection of "L" level Hold Tr. (2) Use of initial reset by simultaneous application of VDD to S1 through S4.	Pull-down resistance is ON during reset.
P2 P3 P4 M1 M2 M3 M3	Input/Output		I/O port with mode switched by instructions to perform the following operations: (1) Input port: Writes data in RAM (2) Output port: Outputs data from RAM.	Selection of "L" level Hold Tr.	
K1 K2 K3 K4	Input		(1) Used to send data to RAM via 7ms or 32ms chatter removal circuit. (2) Is able to operate the decimal counter in the LSI circuit with a K2 and K4 signal, according to instruction. (The chatter removal time is for the 32.768kHz option.)	Selection of "L" level Hold Tr.	
INT	Input		Controls the external interrupt request. (The mask option interlocks with port K.)	Selection of "L" level Hold Tr.	
RES	Input		Resets the internal LSI devices.	(1) Reset at the "H" level (with pull-down resistor) (2) Reset at the "L" level (with pull-up resistor)	

Terminal name	Input/ Output	Circuit configuration	Function	Option	Status during reset																				
CNT1 CNT2	Output		Output-dedicated port	(1) "L" output during reset. (2) "H" output during reset. *Options 1 and 2 can be specified for each of CNT1 and CNT2.	"L" or "H" output (according to mask option).																				
LIGHT	Output		Output-dedicated port Suitable for outputting the signals which drive the light transistor.	(1) "L" output during reset. (2) "H" output during reset.	"L" or "H" output (according to mask option)																				
ALARM	Output		Output-dedicated port Is able to output a 4kHz, 2kHz, or 1kHz modulating signal, according to instruction. Can also output nonmodulating signals. (The modulating frequency is for the 32.768kHz option.)	(1) "L" output during reset. (2) "H" output during reset.	"L" or "H" output (according to mask option).																				
VDD			(+) supply voltage terminal.																						
VSS3 VSS2 VSS1			VSS2 is a supply terminal. VSS1 and VSS3 are used to supply LCD driving power.																						
CUP1 CUP2			Connection terminal for voltage rise (fall) capacitor.																						
COM1 COM2 COM3	Output		Output port for common electrodes of LCD panel. Use of terminals varies. (The alternating frequency is for the 32.768kHz option.) <table border="1" data-bbox="1214 1167 1406 1704"><thead><tr><th></th><th>Static</th><th>1/2 duty</th><th>1/3 duty</th></tr></thead><tbody><tr><td>COM1</td><td>○</td><td>○</td><td>○</td></tr><tr><td>COM2</td><td>—</td><td>○</td><td>○</td></tr><tr><td>COM3</td><td>—</td><td>—</td><td>○</td></tr><tr><td>Alternating frequency</td><td>32Hz</td><td>32Hz</td><td>43Hz</td></tr></tbody></table>		Static	1/2 duty	1/3 duty	COM1	○	○	○	COM2	—	○	○	COM3	—	—	○	Alternating frequency	32Hz	32Hz	43Hz	(1) Lighting specification: • Static • 1/2 bias 1/3 duty • Duplex • 1/3 bias 1/3 duty	
	Static	1/2 duty	1/3 duty																						
COM1	○	○	○																						
COM2	—	○	○																						
COM3	—	—	○																						
Alternating frequency	32Hz	32Hz	43Hz																						

Terminal name	Input/Output	Circuit configuration	Function	Option	Status during reset
Segment driver (A group)	Output		LCD panel segment output port. - The terminal can be switched to the output dedicated port depending on the mask option. - If the internal LSI devices are reset, the static lighting signal is fed to COM1 through COM3 and to each of the LCD segment outputs, and all LCD panel segments go on or go off. (on/off: to be specified by mask option) - The segment PLA system is used to draw all patterns on the LCD panel.	Output for LCD drive CMOS output port Pch open drain output port Options ①, ②, and ③ can be selected in bit units.	To be specified by mask option ① Lighted mode (LCD use) "H" level (DC use) ② Unlighted mode (LCD use) "L" level (DC use)
Segment driver (B group)	Output		LCD panel segment output port. - The terminal can be switched to the output dedicated port depending on the mask option. - If the internal LSI devices are reset the static lighting signal is fed to COM1 through COM3 and to each of the LCD segment outputs, and all LCD panel segments go on or go off. (on/off: to be specified by mask option) - The segment PLA system is used to draw all patterns on the LCD panel.	Output for LCD drive CMOS output port Options ① and ② can be selected in bit units.	To be specified by mask option ① Lighted mode (LCD use) "H" level (DC use) ② Unlighted mode (LCD use) "L" level (DC use)
TEST 3 TEST TEST TEST2 TEST1 TEST			Test terminals (the user should not use these terminals).		
CR IN CR OUT			CR oscillation port. The oscillation can be stopped by the HOLD instruction.	(1) CR oscillation	

Note)  indicates the connection to VSS2.

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Oscillation Circuit Option		
Option	Circuit configuration	Remarks
CR & X'tal		Cycle time = $f_1/4$ Output from the divider circuit is used as program timer input signal, LCD drive waveform generating signal, or interrupt signal generation, etc. Note) For X'tal = 32.768kHz, set $R_d = 0\Omega$
CF & X'tal		Cycle time = $f_1/16$ Output from the divider circuit is used as program timer input signal, LCD drive waveform generating signal, or interrupt signal generation, etc. Note) For X'tal = 32.768kHz, set $R_d = 0\Omega$
CR option		Cycle time = $f_1/4$ Output from the divider circuit is used as program timer input signal, LCD drive waveform generating signal, or interrupt signal generation, etc.

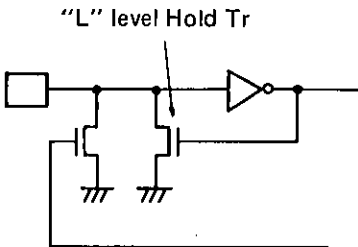
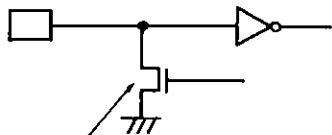
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Option	Circuit configuration	Remarks
CF option		Cycle time = $f_1/16$ Output from the divider circuit is used as program timer input signal, LCD drive waveform generating signal, or interrupt signal generation, etc. LC5812H only.
X'tal option		Cycle time = $f_2/4$ Output from the divider circuit is used as program timer input signal, LCD drive waveform generating signal, or interrupt signal generation, etc. Note) For X'tal = 32.768kHz, set $R_d = 0\Omega$

Input Port Option

Option	Circuit configuration	Remarks:
"L" level Hold Tr is used.	 "L" level Hold Tr	• The Hold Tr option is used to reduce the current required for a push-button switch for S1, or a slide switch for S2. • The "L" level signal can be held after the pull-down resistor is set to ON for a short period of time by software during the opening of input.
"L" level Hold Tr is not used.	 Tr. for pull-down resistor	• The pull-down Tr can be used as a pull-down resistor. • The pull-down Tr can be set to ON/OFF by software.

These options are provided for the S, K, M, and P ports. Be sure to specify NOT USED for the M or P port when using it as an output port.

LCD Output Options

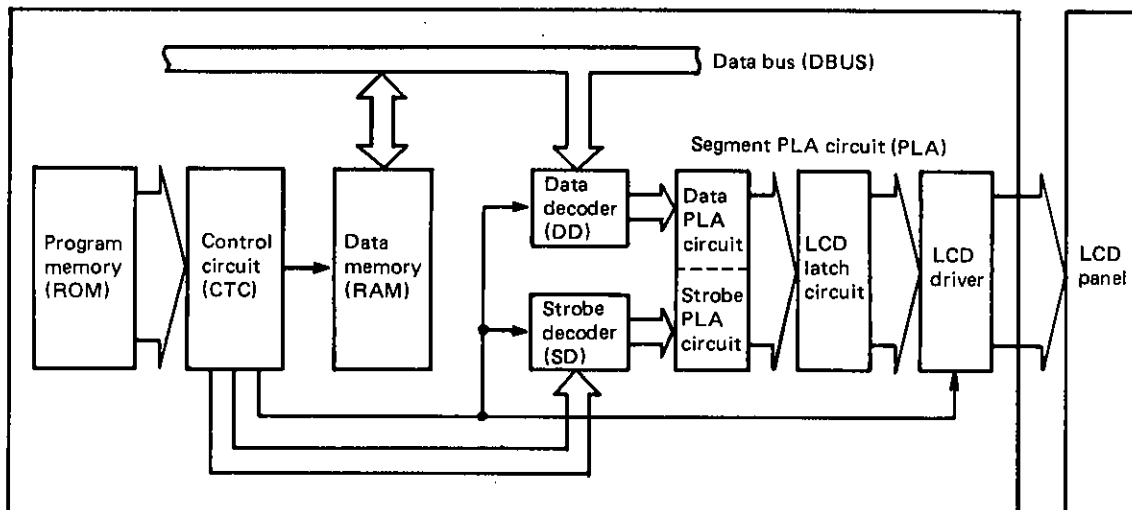
LCD output options for the LCD drive, the CMOS output port and the Pch open drain can be selected.

Option	Output Form
LCD drive	- Terminal for LCD segment drive. - The drive method is determined according to the LCD lighting system specified separately. The LCD lighting system is common to all terminals, and can be selected from among the static, duplex, 1/2 bias-1/3 duty, and 1/3 bias-1/3 duty methods.
CMOS output port	General-purpose CMOS type output port.
Pch open drain output port	- General-purpose Pch open drain type output port. - Usable according to the PLA option for the predetermined ports.

Alternating waveform for the LCD driver for LCD output is generated by hardware logic.

Segment PLA Circuit

The following figure is a schema of the structure of the segment PLA circuit.



The contents of data memory are sent to the LCD latch circuit for display either as is or after being decoded by the data decoder. The PLA circuit is used to rearrange the input data to output it to the display latch. With this circuit, data memory can be edited to suit LCD panel specifications without software processing. The PLA circuit can be specified by ROM for PLA, which is supplied with program ROM.

Alarm Output

The following frequency divider output can be used directly as an alarm output:

- 1) Output signal either as $\phi 3$ or $\phi 4$ or $\phi 5$.
- 2) Any combination output signal at $\phi 10$, $\phi 11$, $\phi 12$, $\phi 13$, $\phi 14$ and $\phi 15$.
- 3) Modulating output signal of 1) or 2).

These signals can be output by software.

ϕN indicates the output at the Nth step of the oscillator frequency divider.

Resetting Internal Logic

There are three functions for resetting internal logic:

- ① Built-in power-ON clear circuit
----- Use of this option can be determined by the mask option.
- ② Reset terminal RES
- ③ Simultaneous operation of S1 through S4
----- Use of this option can be determined by the mask option.

These reset functions are explained below.

1) Built-in power-ON clear circuit

The initial-clear circuit provided in the microcomputer automatically operates and resets internal logic when power is turned on. This function is very useful in that it can be activated without external devices. But it has the two disadvantages listed below. It is, therefore, recommended that this function be used with other reset functions, or that other methods be used according to applications.

Disadvantages:

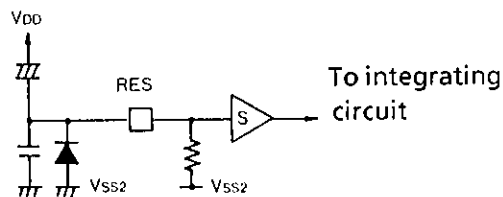
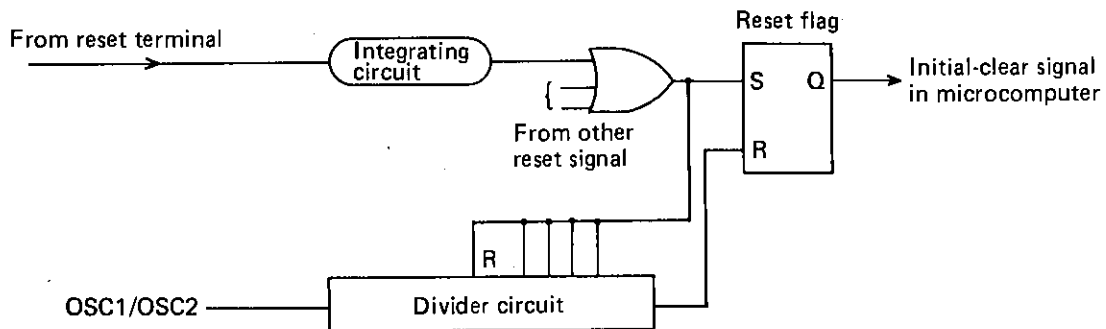
- a) The circuit may not operate under certain power-rise conditions during the power-ON sequence or due to chatter.
- b) Malfunctions may take place due to pulse noise in the power or a sudden change in status.

One of the following two reset options can be selected:

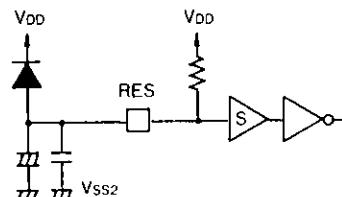
- INHIBIT:** The built-in power-ON clear circuit is not used
 ----- Use this option where malfunctions due to pulse noise in the power may take place.
- NORMAL ACTION:** The built-in power-ON clear circuit is used.
 ----- This option should be selected only when pulse noise does not affect the power.

2) Reset terminal RES

When the reset signal is fed to the reset terminal, the reset flag in the microcomputer is set and part of the divider circuit is reset. Internal logic is reset by the internal reset flag which is reset by the overflow signal from the divider circuit. The reset status of the logic circuit is released and the program counter starts operating.



a) with Pull-down R (H-RESET)

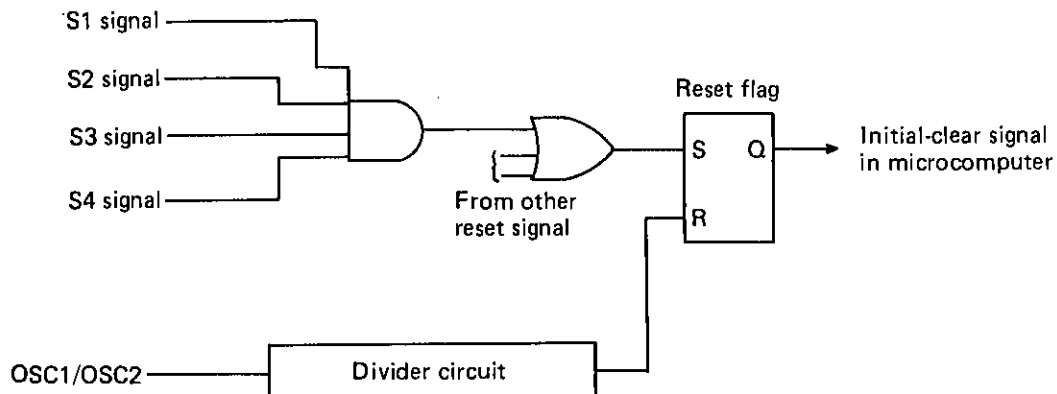


b) with Pull-up R (L-RESET)

3) Simultaneous operation of S1 through S4

By applying V_{DD} level voltage to S1 through S4 simultaneously, internal logic can be cleared (initial clear).

(Use of this option can be specified by the mask option.)



Interrupt Function

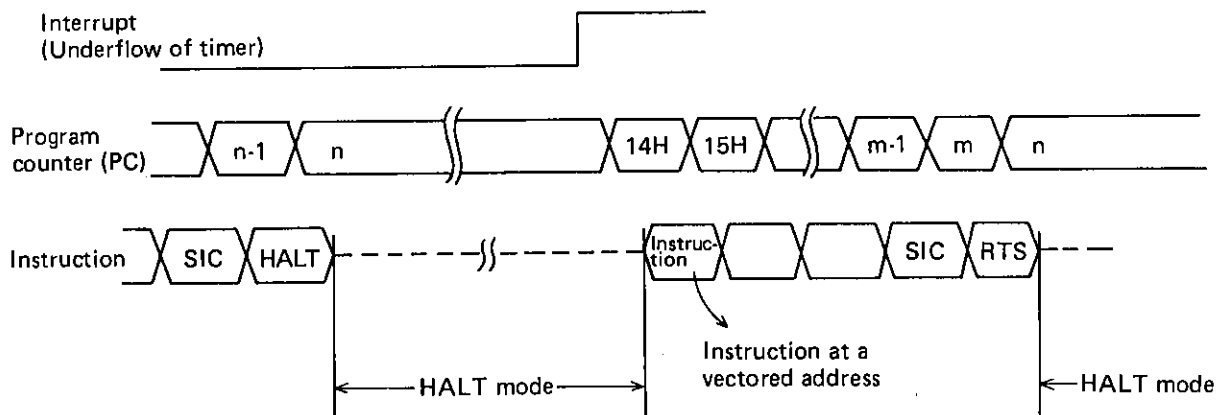
- Five factors and four vector addresses are provided for the interrupt function.
 - External interrupt terminal (INT)
 - Change of signal to port S or K
 - Underflow of programmable timer
 - Overflow of divider circuit
 - Overflow/underflow of decimal UP/DOWN counter
- } Same vector address

HALT function

- Can stop the CPU's system clock in HALT mode with the HALT instruction.
- Reduces the operating current to the oscillation circuit+HALT release signal+LCD drive circuit current during HALT.
- The following five factors cause HALT release request signals:
 - External interrupt terminal (INT)
 - Change of signal to port S or K
 - Underflow of programmable timer
 - Overflow of divider circuit
 - Overflow or underflow of decimal UP/DOWN counter

The factors for the HALT release request signal are the same as those for the interrupt request signal, but the use of any factor can be specified in programs.

If an interrupt occurs in HALT mode, the operation called for by the interrupt is performed, and the CPU returns to HALT mode.



Release of HALT by Interrupt

HOLD Function

- Can stop the operation of the oscillation circuit (OSC1) in HOLD mode with the STOP instruction.
- Reduces the current dissipation to the minimum during HOLD because OSC1 and CPU are stopped.

Relationship between the oscillation options and the HOLD release functions

Item	Reset signal (RES/RES)	Interrupt request signal	HALT release request signal	Note
CR & X'tal option	○	○	○	
CF & X'tal option	○	×	×	
CR option	○	×	×	
CF option	○	×	×	
X'tal option	×	×	×	HOLD function can not be used.

○: can be used to release HOLD.

×: cannot be used to release HOLD.

Decimal UP/DOWN Counter Function

A hardware function that counts external pulse or the internal reference pulse in decimal notation. One of the following three operations can be selected by software:

- ① The counting of pulses from port K4 with UP and DOWN switched by the signal level of port K2.
- ② The counting of pulses from port K4 with UP and DOWN switched by the phase difference signal of port K2.
- ③ The counting of divider circuit signals of the oscillator in ascending order.
----- With this function, a chrono counter in units of 1/100 second can be implemented by using a 32.768 kHz crystal oscillator.

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Option List

		LC5812	LC5812H	Remarks
LCD lighting method		Static	Static	Select "Unused" when the LCD output ports are all used as general-purpose ports.
		Duplex	Duplex	
		1/2 bias 1/3 duty	1/2 bias 1/3 duty	
		1/3 bias 1/3 duty	1/3 bias 1/3 duty	
		Unused	Unused	
"L" level Hold Tr	S ports (S1 to S4)	"L" level Hold Tr is used. "L" level Hold Tr is not used.	"L" level Hold Tr is used. "L" level Hold Tr is not used.	
	M ports (M1 to M4)	"L" level Hold Tr is used. "L" level Hold Tr is not used.	"L" level Hold Tr is used. "L" level Hold Tr is not used.	
	K ports (K1 to K4)	"L" level Hold Tr is used. "L" level Hold Tr is not used.	"L" level Hold Tr is used. "L" level Hold Tr is not used.	
	INT port	"L" level Hold Tr is used. "L" level Hold Tr is not used.	"L" level Hold Tr is used. "L" level Hold Tr is not used.	
	P ports (P1 to P4)	"L" level Hold Tr is used. "L" level Hold Tr is not used.	"L" level Hold Tr is used. "L" level Hold Tr is not used.	
Oscillator selection		CR & XTAL	CR & XTAL	Do not specify CF on the LC5812, because it is not allowed to use CF on the model.
		CR	CF & XTAL	
		XTAL	CR	
			CF	
			XTAL	
Internal power-on reset function		Unused Used	Unused Used	
Simultaneous operation of S1 through S4 for reset		Used Unused	Used Unused	
Selection of RES polarity		"H" level reset (Pull-down) "L" level reset (Pull-up)	"H" level reset (Pull-down) "L" level reset (Pull-up)	
Selection of output terminal polarity	CNT1	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	
	CNT2	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	
	ALARM	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	
	LIGHT	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	

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V_{DD}=0V 1/2bias 1/2duty

Item	Symbol	Conditions	Terminal	Min	Typ	Max	Unit
Absolute Maximum Ratings Ta = 25°C, V _{DD} = 0V							
Maximum supply voltage	V _{SS1}			-4.0		+0.3	V
	V _{SS2}	V _{SS2} =V _{SS3}		-4.0		+0.3	V
Maximum input voltage	V _{IN1}			V _{SS2}		+0.3	V
				-0.3			
Maximum output voltage	V _{OUT1}			V _{SS2}		+0.3	V
				-0.3			
Operating ambient temperature	T _{opr}			-20		+70	°C
Storage ambient temperature	T _{stg}			-30		+125	°C
Allowable Operating Conditions Ta=-20 to +70°C, V _{DD} = 0V							
Power supply voltage	V _{SS1}			-3.6		-1.3	V
	V _{SS2}	V _{SS2} =V _{SS3}		-3.6		-2.0	V
"H" level input voltage	V _{IH1}		RES	0.25X		0	V
	V _{IH2}		Input terminals other than RES	V _{SS2}			V
				0.3X			
"L" level input voltage	V _{IL1}		RES	V _{SS2}		0.75X	V
	V _{IL2}		Input terminals other than RES	V _{SS2}		0.7X	V
						V _{SS2}	
Operation frequency	fopg1	V _{SS2} =-2.0 to -3.6V	XIN/XOUT	32		33	kHz
	fopg2	V _{SS2} =-2.3 to -3.6V	CRIN/CROUT	17	33	50	kHz
Electrical Characteristics Ta=-20 to +70°C, V _{DD} = 0V							
Input resistance	R _{IN1A}	V _{SS2} =-2.9V, V _{IN} =0.8V _{SS2}	"L" level hold Tr	50		500	kohm
			*1, Fig. 1				
	R _{IN1B}	V _{SS2} =-2.9V, V _{IN} =V _{DD}	"L" level pull-in Tr	200	500	2000	kohm
			*1, Fig. 1				
	R _{IN2A}	V _{SS2} =-2.9V, V _{IN} =0.8V _{SS2}	"L" level hold Tr	50		500	kohm
			*2, Fig. 1				
	R _{IN2B}	V _{SS2} =-2.9V, V _{IN} =V _{DD}	"L" level pull-in Tr	200		2000	kohm
			*2, Fig. 1				
	R _{IN3}	V _{SS2} =-2.9V	RES, TEST1, TEST2	10	80	400	kohm
"H" level output voltage	V _{OH} (1)	V _{SS2} =-2.4V, I _{OH} =-0.4mA	ALARM, LIGHT, CNT1, CNT2	-1	-0.3		V
"L" level output voltage	V _{OL} (1)	V _{SS2} =-2.4V, I _{OL} =0.4mA	ALARM, LIGHT, CNT1, CNT2		V _{SS2}	V _{SS2}	V
					+0.3	+1	
"H" level output voltage	V _{OH} (2)	V _{SS2} =-2.4V, I _{OH} =-90μA	Port M, port P	-1	-0.3		V
"H" level output voltage	V _{OH} (3)	V _{SS2} =-2.4V, I _{OH} =-50μA	Port M, port P	-0.6	-0.2		V
"L" level output voltage	V _{OL} (3)	V _{SS2} =-2.4V, I _{OL} =0.1mA	Port M, port P		V _{SS2}	V _{SS2}	V
					+0.3	+1	
"H" level output voltage	V _{OH} (4)	V _{SS2} =-2.4V, I _{OH} =-20μA	Segment	-1	-0.3		V
"H" level output voltage	V _{OH} (5)	V _{SS2} =-2.4V, I _{OH} =-0.4μA	PAD No. 13 to 21, 54 to 61 QIP 80 pin number 4 to 12, 42 to 49	-0.2			V
"L" level output voltage	V _{OL} (4)	V _{SS2} =-2.4V, I _{OL} =40μA			V _{SS2}	V _{SS2}	V
					+0.3	+1	
"L" level output voltage	V _{OL} (5)	V _{SS2} =-2.4V, I _{OL} =0.4μA				V _{SS3}	V
						+0.2	

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Item	Symbol	Condition	Terminal Segment	Min	Typ	Max	Unit
"H" level output voltage	VOH(6)	VSS2=-2.4V, IOH=-5μA		-1	-0.3		V
"H" level output voltage	VOH(7)	VSS2=-2.4V, IOH=-0.4μA	PAD No. 22 to 33, 62 to 74 QIP 80 pin number 13 to 24, 50 to 62	-0.2			V
"L" level output voltage	VOL(6)	VSS2=-2.4V, IOL=20μA			VSS2 +0.3	VSS2 +1	V
"L" level output voltage	VOL(7)	VSS2=-2.4V, IOL=0.4μA				VSS2 +0.2	V
"H" level output voltage	VOH(8)	VSS2=-2.4V, IOH=-4μA	Common 1 - 2	-0.2			V
"M" level output voltage	VOM	VSS2=-2.4V, IOH=-4μA IOL=4μA	Common 1 - 2	VSS2/2 -0.2		VSS2/2 +0.2	V
"L" level output voltage	VOL(8)	VSS2=-2.4V, IOL=4μA	Common 1 - 2			VSS2 +0.2	V
Output voltage	VSS1	VSS2=-2.9V	C1=C2=0.1μF fopg=32.768kHz			-1.35	V
Power supply current	IDD	VSS2=-2.9V Ta=25°C STOP	C1=C2=0.1μF Cl=25kohms fopg=32.768kHz Co = Cg = 20pF Fig.2			5	μA
Oscillation start voltage	Vstt		Co = Cg = 20pF Fig.3			2.2	V
Oscillation hold voltage	VHOLD		Co = Cg = 20pF Fig.3			2.0	V
Oscillation start time	tstt	VSS2=-2.9V	Co = Cg = 20pF Fig.3			10	s
Oscillation correcting capacity	20P	VSS2=-2.9V	XOUT pin	18	22	26	pF
CR oscillation characteristics	fCR	VSS2=-2.3V to -3.6V	REXT=510kohm CEXT=30pF Fig. 4	16	33	50	kHz

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V_{DD}=0V 1/2bias 1/3duty

Item	Symbol	Conditions	Terminal	Min	Typ	Max	Unit
Absolute Maximum Ratings Ta = 25°C, V _{DD} = 0V							
Maximum supply voltage	V _{SS1}			-4.0		+0.3	V
	V _{SS2}	V _{SS2} =V _{SS3}		-4.0		+0.3	V
Maximum input voltage	V _{IN1}			V _{SS2} -0.3		+0.3	V
Maximum output voltage	V _{OUT1}			V _{SS2} -0.3		+0.3	V
Operating ambient temperature	T _{opr}			-20		+70	°C
Storage ambient temperature	T _{stg}			-30		+125	°C
Allowable Operating Conditions Ta = -20 to +70°C, V _{DD} = 0V							
Power supply voltage	V _{SS1}			-3.6		-1.3	V
	V _{SS2}	V _{SS2} =V _{SS3}		-3.6		-2.0	V
				-5.0		-3.9	V
"H" level input voltage	V _{IH1}		RES	0.25X		0	V
	V _{IH2}		Input terminals other than RES	V _{SS2} 0.3X			V
"L" level input voltage	V _{IL1}		RES	V _{SS2}		0.75X	V
	V _{IL2}		Input terminals other than RES	V _{SS2}		0.7X	V
Operation frequency	f _{opg1}	V _{SS2} =-2.0 to -3.6V	XIN/XOUT	32		33	kHz
	f _{opg2}	V _{SS2} =-2.3 to -3.6V	CRIN/CROUT	16	33	50	kHz
Electrical Characteristics Ta = -20 to +70°C, V _{DD} = 0V							
Input resistance	R _{IN1A}	V _{SS2} =-2.9V, V _{IN} =0.8V _{SS2}	"L" level hold Tr *1, Fig. 1	50		500	kohm
	R _{IN1B}	V _{SS2} =-2.9V, V _{IN} =V _{DD}	"L" level pull-in Tr *1, Fig. 1	200	500	2000	kohm
	R _{IN2A}	V _{SS2} =-2.9V, V _{IN} =0.8V _{SS2}	"L" level hold Tr *2, Fig. 1	50		500	kohm
	R _{IN2B}	V _{SS2} =-2.9V, V _{IN} =V _{DD}	"L" level pull-in Tr *2, Fig. 1	200		2000	kohm
	R _{IN3}	V _{SS2} =-2.9V	RES, TEST1, TEST2	10	80	400	kohm
	V _{OH} (1)	V _{SS2} =-2.4V, I _{OH} =-0.4mA	ALARM, LIGHT, CNT1, CNT2	-1	-0.3		V
"L" level output voltage	V _{OL} (1)	V _{SS2} =-2.4V, I _{OL} =0.4mA	ALARM, LIGHT, CNT1, CNT2		V _{SS2} +0.3	V _{SS2} +1	V
"H" level output voltage	V _{OH} (2)	V _{SS2} =-2.4V, I _{OH} =-90μA	Port M, port P	-1	-0.3		V
"H" level output voltage	V _{OH} (3)	V _{SS2} =-2.4V, I _{OH} =-50μA	Port M, port P	-0.6	-0.2		V
"L" level output voltage	V _{OL} (3)	V _{SS2} =-2.4V, I _{OL} =0.1mA	Port M, port P		V _{SS2} +0.3	V _{SS2} +1	V
"H" level output voltage	V _{OH} (4)	V _{SS2} =-2.4V, I _{OH} =-20μA	Segment	-1	-0.3		V
"H" level output voltage	V _{OH} (5)	V _{SS2} =-2.4V, I _{OH} =-0.4μA	PAD No. 13 to 21, 54 to 61 QIP 80 pin number 4 to 12, 42 to 49	-0.2			V
"L" level output voltage	V _{OL} (4)	V _{SS2} =-2.4V, I _{OL} =40μA			V _{SS2} +0.3	V _{SS2} +1	V
"L" level output voltage	V _{OL} (5)	V _{SS2} =-2.4V, I _{OL} =0.4μA				V _{SS3} +0.2	V

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Item	Symbol	Condition	Terminal Segment	Min	Typ	Max	Unit
"H" level output voltage (at CMOS output port)	VOH(6)	VSS2=-2.4V, IOH=-5μA		-1	-0.3		V
"H" level output voltage	VOH(7)	VSS2=-2.4V, IOH=-0.4μA	PAD No. 22 to 33, 62 to 74 QIP 80 pin number 13 to 24, 50 to 62	-0.2			V
"L" level output voltage (at CMOS output port)	VOL(6)	VSS2=-2.4V, IOL=20μA			VSS2 +0.3	VSS2 +1	V
"L" level output voltage	VOL(7)	VSS2=-2.4V, IOL=0.4μA				VSS2 +0.2	V
"H" level output voltage	VOH(8)	VSS2=-2.4V, IOH=-4μA	Common 1 - 3	-0.2			V
"M" level output voltage	VOM	VSS2=-2.4V, IOH=-4μA IOL=4μA	Common 1 - 3	VSS2/2 -0.2		VSS2/2 +0.2	V
"L" level output voltage	VOL(8)	VSS2=-2.4V, IOL=4μA	Common 1 - 3			VSS3 +0.2	V
Output voltage	VSS1	VSS2=-2.9V	C1=C2=0.1μF fopg=32.768kHz			-1.35	V
Power supply current	IDD	VSS2=-2.9V Ta=25°C STOP	C1=C2=0.1μF Cl=25ohms fopg=32.768kHz Co = Cg = 20pF Fig.5			5	μA
Oscillation start voltage	Vstt		Co = Cg = 20pF Fig.3			2.2	V
Oscillation hold voltage	VHOLD		Co = Cg = 20pF Fig.3			2.0	V
Oscillation start time	tstt	VSS2=-2.9V	Co = Cg = 20pF Fig.3			10	s
Oscillation correcting capacity	20P	VSS2=-2.9V	XOUT pin	18	22	26	pF
CR oscillation characteristics	fCR	VSS2=-2.3V to -3.6V	REXT=510kohm CEXT=30pF Fig. 4	17	33	50	kHz

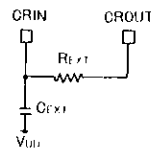


Fig. 1 Input Configuration of S1-4, M1-4, K1-4, P1-4

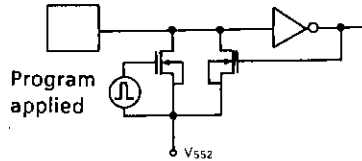


Fig. 4 CR OSC Circuit

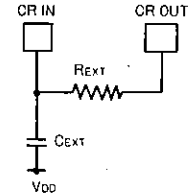


Fig. 2 Output Voltage, Supply Current, OSC HOLD Voltage Test Circuit

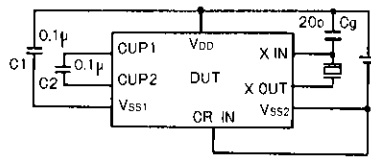


Fig. 5 Output Voltage, Supply Current, OSC Hold Voltage Test Circuit

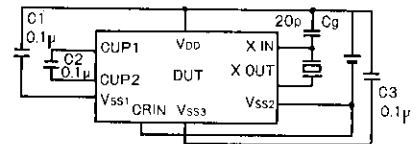
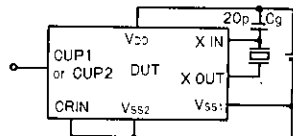


Fig. 3 OSC Start Voltage, OSC Start Time, Frequency Stability Test Circuit



Unit (capacitance: F)

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