CMOS LSI

No.3653B

LC65102A, LC65104A

4-bit Single-chip Microprocessors

OVERVIEW

The LC65102A and LC65104A are 4-bit, single-chip microprocessors that incorporate 2 Kbyte ROM and 128 × 4-bit RAM, and 4 Kbyte ROM and 256 × 4-bit RAM, respectively, making them ideal for timer controllers, audiovisual equipment and domestic appliances.

The LC65102A and LC65104A comprise one 2-bit and five 4-bit bidirectional I/O ports, a three-wire serial interface, an eight-channel, 8-bit A/D converter and a 14-bit D/A converter that can be configured as separate 6-bit and 8-bit modules or as a single 14-bit module. An on-chip oscillator can be directly connected to either an external crystal or ceramic resonator, or alternatively, an external oscillator can be used.

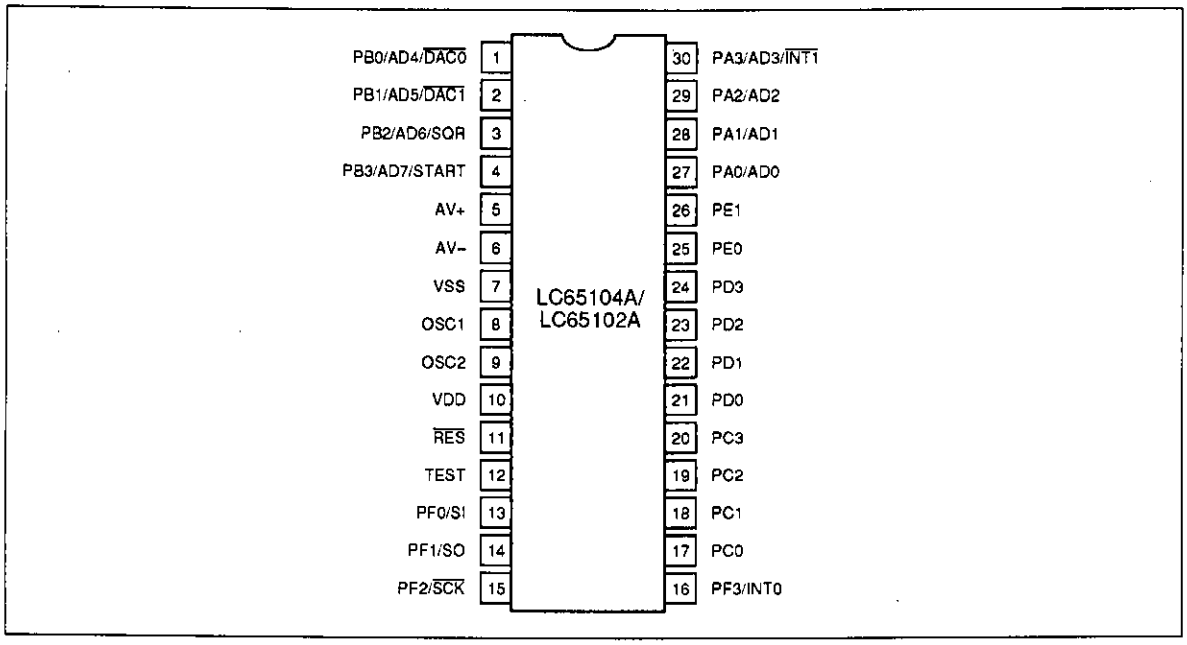
The mask options for the LC65102A and LC65104A comprise a 14-bit general-purpose timer, used to generate pulsewidth modulated output or tone output, a 14-bit clock or overrun watchdog timer, and an AC zero-crossing detector or Schmitt trigger input circuit. Two power-saving standby modes are also provided.

The LC65102A and LC65104A operate over a 2.7 to 6.0 V supply range and are available in 30-pin SDIPs. A 30-pin SMFP is currently under development.

FEATURES

- 77 instructions
- On-chip 2 Kbyte ROM and 128 × 4-bit RAM (LC65102A) and 4 Kbyte ROM and 256 × 4-bit RAM (LC65104A)
- 0.92 µs (4.33 MHz clock and $V_{DD} \geq 4.5$ V) or 1.84 µs (2.17 MHz clock and $V_{DD} \geq 4.0$ V) minimum instruction cycle times
- Software-selectable system clock
- Four banks of eight working registers and 16 flags
- Eight-level stack
- 22 bidirectional I/O lines, including 12 multiplexed lines
- 8-bit precision, eight-channel tracking A/D converter
- 8-bit interval timer for PWM D/A converter and music generator
- 14-bit timer for calendar/clock function
- Separate 6-bit and 8-bit or single 14-bit D/A converter configurations
- Serial I/O interface
- AC zero-crossing detector mask option
- Two external interrupts, two timer interrupts and one serial I/O interrupt
- Wait function allows oscillator to stabilize after reset
- On-chip oscillator supports 4.19 MHz crystal, 400 kHz or 4.0 MHz ceramic resonators
- LC65999 evaluation chip, EVA800/850 emulator, TB65XXX adapter board and LC65PG10X piggy-back connector evaluation tools available
- HALT/HOLD standby functions
- 2.7 to 6.0 V supply operating range
- 30-pin SDIP and 30-pin SMFP (under development)

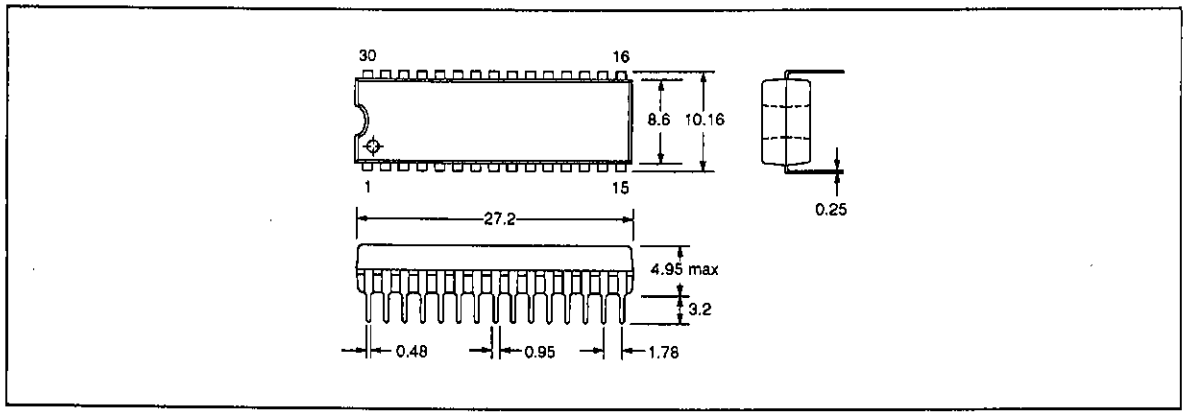
PIN ASSIGNMENT



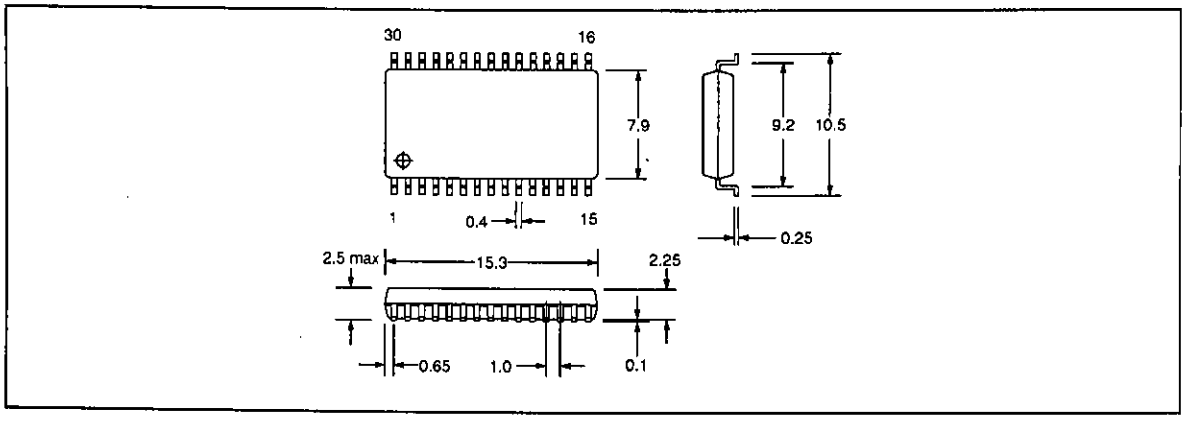
PACKAGE DIMENSIONS

Unit: mm

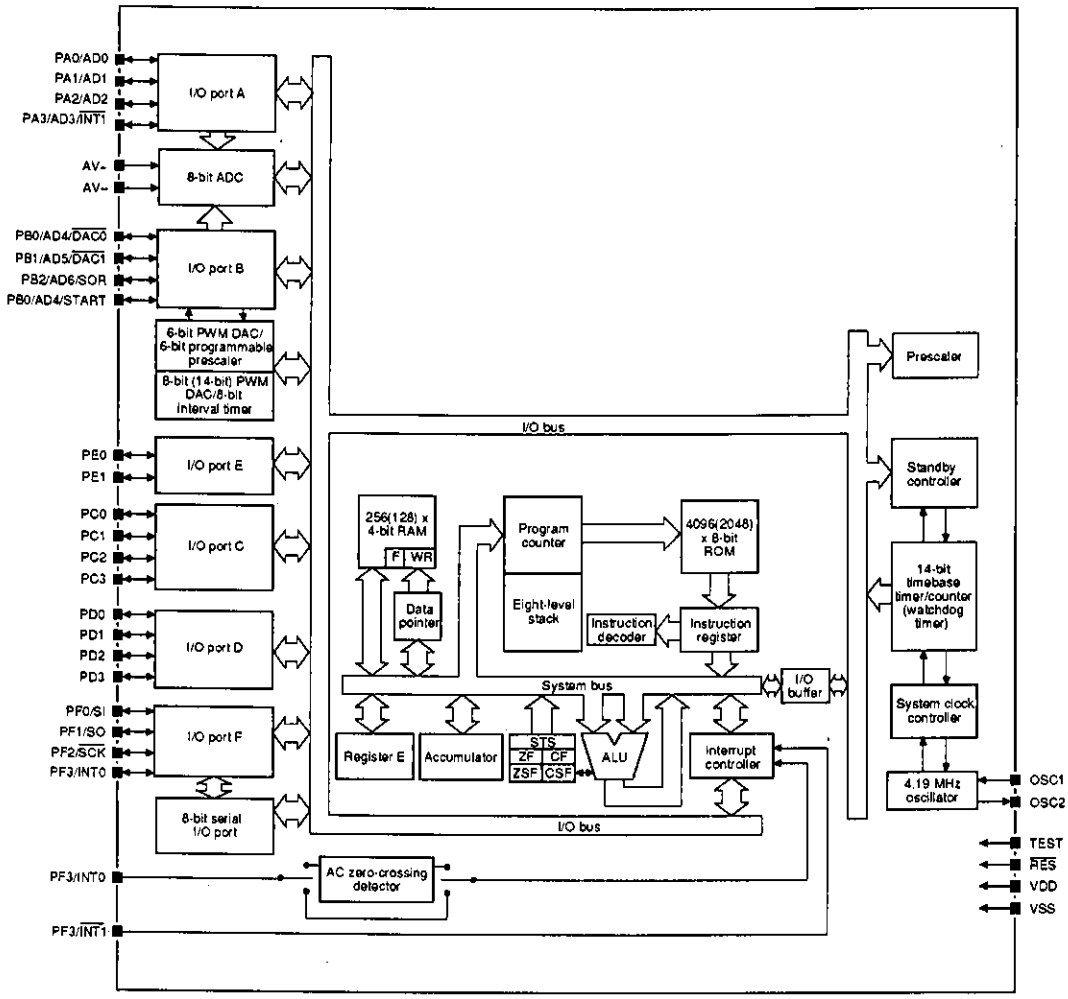
3061-DIP30S



3073A-MFP30S



BLOCK DIAGRAM



Note
Values in parentheses indicate LC65102A RAM and ROM capacities

PIN DESCRIPTION

Number	Name	Description
1	PB0/AD4/$\overline{DAC0}$	4-bit I/O port B multiplexed with A/D converter lines AD4 to AD7, D/A lines $\overline{DAC0}$ and $\overline{DAC1}$, square wave pulse output SQR and standby control line START. Normally HIGH
2	PB1/AD5/$\overline{DAC1}$	
3	PB2/AD6/SQR	
4	PB3/AD7/START	
5	AV+	A/D converter reference voltage input
6	AV−	
7	VSS	Ground
8	OSC1	External crystal or ceramic resonator connection or external clock input
9	OSC2	External crystal or ceramic resonator connection
10	VDD	5 V supply
11	$\overline{RES}$	System reset input. Normally HIGH
12	TEST	Test pin. Normally LOW

Number	Name	Description
13	PF0/SI	4-bit I/O port F multiplexed with serial input and output lines SI and SO, serial clock output $\overline{SCK}$ and interrupt request input INT0. Normally HIGH
14	PF1/SO	
15	PF2/$\overline{SCK}$	
16	PF3/INT0	
17	PC0	4-bit I/O port C
18	PC1	
19	PC2	
20	PC3	
21	PD0	4-bit I/O port D
22	PD1	
23	PD2	
24	PD3	
25	PE0	2-bit I/O port E. Normally HIGH
26	PE1	
27	PA0/AD0	4-bit I/O port A multiplexed with A/D converter input lines AD0 to AD3 and interrupt input $\overline{INT1}$. Normally HIGH
28	PA1/AD1	
29	PA2/AD2	
30	PA3/AD3/$\overline{INT1}$	

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
TEST, $\overline{RES}$ and OSC1 input voltage range	V_{I1}	–0.3 to V_{DD} + 0.3	V
AV^+ input voltage range	V_{I2}	–0.3 to V_{DD} + 0.3	V
AV^- input voltage range	V_{I3}	–0.3 to V_{DD} + 0.3	V
Ports A, B and F3 input/output voltage range	V_{IO1}	–0.3 to V_{DD} + 0.3	V
Ports C, D and E, and F0 to F2 input/output voltage range (open-drain output)	V_{IO2}	–0.3 to 15.0	V
Ports C, D and E, and F0 to F2 input/output voltage range (totem-pole output)	V_{IO3}	–0.3 to V_{DD} + 0.3	V
Ports A, B, E and F peak output current range	I_{OP1}	–2 to 10	mA
Ports C and D peak output current range	I_{OP2}	–2 to 20	mA
Ports A, B, E and F average output current per pin range	I_{OA1}	–2 to 10	mA
Ports C and D average output current per pin range	I_{OA2}	–2 to 20	mA
Ports A, B, E and F average current per port range	ΣI_{OA1}	–24 to 120	mA
Ports C and D average current per port range	ΣI_{OA2}	–20 to 100	mA

Parameter	Symbol	Rating	Unit
30-pin DIP power dissipation	P_D	400	mW
30-pin MFP power dissipation	P_D	200	mW
Operating temperature range	T_{opg}	–40 to 85	deg. C
Storage temperature range	T_{stg}	–55 to 125	deg. C

Recommended Operating Conditions

V_{SS} = 0 V, T_a = 25 deg. C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD}	2.7 to 6.0	V

Electrical Characteristics

V_{DD} = 2.7 to 6.0 V, V_{SS} = 0 V, T_a = –40 to 85 deg. C unless noted otherwise

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD1}	0.92 µs ≤ t_{cyc} < 36 µs	4.5	–	6.0	V
	V_{DD2}	1.84 µs ≤ t_{cyc} < 36 µs	4.0	–	6.0	V
	V_{DD3}	9.8 µs ≤ t_{cyc} < 36 µs	2.7	–	6.0	V
Standby supply voltage	V_{ST}		1.8	–	6.0	V
Port E and F0 to F2 HIGH-level input voltage (open-drain output)	V_{IH1}	n-channel transistor OFF	0.80V_{DD}	–	13.5	V
Port E and F0 to F2 HIGH-level input voltage (totem-pole output)	V_{IH2}	n-channel transistor OFF	0.80V_{DD}	–	V_{DD}	V
Ports A and B HIGH-level input voltage	V_{IH3}	n-channel transistor OFF	1.9	–	V_{DD}	V
Ports C and D HIGH-level input voltage (open-drain output)	V_{IH4}	n-channel transistor OFF, V_{DD} = 4.5 to 6.0 V	0.70V_{DD}	–	13.5	V
		n-channel transistor OFF	0.75V_{DD}	–	13.5	V
Ports C and D HIGH-level input voltage (totem-pole output)	V_{IH5}	n-channel transistor OFF, V_{DD} = 4.5 to 6.0 V	0.70V_{DD}	–	V_{DD}	V
		n-channel transistor OFF	0.75V_{DD}	–	V_{DD}	V
OSC1, START, PF3/INT0 and INT1 HIGH-level input voltage. See note 1.	V_{IH6}	n-channel transistor OFF, external oscillator input. See figure 16.	0.80V_{DD}	–	V_{DD}	V
$\overline{RES}$ HIGH-level input voltage	V_{IH7}	V_{DD} = 4.5 to 6.0 V	0.80V_{DD}	–	V_{DD}	V
		V_{DD} = 1.8 to 6.0 V	0.85V_{DD}	–	V_{DD}	V
Port E and F0 to F2 LOW-level input voltage	V_{IL1}	n-channel transistor OFF, V_{DD} = 4.5 to 6.0 V	V_{SS}	–	0.20V_{DD}	V
		n-channel transistor OFF	V_{SS}	–	0.15V_{DD}	V
Ports A and B LOW-level input voltage	V_{IL2}	n-channel transistor OFF, V_{DD} = 4.5 to 6.0 V	V_{SS}	–	0.5	V
		n-channel transistor OFF	V_{SS}	–	0.35	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Ports C and D LOW-level input voltage	V_{IL3}	n-channel transistor OFF, V_{DD} = 4.5 to 6.0 V	V_{SS}	–	$0.30V_{DD}$	V
		n-channel transistor OFF	V_{SS}	–	$0.25V_{DD}$	V
START LOW-level input voltage	V_{IL4}	V_{DD} = 4.5 to 6.0 V	V_{SS}	–	$0.20V_{DD}$	V
		V_{DD} = 1.8 to 6.0 V	V_{SS}	–	$0.15V_{DD}$	V
OSC1, $\overline{RES}$, PF3/INT0 and $\overline{INT1}$ LOW-level input voltage. See note 1.	V_{IL5}	n-channel transistor OFF, external oscillator input. See figure 16. V_{DD} = 4.5 to 6.0 V	V_{SS}	–	$0.20V_{DD}$	V
		n-channel transistor OFF, external oscillator input. See figure 16.	V_{SS}	–	$0.15V_{DD}$	V
TEST LOW-level input voltage	V_{IL6}	V_{DD} = 4.5 to 6.0 V	V_{SS}	–	$0.30V_{DD}$	V
			V_{SS}	–	$0.25V_{DD}$	V
Ports A, B, C, D, E and F HIGH-level output voltage (totem-pole output)	V_{OH1}	I_{OH} = –50 µA, V_{DD} = 4.5 to 6.0 V	V_{DD} – 1.2	–	–	V
Ports A, B, C, D, E and F HIGH-level output voltage (totem-pole output)	V_{OH2}	I_{OH} = –10 µA	V_{DD} – 0.5	–	–	V
Ports A, B, E and F HIGH-level output voltage	V_{OL1}	I_{OL} = 5 mA, V_{DD} = 4.5 to 6.0 V	–	–	1.5	V
	V_{OL2}	I_{OL} = 1.0 mA, I_{OL} of other ports below 1 mA	–	–	0.5	V
Ports C and D LOW-level output voltage	V_{OL3}	I_{OL} = 15 mA, V_{DD} = 4.5 to 6.0 V	–	–	1.5	V
	V_{OL4}	I_{OL} = 2.0 mA, I_{OL} of other ports below 1 mA	–	–	0.5	V
Port F, INT0, $\overline{INT1}$, $\overline{RES}$ and START hysteresis voltage. See note 1.	V_{HYS}		–	$0.1V_{DD}$	–	V
Ports C, D and E, and F0 to F2 HIGH-level input current (open-drain output)	I_{IH1}	n-channel output transistor OFF (includes output transistor leakage current), V_I = 13.5 V	–	–	5.0	µA
Ports A and B, and F3 HIGH-level input current (open-drain output). See notes 1 and 5.	I_{IH2}	n-channel output transistor OFF (includes output transistor leakage current), V_I = V_{DD}	–	–	1.0	µA
$\overline{RES}$ HIGH-level input current	I_{IH3}	V_I = V_{DD}	–	–	1.0	µA
OSC1 HIGH-level input current	I_{IH4}	V_I = V_{DD}	–	–	10	µA
Ports A, B, C, D, E and F LOW-level input current (open-drain output). See notes 1 and 5.	I_{IL1}	n-channel output transistor OFF, V_I = V_{SS}	–1.0	–	–	µA
Ports A, B, C, D, E and F LOW-level input current (totem-pole output). See notes 1 and 5.	I_{IL2}	n-channel output transistor OFF, V_I = V_{SS}	–1.0	–0.5	–	mA

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{RES}$ LOW-level input current	I_{IL3}	$V_I = V_{SS}$	–60	–25	–	µA
OSC1 LOW-level input current	I_{IL4}	$V_I = V_{SS}$	–10	–	–	
Operating current consumption. See note 4.	I_{DDOP1}	f_{osc} = 4 MHz, divide ratio = 1/1, t_{cyc} = 0.95 µs, V_{DD} = 4.5 to 6.0 V	–	3	6	mA
	I_{DDOP2}	f_{osc} = 4 MHz, divide ratio = 1/2, t_{cyc} = 1.9 µs, V_{DD} = 4.0 to 6.0 V	–	2	4	mA
	I_{DDOP3}	f_{osc} = 4 MHz, divide ratio = 1/32, t_{cyc} = 30.5 µs, V_{DD} = 2.7 V	–	0.3	1.0	mA
	I_{DDOP4}	f_{osc} = 400 kHz, divide ratio = 1/1, t_{cyc} = 10 µs, V_{DD} = 4.0 to 6.0 V	–	0.5	2.0	mA
	I_{DDOP5}	f_{osc} = 400 kHz, divide ratio = 1/1, t_{cyc} = 10 µs, V_{DD} = 2.7 V	–	150	500	µA
Standby current consumption. See note 4.	I_{DDST1}	HALT mode, 4.19 MHz clock, V_{DD} = 6.0 V	–	0.7	1.5	mA
	I_{DDST2}	HALT mode, 4.19 MHz clock, V_{DD} = 2.7 V	–	150	500	µA
	I_{DDST3}	HALT mode, 400 kHz clock, V_{DD} = 6.0 V	–	0.7	1.5	mA
	I_{DDST4}	HALT mode, 400 kHz clock, V_{DD} = 2.7 V	–	100	300	µA
	I_{DDST5}	HOLD mode, V_{DD} = 1.8 V	–	–	1	µA
	I_{DDST6}	HOLD mode, V_{DD} = 6.0 V	–	–	10	µA
Ports A, B, C, D, E and F p-channel MOS output transistor resistance	R_{ifru}	n-channel output transistor OFF, V_{DD} = 5 V, $V_I = V_{SS}$	8	12	30	kΩ
$\overline{RES}$ input pull-up resistance	R_{iu}	V_{DD} = 5 V, $V_I = V_{SS}$	100	–	400	kΩ

Notes

1. This value applies when the AC zero-crossing detector option is not selected.
2. Includes n-channel output transistor leakage current (transistor OFF)
3. Current dissipation values apply to microprocessor circuitry. They do not include currents associated with I/O port transistors.
4. These values do not include I/O port transistor currents.
5. Includes INT0, $\overline{INT1}$ and START

Serial interface

V_{DD} = 4 to 6 V, V_{SS} = 0 V, T_a = –40 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input clock ($\overline{SCK}$) period	t_{CKCY1}		0.8	–	–	µs
Output clock ($\overline{SCK}$) period	t_{CKCY2}	See figure 19.	2.0 × t_{cyc}	–	–	µs
Input clock ($\overline{SCK}$) LOW-level pulsewidth	t_{CKL1}	See figure 19. See note.	0.3	–	–	µs
Output clock ($\overline{SCK}$) LOW-level pulsewidth	t_{CKL2}	See figure 19.	t_{cyc}	–	–	µs
Input clock ($\overline{SCK}$) HIGH-level pulsewidth	t_{CKH1}	See figure 19. See note.	0.3	–	–	µs
Output clock ($\overline{SCK}$) HIGH-level pulsewidth	t_{CKH2}	See figure 19.	t_{cyc}	–	–	µs
SI data setup time	t_{ICK}	Referenced to $\overline{SCK}$ rising edge. See figure 19.	0.2	–	–	µs
SI data hold time	t_{CKI}		0.2	–	–	µs
SO propagation delay	t_{CKO}	Referenced to $\overline{SCK}$ falling edge. 1 kΩ, 50 pF external load. See figure 19.	–	–	0.5	µs

Note

The pullup resistor values should be set so that t_{CKL1} and t_{CKH1} are greater than 0.3 µs.

AC zero-crossing detector input

V_{DD} = 4.5 to 6.0 V, V_{SS} = 0 V, T_a = –40 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input frequency	f_{ZI}		40	–	1,000	Hz
Input voltage	V_{ZI}	C = 1 µF	1.0	–	2.4	V_{p-p}
Detection error	V_{ZA}	60 Hz sinewave input	–	–	±100	mV
HIGH-level input current	I_{IHZ}	$V_I = V_{DD}$	–	–	40	µA
LOW-level input current	I_{ILZ}	$V_I = V_{SS}$	–40	–	–	µA
Threshold voltage	$V_t \times A_{CM}$		0.3 × V_{DD}	–	0.7 × V_{DD}	V
LOW-level input threshold voltage	$V_t \times A_{CL}$		–	$V_t \times A_{CM}$ – 0.2	–	V

Note

Open-drain output with self-bias ON. See figures 21 and 22.

Self-exciting oscillator

V_{DD} = 2.7 to 6.0 V, V_{SS} = 0 V, T_a = –40 to 85 deg. C unless noted otherwise

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Crystal resonator frequency	f_{OSCX}	See figure 14. See note 1.	–	4.19	–	MHz
Crystal oscillator start delay	t_{MXS}	See figure 15.	–	–	20	ms
Ceramic resonator frequency	f_{OSCCF}	See figure 14. See note 1.	392	400	408	kHz
Ceramic oscillator start delay	t_{MCFS}	See figure 15.	–	–	10	ms
Instruction cycle time	t_{CYC}	See note 1.	0.92	–	36	µs
External oscillator frequency	f_{XOSC}	See note 1.	0.39	–	4.33	MHz
External oscillator pulsewidth	t_{WOSCCH}	V_{DD} = 4.5 to 6.0 V. See figure 16.	70	–	–	ns
	t_{WOSCCL}	See figure 16.	140	–	–	ns
External oscillator rise time	t_{OSCR}	See figure 16.	–	–	30	ns
External oscillator fall time	t_{OSCF}					ns

Notes

1. The frequency is limited by the supply voltage, operating cycle time and frequency divider ratio.
2. Oscillator constants are listed in table 3.

A/D converter

V_{DD} = 5.0 V ±10%, V_{SS} = 0 V, T_a = –40 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Resolution			–	8	–	bit
Absolute precision		$AV^+ = V_{DD}$, $AV^- = V_{SS}$	–	±1	±2	lsb
Zero-scale error	E_{ZS}		–	–	±1	lsb
Full-scale error	E_{FS}		–	–	±1	lsb
Conversion time	t_{CAD}	1/1 conversion speed = 26 × t_{cyc} (t_{cyc} = 0.92 to 12 µs)	24	–	312	µs
		1/2 conversion speed = 51 × t_{cyc} (t_{cyc} = 0.92 to 12 µs)	40	–	612	µs
Input reference voltage	AV^+		AV^-	–	V_{DD}	V
	AV^-		V_{SS}	–	AV^+	V
Input reference current	I_{RIF}	$AV^+ = V_{DD}$, $AV^- = V_{SS}$	75	150	300	µA
Analog input voltage	V_{AI}		AV^-	–	AV^+	V
Analog input current	I_{AI}	Includes output OFF-state leakage current, $V_{AI} = V_{DD}$	–	–	1	µA
		$V_{AI} = V_{SS}$	–1	–	–	µA

Comparator

V_{DD} = 5.0 V ±10%, V_{SS} = 0 V, T_a = −40 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Comparison precision	V_{CECON}	$AV^+ = V_{DD}$, $AV^- = V_{SS}$	–	±1	±2	lsb
Threshold voltage	V_{THCON}		AV^-	–	AV^+	V
Input voltage	V_{INCON}		AV^-	–	AV^+	V
Input reference voltage	AV^+		AV^-	–	V_{DD}	V
	AV^-		V_{SS}	–	AV^+	V
Comparison time	t_{CC}	1/1 comparison = 12 × t_{cyc} (t_{cyc} = 0.92 to 12 µs)	11	–	144	µs
		1/2 comparison = 23 × t_{cyc} (t_{cyc} = 0.92 to 12 µs)	21	–	276	µs

INSTRUCTION SET

Abbreviations

AC	Accumulator
ACt	Accumulator bit t
CF	Carry flag
CTL	Control register
DP	Data pointer
E	E register
bFn	Flag bit n
GP(DP)	Pseudo port specified by DP
I_0 to I_3	Immediate data
M	Memory
M(DP)	Memory addressed by DP
MSTEN	Master interrupt enable flag
P(DPL)	I/O port specified by DPL
PC	Program counter
STACK	Stack register
t_0, t_1	Immediate data which specifies the bit within the addressed nibble as follows.

t_1	t_0	Bit
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

bAt, bHa, bLa	Working registers
ZF	Zero flag
( ), [ ]	Indicates memory or register contents
←	Transfer in indicated direction
+	Add
−	Subtract
Λ	AND
V	OR
∀	XOR

Code	Description	Operation	Flag		Instruction code								Bytes	Cycles
					D7	D6	D5	D4	D3	D2	D1	D0		
Accumulator														
CLA	Clear AC. See note 1.	AC ← 0	ZF		1	1	0	0	0	0	0	0	1	1
CLC	Clear CF	CF ← 0		CF	1	1	1	0	0	0	0	1	1	1
STC	Set CF	CF ← 1		CF	1	1	1	1	0	0	0	1	1	1
CMA	Complement AC	AC ← $\overline{(AC)}$	ZF		1	1	1	0	1	0	1	1	1	1
INC	Increment AC	AC ← (AC) + 1	ZF	CF	0	0	0	0	1	1	1	0	1	1
DEC	Decrement AC	AC ← $\overline{(AC)}$ − 1	ZF	CF	0	0	0	0	1	1	1	1	1	1
RAL	Rotate AC left through CF	AC_0 ← (CF).AC_n + 1 ← (AC_n). CF ← (AC_3)	ZF	CF	0	0	0	0	0	0	0	1	1	1
TAE	Transfer AC to E	E ← (AC)			0	0	0	0	0	0	1	1	1	1
XAE	Exchange AC with E	(AC) ↔ (E)			0	0	0	0	1	1	0	1	1	1
Memory														
INM	Increment M	M(DP) ← [M(DP)] + 1	ZF	CF	0	0	1	0	1	1	1	0	1	1
DEM	Decrement M	M(DP) ← [M(DP)] − 1	ZF	CF	0	0	1	0	1	1	1	1	1	1
SMB bit	Set M data bit	M(DP,B_1B_0) ← 1			0	0	0	0	1	0	B_1	B_0	1	1
RMB bit	Reset M data bit	M(DP,B_1B_0) ← 0	ZF		0	0	1	0	1	0	B_1	B_0	1	1
Arithmetic and compare														
AD	Add M to AC	AC ← (AC) + [M(DP)]	ZF	CF	0	1	1	0	0	0	0	0	1	1
ADC	Add M to AC with CF	AC ← (AC) + [M(DP)] + (CF)	ZF	CF	0	0	1	0	0	0	0	0	1	1
DAA	Decimal adjust AC in addition	AC ← (AC) + 6	ZF		1	1	1	0	0	1	1	0	1	1
DAS	Decimal adjust AC in subtraction	AC ← (AC) + 10	ZF		1	1	1	0	1	0	1	0	1	1
EXL	Exclusive OR M with AC	AC ← (AC) ∀ [M(DP)]	ZF		1	1	1	1	0	1	0	1	1	1
AND	AND M to AC	AC ← (AC) ∧ [M(DP)]	ZF		1	1	1	0	0	1	1	1	1	1
OR	OR M with AC	AC ← (AC) ∨ [M(DP)]	ZF		1	1	1	0	0	1	0	1	1	1
CM	Compare AC with M. See table 1.	$\overline{[M(DP)]}$ + (AC) + 1	ZF	CF	1	1	1	1	1	0	1	1	1	1
CI data	Compare AC with immediate data. See table 2.	$\overline{I_3I_2I_1I_0}$ + (AC) + 1	ZF	CF	0 0	0 1	1 0	0 0	1 I_3	1 I_2	0 I_1	0 I_0	2	2
CLI data	Compare DP_L with immediate data	(DP_L) ∀ $I_3I_2I_1I_0$	ZF		0 0	0 1	1 0	0 1	1 I_3	1 I_2	0 I_1	0 I_0	2	2
Load and store														
LI data	Load AC with immediate data. See note 1.	AC ← $I_3I_2I_1I_0$	ZF		1	1	0	0	I_3	I_2	I_1	I_0	1	1
S	Store AC to M	M(DP) ← (AC)			0	0	0	0	0	0	1	0	1	1
L	Load AC from M	AC ← [M(DP)]	ZF		0	0	1	0	0	0	0	1	1	1
XM data	Exchange AC with M, then modify DP_H with immediate data. The zero flag is determined by comparing the data pointer high nibble with $0M_2M_1M_0$.	(AC) [M(DP)] DP_H ← (DP_H) ∀ $0M_2M_1M_0$	ZF		1	0	1	0	0	M_2	M_1	M_0	1	2
X	Exchange AC with M. The zero flag is determined by the contents of the data pointer high nibble.	(AC) harr [M(DP)]	ZF		1	0	1	0	0	0	0	0	1	2
XI	Exchange AC with M, then increment DP_L. The zero flag is determined by the contents of the data pointer low nibble.	(AC) ↔[M(DP)] DP_L ← (DP_L) + 1	ZF		1	1	1	1	1	1	1	0	1	2
XD	Exchange AC with M, then decrement DP_L. The zero flag is determined by the low nibble of the data pointer.	(AC) ↔[M(DP)] DP_L ← (DP_L) − 1	ZF		1	1	1	1	1	1	1	1	1	2
RTBL	Read table data from program ROM	AC.E ↔ROM (PCh. E.AC)			0	1	1	0	0	0	1	1	1	2

Code	Description	Operation	Flag		Instruction code								Bytes	Cycles
					D7	D6	D5	D4	D3	D2	D1	D0		
Data pointer manipulation														
LDZ data	Load DP_H with zero and DP_L with immediate data, respectively.	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3I_2I_1I_0$			1	0	0	0	I_3	I_2	I_1	I_0	1	1
LHI data	Load DP_H with immediate data	$DP_H \leftarrow I_3I_2I_1I_0$			0	1	0	0	I_3	I_2	I_1	I_0	1	1
IND	Increment DP_L	$DP_L \leftarrow (DP_L) + 1$	ZF		1	1	1	0	1	1	1	0	1	1
DED	Decrement DP_L	$DP_L \leftarrow (DP_L) - 1$	ZF		1	1	1	0	1	1	1	1	1	1
TAL	Transfer AC to DP_L	$DP_L \leftarrow (AC)$			1	1	1	1	0	1	1	1	1	1
TLA	Transfer DP_L to AC	$(AC) \leftarrow (DP_L)$	ZF		1	1	1	0	1	0	0	1	1	1
XAH	Exchange AC with DP_H	$(AC) \leftrightarrow (DP_H)$			0	0	1	0	0	0	1	1	1	1
Working register														
XA_t XA0 XA1 XA2 XA3	Exchange AC with working register bA_t	$(AC) \leftrightarrow (bA0)$ $(AC) \leftrightarrow (bA1)$ $(AC) \leftrightarrow (bA2)$ $(AC) \leftrightarrow (bA3)$			1 1 1 1	1 1 1 1	1 1 1 1	0 0 0 0	t_1 0 1 0	t_0 0 1 1	0 0 0 0	0 0 0 0	1 1 1 1	1 1 1 1
XH_a XH0 XH1	Exchange DP_H with working register bH_a	$(DP_H) \leftrightarrow (bH0)$ $(DP_H) \leftrightarrow (bH1)$			1 1	1 1	1 1	1 1	1 1	a 0 1	0 0	0 0	1 1	1 1
XL_a XL0 XL1	Exchange DP_L with working register bL_a	$(DP_L) \leftrightarrow (bL0)$ $(DP_L) \leftrightarrow (bL1)$			1 1	1 1	1 1	1 1	0 0	a 0 1	0 0	0 0	1 1	1 1
SRBA	Set register bank address	$RBF \leftarrow I_1I_0$ of SB			1	1	1	1	0	0	1	0	1	1
Bit manipulation														
SFB flag	Set flag bit	$bF_n \leftarrow 1$			0	1	0	1	B_3	B_2	B_1	B_0	1	1
RFB flag	Clear flag bit. The flags are organized in 16 × 4-bit nibbles from 0F0H to 0F3H to 3FCH to 3FFH. The zero flag is determined by the contents of the specified nibble.	$bF_n \leftarrow 0$	ZF		0	0	0	1	B_3	B_2	B_1	B_0	1	1
Jump and subroutine														
JMP addr	Jump in the current bank. The bank changes when a JMP instruction is followed by a BANK instruction.	$PC \leftarrow PC_{11}$ (or $\overline{PC_{11}}$) $P_{10}P_9P_8P_7$ $P_{10}P_{10}P_{10}P_3\ P_2P_1P_0$			0 P_7	1 P_6	1 P_5	0 P_4	1 P_3	P_{10} P_2	P_9 P_1	P_8 P_0	2	2
JPEA	Jump in the current page modified by E and AC	PC_7 to $0 \leftarrow (E.AC)$			1	1	1	1	1	0	1	0	1	1
CZP addr	Call subroutine in the zero page	$STACK \leftarrow (PC) + 1$ PC_{11} to 6, PC_1 to $0 \leftarrow 0$ PC_5 to $2 \leftarrow$ $P_3P_2P_1P_0$			1	0	1	1	P_3	P_2	P_1	P_0	1	1
CAL addr	Call subroutine in the zero bank	$STACK \leftarrow (PC) + 2$ PC_{11} to $0 \leftarrow 00$ $P_{10}P_9P_8P_7\ P_6P_5P_4P_3$ $P_2P_1P_0$			1 P_7	0 P_6	1 P_5	0 P_4	1 P_3	P_{10} P_2	P_9 P_1	P_8 P_0	2	2
RT	Return from subroutine	$PC \leftarrow (STACK)$			0	1	1	0	0	0	1	0	1	1
RTI	Return from interrupt routine	$PC \leftarrow (STACK)$ $CF\ ZF \leftarrow CSF.ZSF$	ZF	CF	0	0	1	0	0	0	1	0	1	1
BANK	Change bank	$PC_{11} \leftarrow (\overline{PC_{11}})$ GP(DP)			1	1	1	1	1	1	0	1	1	1
SB	Set bank	$RBF \leftarrow I_1I_0$			0	1	1	0	0	1	I_1	I_0	1	1
Branch														
BA_t addr	Branch on AC bit. Immediate data t_0 and t_1 is appended to BA, which is followed by the program counter branch address P_0 to P_7.	PC_7 to $0 \leftarrow$ $P_7P_6P_5P_4\ P_3P_2P_1P_0$ if $AC_t = 1$			0 P_7	1 P_6	1 P_5	1 P_4	0 P_3	0 P_2	t_1 P_1	t_0 P_0	2	2
BNA_t addr	Branch on no AC bit. Immediate data t_0 and t_1 is appended to BNA, which is followed by the program counter branch address P_0 to P_7.	PC_7 to $0 \leftarrow$ $P_7P_6P_5P_4\ P_3P_2P_1P_0$ if $AC_t = 0$			0 P_7	0 P_6	1 P_5	1 P_4	0 P_3	0 P_2	t_1 P_1	t_0 P_0	2	2

Code	Description	Operation	Flag		Instruction code								Bytes	Cycles
					D7	D6	D5	D4	D3	D2	D1	D0		
BM$_t$ addr	Branch on M bit. Immediate data t0 and t1 is appended to BM, which is followed by the program counter branch address P0 to P7.	PC7 to 0 ← P7P6P5P4 P3P2P1P0 if [M(DP,t1t0)] = 1			0 P7	1 P6	1 P5	1 P4	0 P3	1 P2	t1 P1	t0 P0	2	2
BNM$_t$ addr	Branch on no M bit. Immediate data t0 and t1 is appended to BNM, which is followed by the program counter branch address P0 to P7.	PC7 to 0 ← P7P6P5P4 P3P2P1P0 if [M(DP,t1t0)] = 0			0 P7	0 P6	1 P5	1 P4	0 P3	1 P2	t1 P1	t0 P0	2	2
BP$_t$ addr	Branch on port bit. Immediate data t0 and t1 is appended to BP, which is followed by the program counter branch address P0 to P7.	PC7 to 0 ← P7P6P5P4 P3P2P1P0 if [P(DPL,t1t0)] = 1 or [GP(DP,t1t0)] = 1			0 P7	1 P6	1 P5	1 P4	1 P3	0 P2	t1 P1	t0 P0	2	2
BNP$_t$ addr	Branch on no port bit. Immediate data t0 and t1 is appended to BNP, which is followed by the program counter branch address P0 to P7.	PC7 to 0 ← P7P6P5P4 P3P2P1P0 if [P(DPL,t1t0)] = 0 or [GP(DP,t1t0)] = 0			0 P7	0 P6	1 P5	1 P4	1 P3	0 P2	t1 P1	t0 P0	2	2
BC addr	Branch on CF	PC7 to 0 ← P7P6P5P4 P3P2P1P0 if CF = 1			0 P7	0 P6	1 P5	1 P4	1 P3	1 P2	1 P1	0 P0	2	2
BNC addr	Branch on no CF	PC7 to 0 ← P7P6P5P4 P3P2P1P0 if CF = 0			0 P7	0 P6	1 P5	1 P4	1 P3	1 P2	1 P1	1 P0	2	2
BZ addr	Branch on ZF	PC7 to 0 ← P7P6P5P4 P3P2P1P0 if ZF = 1			0 P7	1 P6	1 P5	1 P4	1 P3	1 P2	1 P1	0 P0	2	2
BNZ addr	Branch on no ZF	PC7 to 0 ← P7P6P5P4 P3P2P1P0 if ZF = 0			0 P7	0 P6	1 P5	1 P4	1 P3	1 P2	1 P1	0 P0	2	2
BF$_n$ addr	Branch on flag bit. Immediate data n0, n1, n2 and n3 is appended to BF, which is followed by the program counter branch address P0 to P7.	PC7 to 0 ← P7P6P5P4 P3P2P1P0 if bF$_n$ = 1			1 P7	1 P6	0 P5	1 P4	n3 P3	n2 P2	n1 P1	n0 P0	2	2
BNF$_n$ addr	Branch on no flag bit. Immediate data n0, n1, n2 and n3 is appended to BNF, which is followed by the program counter branch address P0 to P7.	PC7 to 0 ← P7P6P5P4 P3P2P1P0 if bF$_n$ = 0			1 P7	0 P6	0 P5	1 P4	n3 P3	n2 P2	n1 P1	n0 P0	2	2
Input/output														
IP	Input port to AC	AC ← [P(DPL)] or [GP(DP)]	ZF		0	0	0	0	1	1	0	0	1	1
OP	Output AC to port	P(DPL) or GP(DP) ← (AC)			0	1	1	0	0	0	0	1	1	1
SPB bit	Set port bit. The contents of register E are lost.	P(DPL,B1B0) or GP(DP,B1B0) ← 1			0	0	0	0	0	1	B1	B0	1	2
RPB bit	Reset port bit. The contents of register E are lost.	P(DPL,B1B0) or GP(DP,B1B0) ← 0	ZF		0	0	1	0	0	1	B1	B0	1	2
Miscellaneous														
SCTL bit	Set control register bit. See note 2.	CTL, B3B2B1B0 ← 1 or MSTEN ← 1			0 1	0 0	1 0	0 0	1 B3	1 B2	0 B1	0 B0	2	2
RCTL bit	Reset control register bit. See note 2.	CTL, B3B2B1B0 ← 0 or MSTEN ← 0	ZF		0 1	0 0	1 0	0 1	1 B3	1 B2	0 B1	0 B0	2	2
HALT	Halt	Halt, Hold			1	1	1	1	0	1	1	0	1	1
NOP	No operation	No operation			0	0	0	0	0	0	0	0	1	1

Notes

1. After LI and CLA instructions are executed in succession, subsequent instructions are NOPs.
2. $B_3B_2B_1B_0$ = 0000B to 1000B

Table 1. Magnitude conditions

Magnitude condition	CF	ZF
[M(DP)] > (AC)	0	0
[M(DP)] = (AC)	1	1
[M(DP)] < (AC)	1	0

Table 2. Magnitude conditions

Magnitude condition	CF	ZF
$I_3I_2I_1I_0$ > (AC)	0	0
$I_3I_2I_1I_0$ = (AC)	1	1
$I_3I_2I_1I_0$ < (AC)	1	0

USER MASK OPTIONS

The following user-specified mask options are available.

Oscillator Circuit

- Ceramic resonator
- Crystal resonator
- External oscillator

System Clock Divide Ratio

The 1/1 or 1/32 frequency divider ratio mask options can be selected as the default ratios following a reset. The 1/1 ratio is used for the 390 kHz to 4330 kHz external clock input or the 400 kHz ceramic resonators. The 1/32 ratio is used for the 4.19 MHz crystal or the 4.0 MHz ceramic resonators.

Precautions

The evaluation chip has a default frequency divider ratio of 1/32 after reset, and the production chip, 1/1 after reset, unless 1/32 has been specified as a mask option. A four-step routine in the program header is used to change the frequency divider ratio.

Port C and D Output State Select

Port C and D outputs can all be cleared to 0 or set to 1 after a reset.

Watchdog Reset Circuit

A watchdog reset circuit generates interrupts which allows recovery from program runaways. The processor is programmed to reset the interrupt request flag at fixed intervals.

AC Zero-crossing Detector or Schmitt Trigger Input

The bidirectional port F bit (PF3) and interrupt request 0 (INT0) are multiplexed on PF3/INT0. This mask option allows the INT0 line to connect to either a Schmitt trigger input circuit or an AC zero-crossing detector circuit as shown in figure 1.

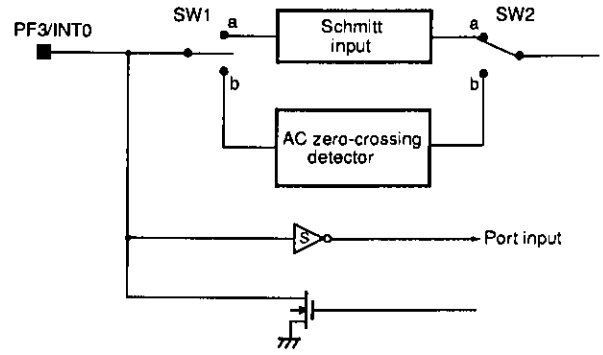


Figure 1. AC zero-crossing detector circuit

Open-drain or Totem-pole Output

I/O port output drivers can have either open-drain or totem-pole configurations as shown in figures 2 and 3. I/O port outputs should be tied LOW if open-drain output is selected.

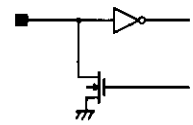


Figure 2. Open-drain output

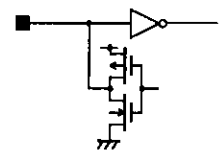


Figure 3. Totem-pole output

Option Code Specification

The client specifies mask options in an EPROM together with the program code. A cross-assembler is available for the LC65102A and LC65104A that allows these options to be specified interactively. The address map shown in figure 4 should be used if the EPROM is programmed manually, resulting in the same format generated by the cross-assembler. Either 2764 or 27128 EPROMs can be used.

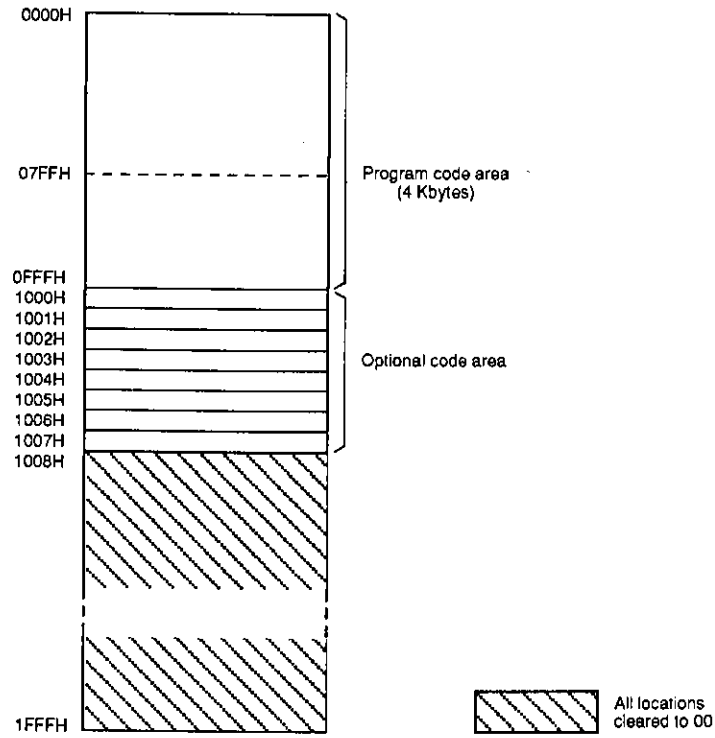


Figure 4. EPROM address map

Note

The memory locations 800H to FFFH of LC65102 should be cleared to 00 during development.

Option codes

Figures 5 to 12 show how option codes are related to their corresponding functions.

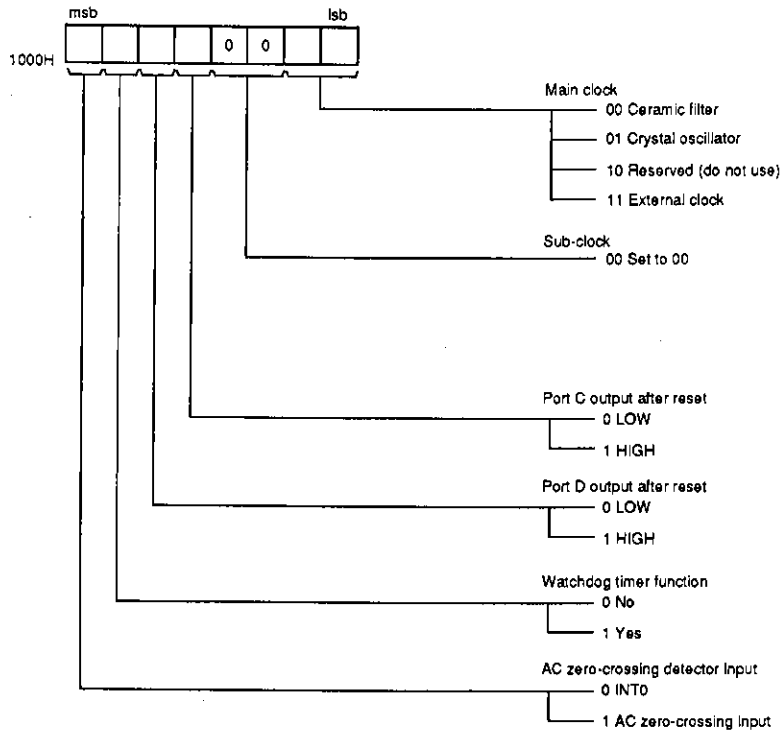


Figure 5. Bit allocation

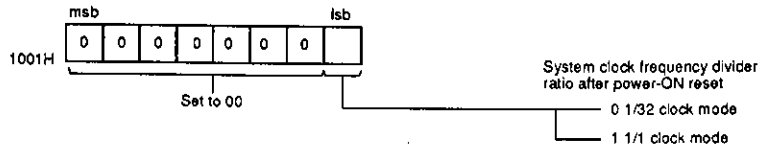


Figure 6. 1001H

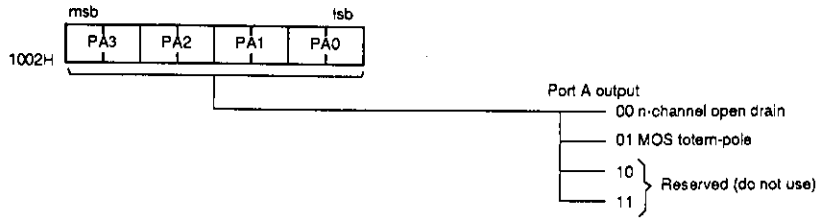


Figure 7. 1002H

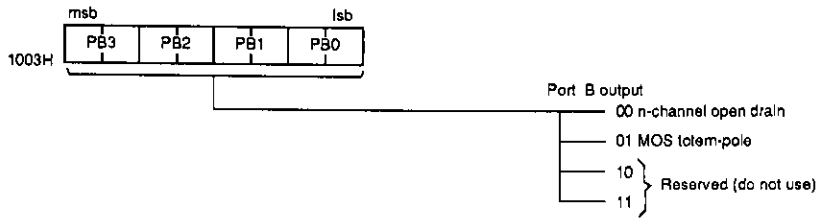


Figure 8. 1003H

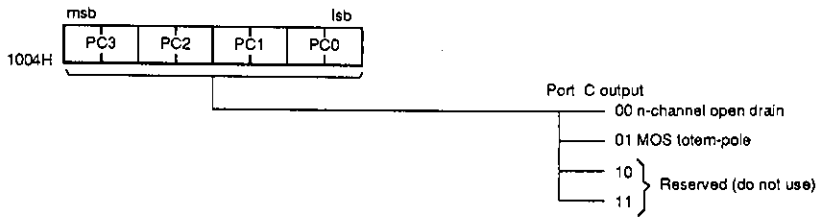


Figure 9. 1004H

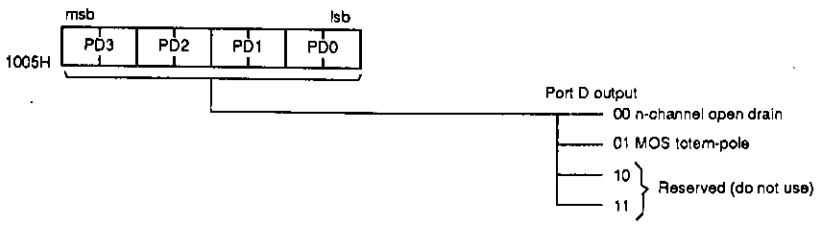


Figure 10. 1005H

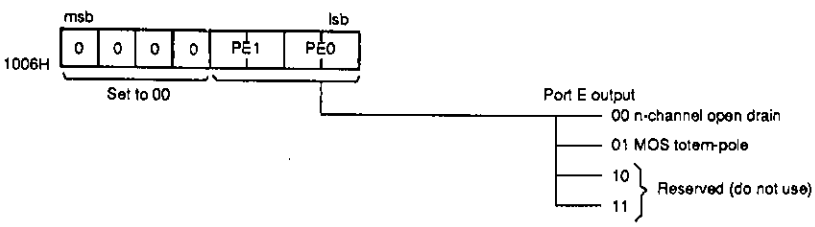


Figure 11. 1006H

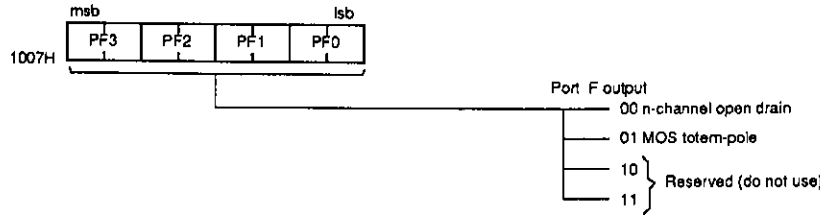


Figure 12. 1007H

DEVELOPMENT SYSTEM

The development system available for the LC65102A and LC65104A comprises the following aids.

- LC65104A/LC65102A User's Manual
- EVA850/800-LC651XX/2XX/3XX/4XX Development Tools Manual
- Development tools

Development Tools

The development tools comprise an MS-DOS based cross-assembler (LC65S.EXE) for program development, an evaluation chip (LC65999), piggyback connector (LC65PG10X), and emulator (EVA-800 or EVA-850 main unit and evaluation chip board) for program evaluation as shown in figure 13.

Notes

1. MS-DOS is a trademark of Microsoft Corporation.
2. Upgrades of the EVA-800 or EVA-850 emulators are indicated by an alphabetic character appended to the emulator name.

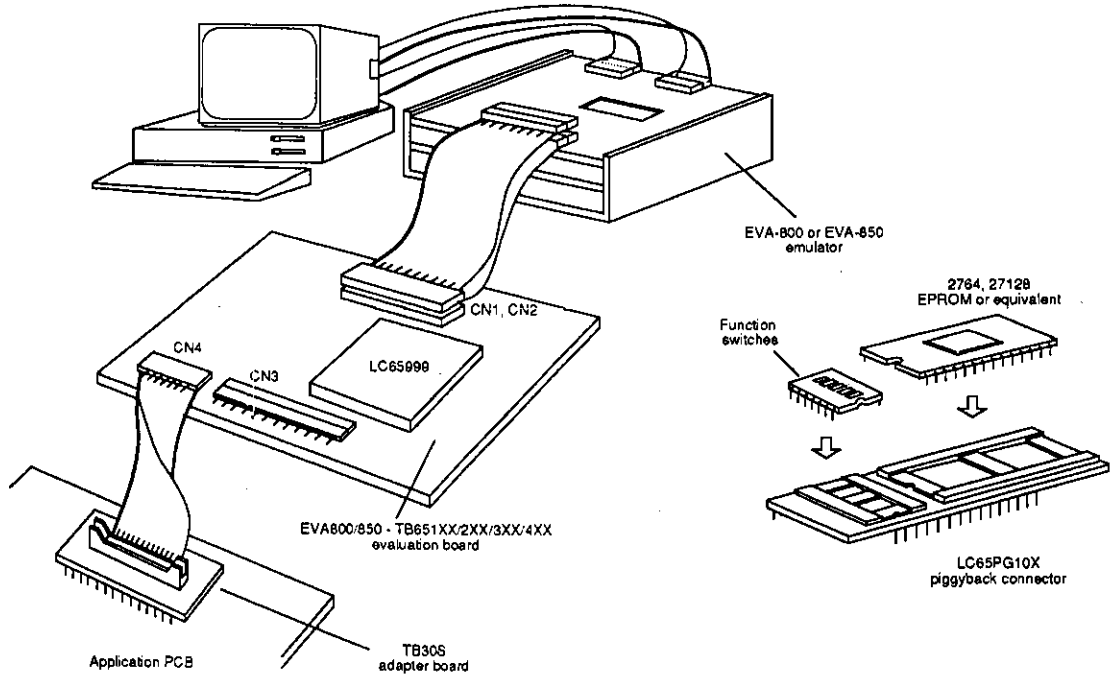


Figure 13. Development system components

Evaluation Notes

The following guidelines should be observed when evaluating programs for the LC65102A/LC65104A using the LC65999 and the LC65PG10X.

Selection

RAM capacity

The RC and RC2 pins are used to select RAM capacity. The LC65102A has a 128 × 4-bit RAM, and the LC65104A, a 256 × 4-bit RAM. The evaluation chip can have either.

Stack nesting

The STC pin is used to select the number of stack nesting levels. The LC65102A and LC65104A support eight levels of nesting.

Ports C, D, E and F output configuration

Ports C, D, E and F have 15 V breakdown-voltage, medium-current drive I/O circuits. The C/FLSEL pin of the evaluation tool is used to select the I/O configuration of ports C and D which can be either p-channel, high voltage or n-channel. Port F output drivers PF0 to PF2 have normal breakdown voltage I/O circuits when masked for the totem-pole configuration, and output driver PF3, in either totem-pole or open-drain configurations.

Mask options

Oscillator circuit

The resonator should be connected to OSC1 and OSC2. The oscillator type is selected by setting jumpers on the evaluation board. The simulation chip is identical to a volume-produced chip.

Port C and D after reset

The four bits of port C and D can be specified to go either all HIGH or all LOW following reset. The CHL pin is used to select the level for port C, and the DHL pin to select the level for port D.

Watchdog reset function

Specify whether to implement the watchdog reset function using the timer or not. The WDC pin is used to select or deselect the watchdog reset function.

AC zero-crossing detector

Specify whether or not to implement the AC zero-crossing detector input circuit on PF3/INT0.

The ACZ/INT0 pin is used to select or deselect the AC zero-crossing detector.

Open-drain or totem-pole output

Specify either totem-pole or open-drain configuration for each output. All evaluation chip ports have n-channel, open-drain outputs. Pull-up resistors of 10 kΩ should be connected to the ports on the simulation and evaluation chips.

Pull-up resistor configuration

The evaluation and simulation chips have open-drain outputs which require external pull-up resistors. When the outputs are LOW, there is continuous current drain through the pull-up resistors. No external pull-up resistors are required and only leakage currents flow in the output transistors if the totem-pole output option is selected for volume-produced chips.

Oscillator circuit

The circuit design and characteristics for evaluation chips differ from those for volume-produced chips. As a result, wiring capacitance may lead to unstable oscillation.

The external components should be trimmed as necessary to obtain stable oscillation.

Operating requirements

Detailed evaluation of the frequency characteristics and current consumption should be carried out using engineering samples ES and commercial samples CS.

The supply voltage should be restricted within the range of the EPROM and connected LSIs. The supply should be 5 V ±5% to ensure that rated voltages are not exceeded. However, this makes it impossible to evaluate circuit operation over the entire supply voltage range of volume-produced chips.

The guaranteed ambient operating temperature range is 10 to 40 deg. C.

The LC65102A has a 2 Kbyte ROM, allowing jumps to any address using the JMP instruction. The LC65104A has a 4 Kbyte ROM, allowing jumps to any address using either a single JMP instruction or a BANK followed by JMP instruction.

External ROM up to 8 Kbytes can be used, allowing jumps to any address using either an SB followed by JMP instruction, a BANK followed by JMP instruction, or a single JMP instruction. Ensure that the program does not exceed 2 Kbytes for the LC65102A or 4 Kbytes for the LC65104A.

DESIGN NOTES

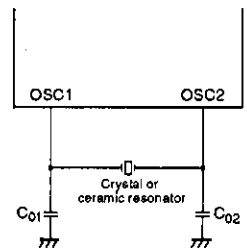


Figure 14. Oscillator circuit

Table 3. Guaranteed oscillator constants

Resonator	Vendor	Part description	C_{O1}	C_{O2}	Unit
4.194304 MHz crystal	Kinseki	HC-49/U C_L = 13.2 pF	18	18	pF
4.0 MHz ceramic resonator	Murata	CSA4.00MG	33	33	pF
		CST4.00MGW. See note 3.	None	None	
	Kyocera	KBR-4.0MS	33	33	
		KBR-4.0MES. See note 3.	None	None	
	Fujicera	POF-4.00	33	33	
400 kHz ceramic resonator	Murata	CSB400P	330	330	pF
	Kyocera	KBR-400B	330	330	
	Fujicera	POE-400	330	330	

Notes

1. Values of CO1 and CO2 (including wiring capacitance when installed) should be within ±10% of specifications.
2. CL is the resonator's built-in capacitor value
3. Three-pin resonator with built-in capacitor

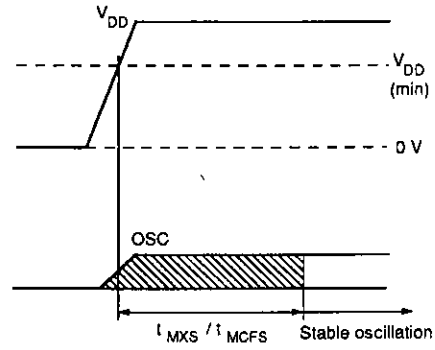


Figure 15. Oscillator start delay

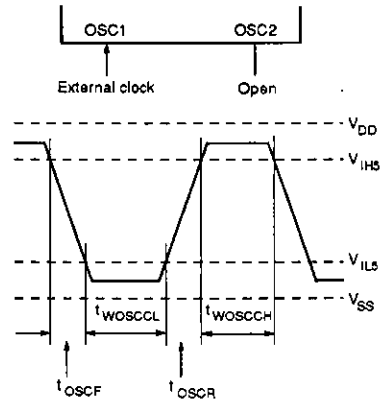


Figure 16. External clock input timing

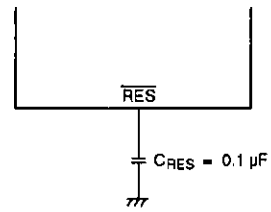


Figure 17. Reset circuit

Note

The reset time is 10 to 100 ms when C_{RES} = 0.1 µF, assuming a power supply with zero rise time. C_{RES} should be selected so that the reset time is greater than the main oscillator start delay if the power supply rise time is excessive.

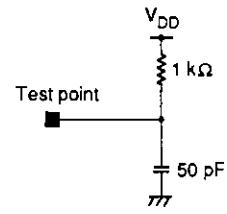


Figure 18. Serial output load

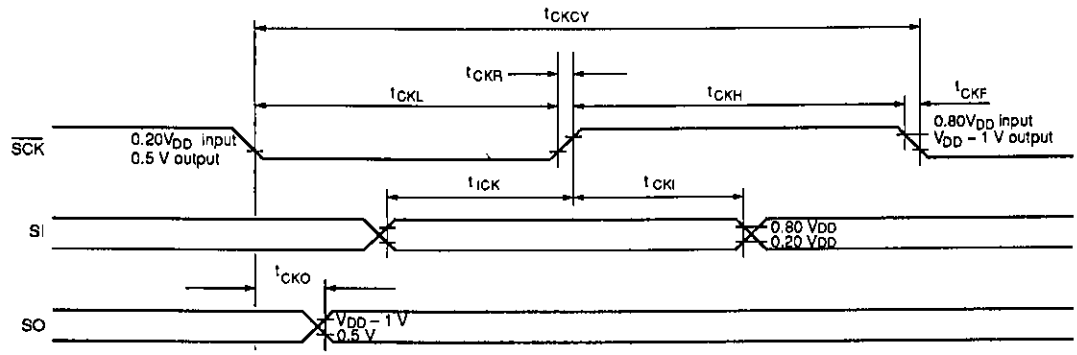


Figure 19. Serial I/O timing

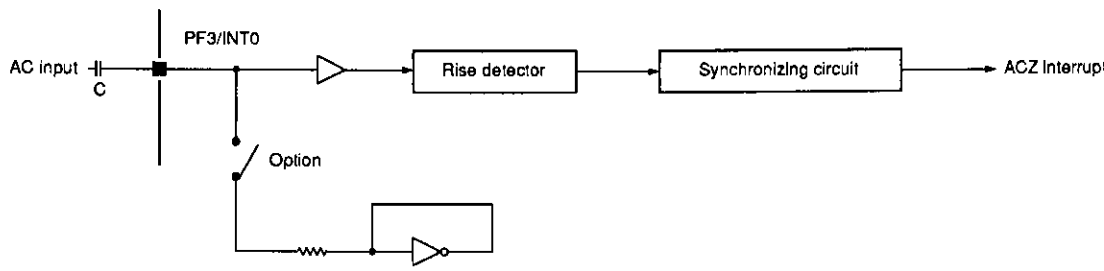


Figure 20. AC zero-crossing detector

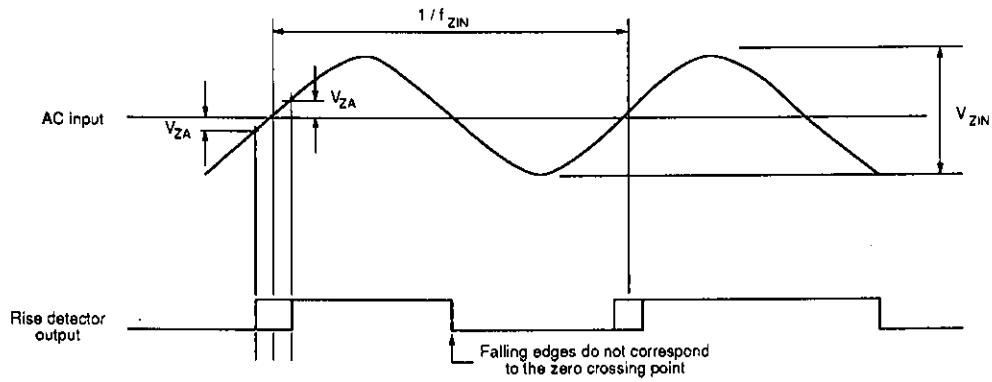


Figure 21. AC zero-crossing timing

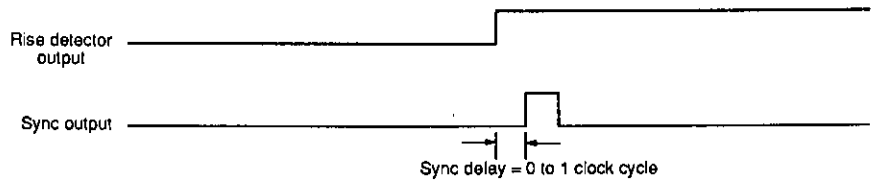


Figure 22. AC zero-crossing sync delay

PROGRAMMING NOTES

The following guidelines should be observed when developing programs for the LC65102A/LC65104A.

System Clock Functions

System clock mode

The LC65102A/LC65104A provides three software-selectable clock modes. Clock modes cannot be changed if the 1/1 frequency divider ratio after reset option is selected.

- Clock 1/1 mode (t_{cyc} = 0.95 µs)
- Clock 1/2 mode (t_{cyc} = 1.90 µs)
- Clock 1/32 mode (t_{cyc} = 30.6 µs)

Notes

1. These values apply for a main clock frequency of 4.19 MHz.
2. A clock signal must be supplied at system startup.

System clock switching mode

The system clock source is selected by the clock mode flags (CMF), a two-bit location in the control register. The default system clock frequency divider ratio after reset is 1/32.

Clock mode flags (CMF)	Clock divide ratio
0	Main clock × 1/32 (default on reset)
1	Main clock × 1/1. See note 3.
2	Main clock × 1/2
3	Do not use

Notes

1. Ensure that the clock oscillator is stable or an external clock signal is applied before changing modes.
2. The mode change occurs at a maximum of 64 main clock cycles after writing to the clock mode flag. A delay should be allowed between a mode change operation and a HALT instruction.
3. The system clock frequency divider ratio cannot be changed if this ratio is selected as the power-ON default.

Standby Modes

HALT mode

The HALT command can be used to override the watchdog timer, which halts operation, whether the WG2 and WG3 flags are set to 1 or not. This enables release by either a HIGH on PB3/START or the interrupt release signal.

Entry

Issuing the HALT instruction when the standby control register SLPF flag is 0 invokes HALT mode. However, it is equivalent to a NOP (no operation) instruction under the following exit conditions.

- Reset
- The PB3/START line goes HIGH while WG2 = 1.
- The interrupt release signal goes active while WG3 = 1.
- The 14-bit frequency divider overflows. Normal operation commences after a maximum of 0.5 seconds if a 4.19 MHz clock is used.

HOLD mode

Entry

Issuing the HALT instruction when the SLPF flag is 1 invokes HOLD mode.

A single NOP instruction is issued prior to entering HOLD mode. The WG1 flag must be set to 1 before entering HOLD mode to enable release by a HIGH on PB3/START. The timebase clock source should be set to 1/128 of the oscillator clock.

Exit

HOLD mode is exit when one of the following conditions occur.

- Reset
- The PB3/START line goes HIGH while WG1 = 1.

Watchdog Timer

The watchdog timer is used to detect program runaway and generate a reset. The following guidelines should be observed.

- Write a routine in the program that resets the TBF flag periodically before a timer overflow occurs. It should be written so that the instruction that resets the TBF flag is not issued at the same time as the timeout interrupt request signal is generated.
- Select a timer divide ratio
- If the timebase interrupt request flag TBF is 1 prior to invoking HALT mode, a timer overflow will initiate a watchdog reset and an exit from HALT mode. To prevent a watchdog reset when HALT mode is exit, either reset the TBF flag immediately before issuing the HALT instruction or set the TBF flag and the WG3 flag (interrupt-invoked HALT exit).

Interrupts

The following guidelines should be observed for interrupts.

- Interrupts are enabled using control register bit 5.
- Each of the 5 interrupt vectors is allocated its own enable flag. The desired interrupts can be enabled by setting the appropriate flags. It is not possible to access multiple bits simultaneously using the SCTL0 to 7 instructions. All flags are cleared when a reset occurs.
- Flags can be cleared by issuing a RCTL instruction for each flag.
- Invoking HOLD mode disables all flags. They should be enabled after exiting HOLD mode.
- The interrupt flags are configured as a pseudo port. Individual flags are selected by setting the corresponding accumulator bits to 1 and copying them to the interrupt request register. When a BANK instruction is issued after an IP instruction, the flags are cleared. When a BANK instruction is issued after an OP instruction, the selected flag is set.
- All interrupt flags except timer 1 flag are cleared to 0 after a reset.
- All interrupt flags are cleared to 0 after HOLD mode is invoked.
- The serial I/O flag SIOF is cleared to 0 when serial data transfer begins.
- Each interrupt flag including the interrupt enable flag should be set individually following an interrupt.
- A BANK instruction followed by a SPB or RPB instruction does not access the interrupt request register.