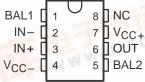
- Low Input Bias Current, 50 pA Typ
- Low Input Noise Current, 0.01 pA/√Hz Typ
- Low Supply Current, 2 mA Typ
- High Input impedance, $10^{12} \Omega$ Typ
- Low Total Harmonic Distortion
- Low 1/f Noise Corner, 50 Hz Typ
- Package Options Include Plastic Small-Outline (D) and Standard (P) DIPs

D OR P PACKAGE (TOP VIEW)



NC - No internal connection

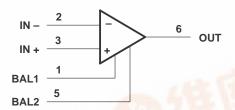
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a maximum input offset voltage drift. It requires low supply current, yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF411 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF411C is characterized for operation from 0°C to 70°C. The LF411I is characterized for operation from –40°C to 85°C.

symbol



AVAILABLE OPTIONS

1-111	Viemov	PACKAGE					
TA	V _{IO} max AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (P)				
0°C to 70°C	2 mV	LF411CD	LF411CP				
–40°C to 85°C	2 mV	LF411ID	LF411IP				

The D packages are available taped and reeled. Add the suffix R to the device type (i.e., LF411CDR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LF411 JFET-INPUT OPERATIONAL AMPLIFIER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC+}	18 V
Supply voltage, V _{CC}	
Differential input voltage, V _{ID}	$\dots\dots \pm 30 \; V$
Input voltage, V _I (see Note 1)	$\dots\dots\dots\pm 15~V$
Duration of output short circuit	Unlimited
Continuous total power dissipation	500 mW
Package thermal impedance, θ _{JA} (see Note 2): D package	197°C/W
P package	104°C/W
Storage temperature range, T _{stg}	\dots -65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	C SU	FFIX	I SUF	UNIT	
	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V _{CC +}	3.5	18	3.5	18	V
Supply voltage, V _{CC} –	-3.5	-18	-3.5	-18	V
Operating free-air temperature, T _A	0	70	-40	-85	°C

electrical characteristics over operating free-air temperature range, $V_{CC\pm}$ = ± 15 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		TA			TVD	MAY	UNIT
				LF411C LF411I		MIN	TYP	MAX	
VIO	Input offset voltage	$V_{IC} = 0$,	$R_S = 10 \text{ k}\Omega$	25°C	25°C		0.8	2	mV
αVIO	Average temperature coefficient of input offset voltage	V _{IC} = 0,	$R_S = 10 \text{ k}\Omega$				10	20†	μV/°C
1	land offer to compare	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	25°C	25°C		25	100	pА	
IIO	Input offset current‡	V _{IC} = 0		70°C	85°C			2	nA
l.s	tt-12	VIC = 0		25°C	25°C		50	200	pА
ΙΙΒ	IB Input bias current‡			70°C	85°C			4	nA
VICR	Common-mode input voltage range					±11	-11.5 to 14.5		V
Vом	Maximum peak output-voltage swing	R _L = 10 kΩ				±12	±13.5		V
۸. هـ	Large-signal differential	$V_{O} = \pm 10 \text{ V},$	R _L = 2 kΩ	25°C	25°C	25	200		V/mV
AVD	voltage			0°C to 70°C	-40°C to 85°C	15	200		V/IIIV
rį	Input resistance	T _J = 25°C					1012		Ω
CMR R	Common-mode rejection ratio	$R_S \le 10 \text{ k}\Omega$				70	100		dB
ksvr	Supply-voltage rejection ratio	See Note 3				70	100		dB
ICC	Supply current						2	3.4	mA

 $[\]overline{\dagger}$ At least 90% of the devices meet this limit for α_{VIO} .

NOTE 3: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.



[‡] Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

LF411 JFET-INPUT OPERATIONAL AMPLIFIER

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operating characteristics, $V_{CC\pm}$ = ± 15 V, T_A = $25^{\circ}C$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/μs
В1	Unity-gain bandwidth		2.7	3		MHz
٧n	Equivalent input noise voltage	$f = 1 \text{ kHz}, R_S = 20 \Omega$		18		nV/√ Hz
In	Equivalent input noise current	f = 1 kHz		0.01		pA/√ Hz



PACKAGE OPTION ADDENDUM

17-Oct-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)
LF411CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LF411CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LF411CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LF411CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LF411CP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
LF411CPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
LF411ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
LF411IDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
LF411IP	OBSOLETE	PDIP	Р	8	•	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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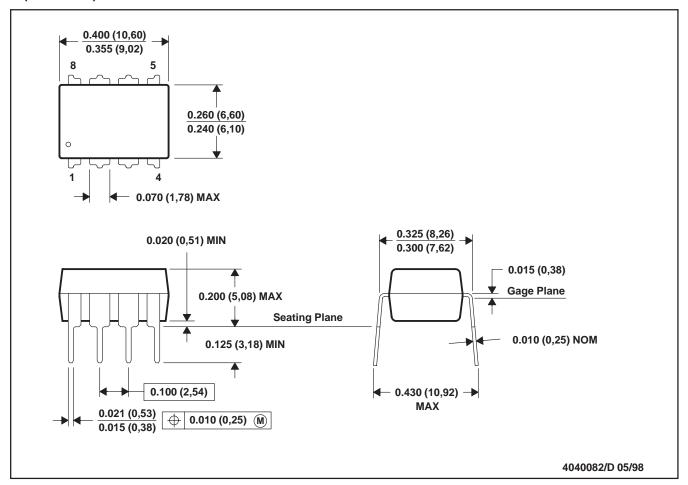
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE

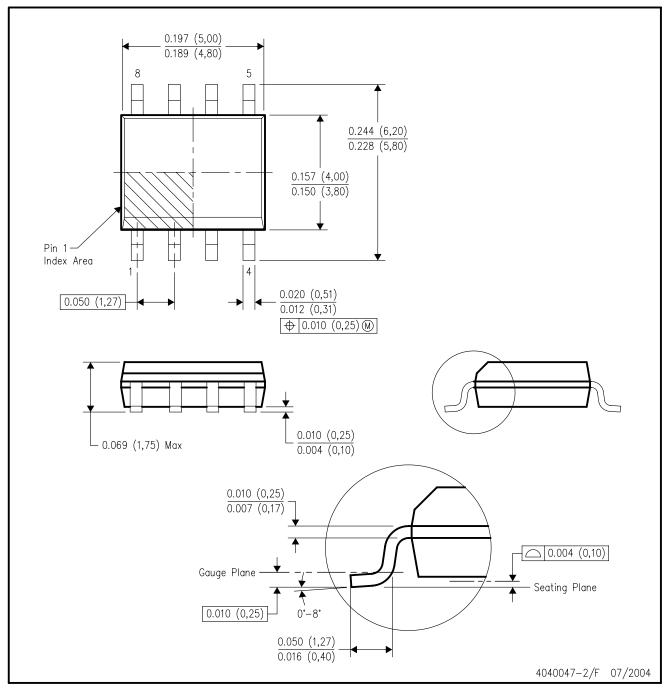


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AA.



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