May 2002

National Semiconductor

LMV243
Single-Channel, Quad-Band GSM Power Controller in micro SMD

General Description

The device is intended for use within an RF transmit power control loop in GSM mobile phones and supports GaAs HBT and bipolar RF single supply power amplifiers. The circuit operates with a single supply from 2.7V to 3.3V.

The LMV243 contains an RF detector, error amplifier, ramp V/I converter and output driver. The LMV243 input interface consists of the RF input, Ramp voltage, and a digital input to perform the function 'Shutdown/Transmit Enable'. The device will be active in the case TX_EN = HI, otherwise, the device goes into a low power consumption shutdown mode. During shutdown the output will be in high impedance (tri-state).

A single external RC combination is used to provide stable operations that accommodates individual PA characteristics. The LMV243 is offered in a 8-bump micro SMD 1.5mm x 1.5mm package. This space savings package supports flexible product placement almost anywhere in the circuitboard.

Features

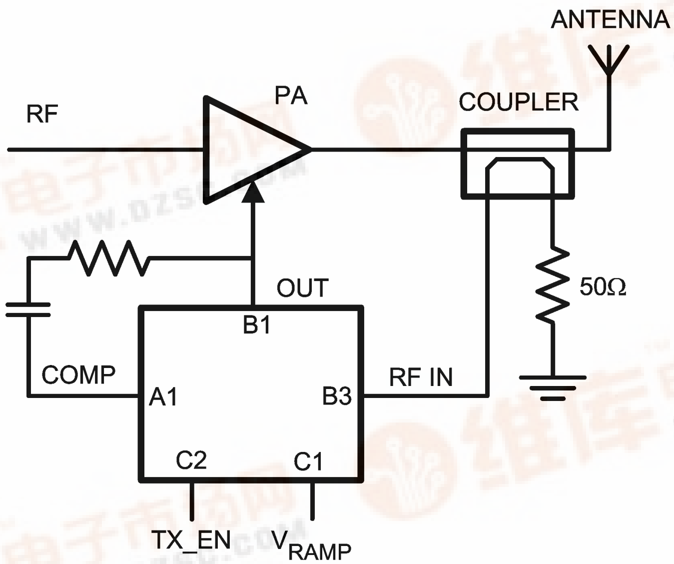
(Typical Unless Otherwise Noted)

- 50dB RF detection range (typical)
- micro SMD package 1.5mm x 1.5mm x 0.995mm
- Support of GaAs HBT, bipolar technology
- Quad-band operation
- Shutdown mode for Power Save in Rx slot
- GPRS compliant
- External loop compensation option
- Accurate temperature compensation
- Frequency range is 450MHz to 2GHz

Applications

- GSM mobile phone
- AGC for digital audio
- TDMA RF control
- Wireless LAN

Typical Application



20029034

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
V_{DD} - GND	4V Max
ESD Tolerance (Note 2)	
Human Body Model	2000V
Machine Model	200V
Storage Temperature Range	−65˚C to 150˚C
Junction Temperature (Note 6)	150˚C Max
Mounting Temperature	
Infrared or convection (20 sec)	235˚C

Operating Ratings (Note 1)

Nominal Supply Voltage	2.7V to 3.3V
Temperature Range	$-40˚C < T_J < 85˚C$
V_{RAMP} Voltage Range	0V to 2V
V_{HOME} Voltage Range	0V to 2V
RF Frequency Range	450MHz to 2GHz

Electrical Characteristics

Unless otherwise specified, all limits are guaranteed to T_J = 25˚C. V_{DD} = 2.8V. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DD}	Supply Current	V_{OUT} = (V_{DD} - GND)/2		8.7	10.5 **12.5**	mA
		In Shutdown (TX_EN = 0.8V) V_{OUT} = (V_{DD} - GND)/2		4.6	**30**	µA
V_{HIGH}	Logic Level to Enable Power	(Note 7)	1.8			V
V_{LOW}	Logic Level to Disable Power	(Note 7)			0.8	V
T_{ON}	Turn-on- Time from Shutdown			3.7	6.5 **7.5**	µs
I_{EN}	Current into TX_EN Pin			0.108	**5**	µA
RAMP Amplifier						
V_{RD}	V_{RAMP} Deadband		170 **150**	210	250 **270**	mV
$1/R_{RAMP}$	Transconductance	(Note 8)		78		µa/V
$I_{OUT\ RAMP}$	Ramp Amplifier Output Current	V_{RAMP} = 2V	**100**	140		µA
RF Input						
P_{IN}	RF Input Power Range (Note 5)	20kΩ // 27pF between V_{OUT} and V_{COMP}		−50 +5		dBm
				−63 −7		dBV
	Logarithmic Slope (Note 9)	@ 900MHz, 20kΩ // 27pF between V_{OUT} and V_{COMP}		−1.79		µa/dB
		@ 1800MHz, 20kΩ // 27pF between V_{OUT} and V_{COMP}		−1.89		µa/dB
		@ 1900MHz, 20kΩ // 27pF between V_{OUT} and V_{COMP}		−1.89		µa/dB
	Logarithmic Intercept (Note 9)	@ 900MHz, 20kΩ // 27pF between V_{OUT} and V_{COMP}		−50.5		dBm
		@ 1800MHz, 20kΩ // 27pF between V_{OUT} and V_{COMP}		−46.9		dBm
		@ 1900MHz, 20kΩ // 27pF between V_{OUT} and V_{COMP}		−45.9		dBm
R_{IN}	DC Resistance	(Note 8)		50		Ω
C_{IN}	Input Capacitance	(Note 8)		0.5		pF
Error Amplifier						
GBW	Gain-Bandwidth Product	(Note 8)		7.6		MHz

Electrical Characteristics

Unless otherwise specified, all limits are guaranteed to T_J = 25°C. V_{DD} = 2.8V. **Boldface** limits apply at temperature extremes. (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_O	Output Swing from Rail	Sourcing, I_O = 5mA		55	85 **105**	mV
		Sinking, I_O = −5mA		45	75 **95**	
I_O	Output Short Circuit Current (Note 3)	Sourcing, V_O = 0V	**25**	145		mA
		Sinking, V_O = 2.8V	**25**	180		
e_n	Output Referred Noise	RF input = 1800 MHz, -10dBm, 20kΩ // 27pF between V_{OUT} and V_{COMP}, V_{OUT} =1.4V, set by V_{RAMP}, (Note 8)		700		nV/ $\sqrt{Hz}$
SR	Slew Rate		8 **5**	11		V/µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model: 1.5kΩ in series with 100pF. Machine model, 0Ω in series with 100pF.

Note 3: Shorting circuit output to either V^+ or V^- will adversely affect reliability.

Note 4: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 5: Power in dBV = dBm + 13 when the impedance is 50Ω.

Note 6: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board

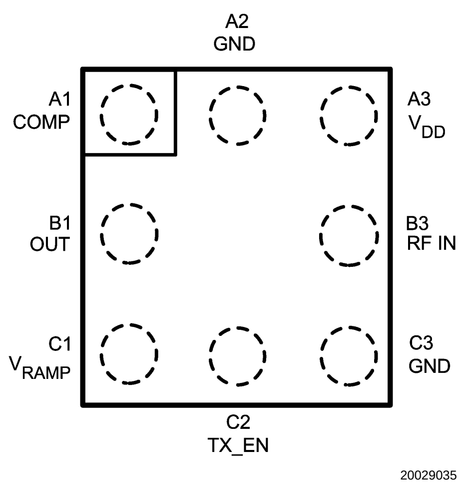
Note 7: All limits are guaranteed by design or statistical analysis

Note 8: Typical values represent the most likely parametric norm.

Note 9: Slope and intercept are calculated from graphs 'V_{OUT} vs. RF input Power' where the current is obtained by division of the voltage by 20kΩ.

Connection Diagram

8-Bump micro SMD



Top View

Pin Descriptions

	Pin	Name	Description
Power Supply	A3	V_{DD}	Supply Voltage
	A2, C3	GND	Power Ground. Operation requires both pins be grounded.
Digital Inputs	C2	TX_EN	A Logic High to enable device.
Analog Inputs	B3	RF IN	RF Input connected to the Coupler output with optional attenuation to measure the Power Amplifier (PA) / Antenna RF power levels.
	C1	RAMP IN	Sets the RF output power level. The useful input voltage range is from 0.2V to 1.8V, although voltages from 0V to V_{DD} are allowed.
Compensation	A1	Comp	Connects an external RC network between the Comp pin and the Output pin for an overall loop compensation and to control the closed loop frequency response. Conventional loop stability techniques can be used in selecting this network, such as Bode plots. A good starting value for the RC combination will be C = 68pF and R = 0Ω.
Output	B1	Out	A rail-to-rail output capable of sourcing 25mA and sinking 25mA, with less than 200mV total voltage drop over the specified temperature. The output is free from glitches when enabled by TX_EN. When TX_EN is low, the output voltage is near GND.

Note: 1. All inputs and outputs are referenced to GND (pin A2, C3).

2. For the digital inputs, a LOW is $<$ 0.8V and a HIGH is $>$ 1.8V.

3. RF power detection is performed internally in the LMV243 and only an RF power coupler with optional extra attenuation has to be used.

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Bump micro SMD	LMV243BL	01	1k Units Tape and Reel	BLA08AAC
	LMV243BLX	01	3k Units tape and Reel	

Block Diagram

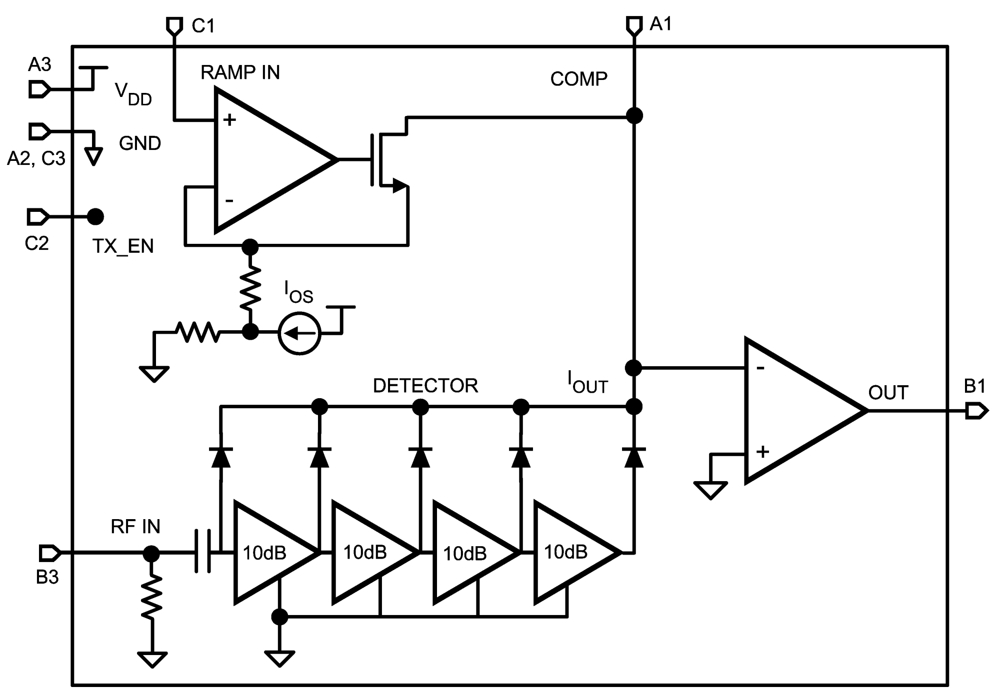
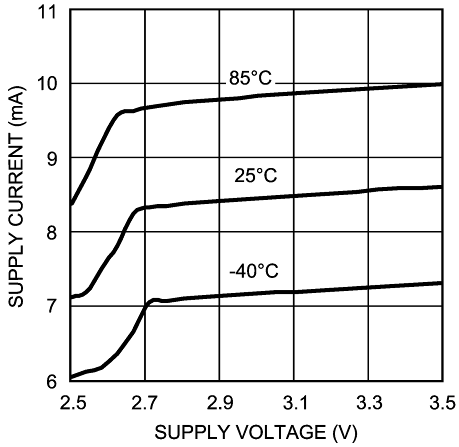


FIGURE 1.

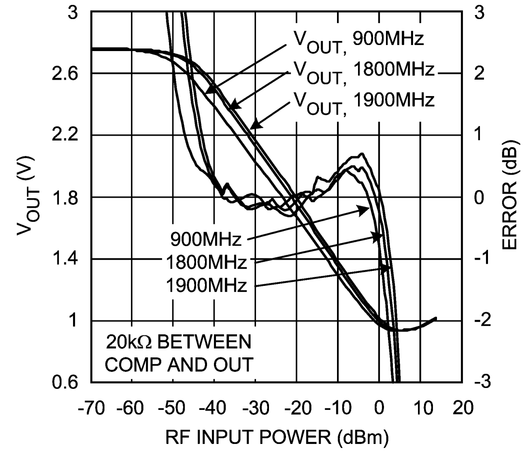
Typical Performance Characteristics Unless otherwise specified, V_{DD} = +2.8V, T_J = 25˚C.

Supply Current vs. Supply Voltage



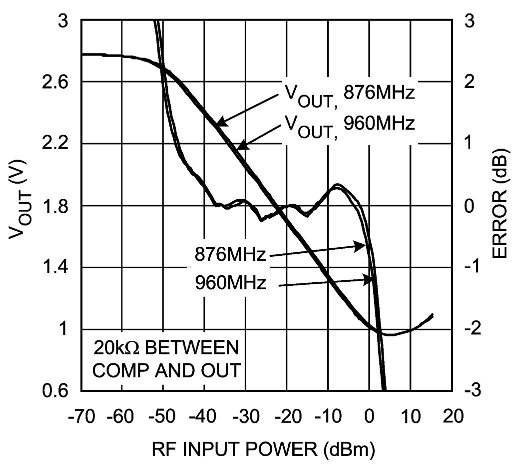
20029024

V_{OUT} and Log Conformance vs. RF Input Power



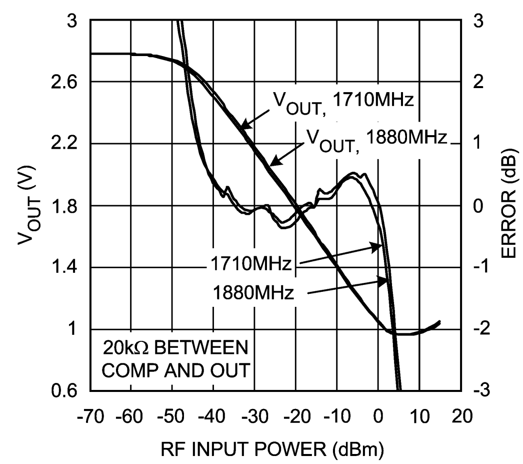
20029001

V_{OUT} and Log Conformance vs. RF Input Power at Corners of GSM



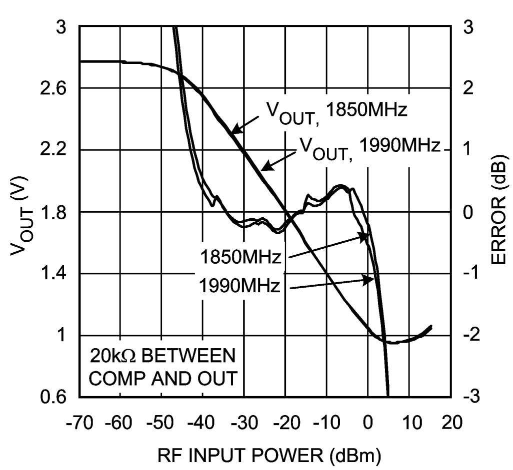
20029002

V_{OUT} and Log Conformance vs. RF Input Power at Corners of DCS



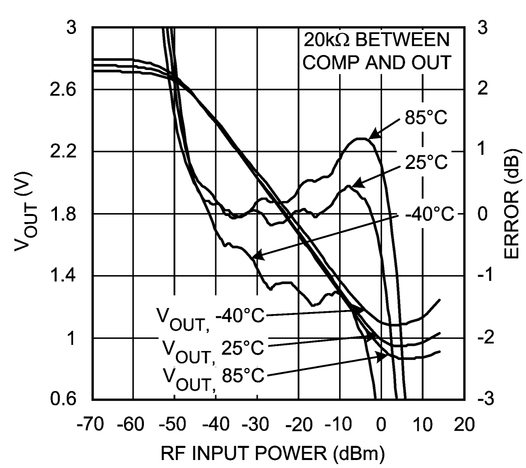
20029008

V_{OUT} and Log Conformance vs. Pin @ Corners of PCS



20029009

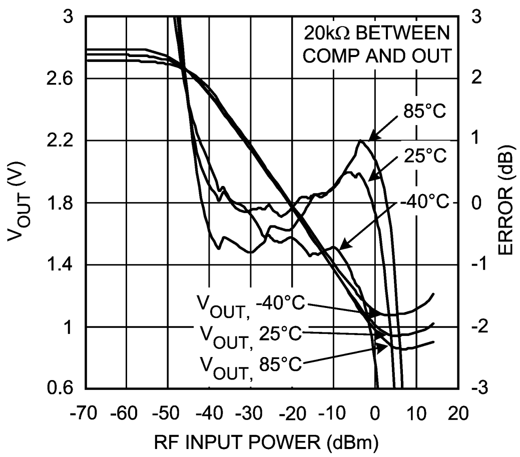
V_{OUT} and Log Conformance vs. RF Input Power at 900MHz



20029003

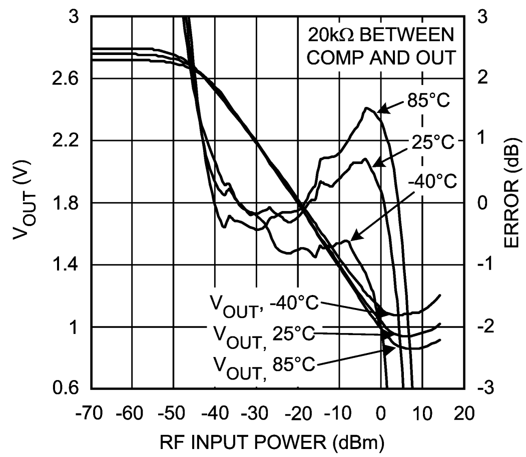
Typical Performance Characteristics Unless otherwise specified, V_{DD} = +2.8V, T_J = 25˚C. (Continued)

V_{OUT} and Log Conformance vs. RF Input Power at 1800MHz



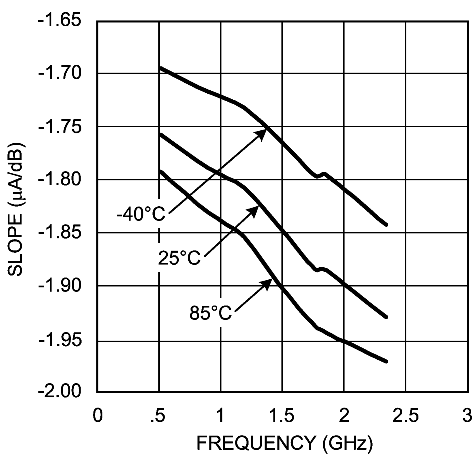
20029004

V_{OUT} and Log Conformance vs. RF Input Power at 1900MHz



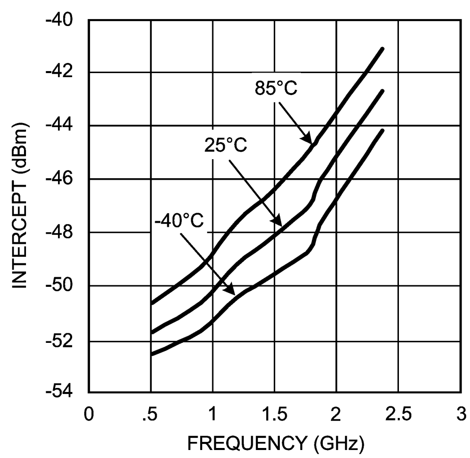
20029005

Logarithmic Slope vs. Frequency



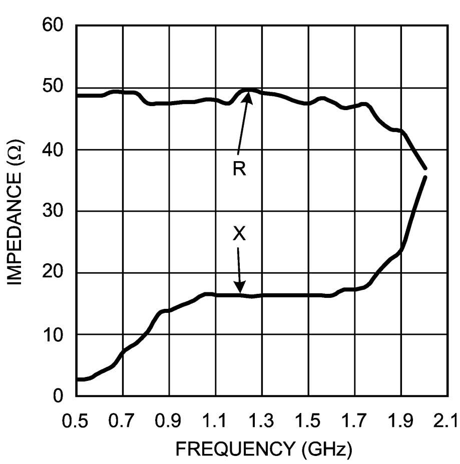
20029006

Logarithmic Intercept vs. Frequency



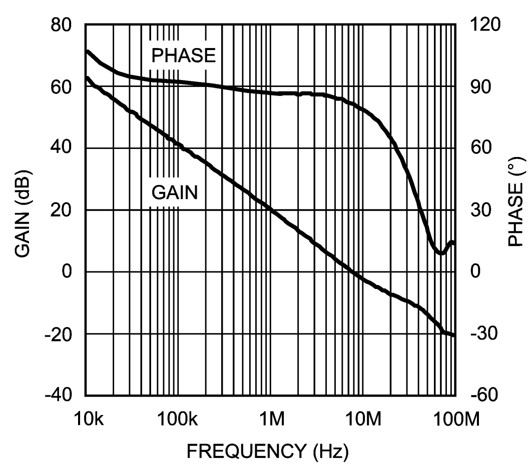
20029007

RF Input Impedance vs. Frequency @ Resistance and Reactance



20029031

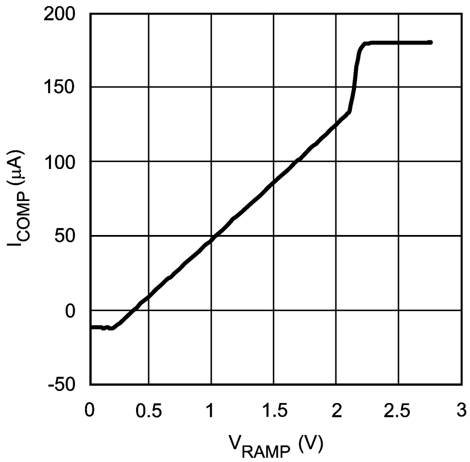
Gain and Phase vs. Frequency Error Amplifier



20029026

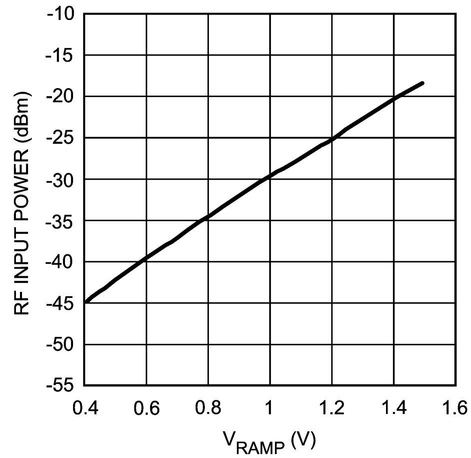
Typical Performance Characteristics
Unless otherwise specified, V_{DD} = +2.8V, T_J = 25˚C. (Continued)

I_{COMP} vs. V_{RAMP}



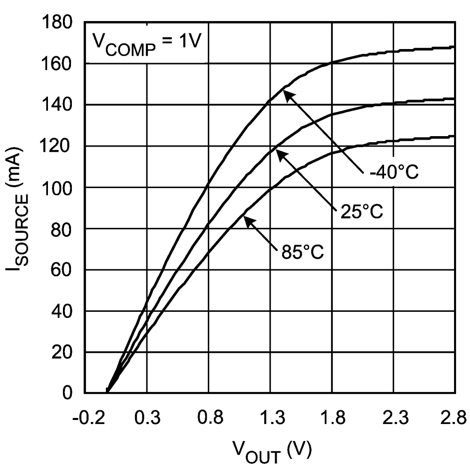
20029027

P_{IN} vs. V_{RAMP}



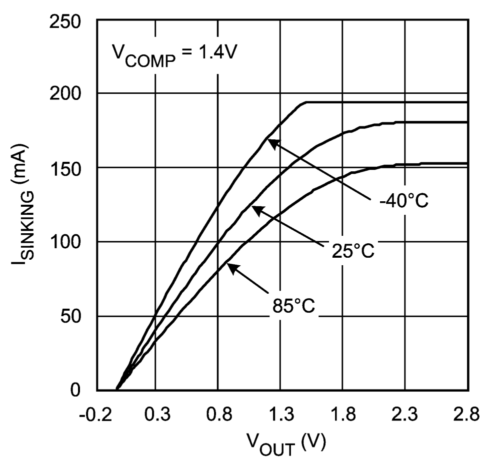
20029028

Sourcing Current vs. Output Voltage



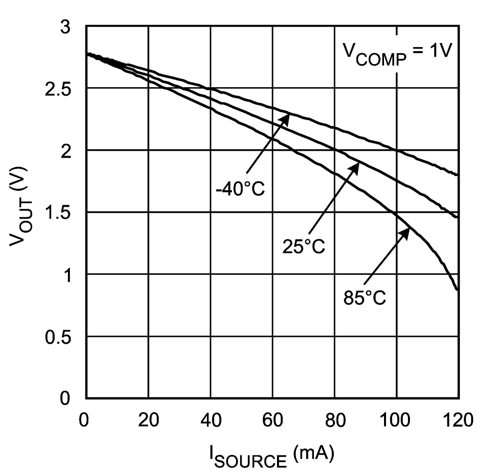
20029032

Sinking Current vs. Output Voltage



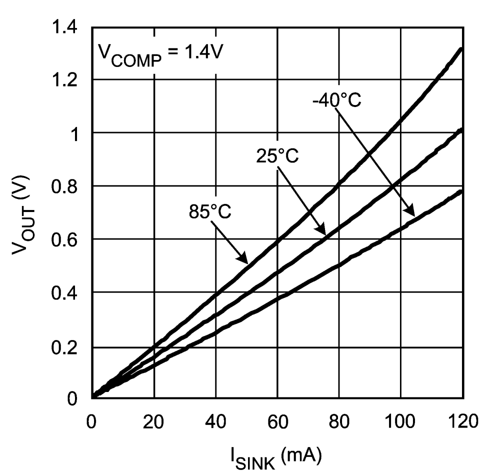
20029033

Output Voltage vs. Sourcing Current



20029029

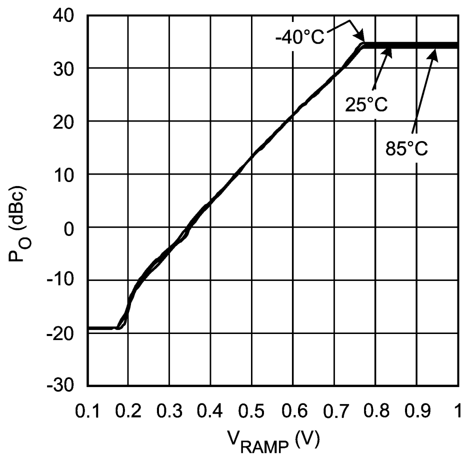
Output Voltage vs. Sinking Current



20029030

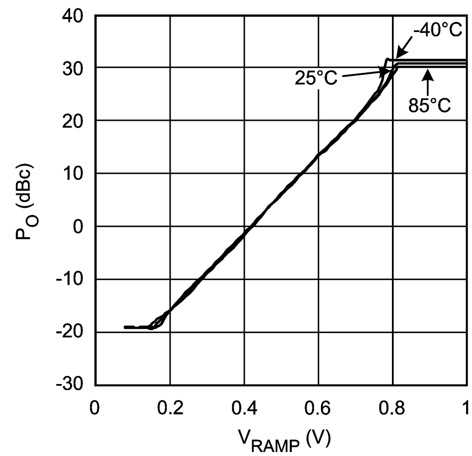
Typical Performance Characteristics Unless otherwise specified, V_{DD} = +2.8V, T_J = 25˚C. (Continued)

Closed Loop P_{OUT} (PA) vs. V_{RAMP} @ 900MHz



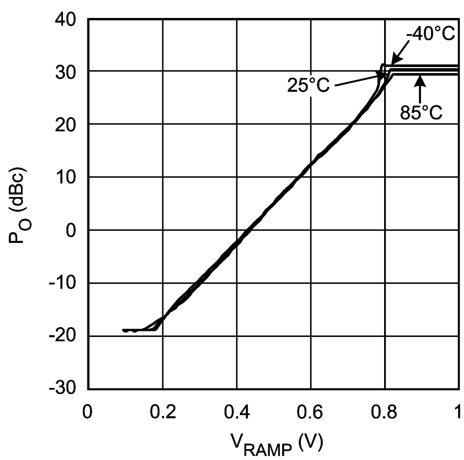
20029011

Closed Loop P_{OUT} (PA) vs. V_{RAMP} @ 1800MHz



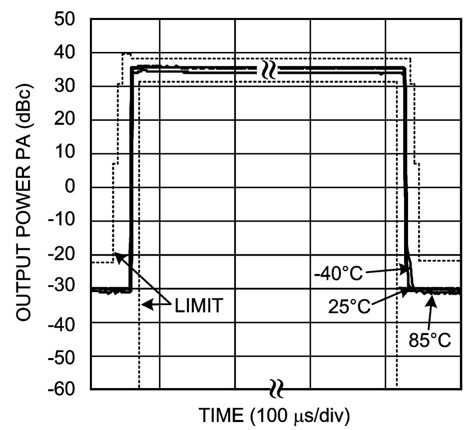
20029012

Closed Loop P_{OUT} (PA) vs. V_{RAMP} @ 1900MHz



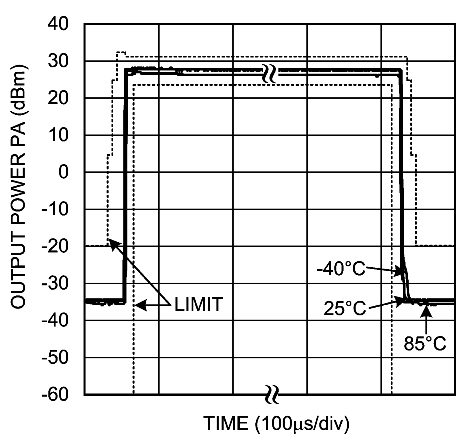
20029013

Time Mask Plot vs. Time @ 900MHz



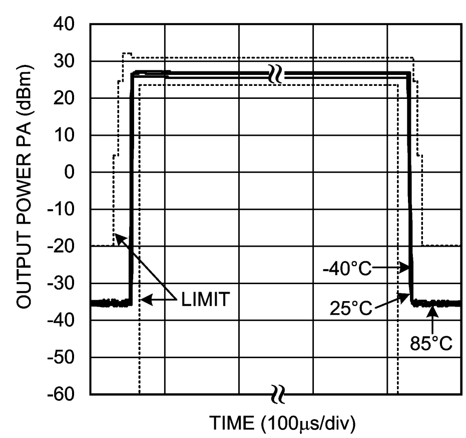
20029014

Time Mask Plot vs. Time @ 1800MHz



20029015

Time Mask Plot vs. Time @ 1900MHz



20029016

Application Information

1.0 The LMV243 as an RF Power Amplifier (PA) Controller

The LMV243 is a member of the power loop controller family of National Semiconductor, for a quad-band TDMA/GSM solution. The typical application diagram demonstrates a basic approach for implementing the quad-band solution around the RF Power Amplifier. The LMV243 contains a 50 dB Logamp detector and interfaces directly with the directional coupler.

The LMV243 Base Band (control) interface consists of 2 signals: *TX_EN* to bring the device out of shutdown status within 5µs, and V_{RAMP} for the transmit burst characteristic determining the desired Output Power level. The LMV243 gives maximum flexibility to meet GSM frequency and time mask criteria for many different single supply Power Amplifier types like HBT or, MesFET in GaAs, SiGe or Si technology. This is accomplished by the Programmable Ramp characteristic from the Base Band and the TX_EN signal along with the external compensation capacitor.

Power consumption requirements are supported by the TX_EN function which puts the entire chip into a Power Saving Mode to enable maximum standby and talk time while ensuring the output does not glitch excessively during Power-up and Power-down.

2.0 A Typical GSM Power Amplifier Controlled Loop

This section should give a general overview and understanding of how a typical Power Amplifier control loop works and how to get rid of some of the most common problems confronted in the design. *Figure 2* shows the generic components of such a loop. Beginning at the output of the GSM Power Amplifier (PA), this signal is fed, usually via a directional coupler, to a detector. The output current of the detector Idet drives the inverting input of an op amp, configured as an integrator. A reference voltage drives the non-inverting input of the op amp. Finally the output of the op amp integrator drives the gain control input of the power amplifier. Now to examine how this circuit works, we will assume initially that the output of the PA is at some low level and that the V_{RAMP} voltage is at 1V. The V/I converter converts the V_{RAMP} voltage to a sinking current I_{RAMP}. This current can only come from the integrator capacitor C. Current flow in this direction increases the output voltage of the integrator. This voltage, which drives the PA, increases the gain (we assume that the PA's gain control input has a positive sense, that is, increasing voltage increases gain). The gain will increase, thereby increasing the amplifier's output level until the detector output current equals the ramp current I_{RAMP}. At that point, the current through the capacitor will decrease to zero and the integrator output will be held steady, thereby settling the loop. If capacitor charge is lost over time, the gain will decrease. However, this leakage will quickly be corrected by additional integrator current from the newly reduced detector current.

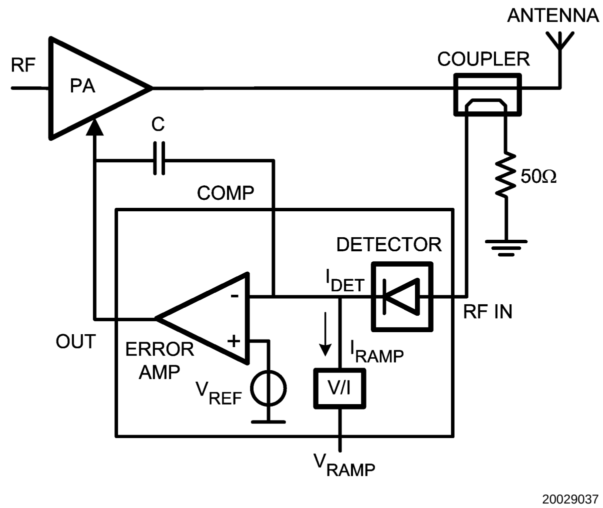


FIGURE 2. PA Control Loop

The key usefulness of this circuit lies in its immunity to changes in the PA gain control function. From a static perspective at least, the relationship between gain and gain control voltage is of no consequence to the overall transfer function. Based upon the value of V_{RAMP}, the integrator will set the gain control voltage to whatever level is necessary to produce the desired output level. Any temperature dependency in the gain control function will be eliminated. Also, non-linearity's in the gain transfer function of the PA do not appear in the overall transfer function (V_{OUT} vs. V_{RAMP}). The only requirement is that the gain control function of the PA be monotonic. It is crucial, however, that the detector is temperature stable.

The circuit as described so far, has been designed to produce a constant output level for varying input levels. The only requirement is for it to be temperature stable for input levels that correspond to the setpoint voltage V_{RAMP}. If the detector used has a higher dynamic range, the circuit to precisely set PA output levels over a wide dynamic range. To do this, the integrator reference voltage, V_{RAMP}, is varied. The voltage range on V_{RAMP} follows directly from the detector's transfer function. For example, if the detector delivers 0.5V for an input of −7dBm, a reference voltage of 0.5V will cause the loop to settle when the detector input is −7dBm (the PA output will be greater than this amount by whatever coupling factor exists between PA and detector). The dynamic range for the variable RF P_{OUT} case will be determined by the device in the circuit with the least dynamic range (i.e. the gain control range PA or linear dynamic of detector).

Application Information (Continued)

The response time of this loop can be controlled by varying the RC time constant of the integrator. Setting this at a low level will result in fast output settling but can result in ringing in the output envelope. Settling the RC time constant high will give the loop good stability but will increase settling time.

Figure 3 shows a typical RF power control loop realized by using the National's LMV243 with integrated RF detector. The RF signal from the PA passes through a directional coupler on its way to the antenna. Directional couplers are characterized by their coupling factor which is in the 10dB to 30dB range, typical 20dB. Because the coupled output must in its own right deliver some power (in this case to the detector), the coupling process takes some power from the main output. This manifests itself as insertion loss, the insertion loss being higher for lower coupling factors.

3.0 Attenuation between coupler and LMV243 detector

It is very important to choose the right attenuation between PA output and detector input, i.e. the total of coupling factor and extra attenuation, in order to achieve power control over the full output power range of the PA. A typical value for the output power of the PA is +35.5 dBm for GSM and +30 dBm for PCS/DCS. In order to accommodate these levels into the LMV243 detection range the minimum required total attenuation is about 35 dBm (please refer to typical performance characteristics in the datasheet). A typical coupler factor is 20dB. An extra attenuation of about 15 dB should be inserted.

Extra attenuation Z between the coupler and the RF input of the LMV243 can be achieved by 2 resistors R_X and R_Y according to *Figure 3*, where

$$Z = 20 \log [R_{IN} / (R_{IN} + R_Y)]$$

e.g. $R_Y = 300\Omega$ results in an attenuation of 16.9dB.

To prevent reflection back to the coupler the impedance seen by the coupler should be 50Ω. The impedance R_O consists of R_X // (R_Y, R_O, + R_{IN}). R_X can be calculated with the formula:

$$R_X = [R_O * (R_Y + R_{IN})] / R_Y$$

$$R_X = 50 * [1 + (50/R_Y)]$$

e.g. with $R_Y = 300\Omega$, $R_{IN} = 50\Omega \rightarrow R_X = 58\Omega$.

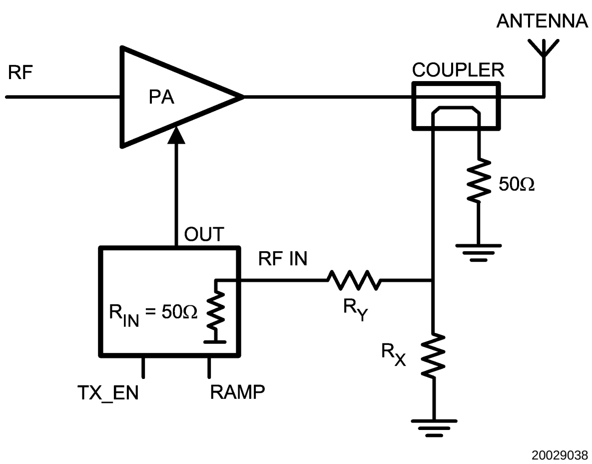


FIGURE 3. PA Control Loop With Extra Attenuation

4.0 Components of a Power Amplifier Loop

Figure 3 shows the basics of a typical LMV243 quad-band application.

The key components are:

- The LMV243
- One power amplifier, usually for the GSM and PCN/DCS bands
- A single two channel RF coupler is used instead of the two RF couplers
- A dual or quad-band antenna.

Figure 1 shows the LMV243's internal architecture. The LMV243 contains an RF detector, error amplifier, a ramp V/I converter and an output driver. The LMV243 input interface consists of an RF input, Ramp voltage, and a digital input to perform the function 'Shutdown/Transmit Enable'.

5.0 Analog and Digital Input Signals of the LMV243

The LMV243 has the following inputs:

–V_{RAMP} is an analog signal (Base band DAC ramp signal)

–TX_EN is a digital signal (performs the function 'Shutdown/ Transmit Enable').

5.1 V_{RAMP} in signal

The actual V_{RAMP} input value sets the RF output power. By applying a certain mask shape to the 'Ramp in' pin, the output voltage level of the LMV243 adjusts the PA control voltage to get a power level (P_{OUT}/dBm) out of the PA which is proportional to the single ramp voltage steps. The recommended V_{RAMP} voltage range for RF power control is 0.2V to 2.0V. The V_{RAMP} input will tolerate voltages from 0V to V_{DD} without malfunction or damage. The V_{RAMP} input does not change the output level until the level reaches about 200mV, so offset voltages in the DAC or amplifier supplying the Ramp signal will not cause excess RF signal output and increased power consumption.

6.0 Analog Output

The Output is driven by a rail-to-rail amplifier capable of both sourcing and sinking. It is able to source and sink 25mA with less than 200mV voltage drop from either rail over recommended operating conditions. Please refer to the typical performance characteristics. The output voltage vs. Sourcing/Sinking current show the typical voltage drop from the rail over temperature. The Sourcing/Sinking current vs. output voltage characteristics show the typical charging/discharging current, which the output is capable of delivering at a current voltage. The output is free from glitches when enabled by TX_EN. When TX_EN is low, the selected output voltage is fixed or near GND.

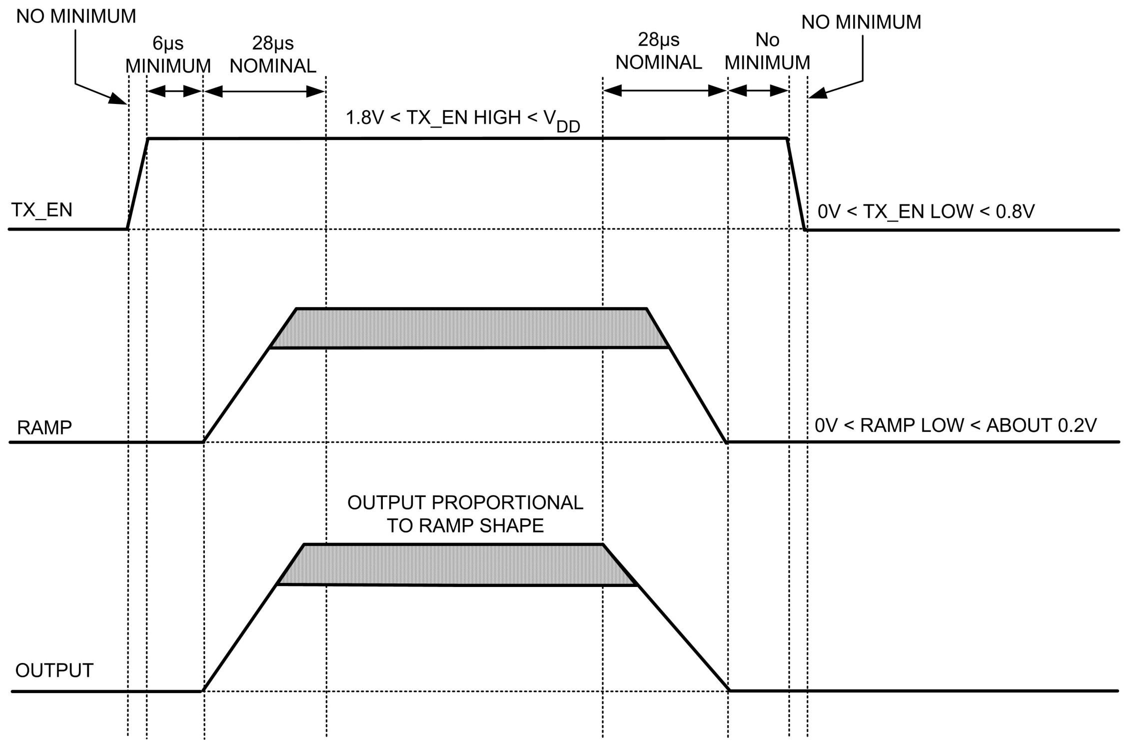
7.0 Bandwidth Compensation

To compensate and prevent the closed loop arrangement from oscillations and overshoots at the output of the RF detector/error amplifier LMV243, the system can be adjusted by means of external RC components connected between Comp and Out . Exact values heavily depend on PA characteristics. A good starting point is R = 0Ω and C = 68pF. The vast combinations of PA's and couplers available preclude a generalized formula for choosing these component. Please contact National Semiconductor for additional assistance.

8.0 Evaluation Board

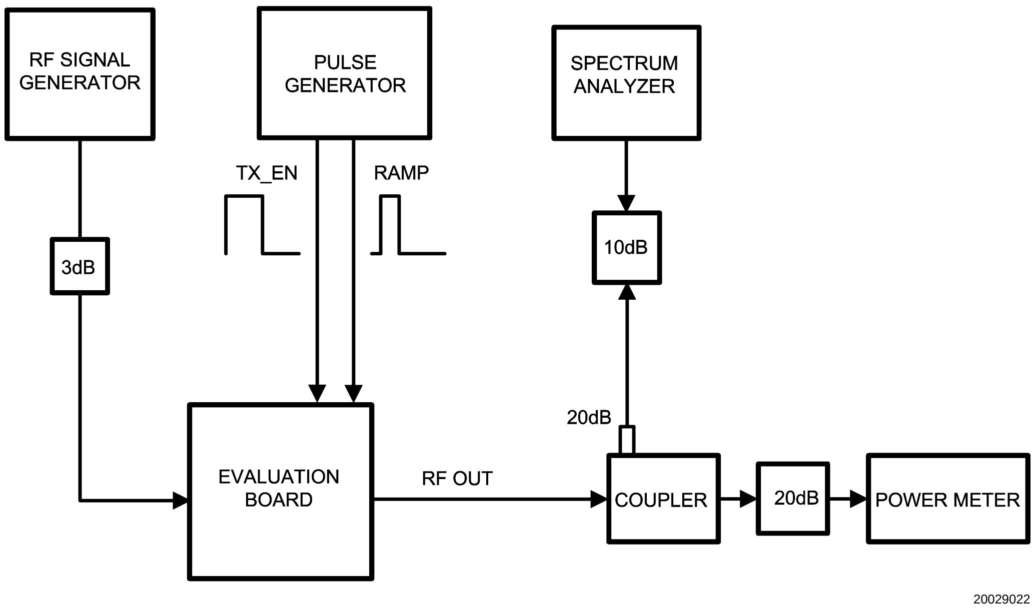
An evaluation board in available for the LMV243. Please contact your local distributor or National Semiconductor sales office.

Typical Timing Diagram



20029039

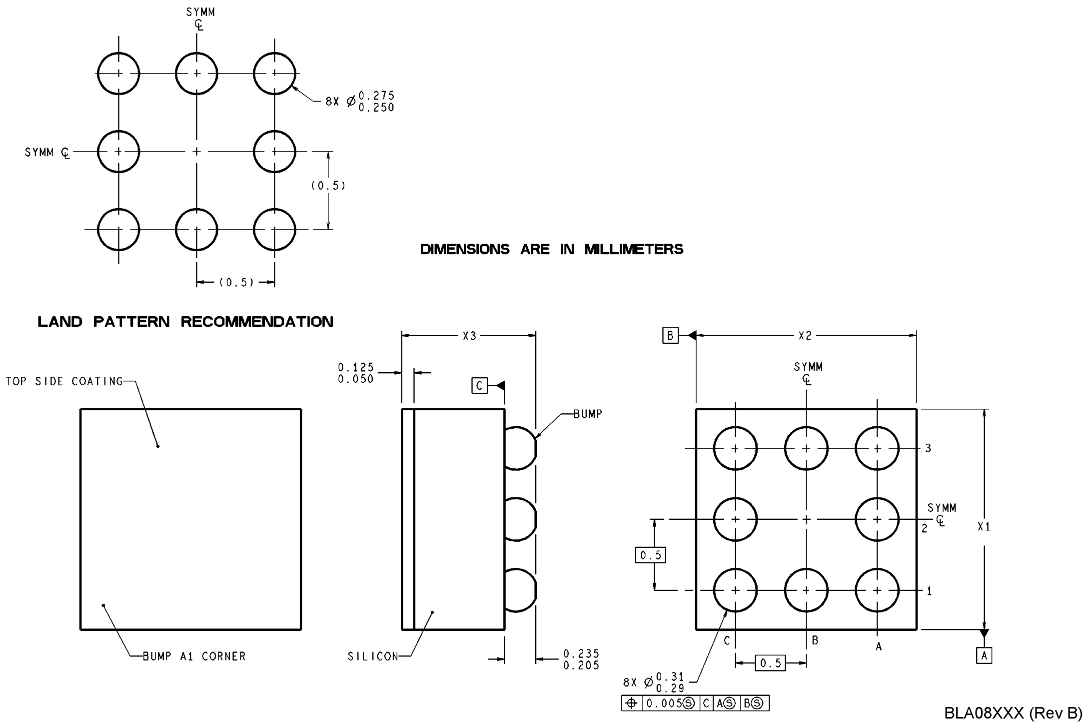
Typical Test Setup Diagram



Equipment List:

RF Signal Generator	**Rohde & Schwarz SMIQ 03B**
Pulse Generator	Tektronix AFG2020
Spectrum Analyzer	Rohde & Schwarz FSP
Power Meter	HP E4418B, with Powersensor HP E4413A
Coupler	Pasternack PE 2208-10

Physical Dimensions inches (millimeters) unless otherwise noted



8-Bump micro SMD
NS Package Number BLA08AAC
X1 = 1.514 ±0.03mm X2 = 1.514 ±0.03mm X3 = 0.995 ±0.1mm

NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING

2.Sn/37Pb EUTECTIC BUMP

3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.

4. PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTER CLOCKWISE.

5.XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.

REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

National Semiconductor Corporation
Americas
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507