

# LSI/CSI



# LS7031



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## 6 DECADE MOS UP COUNTER WITH 8 DECADE LATCH AND MULTIPLEXER

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### FEATURES:

- DC to 7.5 MHz Count Frequency
- Multiplexed BCD Outputs
- DC to 500kHz Scan Frequency
- +4.75V to +15V Operation (VDD-VSS)
- Compatible with CMOS Logic
- High Input Noise Immunity
- Ability to Latch External BCD Data in the two LSD Positions
- Leading Zero Blanking with Decimal Point and Overflow Controls
- All inputs protected
- Low Power Dissipation
- 40 Pin DIP - See Figure 1

### DESCRIPTION:

The LS7031 is a monolithic, ion implanted MOS, 6 decade up counter. The circuit includes latches, a multiplexer, leading zero blanking and BCD data outputs.

### CLOCK GENERATOR

The clock for the six decade counter (digit positions 3-8) is formed from the internal 'OR' combination of B4/D2 and B8/D2 if LS7031 is used with external prescaling counters. When operated in this fashion the maximum allowable propagation delay between B4/D2 (H-L) and B8/D2 (L-H), measured at Vss - 1V, is 10ns. If used as a straight six decade counter, clock pulses may be applied to inputs B4/D2 or B8/D2 with the unused input held low. In either mode of operation total pulse width must be minimum 62ns. See Block Diagram.

### 6 DECADE UP COUNTER

The six decade ripple through counter increments on the negative edge of the input count pulse. Maximum ripple time is 12µs (999999 to 000000). Maximum count frequency is 7.5MHz.

### RESET

All 6 counter decades are reset to zero when Reset input is brought low for a minimum of 4µs. The Overflow flip-flop is reset at the same time. Reset must be high for a minimum of 1µs before next valid count can be recorded.

### SCAN OSCILLATOR AND COUNTER

The scan counter is driven by an internal oscillator whose frequency is determined by a capacitor connected between Oscillator input and Scan input. An external scan clock applied to Scan input can also drive the scan counter. Scan counter advances on negative edge of scan clock.

The counter scans from MSD to LSD. When Scan Reset input is brought high the scan counter is forced to MSD state. Internal synchronization guarantees proper scanning no matter when Scan Reset is brought low relative to scan clock. Maximum scan frequency is 500kHz.

A high at the Decimal Point input resets the Blanking flip-flop causing the display to unblank. Decimal Point should be brought high at start of digit time which has active Decimal Point.

CONNECTION DIAGRAM - TOP VIEW

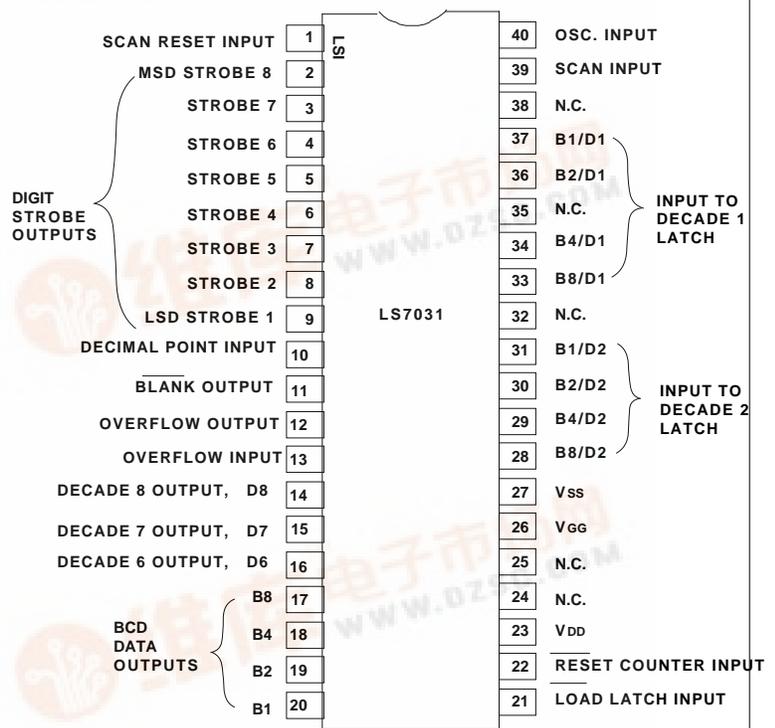


FIGURE 1

### DIGIT STROBES

Timing of Digit Strokes is arranged such that both edges of strobe are guardbanded by a minimum 400ns within valid BCD data when scan frequency is 100kHz or less. The guardband is a minimum of 200ns at 250kHz scan frequency. At 500kHz only negative edge of Strobe is guaranteed to be within valid BCD data by a minimum 200ns.

### OVERFLOW

The Overflow flip-flop sets on the first negative transition of the Overflow Input and remains set until Reset is brought low. Data is transferred from Overflow flip-flop to Overflow Latch when Load is brought low. A high at the Overflow Latch causes display to unblank. Overflow Output is output of Overflow Latch. MSB outputs of Decades 6, 7, 8 are available for use as Overflow Input.

### LATCHES

Eight decades of latch are provided, two for storage of the two external least significant decade counters and the remaining 6 for internal counter outputs. All latches when Load signal is brought low for a minimum of 4µs and kept low until a minimum of 12µs has elapsed from previous negative edge of count pulse (ripple time). Storage of valid data occurs when Load signal is high for a minimum of 1µs before next negative edge of count pulse or reset. Data is transferred from Overflow flip-flop to Overflow latch at the same time.

## BLANKING

Leading zero blanking is employed. At start of each MSD to LSD scan, display is blanked until a non-zero digit or active decimal point is encountered. Display unblanks during LSD time and whenever Overflow output is high. When Scan Reset is applied, display blanks to prevent display damage. \_\_\_\_\_  
Blanking information is available at Blank output.

## BCD DATA

Data is available in multiplexed BCD format. BCD data can be readily demultiplexed using Digit Strokes as latch enable signals.

## POWER SUPPLIES

+4.75V to +15V single power supply operation is obtained when VGG and VDD are tied together. Inputs and outputs are CMOS compatible and Minimum Input Noise Immunity of 25% of power supply is guaranteed except for Decade 1 and 2 inputs. (All inputs are TTL compatible at +4.75V to +5.25V operation.) With VGG at -12V, VDD at 0V and VSS at +5V all inputs are TTL and CMOS compatible. All outputs are CMOS compatible and BCD and BLANK outputs also provide standard TTL compatibility. In addition, Overflow Output is low power TTL compatible. In either mode outputs swing between VDD and VSS.

## MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	Tstg	-65 to +150	°C
Operating Temperature	TA	-25 to +70	°C
Voltage (any pin to VSS)	Vmax	-30 to +0.5	V

## DC ELECTRICAL CHARACTERISTICS

(VDD = VGG = 0V, VSS = +4.75 to +15V, -25°C TA +70°C unless otherwise specified.)

	PARAMETER	SYMBOL	MIN	MAX	UNITS
	Operating Supply Current (fc = 7.5MHz)	Idds	-	15	mA
	Input Noise Immunity Low and High	Vni	25% (VSS-VDD)	-	V
EXTERNAL DECADE INPUTS	Input Voltage "0"	Vil	VSS - 20	VSS - 3.95	V
	Input Voltage "1"	Vih	VSS - 1.0	VSS	V
D6, D7, D8 OF, BCD Blank (See Note 1)	Output Voltage "0"	Vol	-	+0.2	V
	Output Voltage "1"	Voh	VSS - 1.0	-	V
Segment and Strobe Outputs (See Note 2)	Output Voltage "0" (sinking 10µA)	Vol	-	+0.5	V
	Output Current "1"				
	VSS = 4.75V (Voh = VSS - 0.5V)	-	0.05	-	mA
	(Voh = VSS - 1V)	-	0.25	-	mA
	(Voh = VSS - 4V)	-	0.90	-	mA
	VSS = 10V (Voh = VSS - 2V)	-	2.0	-	mA
(Voh = VSS - 3V)	-	3.0	-	mA	
VSS = 15V (Voh = VSS - 2V)	-	3.0	-	mA	
(Voh = VSS - 3V)	-	4.5	-	mA	

**NOTE 1:** Current Sink = Same as segment and strobe outputs.

Current Source = N/A at Voh = VSS - 0.5V for VSS = +4.75V

35µA at Voh = VSS - 1V for VSS = +4.75V

40% of segment and strobe outputs at all other specified operating points.

**NOTE 2:** Limit segment current to 6mA maximum.

The following inputs have internal pull down resistors to VDD with maximum sink current of 5µA at VSS input.

Scan Reset	B1/D1	B1/D2
Decimal	B2/D1	B2/D2
Overflow	B4/D1	B4/D2
	B8/D1	B8/D2

## TTL COMPATIBLE OUTPUTS:

**POWER SUPPLIES:** VSS = +5V ± 5%, VDD = 0V, VGG = -12V ± 5%

<b>OUTPUT LEVELS:</b>	"1" Level	VSS - 0.5V (sourcing 100µA)	} BLANK AND BCD DATA OUTPUTS
	"0" Level	0.4V (sinking 1.6mA)	
	"1" Level	VSS - .5V (sourcing 40µA)	} OVERFLOW OUTPUT
	"0" Level	0.4V (sinking .18mA)	

All other outputs as specified for single power supply, VSS = +15V operation.  
Inputs as specified for single power supply, VSS = +5V ± 5% operation.

## SCAN OSCILLATOR CAPACITANCE

### TYPICAL OSCILLATOR FREQUENCY

	4.75V	10V	15V
50pF	40.0 kHz	24.2kHz	22.2 kHz
100pF	22.2 kHz	14.8kHz	13.8 kHz
470pF	5.0 kHz	3.6kHz	3.5 kHz

**ELECTRICAL CHARACTERISTICS:**

(VDD = VGG = 0V, VSS = +4.75 to +15V, -25°C TA +70°C unless otherwise specified.)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Count Test and Count frequency (VSS = +5V ± 5%)	fc, ftc	DC	7.5	MHz
(VSS = +10V)	fc, ftc	DC	6	MHz
(VSS = +15V)	fc, ftc	DC	5	MHz
Scan frequency	fsc	DC	500	kHz
Count Pulse Width (Pulse applied to B4/D2 or B8/D2; 'OR' combination of B4/D2 and B8/D2)				
(VSS = +5V ± 5%)	tcpw	62	-	ns
(VSS = +10V)	tcpw	83	-	ns
(VSS = +15V)	tcpw	100	-	ns
**Propagation Delay (B4/D2(H-L) to B8/D2 (L-H) at VSS -1.0V)				
Count Ripple Time	tcr	Overlap	10	ns
Load Pulse Width	tipw	4	-	µs
Load Removal Time	tir	-	1	µs
Reset Pulse Width	trpw	4	-	µs
Reset Removal Time	trr	-	1	µs
Rise and Fall Time				
Count Pulse	trfc	-	4	µs
Reset Pulse	trfr	-	4	µs
Test Count Pulse	trffc	-	80	µs
*Strobe Guard Band time (fSC 100kHz 250kHz)	tgb	400	-	ns
*Strobe Guard Band time (100kHz fSC 250kHz)	tgb	200	-	ns
*Strobe Guard Band time (250kHz fSC 500kHz) negative edge only	tgb	200	-	ns

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.

\*Defines the minimum time from strobe edges to switching BCD data.

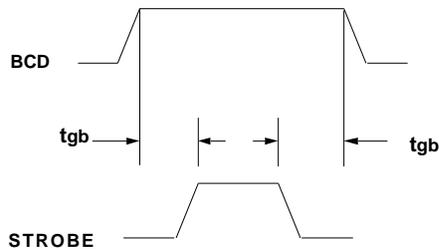


FIGURE 2. GUARD BANDED STROBE

\*\*Propagation Delay and Pulse Width

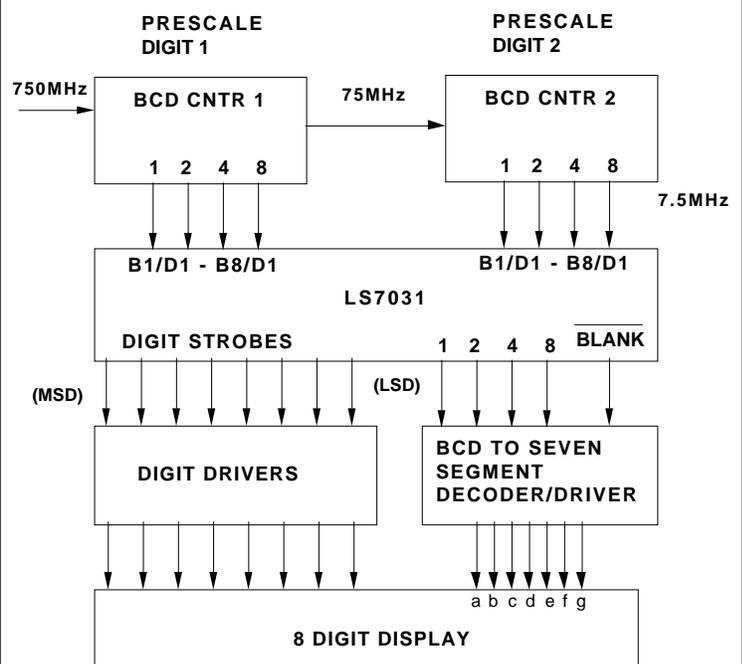
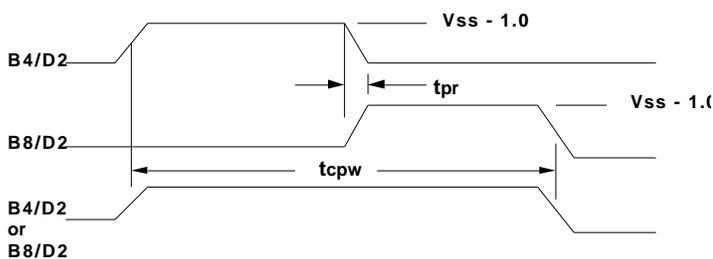


FIGURE 3. TYPICAL APPLICATION

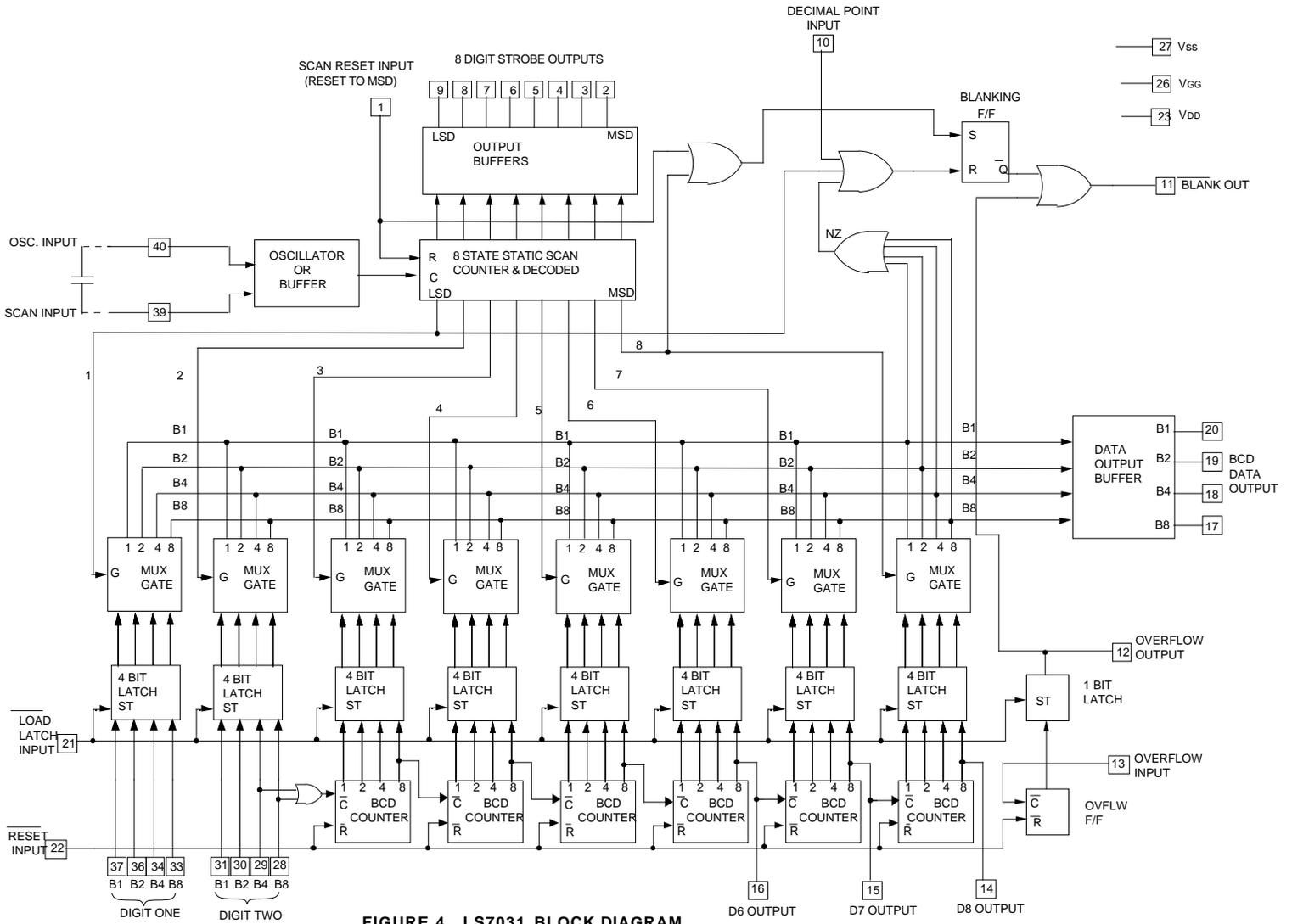


FIGURE 4. LS7031 BLOCK DIAGRAM