查询LT6200供应商

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LT6200/LT6200-5 LT6200-10/LT6201

165MHz, Rail-to-Rail Input and Output, 0.95nV/√Hz Low Noise, Op Amp Family

FEATURES

- **Low Noise Voltage: 0.95nV/√Hz (100kHz)**
- **Gain Bandwidth Product:**

LT6200/LT6201	**165MHz**	**$A_V = 1$**
LT6200-5	**800MHz**	**$A_V \geq 5$**
LT6200-10	**1.6GHz**	**$A_V \geq 10$**

- **Low Distortion: –80dB at 1MHz, $R_L = 100\Omega$**
- **Dual LT6201 in Tiny DFN Package**
- **Input Common Mode Range Includes Both Rails**
- Output Swings Rail-to-Rail
- Low Offset Voltage: 1mV Max
- Wide Supply Range: 2.5V to 12.6V
- Output Current: 60mA Min
- SOT-23 and SO-8 Packages
- Operating Temperature Range –40°C to 85°C
- Power Shutdown, Thermal Shutdown

APPLICATIONS

- Transimpedance Amplifiers
- Low Noise Signal Processing
- Active Filters
- Rail-to-Rail Buffer Amplifiers
- Driving A/D Converters

DESCRIPTION

The LT®6200/LT6201 are single and dual ultralow noise, rail-to-rail input and output unity gain stable op amps that feature 0.95nV/√Hz noise voltage. These amplifiers combine very low noise with a 165MHz gain bandwidth, 50V/µs slew rate and are optimized for low voltage signal conditioning systems. A shutdown pin reduces supply current during standby conditions and thermal shutdown protects the part from overload conditions.

The LT6200-5/LT6200-10 are single amplifiers optimized for higher gain applications resulting in higher gain bandwidth and slew rate. The LT6200 family maintains its performance for supplies from 2.5V to 12.6V and are specified at 3V, 5V and ±5V.

For compact layouts the LT6200/LT6200-5/LT6200-10 are available in the 6-lead ThinSOT™ and the 8-pin SO package. The dual LT6201 is available in an 8-pin SO package with standard pinouts as well as a tiny, dual fine pitch leadless package (DFN). These amplifiers can be used as plug-in replacements for many high speed op amps to improve input/output range and noise performance.

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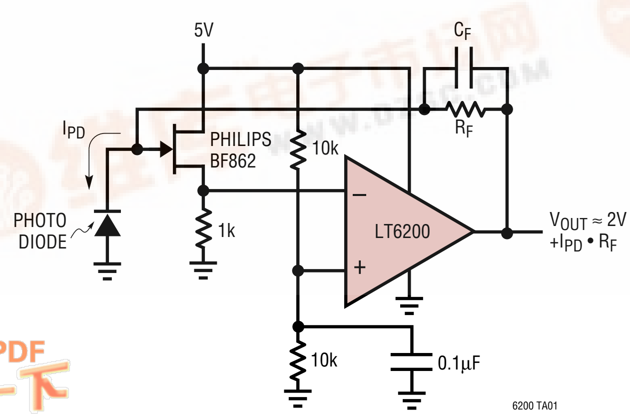
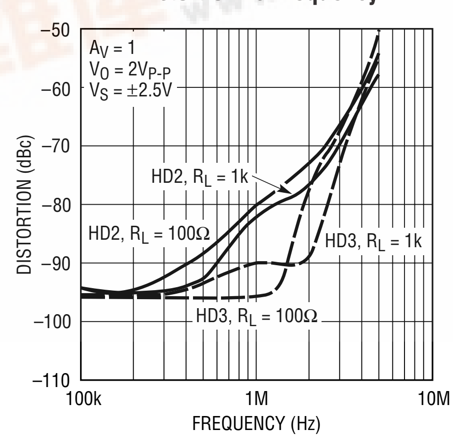
ThinSOT is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

Single Supply, 1.5nV/√Hz, Photodiode Amplifier



Distortion vs Frequency



ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Total Supply Voltage (V^+ to V^-) (LT6201DD) 7V
Input Current (Note 2) .... ±40mA
Output Short-Circuit Duration (Note 3) .... Indefinite
Pin Current While Exceeding Supplies
(Note 12) .... ±30mA
Operating Temperature Range (Note 4) ...–40°C to 85°C
Specified Temperature Range (Note 5) ....–40°C to 85°C
Junction Temperature .... 150°C
Junction Temperature (DD Package) .... 125°C
Storage Temperature Range ....–65°C to 150°C
Storage Temperature Range
(DD Package) .... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

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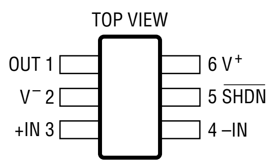
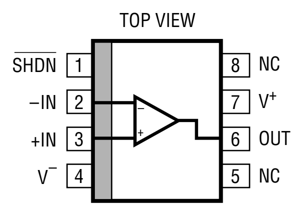
<tr><td rowspan="5">

S6 PACKAGE
6-LEAD PLASTIC SOT-23
T_{JMAX} = 150°C, θ_{JA} = 160°C/W (Note 10)</td><td>ORDER PART NUMBER</td><td rowspan="5">

S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 100°C/W</td><td>ORDER PART NUMBER</td></tr>
<tr><td>LT6200CS6
LT6200IS6
LT6200CS6-5
LT6200IS6-5
LT6200CS6-10
LT6200IS6-10</td><td>LT6200CS8
LT6200IS8
LT6200CS8-5
LT6200IS8-5
LT6200CS8-10
LT6200IS8-10</td></tr>
<tr><td>S6 PART MARKING*</td><td>S8 PART MARKING</td></tr>
<tr><td>LTJZ
LTACB
LTACC</td><td>6200
6200I
62005
6200I5
620010
200I10</td></tr>
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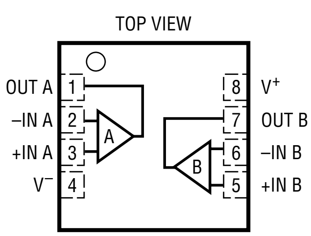
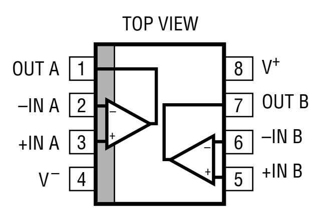
<tr><td rowspan="5">

DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 160°C/W (NOTE 3)
UNDERSIDE METAL CONNECTED TO V⁻</td><td>ORDER PART NUMBER</td><td rowspan="5">

S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 100°C/W</td><td>ORDER PART NUMBER</td></tr>
<tr><td>LT6201CDD</td><td>LT6201CS8
LT6201IS8</td></tr>
<tr><td>DD PART MARKING*</td><td>S8 PART MARKING</td></tr>
<tr><td>LADG</td><td>6201
6201I</td></tr>
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*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = 5V, 0V$; $V_S = 3V, 0V$; $V_{CM} = V_{OUT}$ = half supply, $V_{\overline{SHDN}}$ = OPEN, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = 5V$, V_{CM} =Half Supply $V_S = 3V$, V_{CM} = Half Supply		0.1 0.9	1 2.5	mV mV
		$V_S = 5V$, $V_{CM} = V^+$ to V^- $V_S = 3V$, $V_{CM} = V^+$ to V^-		0.6 1.8	2 4	mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 11)	V_{CM} = Half Supply $V_{CM} = V^-$ to V^+		0.2 0.5	1.1 2.2	mV mV
I_B	Input Bias Current	V_{CM} = Half Supply $V_{CM} = V^+$ $V_{CM} = V^-$	–40 –50	–10 8 –23	 18 	µA µA µA
ΔI_B	I_B Shift	$V_{CM} = V^-$ to V^+		31	68	µA
	I_B Match (Channel-to-Channel) (Note 11)	$V_{CM} = V^-$ to V^+		0.3	5	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply $V_{CM} = V^+$ $V_{CM} = V^-$		0.1 0.02 0.4	4 4 5	µA µA µA
	Input Noise Voltage	0.1Hz to 10Hz		600		nV_{P-P}
e_n	Input Noise Voltage Density	f = 100kHz, $V_S = 5V$ f = 10kHz, $V_S = 5V$		1.1 1.5	 2.4	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density, Balanced Source Unbalanced Source	f = 10kHz, $V_S = 5V$ f = 10kHz, $V_S = 5V$		2.2 3.5		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Input Resistance	Common Mode Differential Mode		0.57 2.1		MΩ kΩ
C_{IN}	Input Capacitance	Common Mode Differential Mode		3.1 4.2		pF pF
A_{VOL}	Large-Signal Gain	$V_S = 5V$, V_O = 0.5V to 4.5V, R_L = 1k to $V_S/2$ $V_S = 5V$, V_O = 1V to 4V, $R_L = 100Ω$ to $V_S/2$ $V_S = 3V$, V_O = 0.5V to 2.5V, R_L = 1k to $V_S/2$	70 11 17	120 18 70		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5V$, $V_{CM} = V^-$ to V^+ $V_S = 5V$, V_{CM} = 1.5V to 3.5V $V_S = 3V$, $V_{CM} = V^-$ to V^+	65 85 60	90 112 85		dB dB dB
	CMRR Match (Channel-to-Channel) (Note 11)	$V_S = 5V$, V_{CM} = 1.5V to 3.5V	80	105		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, LT6201DD V_S = 2.5V to 7V	60	68		dB
	PSRR Match (Channel-to-Channel) (Note 11)	V_S = 2.5V to 10V, LT6201DD V_S = 2.5V to 7V	65	100		dB
	Minimum Supply Voltage (Note 6)		2.5			V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA $V_S = 5V$, I_{SINK} = 20mA $V_S = 3V$, I_{SINK} = 20mA		9 50 150 160	50 100 290 300	mV mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA $V_S = 5V$, I_{SOURCE} = 20mA $V_S = 3V$, I_{SOURCE} = 20mA		55 95 220 240	110 190 400 450	mV mV mV mV
I_{SC}	Short-Circuit Current	$V_S = 5V$ $V_S = 3V$	±60 ±50	±90 ±80		mA mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	$V_S = 5V$ $V_S = 3V$ $V_{\overline{SHDN}}$ = 0.3V		16.5 15 1.3	20 18 1.8	mA mA mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0.3V		200	280	µA
V_L	$V_{\overline{SHDN}}$ Pin Input Voltage LOW				0.3	V
V_H	$V_{\overline{SHDN}}$ Pin Input Voltage HIGH		$V^+ - 0.5$			V

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, $V_{\overline{SHDN}}$ = OPEN, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V		0.1	75	µA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω, V_S = 5V		130		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω, V_S = 5V		180		ns
GBW	Gain Bandwidth Product	Frequency = 1MHz, V_S = 5V LT6200-5 LT6200-10		145 750 1450		MHz MHz MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 4V	31	44		V/µs
		V_S = 5V, A_V = –10, R_L = 1k, V_O = 4V LT6200-5 LT6200-10		 210 340		 V/µs V/µs
FPBW	Full Power Bandwidth (Note 9)	V_S = 5V, V_{OUT} = $3V_{P-P}$ (LT6200)	3.28	4.66		MHz
t_S	Settling Time (LT6200, LT6201)	0.1%, V_S = 5V, V_{STEP} = 2V, A_V = –1, R_L = 1k		165		ns

The ● denotes the specifications which apply over 0°C < T_A < 70°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, $V_{\overline{SHDN}}$ = OPEN, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = 5V, V_{CM} = Half Supply V_S = 3V, V_{CM} = Half Supply	● ●		0.2 1.0	1.2 2.7	mV mV
		V_S = 5V, V_{CM} = V^+ to V^- V_S = 3V, V_{CM} = V^+ to V^-	● ●		0.3 1.5	3 4	mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 11)	V_{CM} = Half Supply V_{CM} = V^- to V^+	● ●		0.2 0.4	1.8 2.8	mV mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	V_{CM} = Half Supply	●		2.5	8	µV/°C
I_B	Input Bias Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-	● ● ●	–40 –50	–10 8 –23	 18 	µA µA µA
	I_B Match (Channel-to-Channel) (Note 11)	V_{CM} = V^- to V^+	●		0.5	6	µA
ΔI_B	I_B Shift	V_{CM} = V^- to V^+	●		31	68	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-	● ● ●		0.1 0.02 0.4	4 4 5	µA µA µA
A_{VOL}	Large-Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to $V_S/2$ V_S = 5V, V_O = 1.5V to 3.5V, R_L = 100Ω to $V_S/2$ V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k to $V_S/2$	● ● ●	46 7.5 13	80 13 22		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^- to V^+ V_S = 5V, V_{CM} = 1.5V to 3.5V V_S = 3V, V_{CM} = V^- to V^+	● ● ●	64 80 60	88 105 83		dB dB dB
	CMRR Match (Channel-to-Channel) (Note 11)	V_S = 5V, V_{CM} = 1.5V to 3.5V	●	80	105		dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V, LT6201DD V_S = 3V to 7V	●	60	65		dB
	PSRR Match (Channel-to-Channel) (Note 11)	V_S = 3V to 10V, LT6201DD V_S = 3V to 7V	●	60	100		dB
	Minimum Supply Voltage (Note 6)		●	3			V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA V_S = 5V, I_{SINK} = 20mA V_S = 3V, I_{SINK} = 20mA	● ● ● ●		12 55 170 170	60 110 310 310	mV mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA V_S = 5V, I_{SOURCE} = 20mA V_S = 3V, I_{SOURCE} = 20mA	● ● ● ●		65 115 260 270	120 210 440 490	mV mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over 0°C < T_A < 70°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, $V_{\overline{SHDN}}$ = OPEN, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	±60 ±45	±90 ±75		mA mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	V_S = 5V V_S = 3V $V_{\overline{SHDN}}$ = 0.3V	● ● ●		20 19 1.35	23 22 1.8	mA mA mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0.3V	●		215	295	µA
V_L	$V_{\overline{SHDN}}$ Pin Input Voltage LOW		●			0.3	V
V_H	$V_{\overline{SHDN}}$ Pin Input Voltage HIGH		●	V^+ – 0.5			V
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V	●		0.1	75	µA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω, V_S = 5V	●		130		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω, V_S = 5V	●		180		ns
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 4V	●	29	42		V/µs
		A_V = –10, R_L = 1k, V_O = 4V LT6200-5 LT6200-10	 ● ●		 190 310		 V/µs V/µs
FPBW	Full Power Bandwidth (Note 9)	V_S = 5V, V_{OUT} = $3V_{P-P}$ (LT6200)	●	3.07	4.45		MHz

The ● denotes the specifications which apply over –40°C < T_A < 85°C temperature range. Excludes the LT6201 in the DD package (Note 3). V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, $V_{\overline{SHDN}}$ = OPEN, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = 5V, V_{CM} = Half Supply V_S = 3V, V_{CM} = Half Supply	● ●		0.2 1.0	1.5 2.8	mV mV
		V_S = 5V, V_{CM} = V^+ to V^- V_S = 3V, V_{CM} = V^+ to V^-	● ●		0.3 1.5	3.5 4.3	mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 11)	V_{CM} = Half Supply V_{CM} = V^- to V^+	● ●		0.2 0.4	2 3	mV mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	V_{CM} = Half Supply	●		2.5	8.0	µV/°C
I_B	Input Bias Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-	● ● ●	–40 –50	–10 8 –23	 18 	µA µA µA
ΔI_B	I_B Shift	V_{CM} = V^- to V^+	●		31	68	µA
	I_B Match (Channel-to-Channel) (Note 11)	V_{CM} = V^- to V^+	●		1	9	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-	● ● ●		0.1 0.02 0.4	4 4 5	µA µA µA
A_{VOL}	Large-Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2 V_S = 5V, V_O = 1.5V to 3.5V, R_L = 100Ω to V_S/2 V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k to V_S/2	● ● ●	40 7.5 11	70 13 20		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^- to V^+ V_S = 5V, V_{CM} = 1.5V to 3.5V V_S = 3V, V_{CM} = V^- to V^+	● ● ●	60 80 60	80 100 80		dB dB dB
	CMRR Match (Channel-to-Channel) (Note 11)	V_S = 5V, V_{CM} = 1.5V to 3.5V	●	75	105		dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V	●	60	68		dB
	PSRR Match (Channel-to-Channel) (Note 11)	V_S = 3V to 10V	●	60	100		dB
	Minimum Supply Voltage (Note 6)		●	3			V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA V_S = 5V, I_{SINK} = 20mA V_S = 3V, I_{SINK} = 20mA	● ● ● ●		18 60 170 175	70 120 310 315	mV mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over −40°C < T_A < 85°C temperature range. Excludes the LT6201 in the DD package (Note 3). V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, $V_{\overline{SHDN}}$ = OPEN, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA V_S = 5V, I_{SOURCE} = 20mA V_S = 3V, I_{SOURCE} = 20mA	● ● ● ●		65 115 270 280	120 210 450 500	mV mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	±50 ±30	±80 ±60		mA mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	V_S = 5V V_S = 3V $V_{\overline{SHDN}}$ = 0.3V	● ● ●		22 20 1.4	25.3 23 1.9	mA mA mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0.3V	●		220	300	µA
V_L	$V_{\overline{SHDN}}$ Pin Input Voltage LOW		●			0.3	V
V_H	$V_{\overline{SHDN}}$ Pin Input Voltage HIGH		●	V^+ – 0.5			V
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V	●		0.1	75	µA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω, V_S = 5V	●		130		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω, V_S = 5V	●		180		ns
SR	Slew Rate	V_S = 5V, A_V = −1, R_L = 1k, V_O = 4V	●	23	33		V/µs
		A_V = −10, R_L = 1k, V_O = 4V LT6200-5 LT6200-10	 ● ●		 160 260		 V/µs V/µs
FPBW	Full Power Bandwidth (Note 9)	V_S = 5V, V_{OUT} = $3V_{P-P}$ (LT6200)	●	2.44	3.5		MHz

T_A = 25°C, V_S = ±5V, V_{CM} = V_{OUT} = 0V, $V_{\overline{SHDN}}$ = OPEN, unless otherwise noted. Excludes the LT6201 in the DD package (Note 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-		1.4 2.5 2.5	4 6 6	mV mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 11)	V_{CM} = 0V V_{CM} = V^- to V^+		0.2 0.4	1.6 3.2	mV mV
I_B	Input Bias Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-	−40 −50	−10 8 −23	 18 	µA µA µA
ΔI_B	I_B Shift	V_{CM} = V^- to V^+		31	68	µA
	I_B Match (Channel-to-Channel) (Note 11)	V_{CM} = V^- to V^+		0.2	6	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-		1.3 1 3	7 7 12	µA µA µA
	Input Noise Voltage	0.1Hz to 10Hz		600		nV_{P-P}
e_n	Input Noise Voltage Density	f = 100kHz f = 10kHz		0.95 1.4	 2.3	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density, Balanced Source Unbalanced Source	f = 10kHz f = 10kHz		2.2 3.5		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Input Resistance	Common Mode Differential Mode		0.57 2.1		MΩ kΩ
C_{IN}	Input Capacitance	Common Mode Differential Mode		3.1 4.2		pF pF
A_{VOL}	Large-Signal Gain	V_O = ±4.5V, R_L = 1k V_O = ±2V, R_L = 100	115 15	200 26		V/mV V/mV

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±5V, V_{CM} = V_{OUT} = 0V, $V_{\overline{SHDN}}$ = OPEN, unless otherwise noted. Excludes the LT6201 in the DD package (Note 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- to V^+ V_{CM} = –2V to 2V	68 75	96 100		dB dB
	CMRR Match (Channel-to-Channel) (Note 11)	V_{CM} = –2V to 2V	80	105		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.25V to ±5V	60	68		dB
	PSRR Match (Channel-to-Channel) (Note 6)	V_S = ±1.25V to ±5V	65	100		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 20mA		12 55 150	50 110 290	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA		70 110 225	130 210 420	mV mV mV
I_{SC}	Short-Circuit Current		±60	±90		mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $V_{\overline{SHDN}}$ = 0.3V		20 1.6	23 2.1	mA mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0.3V		200	280	µA
V_L	$V_{\overline{SHDN}}$ Pin Input Voltage LOW				0.3	V
V_H	$V_{\overline{SHDN}}$ Pin Input Voltage HIGH		V^+ – 0.5			V
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V		0.1	75	µA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω, V_S = 5V		130		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω, V_S = 5V		180		ns
GBW	Gain Bandwidth Product	Frequency = 1MHz LT6200-5 LT6200-10	110 530 1060	165 800 1600		MHz MHz MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = 4V	35	50		V/µs
		A_V = –10, R_L = 1k, V_O = 4V LT6200-5 LT6200-10	 175 315	 250 450		 V/µs V/µs
FPBW	Full Power Bandwidth (Note 9)	V_{OUT} = $3V_{P-P}$ (LT6200-10)	33	47		MHz
t_S	Settling Time (LT6200, LT6201)	0.1%, V_{STEP} = 2V, A_V = –1, R_L = 1k		140		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over 0°C < T_A < 70°C temperature range. Excludes the LT6201 in the DD package (Note 3). V_S = ±5V, V_{CM} = V_{OUT} = 0V, $V_{\overline{SHDN}}$ = OPEN, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-	● ● ●		1.9 3.5 3.5	4.5 7.5 7.5	mV mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 11)	V_{CM} = 0V V_{CM} = V^- to V^+	● ●		0.2 0.4	1.8 3.4	mV mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	V_{CM} = Half Supply	●		8.2	24	µV/°C
I_B	Input Bias Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-	● ● ●	–40 –50	–10 8 –23	 18 	µA µA µA
ΔI_B	I_B Shift	V_{CM} = V^- to V^+	●		31	68	µA
	I_B Match (Channel-to-Channel) (Note 11)	V_{CM} = V^- to V^+	●		1	9	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-	● ● ●		1.3 1.0 3.5	10 10 15	µA µA µA
A_{VOL}	Large-Signal Gain	V_O = ±4.5V, R_L = 1k V_O = ±2V, R_L = 100	● ●	46 7.5	80 13.5		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- to V^+ V_{CM} = –2V to 2V	● ●	65 75	90 100		dB dB
	CMRR Match (Channel-to-Channel) (Note 11)	V_{CM} = –2V to 2V	●	75	105		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±5V	●	60	65		dB
	PSRR Match (Channel-to-Channel) (Note 6)	V_S = ±1.5V to ±5V	●	60	100		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 20mA	● ● ●		16 60 170	70 120 310	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●		85 125 265	150 230 480	mV mV mV
I_{SC}	Short-Circuit Current		●	±60	±90		mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $V_{\overline{SHDN}}$ = 0.3V	● ●		25 1.6	29 2.1	mA mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0.3V	●		215	295	µA
V_L	$V_{\overline{SHDN}}$ Pin Input Voltage LOW		●			0.3	V
V_H	$V_{\overline{SHDN}}$ Pin Input Voltage HIGH		●	V^+ – 0.5			V
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V	●		0.1	75	µA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω, V_S = 5V	●		130		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω, V_S = 5V	●		180		ns
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = 4V	●	31	44		V/µs
		A_V = –10, R_L = 1k, V_O = 4V LT6200-5 LT6200-10	 ● ●	 150 290	 215 410		 V/µs V/µs
FPBW	Full Power Bandwidth (Note 9)	V_{OUT} = $3V_{P-P}$ (LT6200-10)	●	30	43		MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over –40°C < T_A < 85°C temperature range. Excludes the LT6201 in the DD package (Note 3). V_S = ±5V, V_{CM} = V_{OUT} = 0V, $V_{\overline{SHDN}}$ = OPEN, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-	● ● ●		1.9 3.5 3.5	4.5 7.5 7.5	mV mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 11)	V_{CM} = 0V V_{CM} = V^- to V^+	● ●		0.2 0.4	2.0 3.6	mV mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	V_{CM} = Half Supply	●		8.2	24	µV/°C
I_B	Input Bias Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-	● ● ●	–40 –50	–10 8 –23	 18 	µA µA µA
ΔI_B	I_B Shift	V_{CM} = V^- to V^+	●		31	68	µA
	I_B Match (Channel-to-Channel) (Note 11)		●		4	12	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-	● ● ●		1.3 1.0 3.5	10 10 15	µA µA µA
A_{VOL}	Large-Signal Gain	V_O = ±4.5V, R_L = 1k V_O = ±2V R_L = 100	● ●	46 7.5	80 13.5		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- to V^+ V_{CM} = –2V to 2V	● ●	65 75	90 100		dB dB
	CMRR Match (Channel-to-Channel) (Note 11)	V_{CM} = –2V to 2V	●	75	105		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±5V	●	60	65		dB
	PSRR Match (Channel-to-Channel) (Note 6)	V_S = ±1.5V to ±5V	●	60	100		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 20mA	● ● ●		16 60 170	75 125 310	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●		85 125 265	150 230 480	mV mV mV
I_{SC}	Short-Circuit Current		●	±60	±90		mA
I_S	Supply Current Disabled Supply Current	 $V_{\overline{SHDN}}$ = 0.3V	● ●		25 1.6	29 2.1	mA mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0.3V	●		215	295	µA
V_L	$V_{\overline{SHDN}}$ Pin Input Voltage LOW		●			0.3	V
V_H	$V_{\overline{SHDN}}$ Pin Input Voltage HIGH		●	V^+ – 0.5			V
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V	●		0.1	75	µA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω, V_S = 5V	●		130		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω, V_S = 5V	●		180		ns
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = 4V	●	31	44		V/µs
		A_V = –10, R_L = 1k, V_O = 4V LT6200-5 LT6200-10	 ● ●	 125 260	 180 370		 V/µs V/µs
FPBW	Full Power Bandwidth (Note 9)	V_{OUT} = $3V_{P-P}$ (LT6200-10)	●	27	39		MHz

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Inputs are protected by back-to-back diodes. If the differential input voltage exceeds 0.7V, the input current must be limited to less than 40mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely. The LT6201 in the DD package is limited by power dissipation to V_S ≤ 5V, 0V over the commercial temperature range only.

Note 4: The LT6200C/LT6200I and LT6201C/LT6201I are guaranteed functional over the temperature range of –40°C and 85°C (LT6201DD excluded).

ELECTRICAL CHARACTERISTICS

Note 5: The LT6200C/LT6201C are guaranteed to meet specified performance from 0°C to 70°C. The LT6200C/LT6201C are designed, characterized and expected to meet specified performance from –40°C to 85°C, but are not tested or QA sampled at these temperatures. The LT6200I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 7: Output voltage swings are measured between the output and power supply rails.

Note 8: This parameter is not 100% tested.

Note 9: Full-power bandwidth is calculated from the slew rate: FPBW = $SR/2\pi V_P$

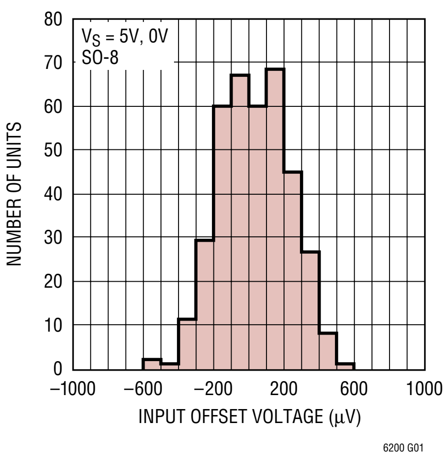
Note 10: Thermal resistance varies depending upon the amount of PC board metal attached to the V^- pin of the device. θ_{JA} is specified for a certain amount of 2oz copper metal trace connecting to the V^- pin as described in the thermal resistance tables in the Application Information section.

Note 11: Matching parameters on the LT6201 are the difference between the two amplifiers. CMRR and PSRR match are defined as follows: CMRR and PSRR are measured in µV/V on the identical amplifiers. The difference is calculated in µV/V. The result is converted to dB.

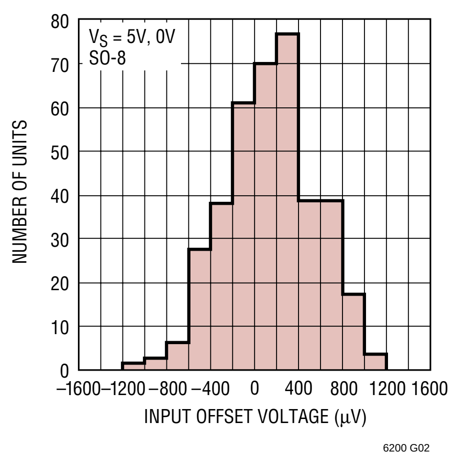
Note 12: There are reverse biased ESD diodes on all inputs and outputs as shown in Figure 1. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient in nature and limited to less than 30mA, no damage to the device will occur.

TYPICAL PERFORMANCE CHARACTERISTICS

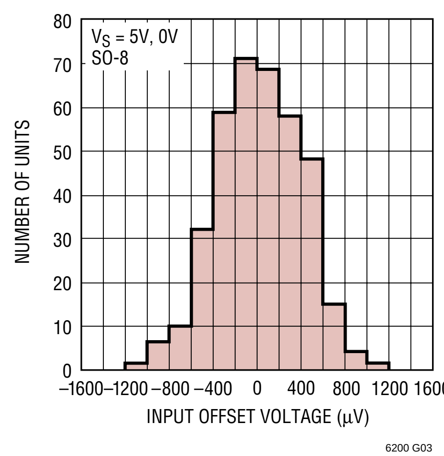
V_{OS} Distribution, $V_{CM} = V^+/2$



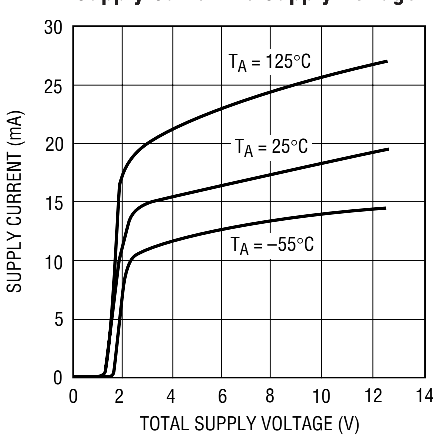
V_{OS} Distribution, $V_{CM} = V^+$



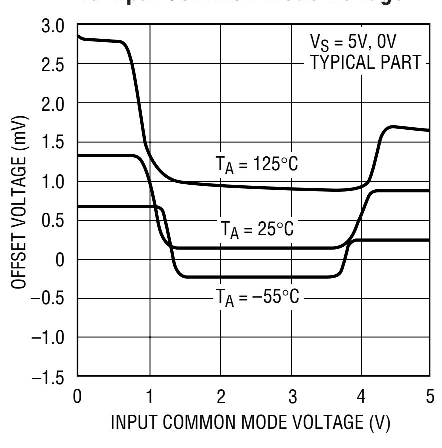
V_{OS} Distribution, $V_{CM} = V^-$



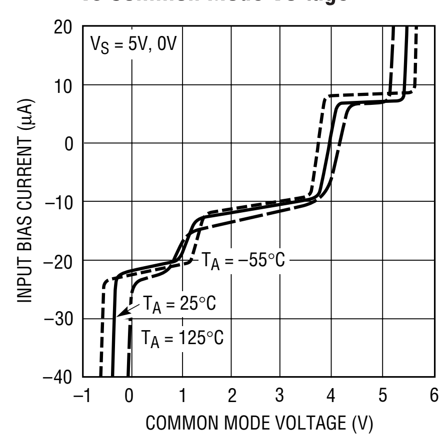
Supply Current vs Supply Voltage



Offset Voltage vs Input Common Mode Voltage

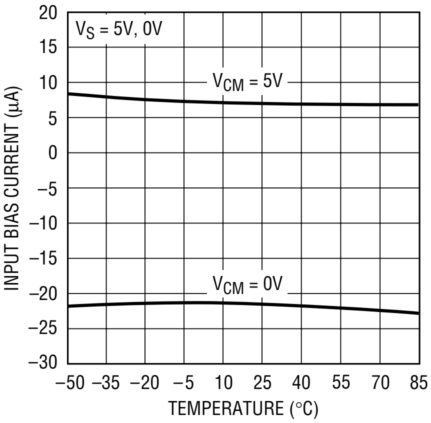


Input Bias Current vs Common Mode Voltage

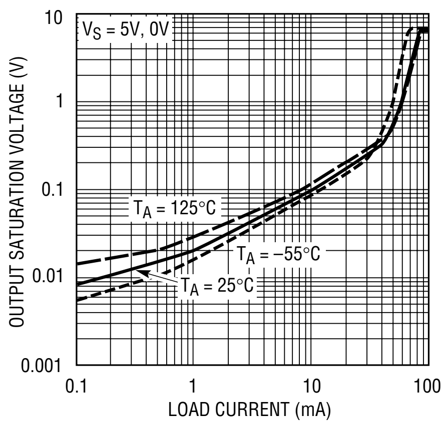


TYPICAL PERFORMANCE CHARACTERISTICS

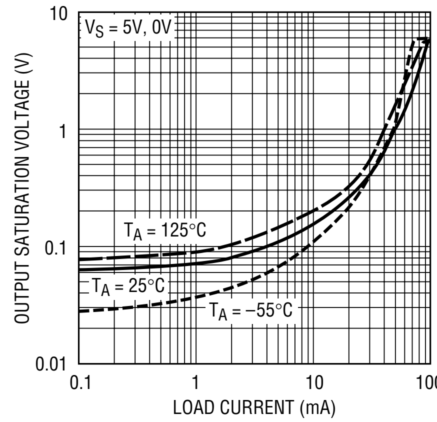
Input Bias Current vs Temperature



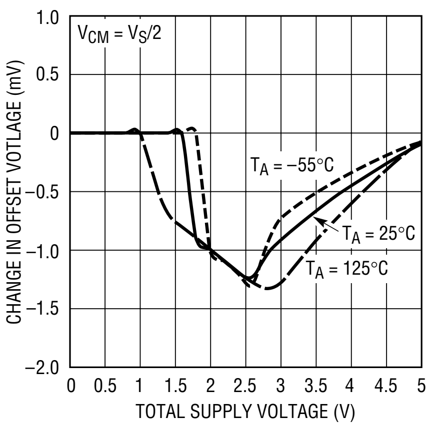
Output Saturation Voltage vs Load Current (Output Low)



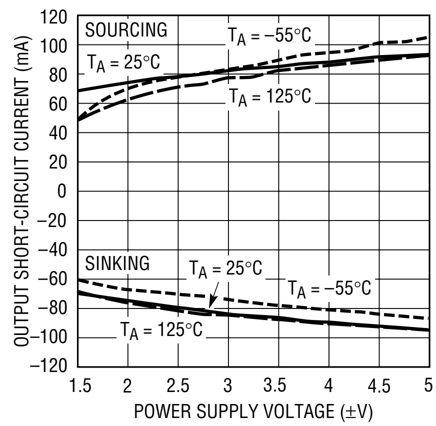
Output Saturation Voltage vs Load Current (Output High)



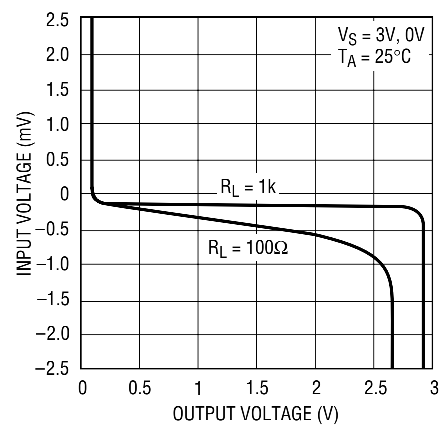
Minimum Supply Voltage



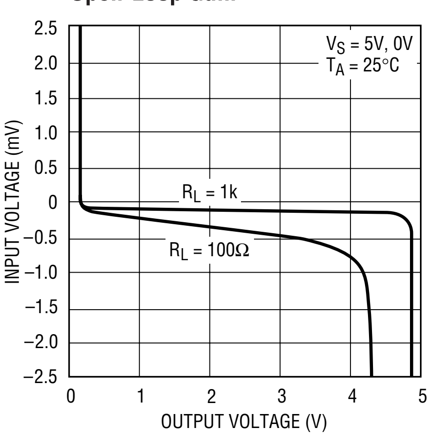
Output Short-Circuit Current vs Power Supply Voltage



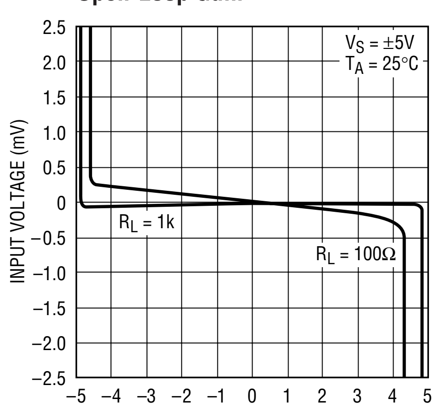
Open-Loop Gain



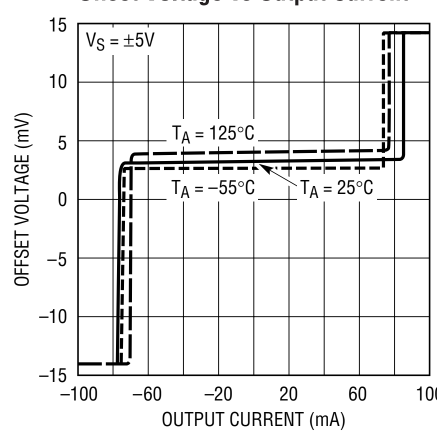
Open-Loop Gain



Open-Loop Gain

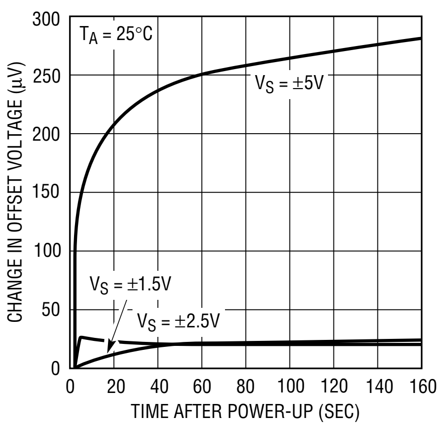


Offset Voltage vs Output Current



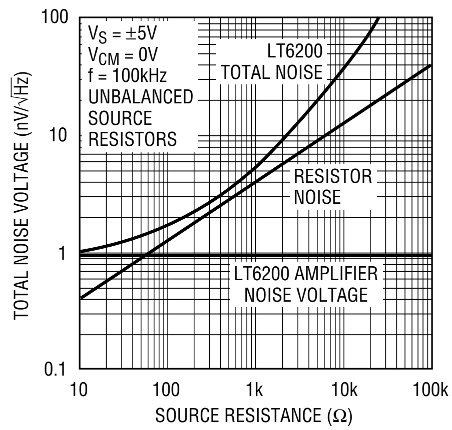
TYPICAL PERFORMANCE CHARACTERISTICS

Warm-Up Drift vs Time (LT6200S8)



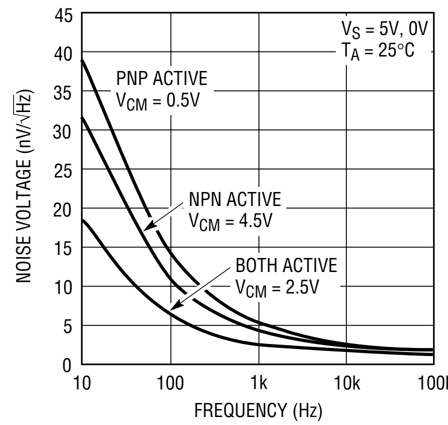
6200 G16

Total Noise vs Source Resistance



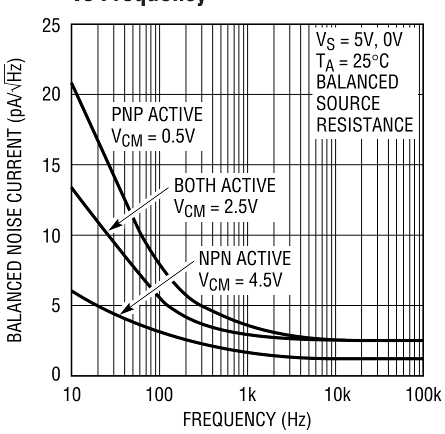
6200 G17

Input Noise Voltage vs Frequency



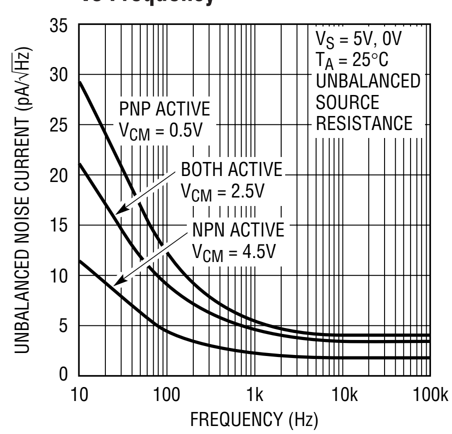
6200 G18

Balanced Noise Current vs Frequency



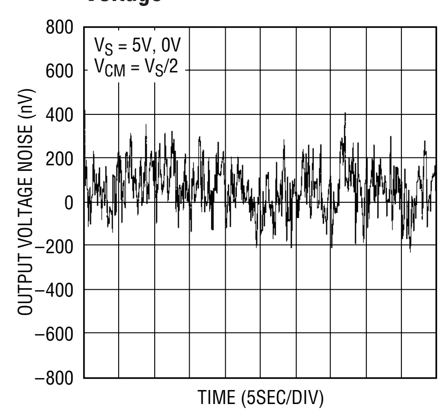
6200 G19

Unbalanced Noise Current vs Frequency



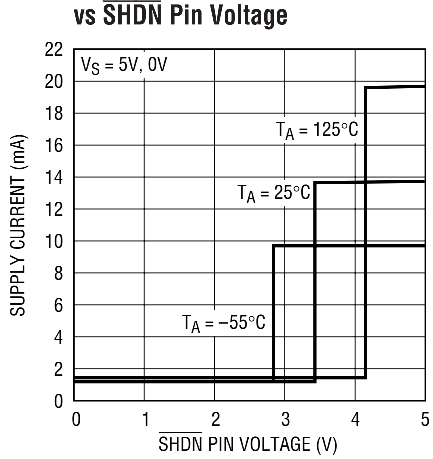
6200 G20

0.1Hz to 10Hz Output Noise Voltage



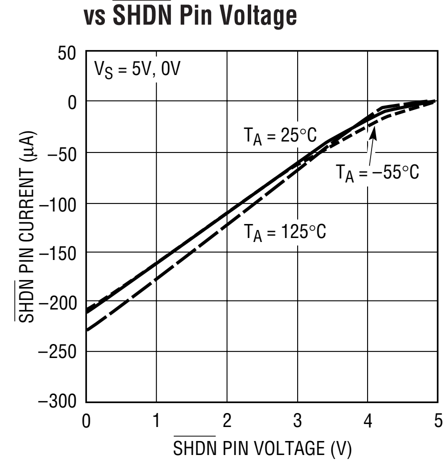
6200 G21

Supply Current vs $\overline{SHDN}$ Pin Voltage



6200 G43

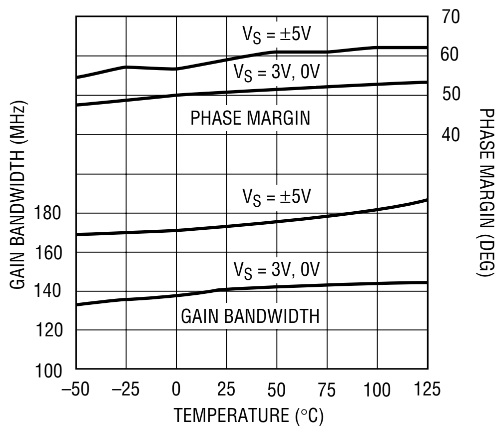
$\overline{SHDN}$ Pin Current vs $\overline{SHDN}$ Pin Voltage



6200 G44

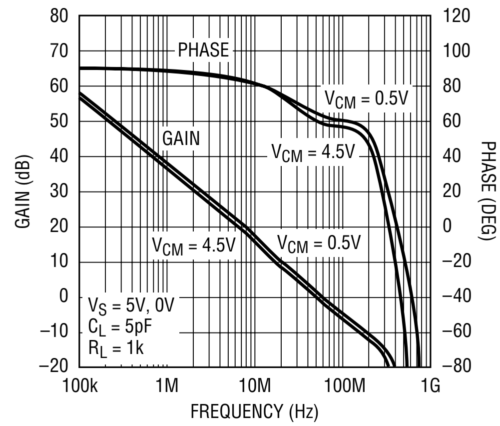
TYPICAL PERFORMANCE CHARACTERISTICS LT6200, LT6201

Gain Bandwidth and Phase Margin vs Temperature



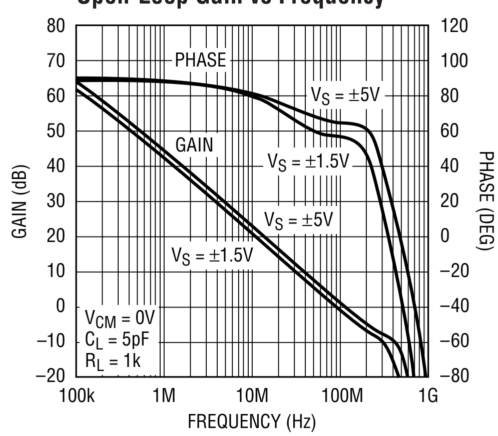
6200 G22

Open-Loop Gain vs Frequency



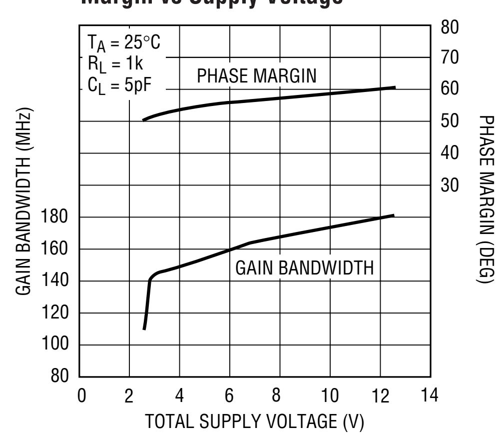
6200 G23

Open-Loop Gain vs Frequency



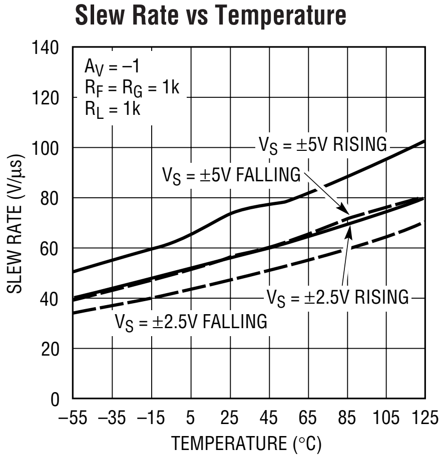
6200 G24

Gain Bandwidth and Phase Margin vs Supply Voltage



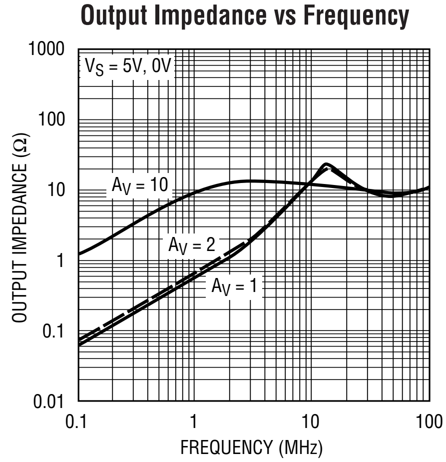
6200 G25

Slew Rate vs Temperature



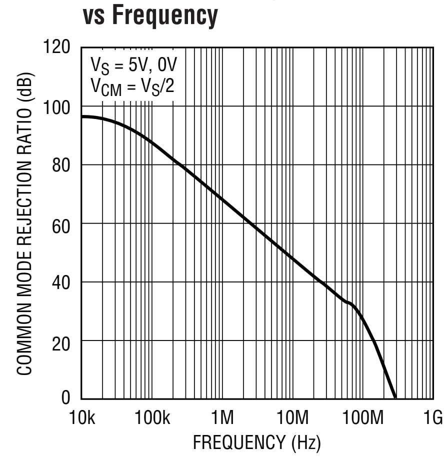
6200 G26

Output Impedance vs Frequency



6200 G27

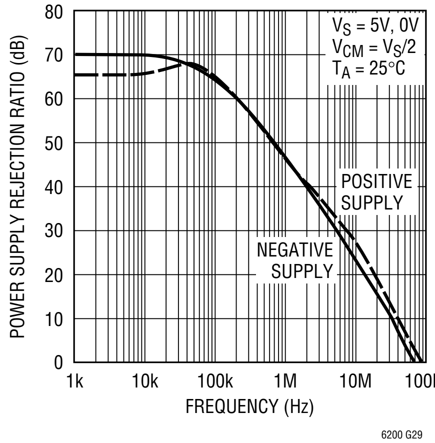
Common Mode Rejection Ratio vs Frequency



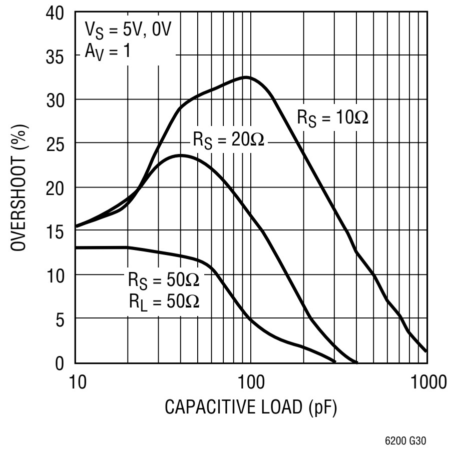
6200 G28

TYPICAL PERFORMANCE CHARACTERISTICS LT6200, LT6201

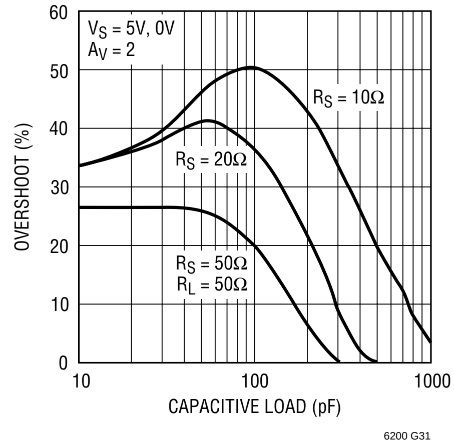
Power Supply Rejection Ratio vs Frequency



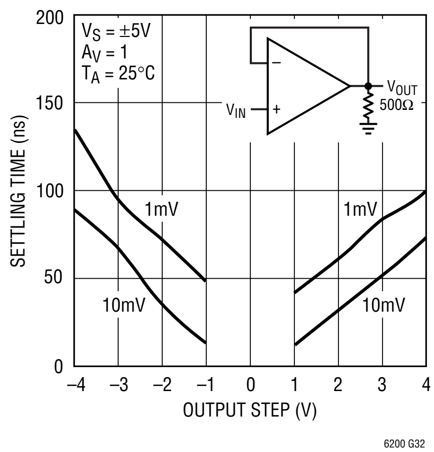
Overshoot vs Capacitive Load



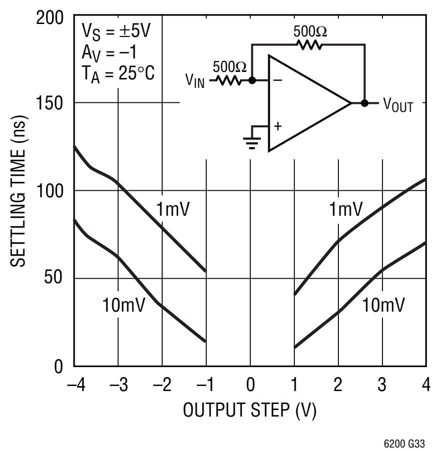
Overshoot vs Capacitive Load



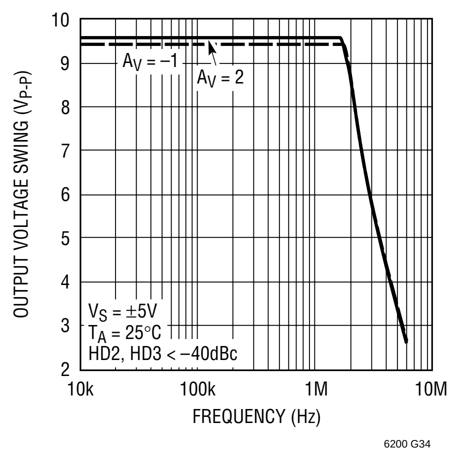
Settling Time vs Output Step (Noninverting)



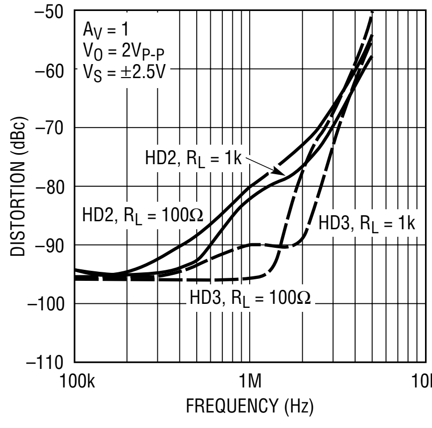
Settling Time vs Output Step (Inverting)



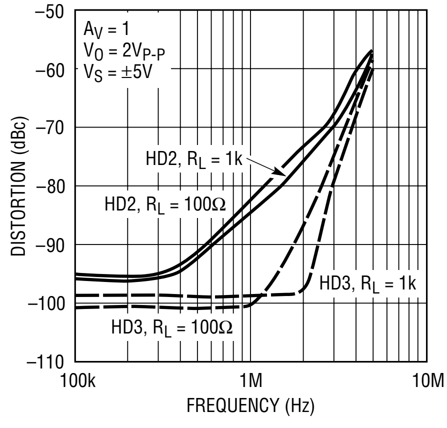
Maximum Undistorted Output Signal vs Frequency



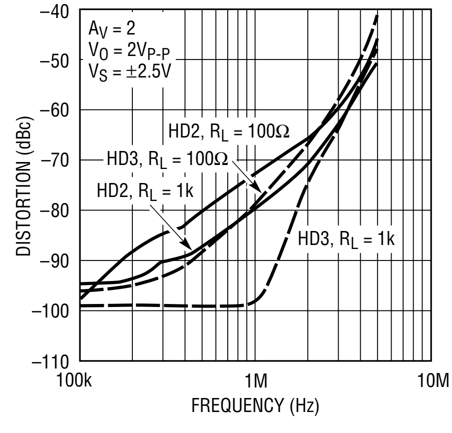
Distortion vs Frequency, $A_V = 1$



Distortion vs Frequency, $A_V = 1$

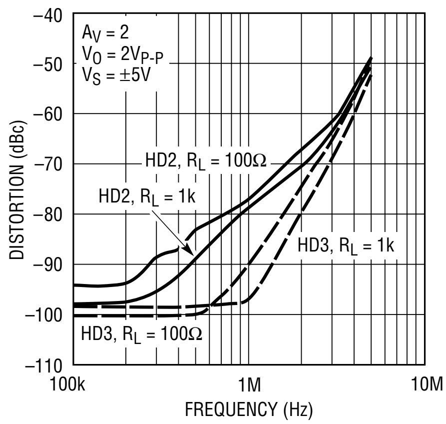


Distortion vs Frequency, $A_V = 2$



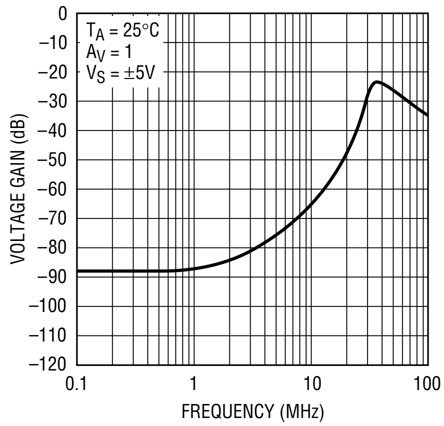
TYPICAL PERFORMANCE CHARACTERISTICS LT6200, LT6201

Distortion vs Frequency, $A_V = 2$



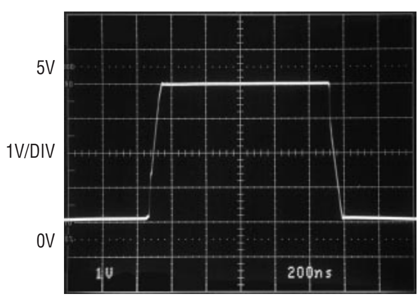
6200 G38

Channel Separation vs Frequency



6200 G77

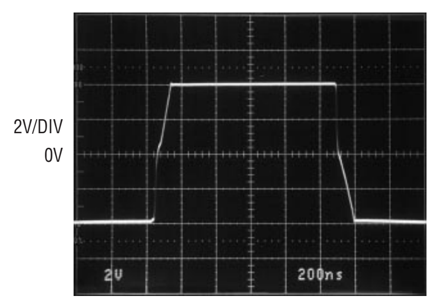
5V Large-Signal Response



$V_S = 5V, 0V$ 200ns/DIV
$A_V = 1$
$R_L = 1k$

6200 G39

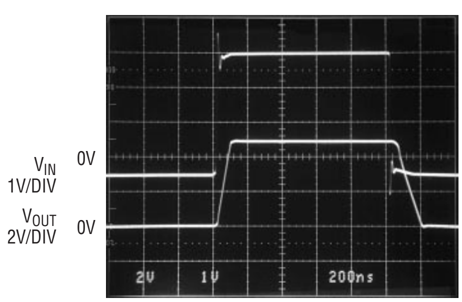
±5V Large-Signal Response



$V_S = \pm 5V$ 200ns/DIV
$A_V = 1$
$R_L = 1k$

6200 G41

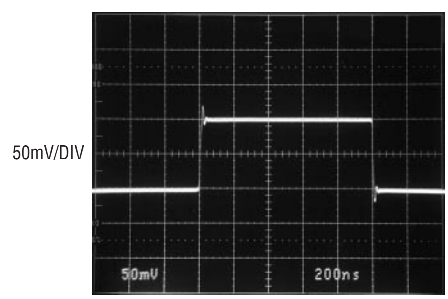
Output Overdrive Recovery



$V_S = 5V, 0V$ 200ns/DIV
$A_V = 2$

6200 G42

5V Small-Signal Response

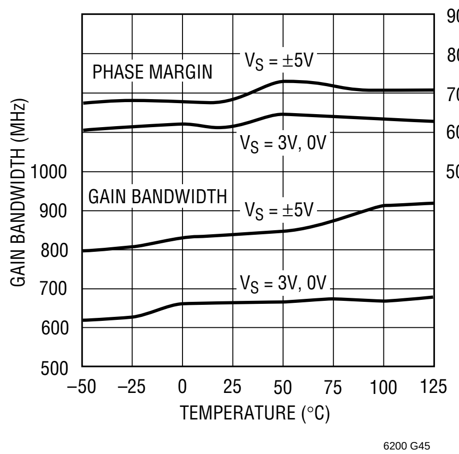


$V_S = 5V, 0V$ 200ns/DIV
$A_V = 1$
$R_L = 1k$

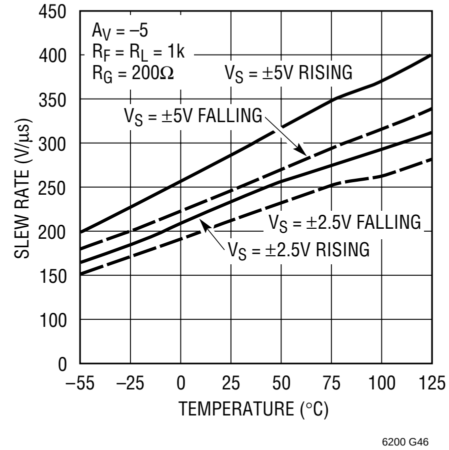
6200 G40

TYPICAL PERFORMANCE CHARACTERISTICS LT6200-5

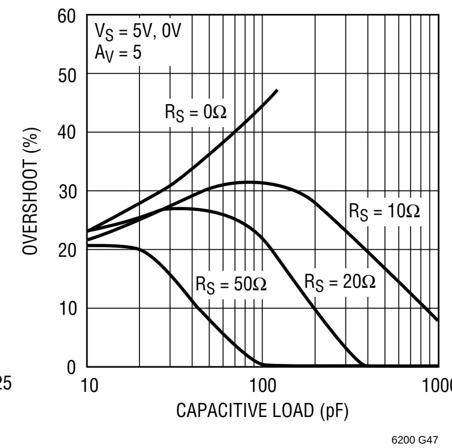
Gain Bandwidth and Phase Margin vs Temperature



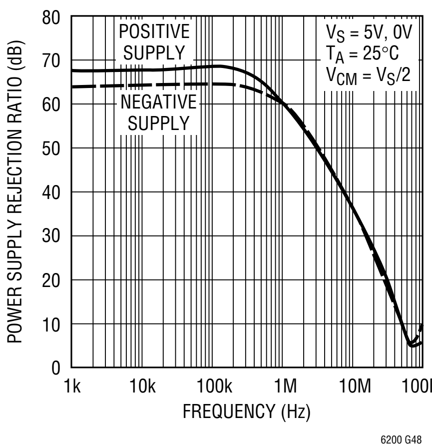
Slew Rate vs Temperature



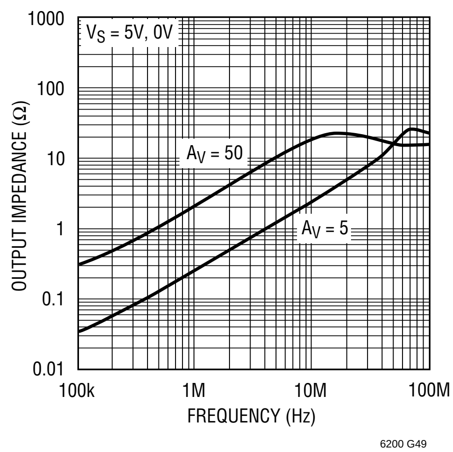
Overshoot vs Capacitive Load



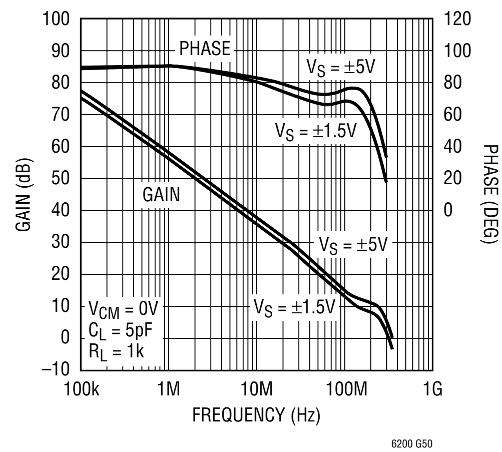
Power Supply Rejection Ratio vs Frequency



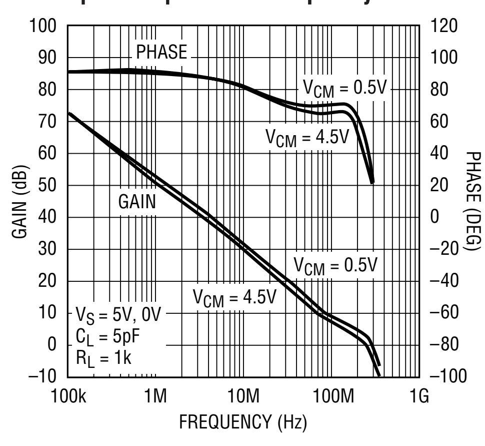
Output Impedance vs Frequency



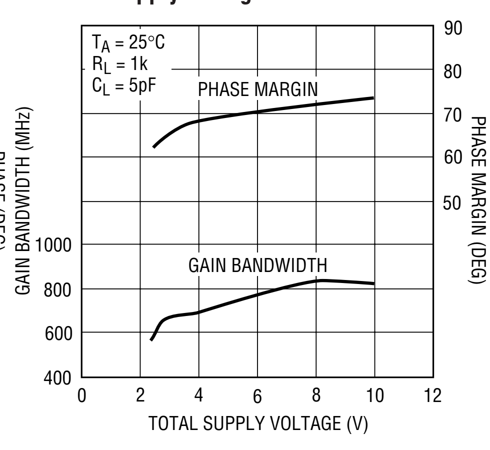
Open-Loop Gain vs Frequency



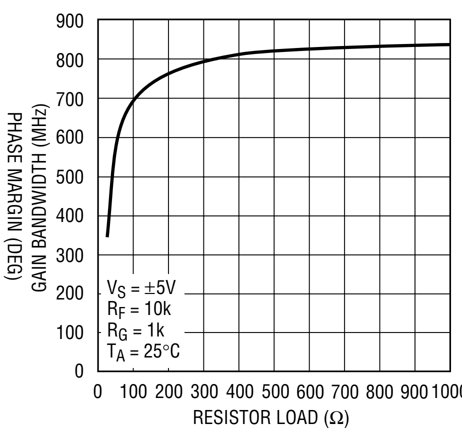
Open-Loop Gain vs Frequency



Gain Bandwidth and Phase Margin vs Supply Voltage

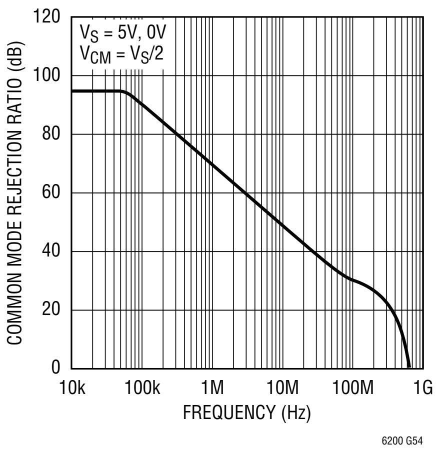


Gain Bandwidth vs Resistor Load

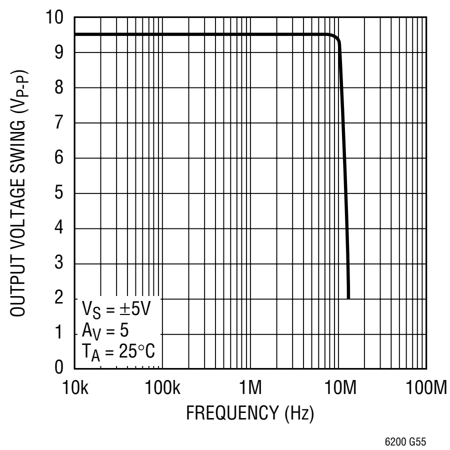


TYPICAL PERFORMANCE CHARACTERISTICS LT6200-5

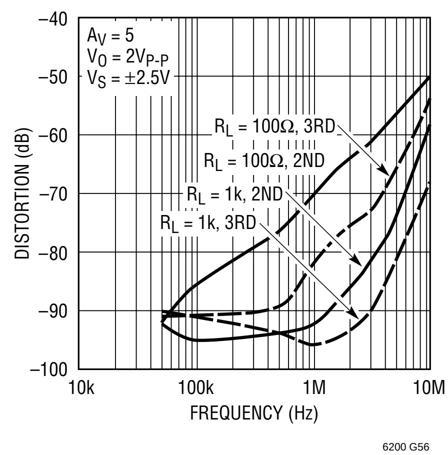
Common Mode Rejection Ratio vs Frequency



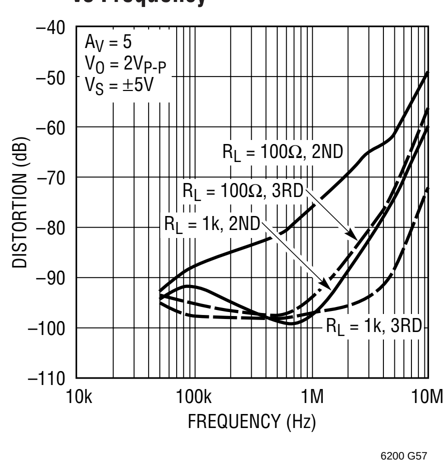
Maximum Undistorted Output Signal vs Frequency



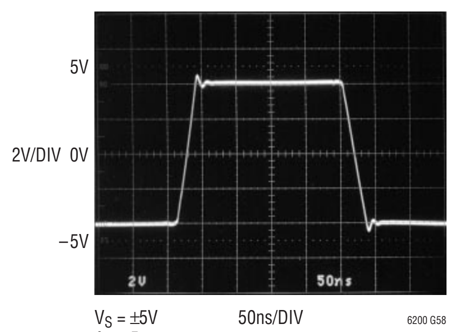
2nd and 3rd Harmonic Distortion vs Frequency



2nd and 3rd Harmonic Distortion vs Frequency

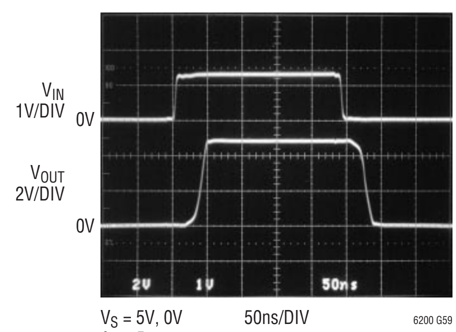


±5V Large-Signal Response



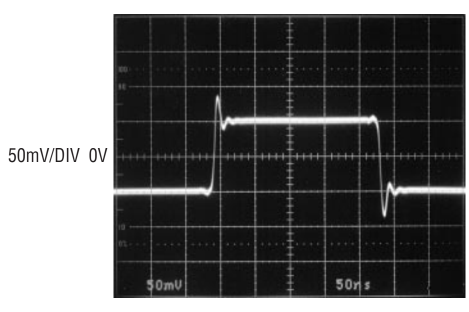
V_S = ±5V 50ns/DIV
A_V = 5
R_L = 1k
C_L = 10.8pF SCOPE PROBE
6200 G58

Output-Overdrive Recovery



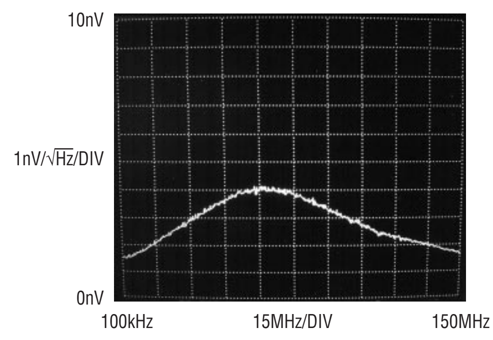
V_S = 5V, 0V 50ns/DIV
A_V = 5
C_L = 10.8pF SCOPE PROBE
6200 G59

5V Small-Signal Response



V_S = 5V, 0V 50ns/DIV
A_V = 5
R_L = 1k
C_L = 10.8pF SCOPE PROBE
6200 G61

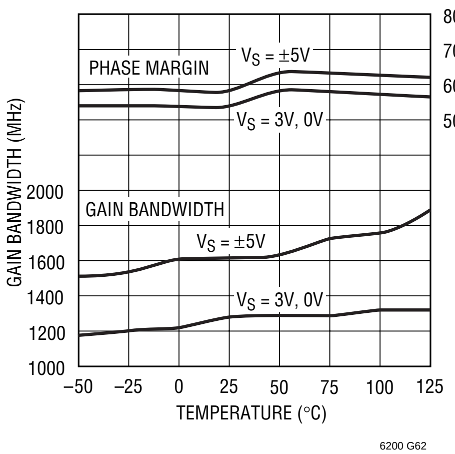
Input Referred High Frequency Noise Spectrum



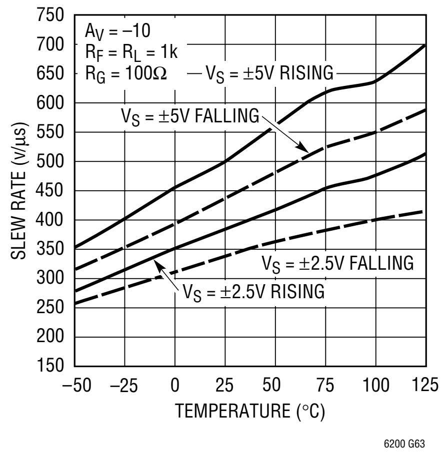
NOISE LIMITED BY INSTRUMENT NOISE FLOOR

TYPICAL PERFORMANCE CHARACTERISTICS LT6200-10

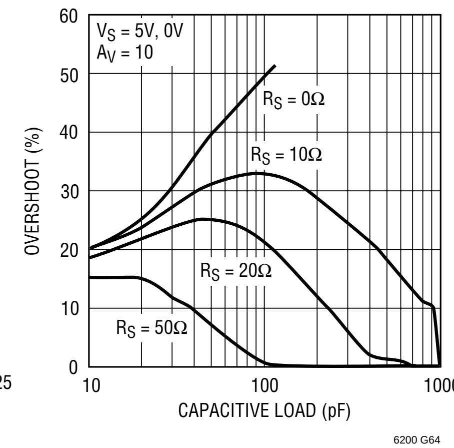
Gain Bandwidth and Phase Margin vs Temperature



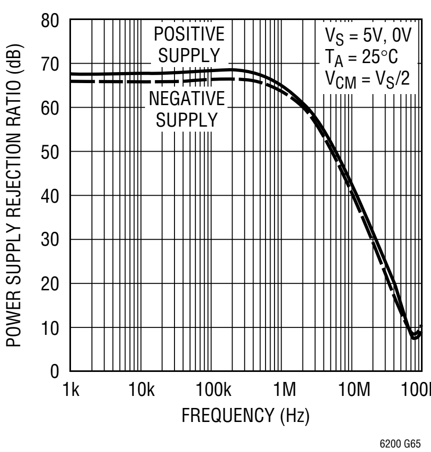
Slew Rate vs Temperature



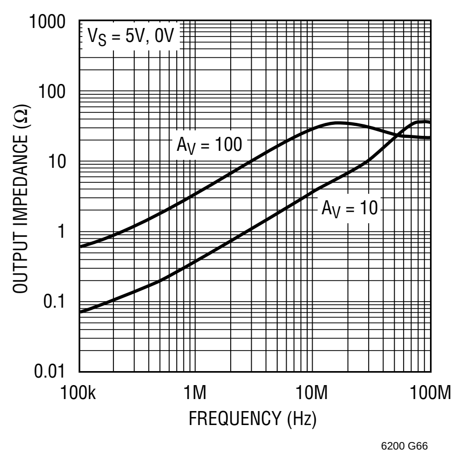
Overshoot vs Capacitive Load



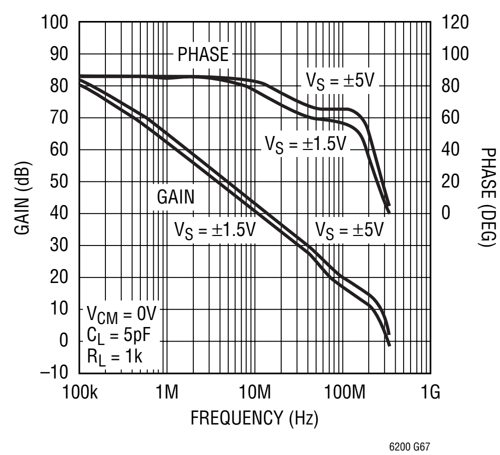
Power Supply Rejection Ratio vs Frequency



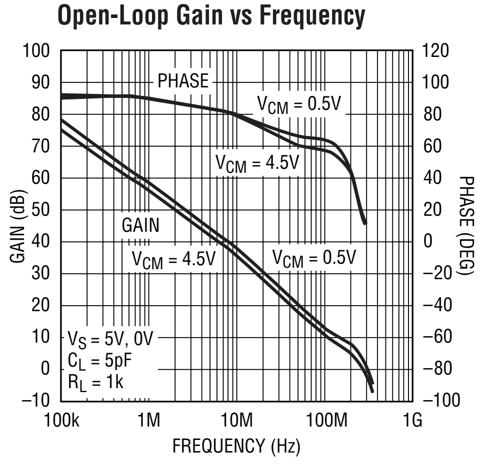
Output Impedance vs Frequency



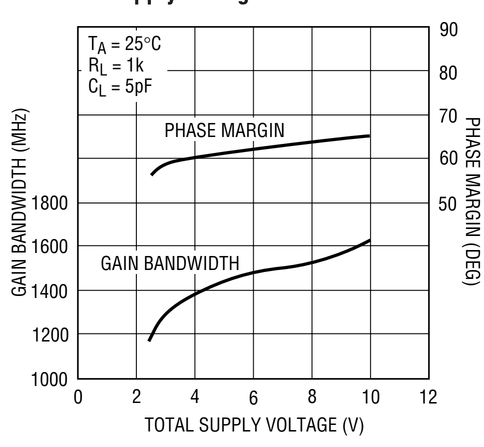
Open-Loop Gain vs Frequency



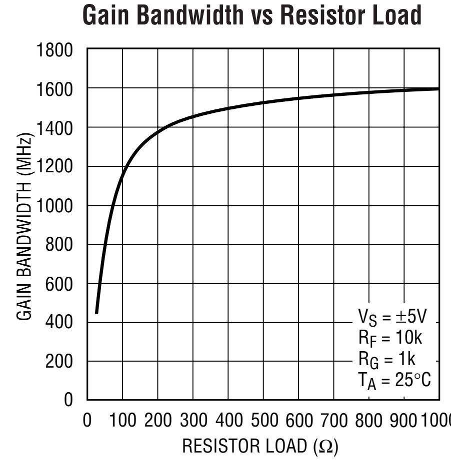
Open-Loop Gain vs Frequency



Gain Bandwidth and Phase Margin vs Supply Voltage

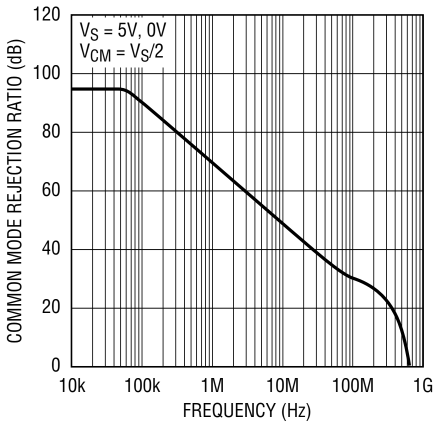


Gain Bandwidth vs Resistor Load



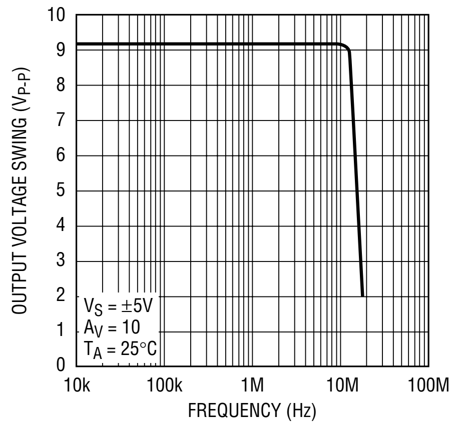
TYPICAL PERFORMANCE CHARACTERISTICS LT6200-10

Common Mode Rejection Ratio vs Frequency



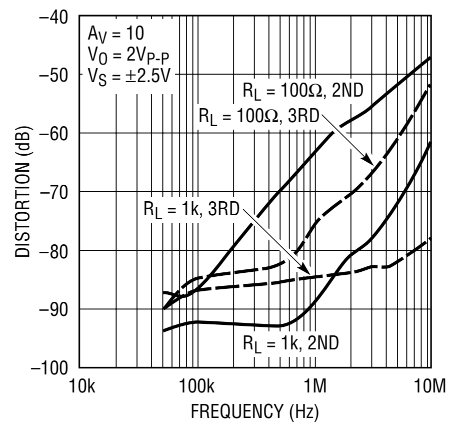
6200 G71

Maximum Undistorted Output Signal vs Frequency



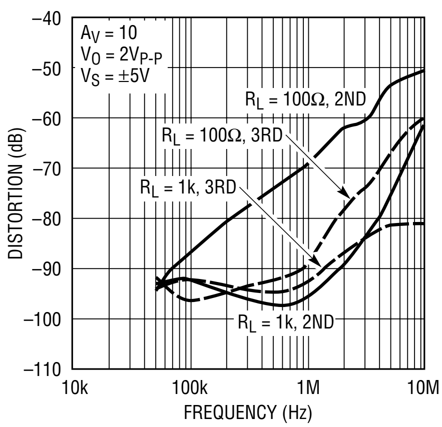
6200 G72

2nd and 3rd Harmonic Distortion vs Frequency



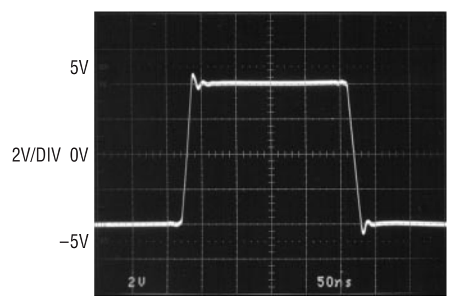
6200 G73

2nd and 3rd Harmonic Distortion vs Frequency



6200 G74

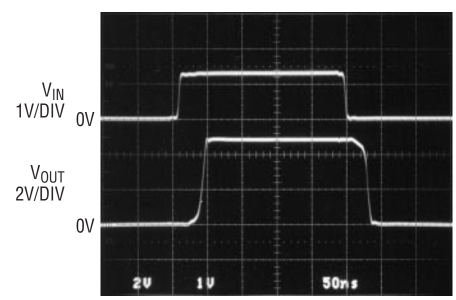
±5V Large-Signal Response



V_S = ±5V 50ns/DIV
A_V = 10
R_L = 1k
C_L = 10.8pF SCOPE PROBE

6200 G75

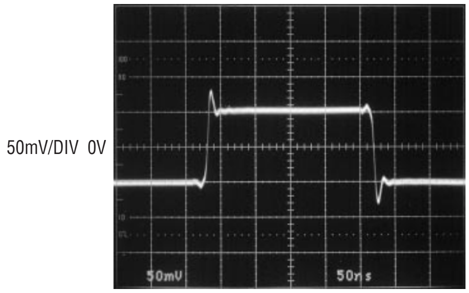
Output-Overdrive Recovery



V_S = 5V, 0V 50ns/DIV
A_V = 10
C_L = 10.8pF SCOPE PROBE

6200 G76

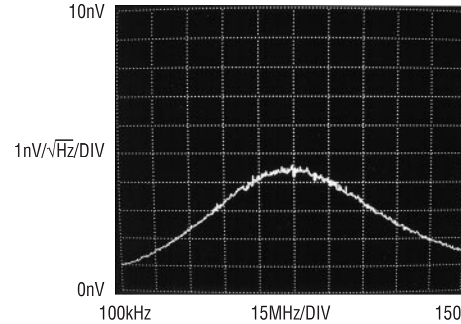
5V Small-Signal Response



V_S = 5V, 0V 50ns/DIV
A_V = 10
R_L = 1k
C_L = 10.8pF SCOPE PROBE

6200 G78

Input Referred High Frequency Noise Spectrum



6200 G77

APPLICATIONS INFORMATION

Amplifier Characteristics

Figure 1 shows a simplified schematic of the LT6200 family, which has two input differential amplifiers in parallel that are biased on simultaneously when the common mode voltage is at least 1.5V from either rail. This topology allows the input stage to swing from the positive supply voltage to the negative supply voltage. As the common mode voltage swings beyond V_{CC} – 1.5V, current source I_1 saturates and current in Q1/Q4 is zero. Feedback is maintained through the Q2/Q3 differential amplifier, but with an input g_m reduction of 1/2. A similar effect occurs with I_2 when the common mode voltage swings within 1.5V of the negative rail. The effect of the g_m reduction is a shift in the V_{OS} as I_1 or I_2 saturate.

Input bias current normally flows out of the + and – inputs. The magnitude of this current increases when the input common mode voltage is within 1.5V of the negative rail, and only Q1/Q4 are active. The polarity of this current reverses when the input common mode voltage is within 1.5V of the positive rail and only Q2/Q3 are active.

The second stage is a folded cascode and current mirror that converts the input stage differential signals to a single ended output. Capacitor C1 reduces the unity cross frequency and improves the frequency stability without degrading the gain bandwidth of the amplifier. The differential drive generator supplies current to the output transistors that swing from rail-to-rail.

The LT6200-5/LT6200-10 are decompensated op amps for higher gain applications. These amplifiers maintain identical DC specifications with the LT6200, but have a reduced Miller compensation capacitor C_M. This results in a significantly higher slew rate and gain bandwidth product.

Input Protection

There are back-to-back diodes, D1 and D2, across the + and – inputs of these amplifiers to limit the differential input voltage to ±0.7V. The inputs of the LT6200 family do not have internal resistors in series with the input transistors. This technique is often used to protect the input devices from overvoltage that causes excessive currents to flow. The addition of these resistors would significantly degrade the low noise voltage of these amplifiers. For instance, a 100Ω resistor in series with each input would generate 1.8nV/$\sqrt{Hz}$ of noise, and the total amplifier noise voltage would rise from 0.95nV/$\sqrt{Hz}$ to 2.03nV/$\sqrt{Hz}$. Once the input differential voltage exceeds ±0.7V, steady-state current conducted though the protection diodes should be limited to ±40mA. This implies 25Ω of protection resistance per volt of continuous overdrive beyond ±0.7V. The input diodes are rugged enough to handle transient currents due to amplifier slew rate overdrive or momentary clipping without these resistors.

Figure 2 shows the input and output waveforms of the LT6200 driven into clipping while connected in a gain of

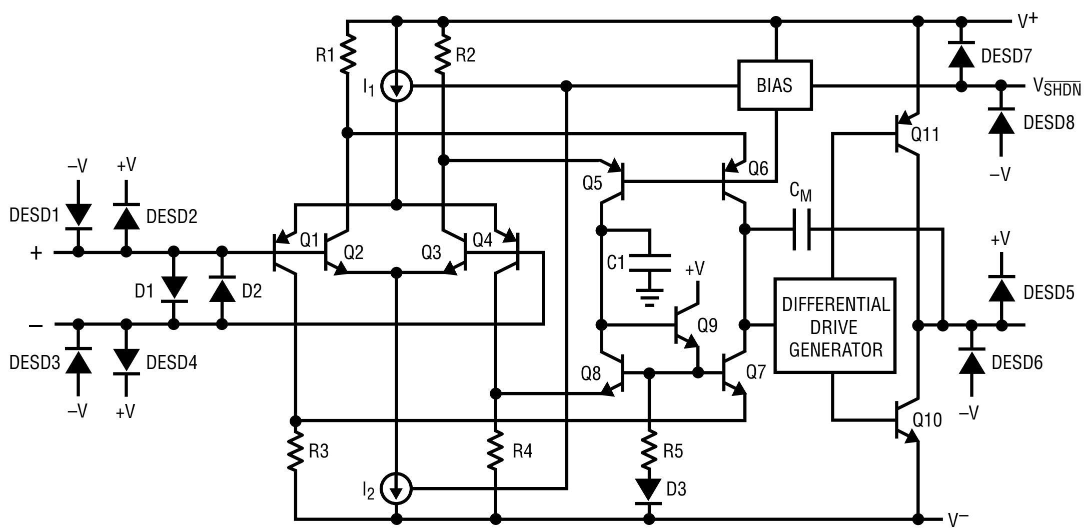


Figure 1. Simplified Schematic

APPLICATIONS INFORMATION

A_V = 1. In this photo, the input signal generator is clipping at ±35mA, and the output transistors supply this generator current through the protection diodes.

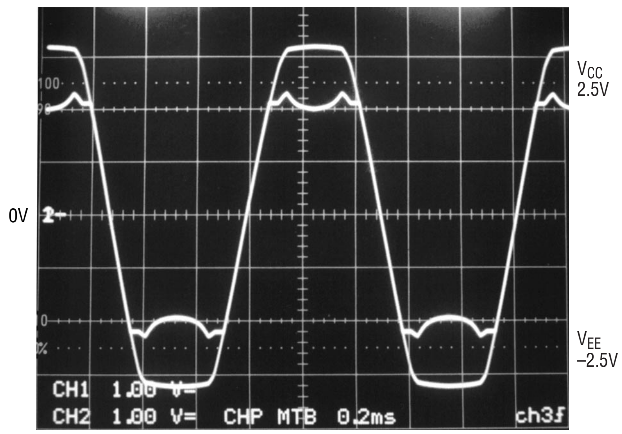


Figure 2. V_S = ±2.5V, A_V = 1 with Large Overdrive

ESD

The LT6200 has reverse-biased ESD protection diodes on all inputs and outputs as shown in Figure 1. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to 30mA or less, no damage to the device will occur.

Noise

The noise voltage of the LT6200 is equivalent to that of a 56Ω resistor, and for the lowest possible noise it is desirable to keep the source and feedback resistance at or below this value, i.e., $R_S + R_G//R_{FB} \le 56\Omega$. With $R_S + R_G//R_{FB} = 56\Omega$ the total noise of the amplifier is: $e_n = \sqrt{(0.95nV)^2 + (0.95nV)^2} = 1.35nV$. Below this resistance value, the amplifier dominates the noise, but in the resistance region between 56Ω and approximately 6kΩ, the noise is dominated by the resistor thermal noise. As the total resistance is further increased, beyond 6k, the noise current multiplied by the total resistance eventually dominates the noise.

For a complete discussion of amplifier noise, see the LT1028 data sheet.

Power Dissipation

The LT6200 combines high speed with large output current in a small package, so there is a need to ensure that the die's junction temperature does not exceed 150°C. The LT6200 is housed in a 6-lead TSOT-23 package. The package has the V^- supply pin fused to the lead frame to enhance the thermal conductance when connecting to a ground plane or a large metal trace. Metal trace and plated through-holes can be used to spread the heat generated by the device to the backside of the PC board. For example, on a 3/32" FR-4 board with 2oz copper, a total of 270 square millimeters connects to Pin 2 of the LT6200 in an TSOT-23 package will bring the thermal resistance, θ_{JA}, to about 135°C/W. Without extra metal trace beside the power line connecting to the V^- pin to provide a heat sink, the thermal resistance will be around 200°C/W. More information on thermal resistance with various metal areas connecting to the V^- pin is provided in Table 1.

Table 1. LT6200 6-Lead TSOT-23 Package

COPPER AREA TOPSIDE (mm^2)	BOARD AREA (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
270	2500	135°C/W
100	2500	145°C/W
20	2500	160°C/W
0	2500	200°C/W

Device is mounted on topside.

Junction temperature T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The power dissipation in the IC is the function of the supply voltage, output voltage and the load resistance. For a given supply voltage, the worst-case power dissipation $P_{D(MAX)}$ occurs at the maximum quiescent supply current and at the output voltage which is half of either supply voltage (or the maximum swing if it is less than 1/2 the supply voltage). $P_{D(MAX)}$ is given by:

$$P_{D(MAX)} = (V_S \bullet I_{S(MAX)}) + (V_S/2)^2/R_L$$

Example: An LT6200 in TSOT-23 mounted on a 2500mm^2 area of PC board without any extra heat spreading plane connected to its V^- pin has a thermal resistance of

APPLICATIONS INFORMATION

200°C/W, θ_{JA}. Operating on ±5V supplies driving 50Ω loads, the worst-case power dissipation is given by:

$$P_{D(MAX)} = (10 \bullet 23mA) + (2.5)^2/50$$
$$= 0.23 + 0.125 = 0.355W$$

The maximum ambient temperature that the part is allowed to operate is:

$$T_A = T_J – (P_{D(MAX)} \bullet 200°C/W)$$
$$= 150°C – (0.355W \bullet 200°C/W) = 79°C$$

To operate the device at higher ambient temperature, connect more metal area to the $V^–$ pin to reduce the thermal resistance of the package as indicated in Table 1.

DD Package Heat Sinking

The underside of the DD package has exposed metal ($4mm^2$) from the lead frame where the die is attached. This provides for the direct transfer of heat from the die junction to printed circuit board metal to help control the maximum operating junction temperature. The dual-in-line pin arrangement allows for extended metal beyond the ends of the package on the topside (component side) of a PCB. Table 2 summarizes the thermal resistance from the die junction-to-ambient that can be obtained using various amounts of topside metal (2oz copper) area. On mulitlayer boards, further reductions can be obtained using additional metal on inner PCB layers connected through vias beneath the package.

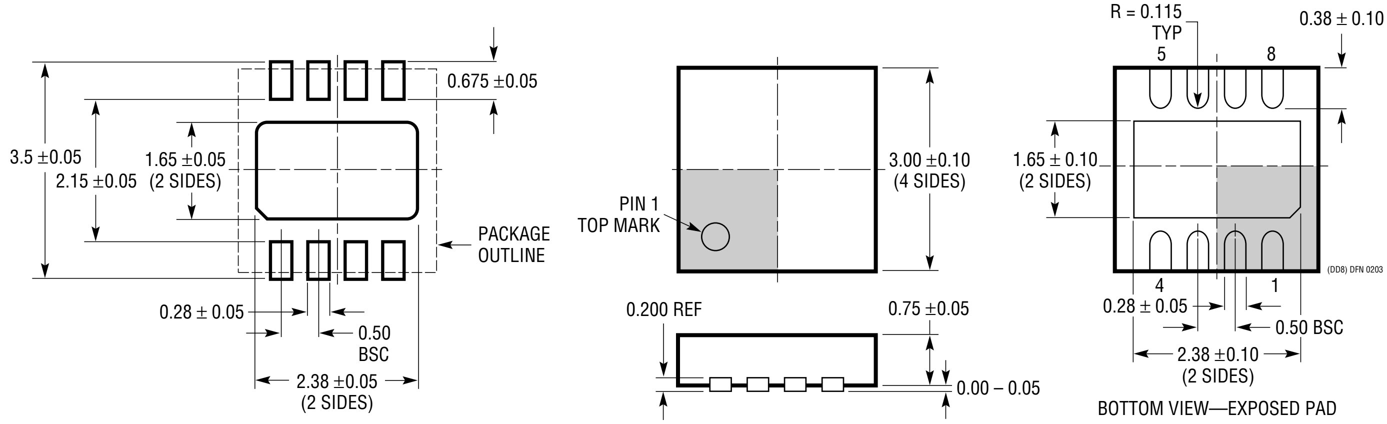
Table 2. LT6200 8-Lead DD Package

COPPER AREA TOPSIDE (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
4	160°C/W
16	135°C/W
32	110°C/W
64	95°C/W
130	70°C/W

The LT6200 amplifier family has thermal shutdown to protect the part from excessive junction temperature. The amplifier will shut down to approximately 1.2mA supply current per amplifier if the maximum temperature is exceeded. The LT6200 will remain off until the junction temperature reduces to about 135°C, at which point the amplifier will return to normal operation.

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)

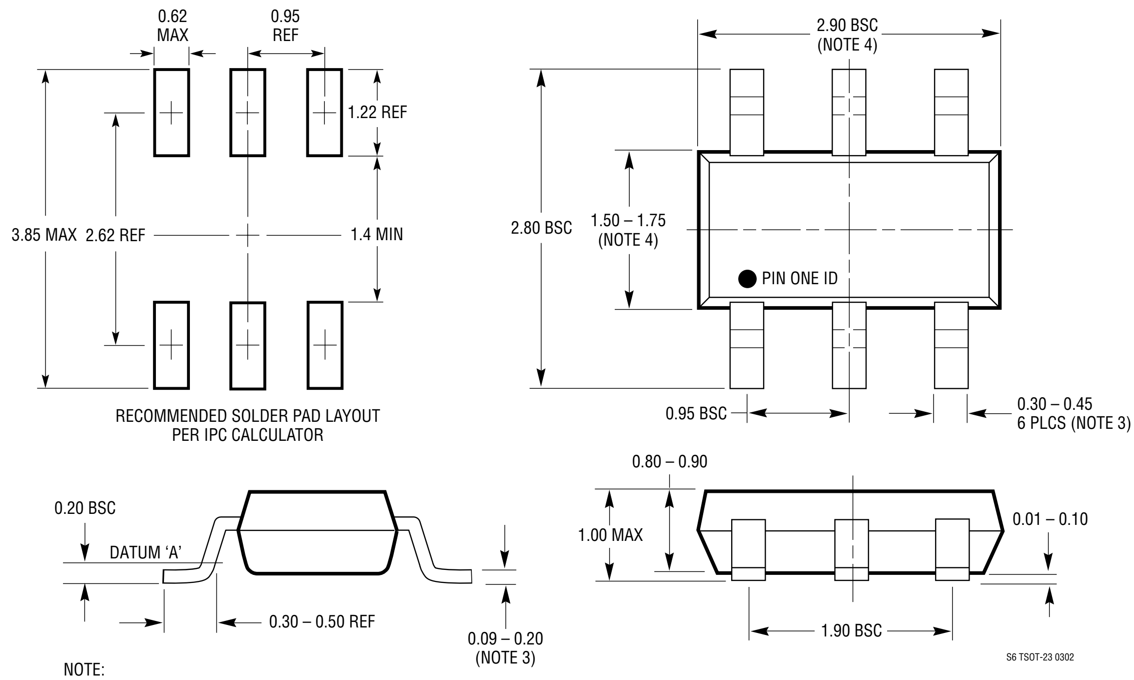


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED

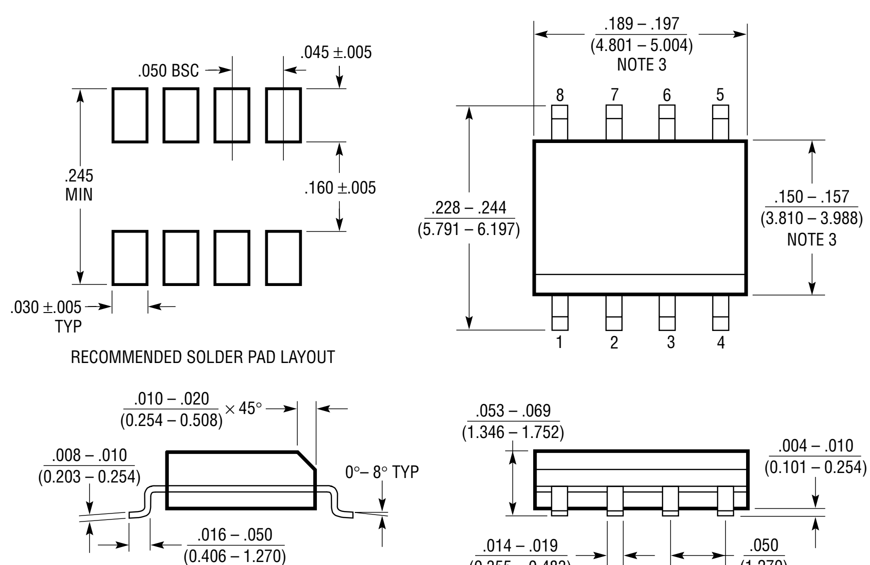
PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

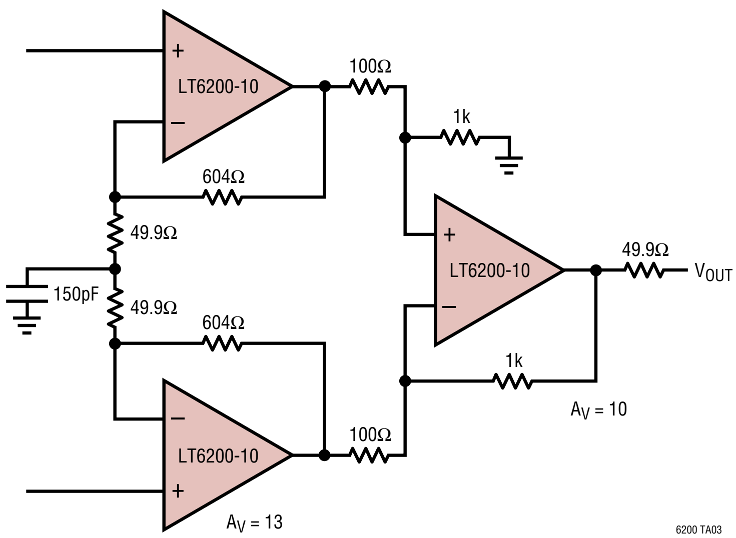


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

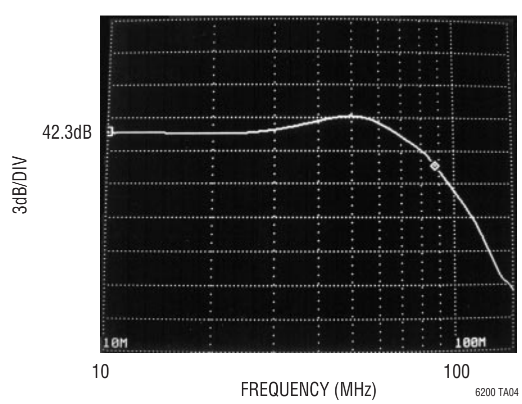
SO8 0303

TYPICAL APPLICATION

Rail-to-Rail High Speed Low Noise Instrumentation Amplifier



Instrumentation Amplifier Frequency Response



A_V = 130
BW_{-3dB} = 85MHz
SLEW RATE = 500V/µs
CMRR = 55dB at 10MHz

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1028	Single, Ultra Low Noise 50MHz Op Amp	1.1nV/$\sqrt{Hz}$
LT1677	Single, Low Noise Rail-to-Rail Amplifier	3V Operation, 2.5mA, 4.5nV/$\sqrt{Hz}$, 60µV Max V_{OS}
LT1722/LT1723/LT1724	Single/Dual/Quad Low Noise Precision Op Amp	70V/µs Slew Rate, 400µV Max V_{OS}, 3.8nV/$\sqrt{Hz}$, 3.7mA
LT1806/LT1807	Single/Dual, Low Noise 325MHz Rail-to-Rail Amplifier	2.5V Operation, 550µV Max V_{OS}, 3.5nV/$\sqrt{Hz}$
LT6203	Dual, Low Noise, Low Current Rail-to-Rail Amplifier	1.9nV/$\sqrt{Hz}$, 3mA Max, 100MHz Gain Bandwidth

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