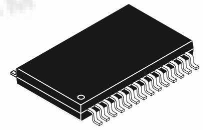
Burr-Brown Products from Texas Instruments

PCM1730



SLES021 – NOVEMBER 2001

24-BIT, 192-kHz SAMPLING ADVANCED SEGMENT, AUDIO STEREO DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **24-Bit Resolution**
- **Analog Performance (V_{CC} = 5 V):**
  - **Dynamic Range: 117 dB (Typically)**
  - **SNR: 117 dB (Typically)**
  - **THD+N: 0.0004% (Typically)**
  - **Full-Scale Output (At Post Amp): 2.2-Vrms**
- **Differential Current Output: ±2.48 mA**
- **8× Oversampling Digital Filter:**
  - **Stop-Band Attenuation: –82 dB**
  - **Pass-Band Ripple: ±0.002 dB**
- **Sampling Frequency of 10 kHz to 200 kHz**
- **System Clock: 128, 192, 256, 384, 512, or 768 f_S With Auto Detect**
- **Accepts 16-, 20-, and 24-Bit Audio Data**
- **Data Formats: Standard, I^2S, and Left-Justified**
- **Digital De-Emphasis**
- **Soft Mute**
- **Zero Flags for Each Output**
- **Dual Supply Operation:**
  - **5 V for Analog**
  - **3.3 V for Digital**
- **5-V Tolerant Digital Inputs**
- **Small 28-Lead SSOP Package**

APPLICATIONS

- **A/V Receivers**
- **DVD Movie Players**
- **SACD Player**
- **HDTV Receivers**
- **Car Audio Systems**
- **Digital Multi-Track Recorders**
- **Other Applications Requiring 24-Bit Audio**

DESCRIPTION

The PCM1730 is a CMOS, monolithic integrated circuit that includes stereo digital-to-analog converters and support circuitry in a small 28-lead SSOP package. The data converters utilize Texas Instruments' advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1730 provides balanced current outputs, allowing the user to optimize analog performance externally. Sampling rates up to 200 kHz are supported.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	OPERATING TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER†
PCM1730E	28-Lead SSOP	28DB	–25°C to 85°C	PCM1730E	PCM1730E
					PCM1730E/2K

† Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of PCM1730E/2K will get a single 2000-piece tape and reel.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

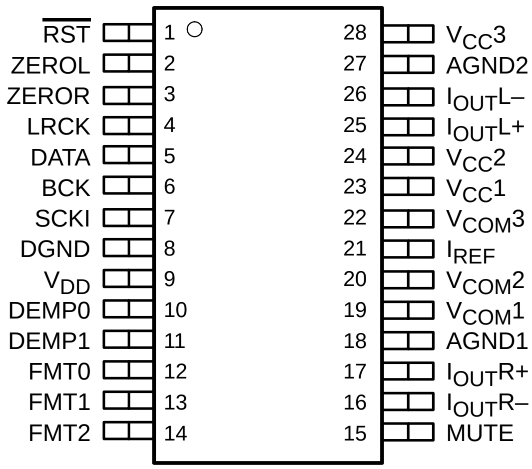
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

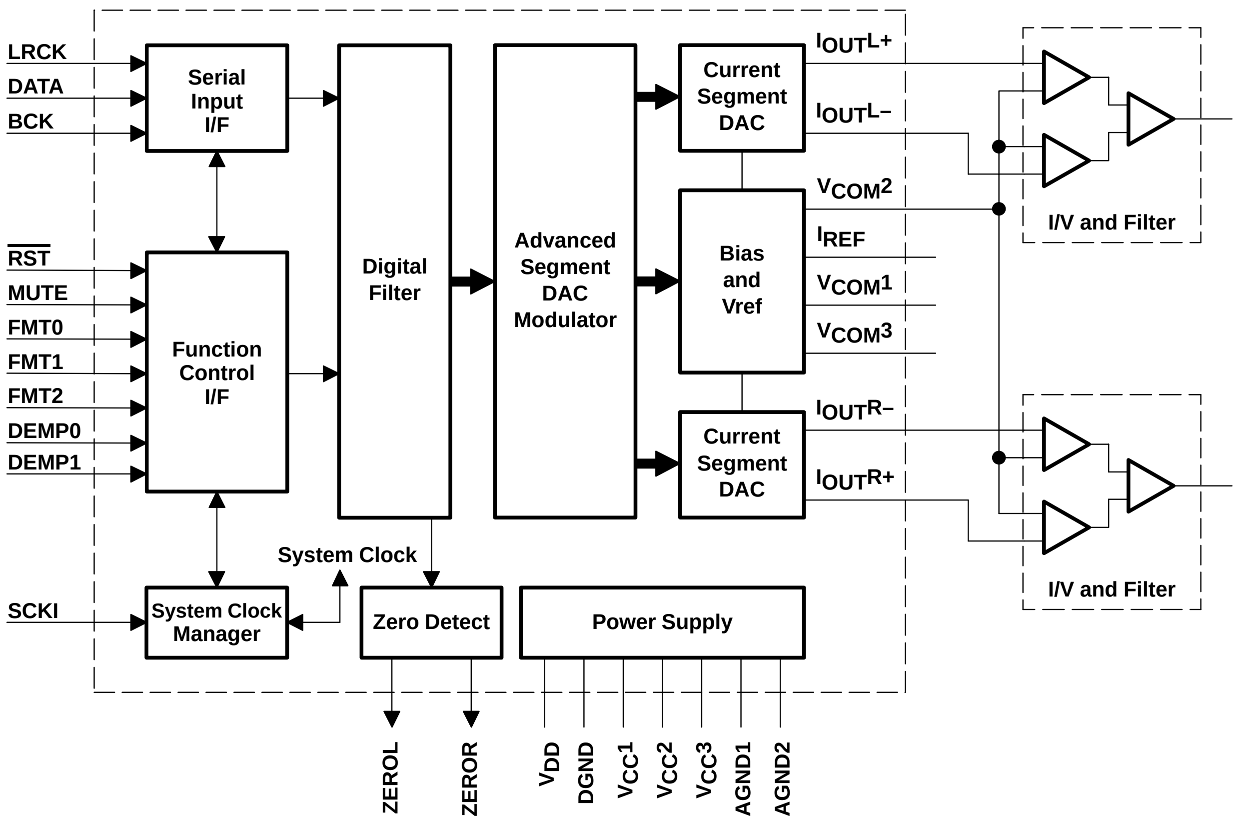
Texas Instruments

pin assignments

SSOP PACKAGE
(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL NAME	PIN	I/O	DESCRIPTION
AGND1	18	–	Analog ground
AGND2	27	–	Analog ground
BCK	6	I	Bit clock input†
DATA	5	I	Serial audio data input†
DEMP0	10	I	De-emphasis control‡
DEMP1	11	I	De-emphasis control‡
DGND	8	–	Digital ground
FMT0	12	I	Audio data format select†
FMT1	13	I	Audio data format select†
FMT2	14	I	Audio data format select†
$I_{OUT}L–$	26	O	L-channel analog current output –
$I_{OUT}L+$	25	O	L-channel analog current output +
$I_{OUT}R–$	16	O	R-channel analog current output –
$I_{OUT}R+$	17	O	R-channel analog current output +
I_{REF}	21	–	Output current reference bias pin. Connect a 16-kΩ resistor to GND.
LRCK	4	I	Left and right clock (f_S)†
MUTE	15	I	Analog output mute control†
$\overline{RST}$	1	I	Reset†
SCKI	7	I	System clock input†
$V_{CC}1$	23	–	Analog supply, 5 V
$V_{CC}2$	24	–	Analog supply, 5 V
$V_{CC}3$	28	–	Analog power supply, 5 V
$V_{COM}1$	19	–	Internal bias decoupling pin
$V_{COM}2$	20	–	Common voltage for I/V
$V_{COM}3$	22	–	Internal bias decoupling pin
V_{DD}	9	–	Digital supply, 3.3 V
ZEROL	2	O	Zero flag for L-channel
ZEROR	3	O	Zero flag for R-channel

† Schmitt-trigger input, 5-V tolerant
‡ Schmitt-trigger input with internal pulldown, 5-V tolerant

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: $V_{CC}1$, $V_{CC}2$, $V_{CC}3$ . . . . 6.5 V
Supply voltage: V_{DD} . . . . 4 V
Supply voltage differences: $V_{CC}1$, $V_{CC}2$, and $V_{CC}3$ . . . . ±0.1 V
Ground voltage differences: AGND1, AGND2, and DGND . . . . ±0.1 V
Digital input voltage: LRCK, DATA, BCK, SCKI, DEMP0, DEMP1, FMT0, FMT1,
FMT2, $\overline{RST}$, and MUTE . . . . –0.3 V to 6.5 V
Digital input voltage: ZEROL, ZEROR . . . . –0.3 V to (V_{DD} + 0.3 V)
Analog input voltage: . . . . –0.3 V to (V_{CC} + 0.3 V)
Input current (any pins except supplies) . . . . ±10 mA
Ambient temperature under bias, T_A . . . . –40°C to 125°C
Storage temperature, T_{stg} . . . . –55°C to 150°C
Junction temperature, T_J . . . . 150°C
Lead temperature (soldering) . . . . 260°C, 5 s
Package temperature (IR reflow, peak) . . . . 235°C, 10 s

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 256 f_S and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM1730E			UNIT
			MIN	TYP	MAX	
RESOLUTION				24		Bits
DATA FORMAT						
	Audio data interface format		Standard, I^2S, left justified			
	Audio data bit length		16, 20, 24-bits selectable			
	Audio data format		MSB first, 2’s complement			
f_S	Sampling frequency		10		200	kHz
	System clock frequency		128, 192, 256, 384, 512, 768 f_S			
DIGITAL INPUT/OUTPUT						
	Logic family		TTL compatible			
V_{IH}	High-level input logic level		2			VDC
V_{IL}	Low-level input logic level				0.8	VDC
I_{IH}	Input logic current (see Note 1)	$V_{IN} = V_{DD}$			10	µA
I_{IL}	Input logic current (see Note 1)	V_{IN} = 0 V			–10	µA
I_{IH}	Input logic current (see Note 2)	$V_{IN} = V_{DD}$		65	100	µA
I_{IL}	Input logic current (see Note 2)	V_{IN} = 0 V			–10	µA
V_{OH}	High-level output logic level	I_{OH} = –2 mA	2.4			VDC
V_{OL}	Low-level output logic level	I_{OL} = 2 mA			1	VDC

NOTES: 1. Pins 1, 4, 5, 6, 7, 12, 13, 14, and 15: $\overline{RST}$, LRCK, DATA, BCK, SCKI, FMT0, FMT1, FMT2, and MUTE
2. Pins 10 and 11: DEMP0, DEMP1

electrical characteristics, all specifications at $T_A = 25°C$, $V_{CC} = 5$ V, $V_{DD} = 3.3$ V, $f_S = 44.1$ kHz, system clock = 256 f_S and 24-bit data (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		PCM1730E MIN	PCM1730E TYP	PCM1730E MAX	UNIT
DYNAMIC PERFORMANCE (see Note 3)							
THD+N	Total harmonic distortion plus noise	V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0004%	0.008%	
			f_S = 96 kHz		0.0006%		
			f_S = 192 kHz		0.0012%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz		114	117		dB
		EIAJ, A-weighted, f_S = 96 kHz			117		dB
		EIAJ, A-weighted, f_S = 192 kHz					
	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz		114	117		dB
		EIAJ, A-weighted, f_S = 96 kHz			117		dB
		EIAJ, A-weighted, f_S = 192 kHz					
	Channel separation	f_S = 44.1 kHz		110	115		dB
		f_S = 96 kHz			113		dB
		f_S = 192 kHz			111		dB
	Level linearity error	V_{OUT} = –110 dB			±1		dB
DC ACCURACY							
	$V_{COM}2$ voltage				2.45		V
	$V_{COM}2$ output current	Delta $V_{COM}2$ < 5%			100		µA
	Gain error				±2		%/FSR
	Gain mismatch, channel-to-channel				±0.5		%/FSR
	Bipolar zero error	At BPZ			±0.5		%/FSR
ANALOG OUTPUT							
	Output current	Full scale (–0 dB)			±2.48		mA_{p-p}
	Center current	BPZ input			0		mA_{p-p}
DIGITAL FILTER PERFORMANCE—FILTER CHARACTERISTICS							
	Pass band	±0.002 dB				0.454 f_S	
		–3 dB				0.49 f_S	
	Stop band			0.546 f_S			
	Pass-band ripple			–75		±0.002	dB
	Stop-band attenuation	Stop band = 0.546 f_S					dB
		Stop band = 0.567 f_S		–82			dB
	Delay time				29/f_S		s
	De-emphasis error					±0.1	dB

NOTE 3: Analog performance specifications are measured by audio precision II under averaging mode. At 44.1-kHz operation, measurement bandwidth is limited to 20 kHz. At 96-kHz and 192-kHz operation, measurement bandwidth is limited to 40 kHz.

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 256 f_S and 24-bit data (unless otherwise noted)(continued)

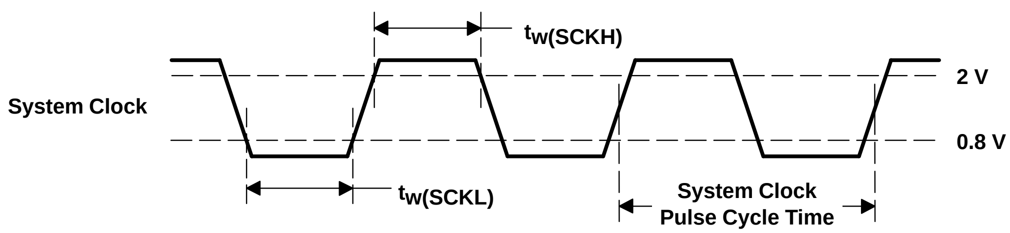
PARAMETER		TEST CONDITIONS	PCM1730E MIN	PCM1730E TYP	PCM1730E MAX	UNIT
POWER SUPPLY REQUIREMENTS						
V_{DD}	Voltage range		3	3.3	3.6	VDC
V_{CC}			4.75	5	5.25	
I_{DD}	Supply current	f_S = 44.1 kHz		7	9.8	mA
		f_S = 96 kHz		15		
		f_S = 192 kHz		30		
I_{CC}		f_S = 44.1 kHz		33	46.2	
		f_S = 96 kHz		34.5		
		f_S = 192 kHz		36.5		
P_D	Power dissipation	f_S = 44.1 kHz		188	263	mW
		f_S = 96 kHz		222		
		f_S = 192 kHz		282		
TEMPERATURE RANGE						
	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance	28-pin SSOP		100		°C/W

functional description

system clock and reset functions

The PCM1730 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCKI input (pin 7). The PCM1730 has a system clock detection circuit, which automatically senses if the system clock is operating at 128 f_S to 768 f_S. Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 1 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. Texas Instruments' PLL1700 multi-clock generator is an excellent choice for providing the PCM1730 system clock.



PARAMETER	MIN	UNIT
System clock pulse width high, $t_{w(SCKH)}$	5	ns
System clock pulse width high, $t_{w(SCKL)}$	5	ns

Figure 1. System Clock Input Timing

system clock and reset functions (continued)

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)					
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1 kHz	5.6488	8.4672	11.2896	16.9344	22.5792	33.8688
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864
96 kHz	12.288	18.432	24.576	36.864	49.152	73.728
192 kHz	24.576	36.864	49.152	73.728	See Note 4	See Note 4

NOTE 4: This system clock rate is not supported for the given sampling frequency.

power-on and external reset functions

The PCM1730 includes a power-on reset function. Figure 2 shows the operation of this function. The system clock input at SCKI should be active for at least one clock period prior to V_{DD} = 2 V. With the system clock active and V_{DD} > 2 V, the power-on reset function will be enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2 V. The PCM1730 also includes an external reset capability using the $\overline{RST}$ input (pin 1). This allows an external controller or master reset circuit to force the PCM1730 to initialize to its reset state. Figure 3 shows the external reset operation and timing. The $\overline{RST}$ pin is set to logic 0 for a minimum of 20 ns. The $\overline{RST}$ pin is then set to a logic 1 state, which starts the initialization sequence, which requires 1024 system clock periods. The external reset is especially useful in applications where there is a delay between PCM1730 power up and system clock activation. In this case, the $\overline{RST}$ pin should be held at a logic 0 level until the system clock has been activated. The $\overline{RST}$ pin may then be set to logic 1 state to start the initialization sequence.

functional description (continued)

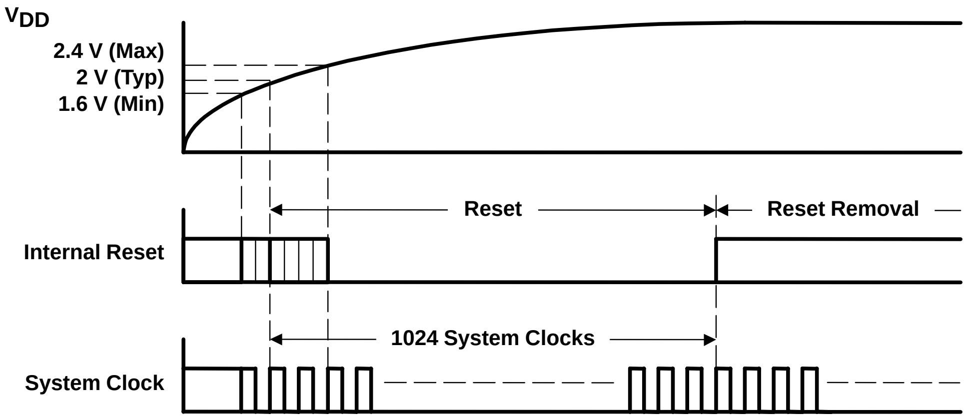
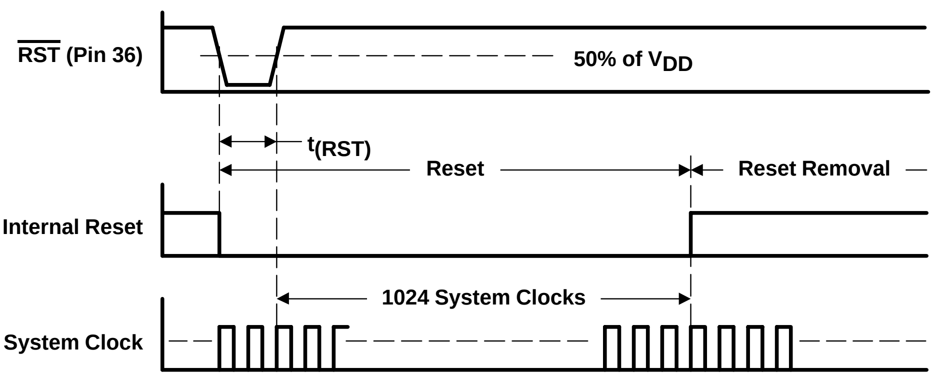


Figure 2. Power-On Reset Timing



PARAMETER	MIN	UNIT
Reset pulse width low, $t_{(RST)}$	20	ns

Figure 3. External Reset Timing

audio data interface

audio serial interface

The audio serial interface for the PCM1730 is comprised of a 3-wire synchronous serial port. It includes LRCK (pin 4), BCK (pin 6), and DATA (pin 5). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the audio interface's serial shift register. Serial data is clocked into the PCM1730 on the rising edge of BCK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the serial audio interface's internal registers.

LRCK should be synchronous with the system clock. In the event these clocks are not synchronized, the PCM1730 can compensate for the phase difference internally. If the phase difference between LRCK and SCKI is greater than 6-bit clocks (BCK), the synchronization is performed internally. While the synchronization is processing, the analog output is forced to bipolar zero level. The synchronization typically occurs in less than one cycle of LRCK.

Ideally, it is recommended that LRCK and BCK be derived from the system clock input or output, SCKI or SCKO. The left/right clock, LRCK, is operated at the sampling frequency, f_S.

audio data formats and timing

The PCM1730 supports industry-standard audio data formats, including standard right-justified, I^2S, and left-justified. The data formats are shown in Figure 4. Data formats are selected by using the FMT2 (pin 14), FMT1 (pin 13) and FMT0 (pin 12) as shown in Table 2. All formats require binary 2's complement, MSB-first audio data. Figure 5 shows a detailed timing diagram for the serial audio interface.

Table 2. Audio Data Format Select

FMT2 (PIN 14)	FMT1 (PIN 13)	FMT0 (PIN 12)	FORMAT
Low	Low	Low	16-bit standard format, right-justified
Low	Low	High	20-bit standard format, right-justified
Low	High	Low	24-bit standard format, right-justified
Low	High	High	24-bit MSB-first, left-justified format
High	Low	Low	16-bit I^2S format
High	Low	High	24-bit I^2S format
High	High	Low	Reserved
High	High	High	Reserved

zero detect

When the PCM1730 detects that the audio input data in L-channel or R-channel is continuously zero for 1024 f_S, the PCM1730 sets ZEROL (pin 2) or ZEROR (pin 3) to high.

soft mute

The PCM1730 supports mute operation. When MUTE (pin 15) is set to HIGH, both analog outputs are turned to bipolar zero levels by –0.5-dB steps with transition speed of $1/f_S$ per step. This system provides pop-free muting of DAC output.

de-emphasis

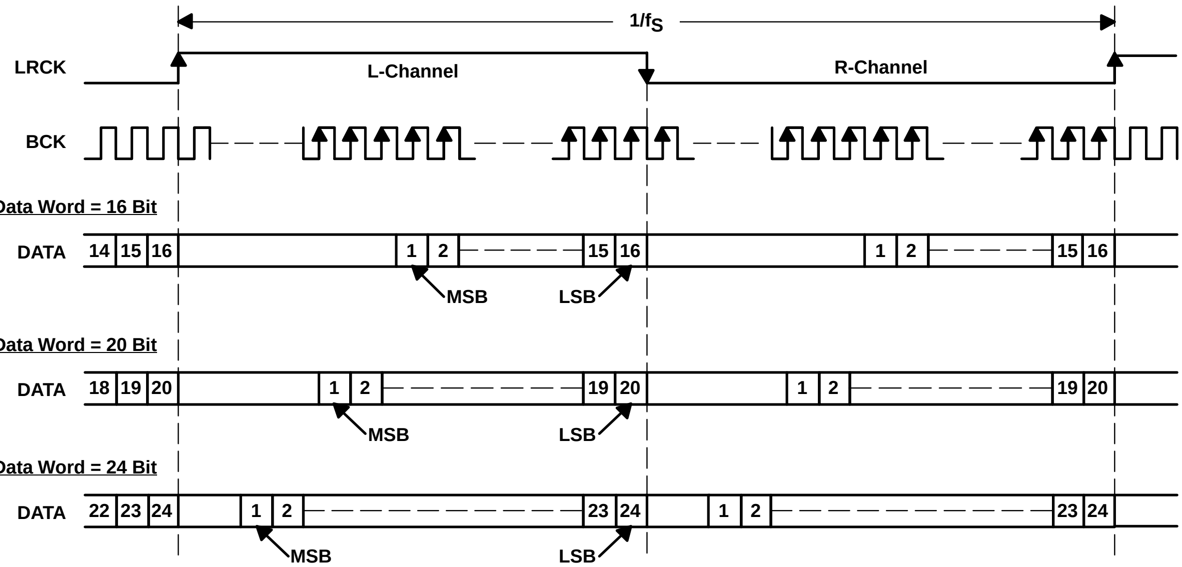
The PCM1730 supports de-emphasis filter performance for sampling frequency 32 kHz, 44.1 kHz, 48 kHz. Sampling frequency is selectable by using DEMP1 (pin 11) DEMP0 (pin 10) as shown in Table 3.

Table 3. De-Emphasis Control

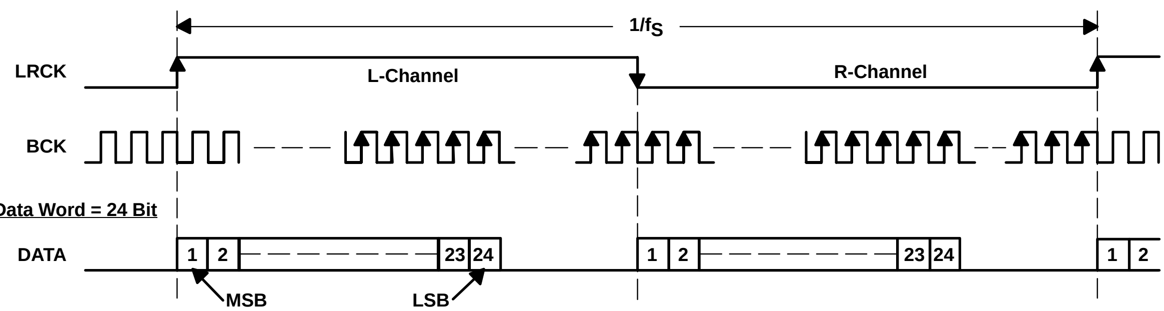
DEMP1 (PIN 11)	DEMP0(PIN 10)	DE-EMPHASIS FUNCTION
Low	Low	Disabled
Low	High	48 kHz
High	Low	44.1 kHz
High	High	32 kHz

functional description (continued)

(1) Standard Data Format (Right Justified); L-channel = High, R-channel = Low



(2) Left Justified Data Format: L-channel = High, R-channel = Low



(3) I²S Data Format: L-channel = Low, R-channel = High

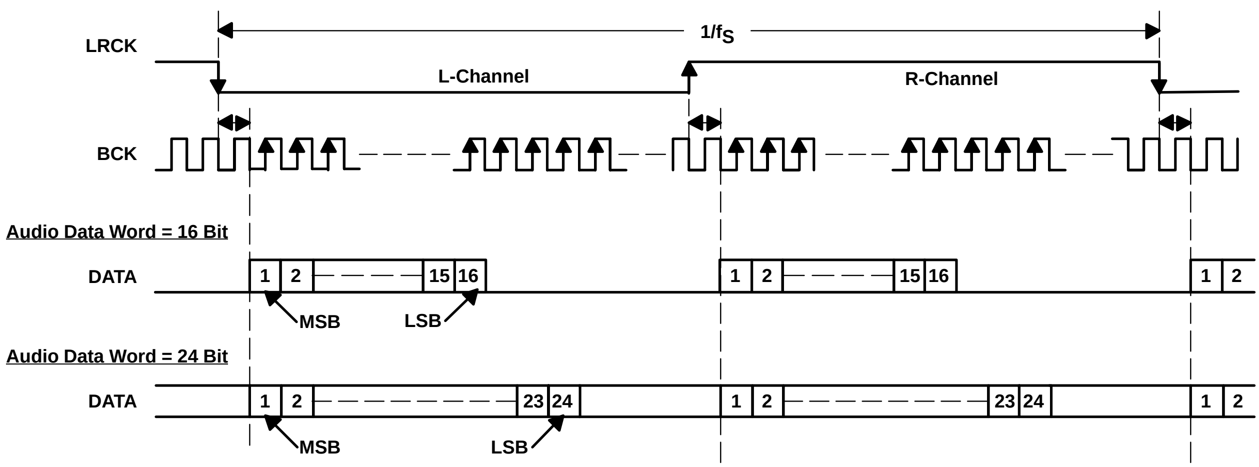
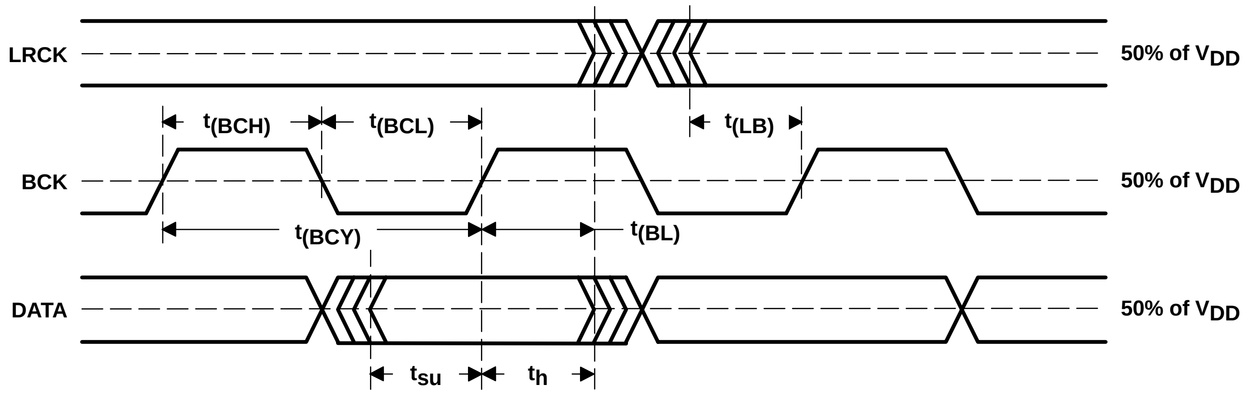


Figure 4. Audio Data Input Formats

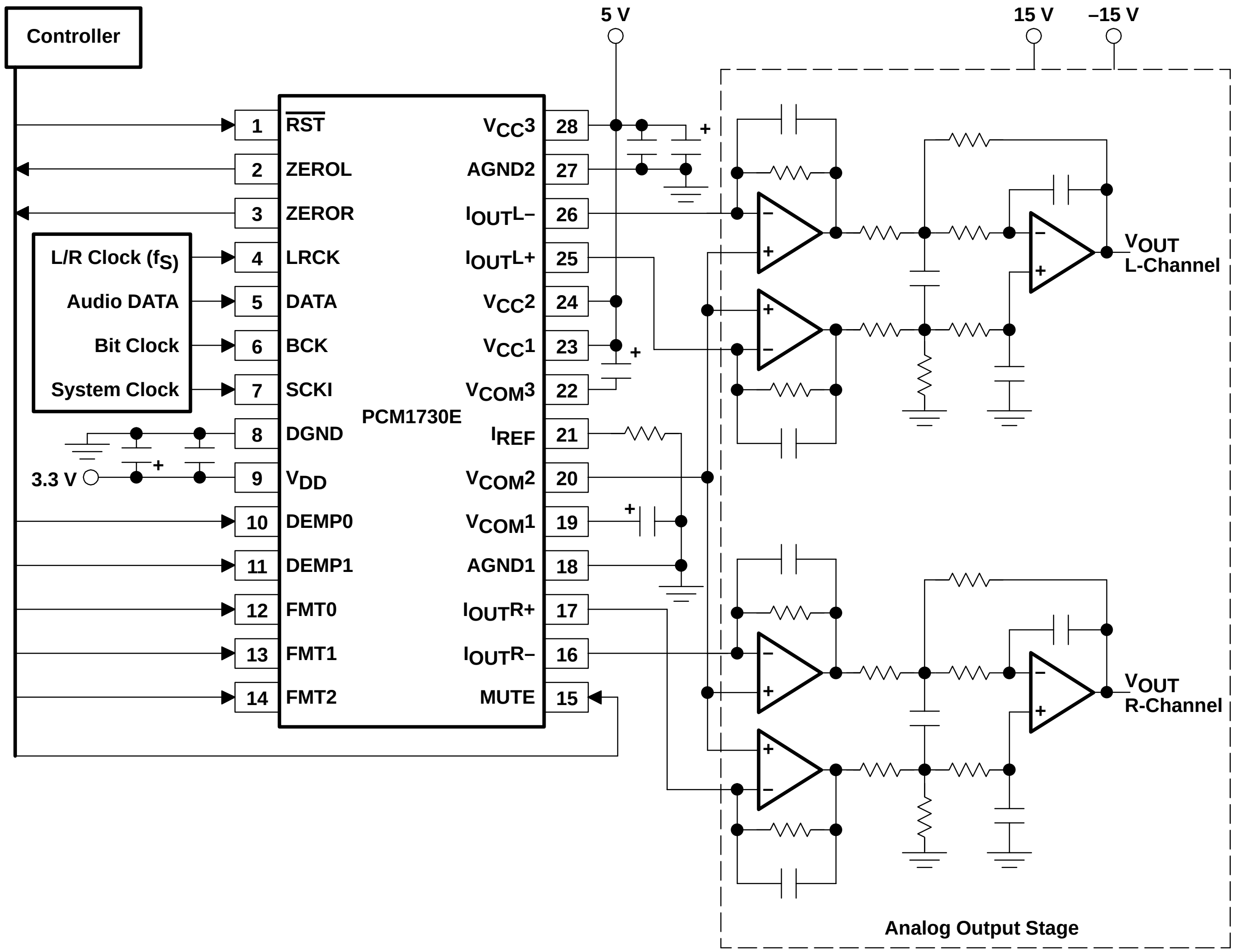
functional description (continued)



PARAMETER	MIN	UNIT
BCK pulse cycle time, $t_{(BCY)}$	70	ns
BCK pulse width low, $t_{w(BCL)}$	30	ns
BCK pulse width high, $t_{w(BCH)}$	30	ns
BCK rising edge to LRCK edge, $t_{(BL)}$	10	ns
LRCK edge to BCK rising edge, $t_{(LB)}$	10	ns
DATA set up time, t_{su}	10	ns
DATA hold time, t_h	10	ns
LRCK clock duty	50% ±2 bit clock	

Figure 5. Audio Interface Timing

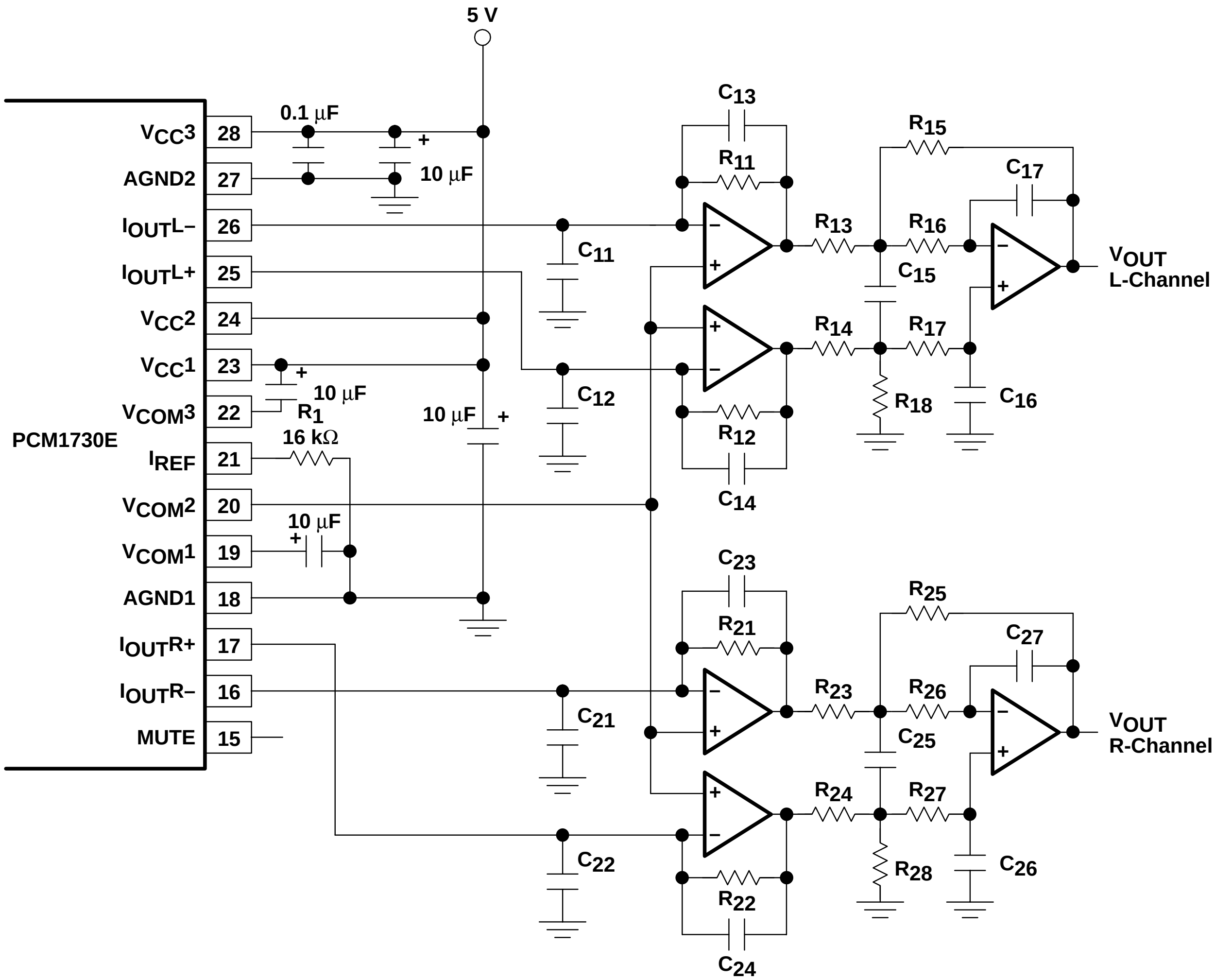
typical connection diagram



NOTE: Regarding R/C values for analog output stage, see Figure 9.

Figure 6. Typical Application Circuit for Standard PCM Audio Operation

analog outputs



NOTE: Example R/C values for f_C 45 kHz
R_{11}–R_{18}, R_{21}–R_{28}: 620 Ω, C_{11}, C_{12}, C_{21}, C_{22}: not populated, C_{13}, C_{14}, C_{23}, C_{24}: 5600 pF, C_{15}, C_{25}: 8200 pF, C_{16}, C_{17}, C_{26}, C_{27}: 1800 pF

Figure 7. Typical Application for Analog Output Stage

analog output level and I/V converter

The signal level of DAC current output pins ($I_{OUT}L+$, $I_{OUT}L–$, $I_{OUT}R+$, $I_{OUT}R–$) is ±2.48 mAp-p at 0 dB (full scale). The voltage output of the I/V converter is given by following equation:

V_{OUT} = ±2.48 mAp–p × R_f

Here, R_f is the feedback resistor in the I/V conversion circuit, R_{11}, R_{12}, R_{21}, R_{22} on typical application circuit. The common level of the I/V conversion circuit must be same as common level of DAC I_{OUT} which is given by $V_{COM}2$ reference voltage, which is 2.48 V dc typically. The noninverting inputs of the op amps shown in the I/V circuits are connected to $V_{COM}2$ to provide the common bias voltage.

op amp for I/V converter circuit

OPA627BP/BM or NE5534 type op amp is recommended for I/V conversion circuit to obtain specified audio performance. Dynamic performance such as gain bandwidth, settling time and slew rate of op amp gives audio dynamic performance at I/V section. Input noise specification of op amp should be considered to obtain 120 dB S/N ratio.

analog gain by balanced amp

The I/V converters are followed by balanced amplifier stages, which sum the differential signals for each channel, creating a single-ended voltage output. In addition, the balanced amplifiers provide a second-order low pass filter function, which band limits the audio output signal. The cutoff frequency and gain are given by the external R and C component values. In this case, the cutoff frequency is 45 kHz with a gain of 1. The output voltage for each channel is 6.2 Vp-p, or 2.2 Vrms.

reference current resistor

As shown in the analog output application circuit, there is a resistor connected from I_{REF} (pin 21) to analog ground, designated as R_1. This resistor sets the current for the internal reference circuit. The value of R_1 must be 16 kΩ ±1% in order to match the specified gain error shown in the specifications table.

theory of operation

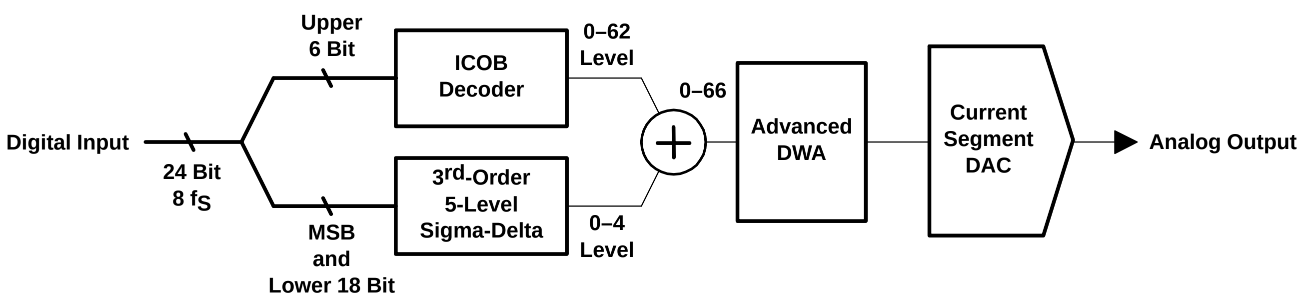


Figure 8. Advanced Segments DAC

The PCM1730 utilizes Texas Instruments' newly developed advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1730 provides balanced current outputs, allowing the user to optimize analog performance externally.

Digital input data via digital filter separates into the upper 6 bits and lower the 18 bits. The upper 6 bits are converted to ICOB (inverted complementary offset binary) code. The lower 18 bits associated with the MSB are processed by five level third order delta-sigma modulator operated at 64 f_S. The one level of the modulator is equivalent to the 1 LSB of the above code converter. The data groups processed in the ICOB converter and third order delta-sigma modulator are summed together to be created over the 64 level digital code, and then processed in DWA (data weighted averaging) to reduce noise produced by element mismatch. The data of over 64 level via DWA is converted to analog output in the differential current segment portion.

This architecture has overcome the various drawbacks of conventional multi-bit and also achieves excellent dynamic performance.

considerations for application circuit

PCB layout guidelines

A typical PCB floor plan for the PCM1730 is shown in Figure 9. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1730 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

PCB layout guidelines (continued)

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the D/A converters. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 10 shows the recommended approach for single-supply applications.

bypass and decoupling capacitor requirements

Various-sized decoupling capacitors can be used, with no special tolerances being required. All capacitors should be located as close to the appropriate pins of the PCM1730 as possible to reduce noise pickup from surrounding circuitry. Aluminum electrolytic capacitors that are designed for hi-fi audio applications are recommended for larger values, while metal-film or monolithic ceramic capacitors are used for smaller values.

I/V section

I/V conversion circuit by op amp IC and feedback resistor should achieve excellent performance of the PCM1730. To obtain 0.0004% THD+N, 117-dB signal-to-noise ratio audio performance, THD+N and input noise performance by the op amp IC should be considered, especially if the input noise of the op amp directly gives output noise level of the application. The I_{OUT}– pin on the PCM1730 and the inverted input on the I/V amp should be connected as short distance.

post LPF design

Out-band noise level and attenuated sampling spectrum level are much lower than typical delta-sigma type DAC due to the combination of a high-performance digital filter and advanced segment DAC architecture. Second-order or third-order post LPF is recommended as post LPF of the PCM1730. Cutoff frequency of post LPF is depends on applications to that there are many sampling rate operation such as f_S = 44.1 kHz on CDDA, f_S = 96 kHz on DVD–M, f_S = 192 kHz on DVD–A.

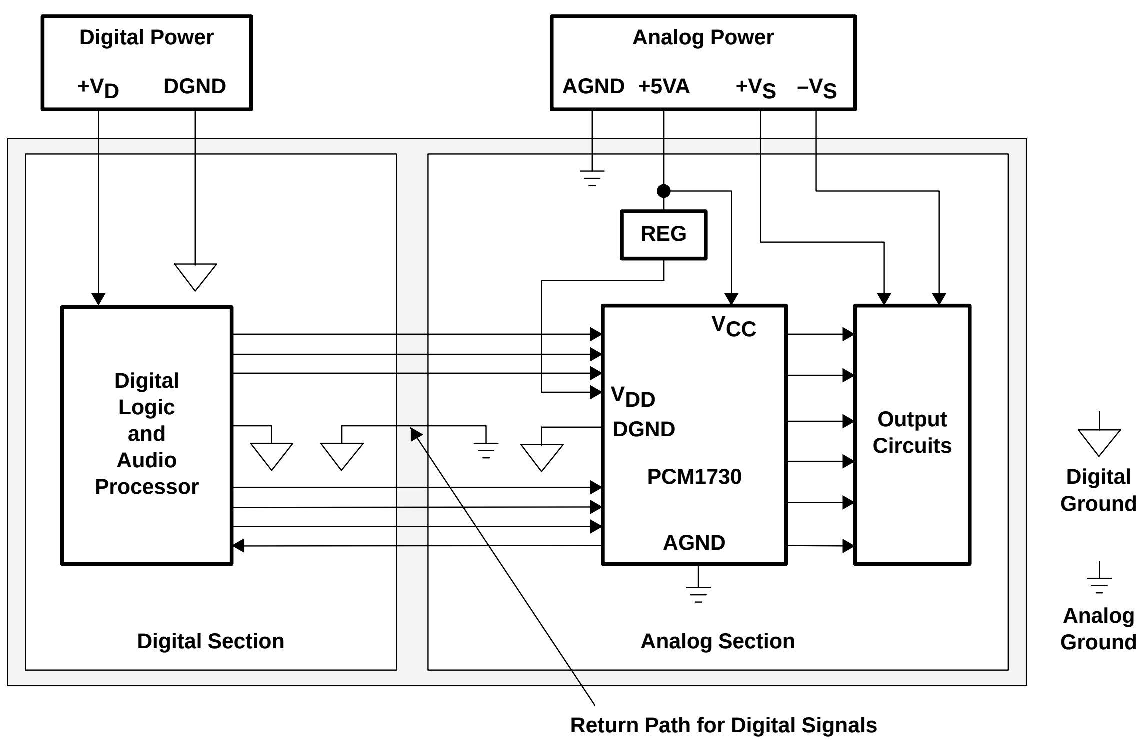


Figure 9. Recommended PCB Layout

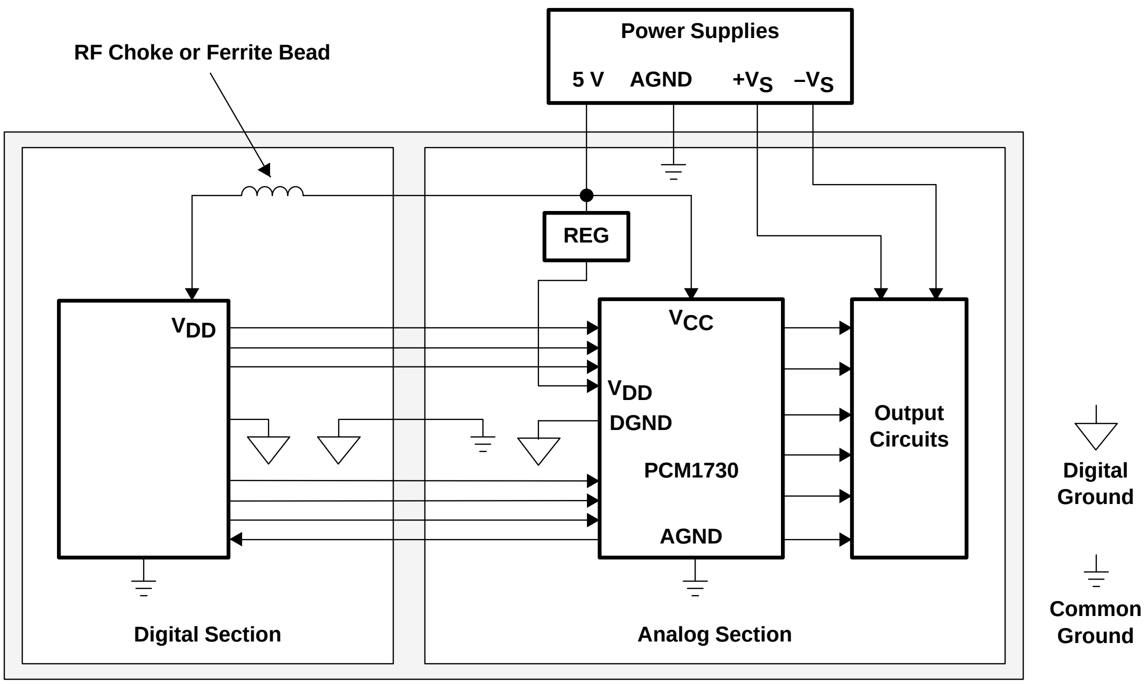


Figure 10. Single-Supply PCB Layout

TYPICAL CHARACTERISTICS

digital filter

de-emphasis off

AMPLITUDE
vs
FREQUENCY

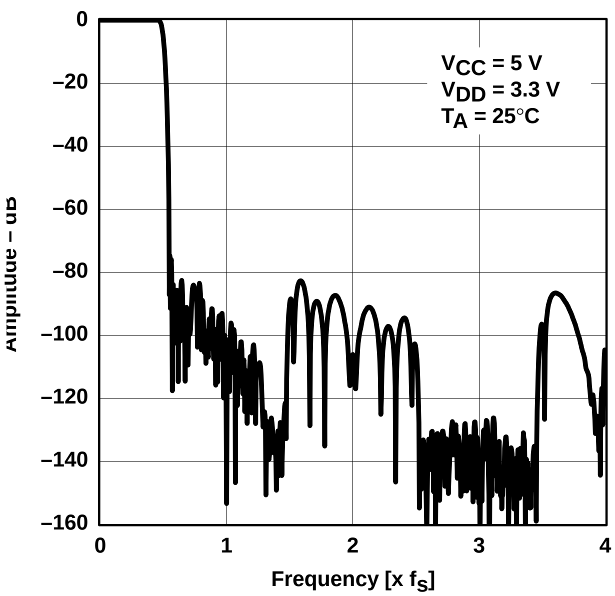


Figure 11

AMPLITUDE
vs
FREQUENCY

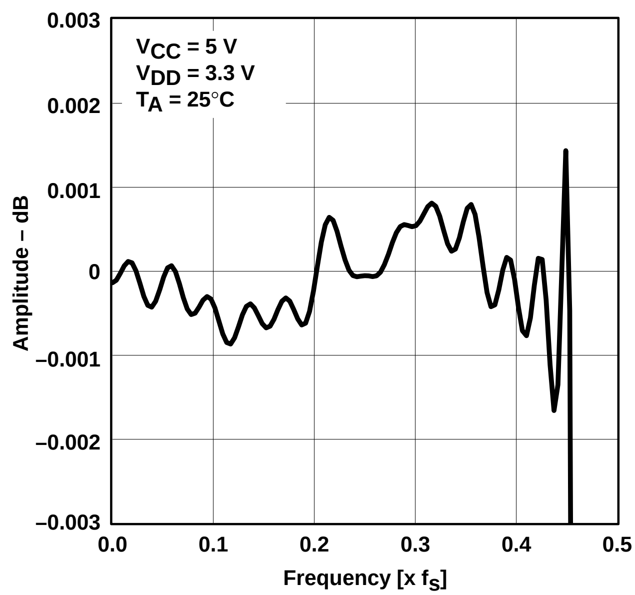


Figure 12

† All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted)

TYPICAL CHARACTERISTICS

de-emphasis error

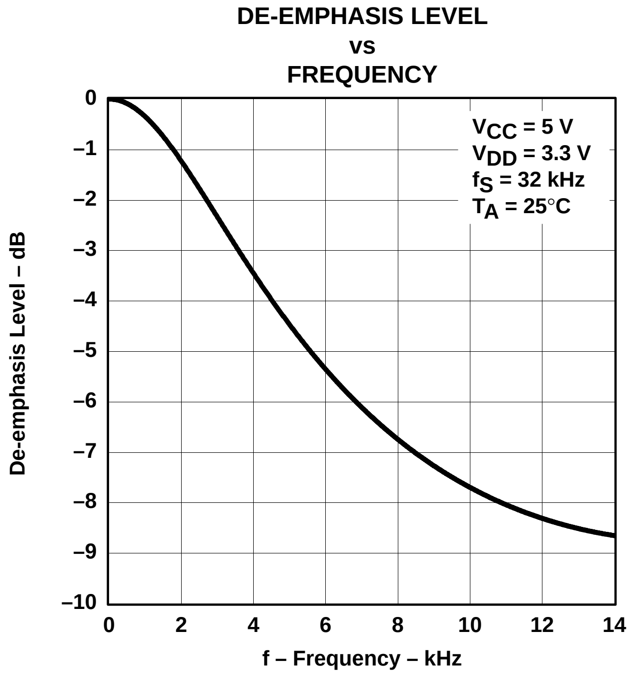


Figure 13

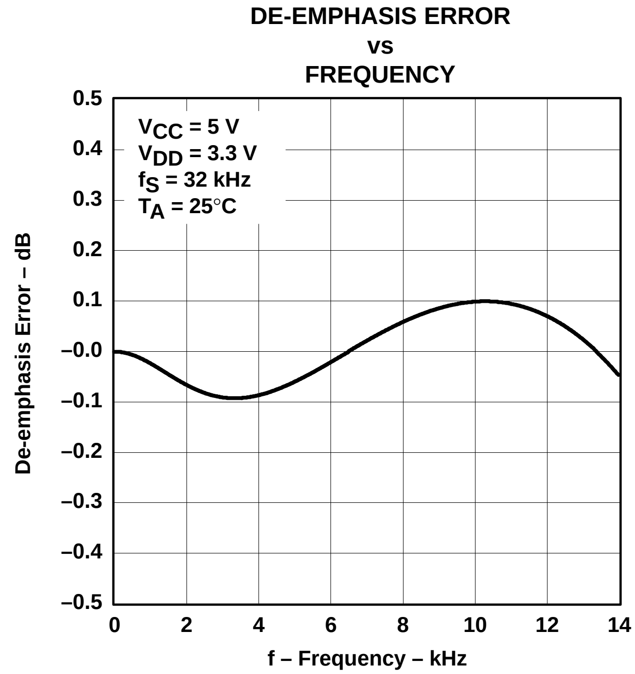


Figure 14

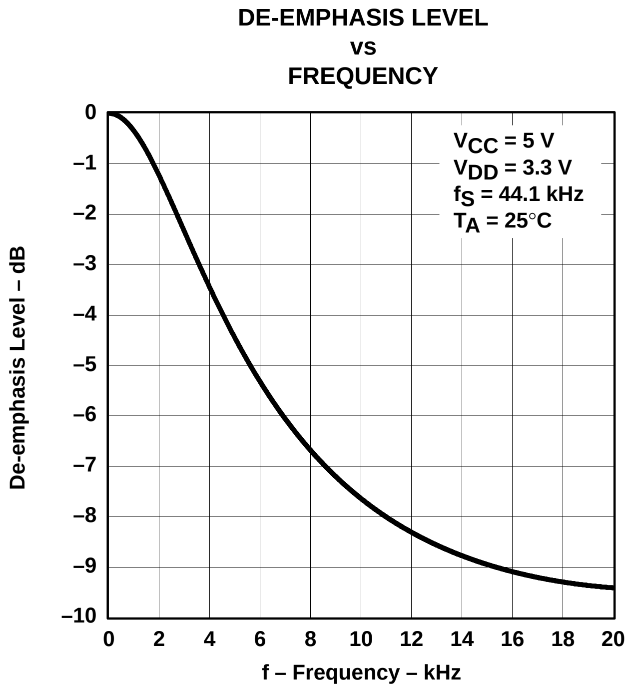


Figure 15

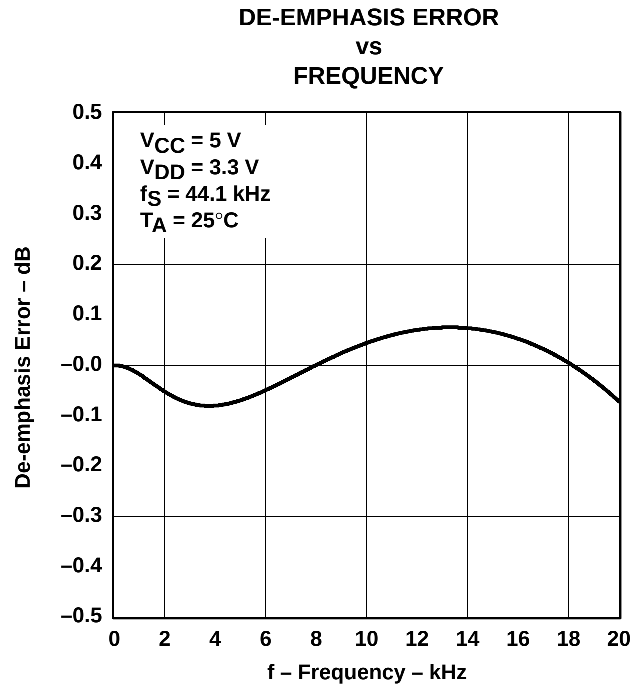


Figure 16

† All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted)

TYPICAL CHARACTERISTICS

de-emphasis error (continued)

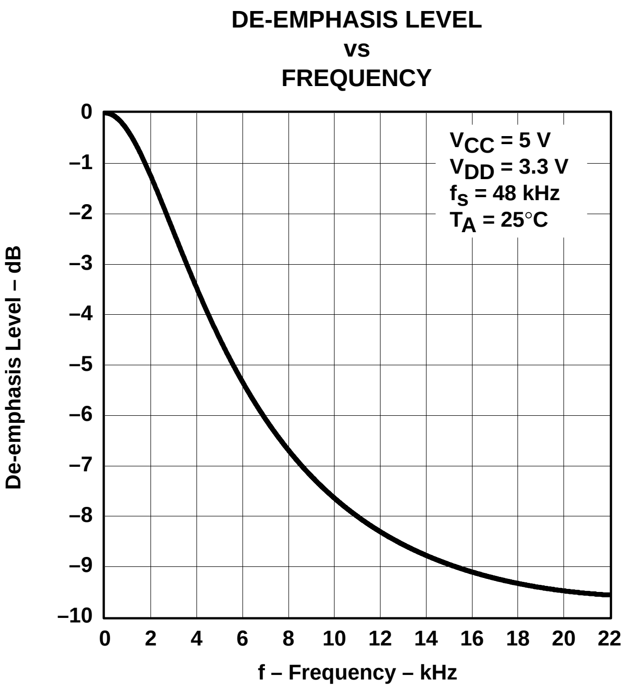


Figure 17

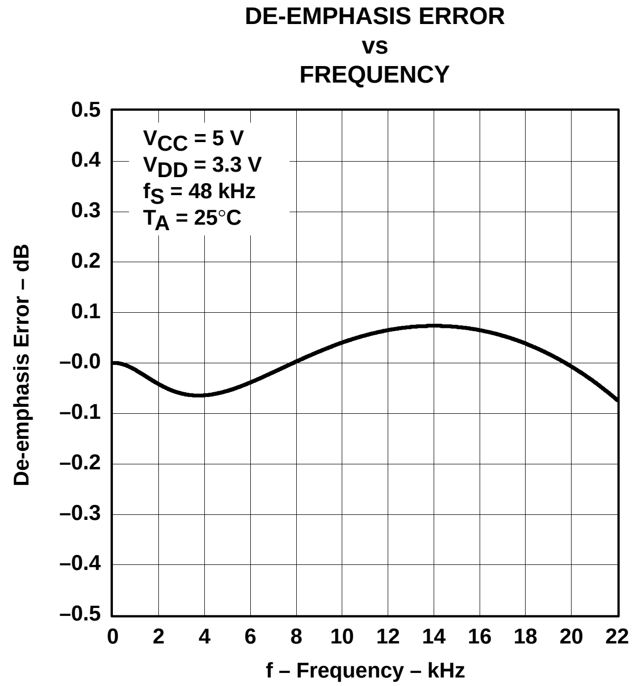


Figure 18

analog dynamic performance

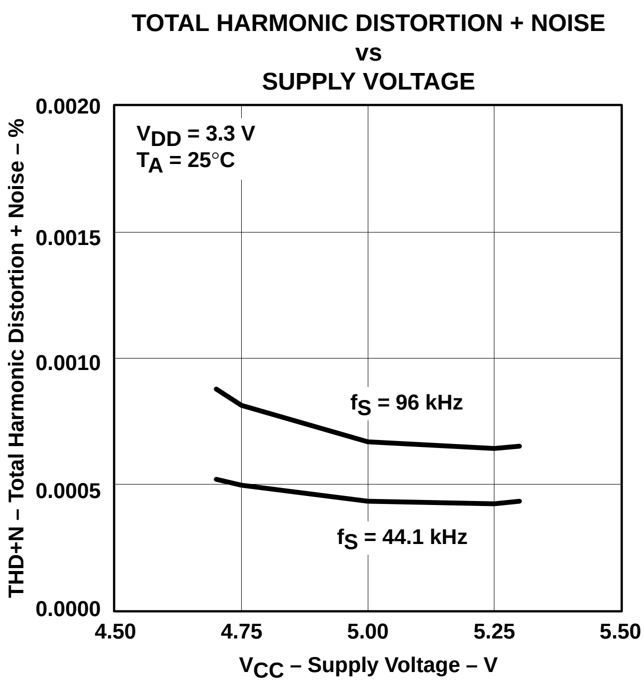


Figure 19

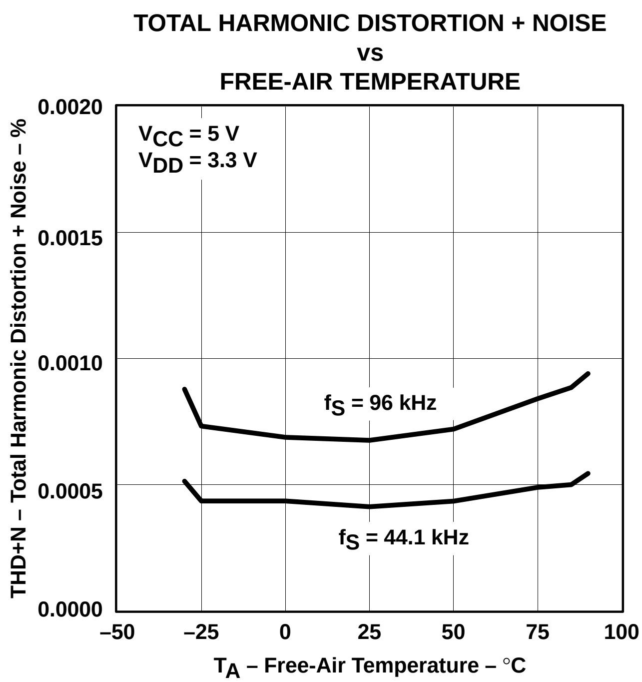


Figure 20

† All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted)

TYPICAL CHARACTERISTICS

analog dynamic performance (continued)

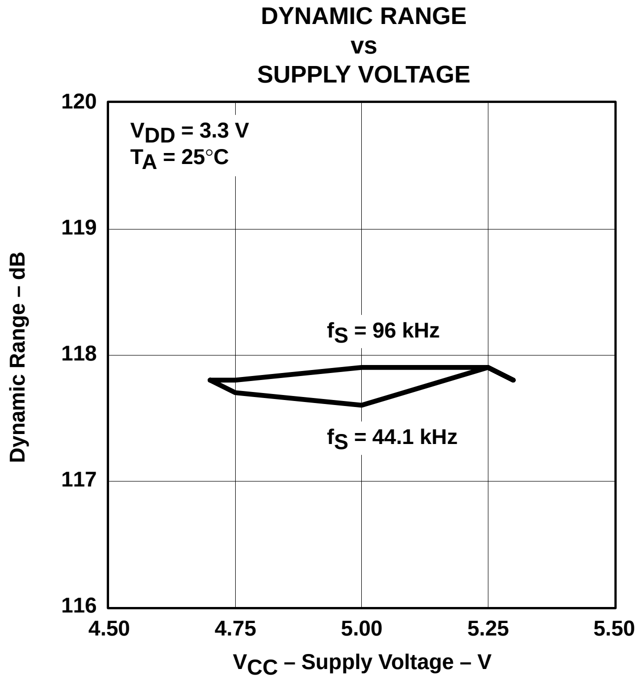


Figure 21

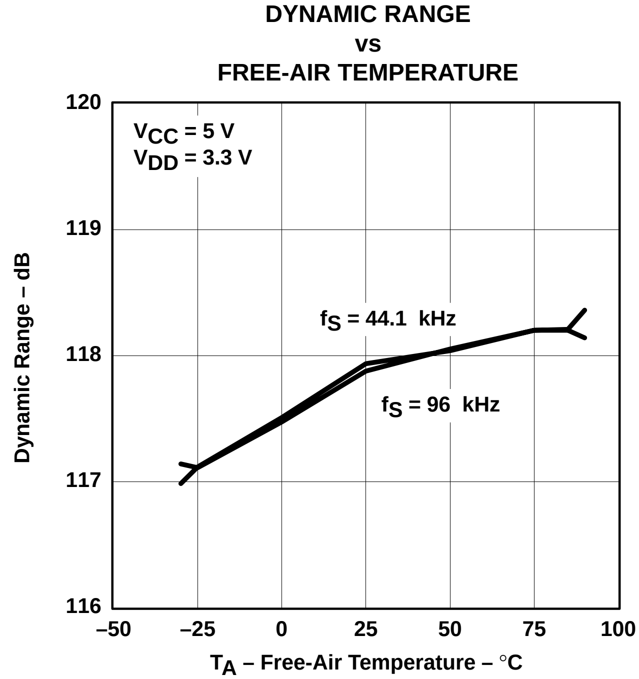


Figure 22

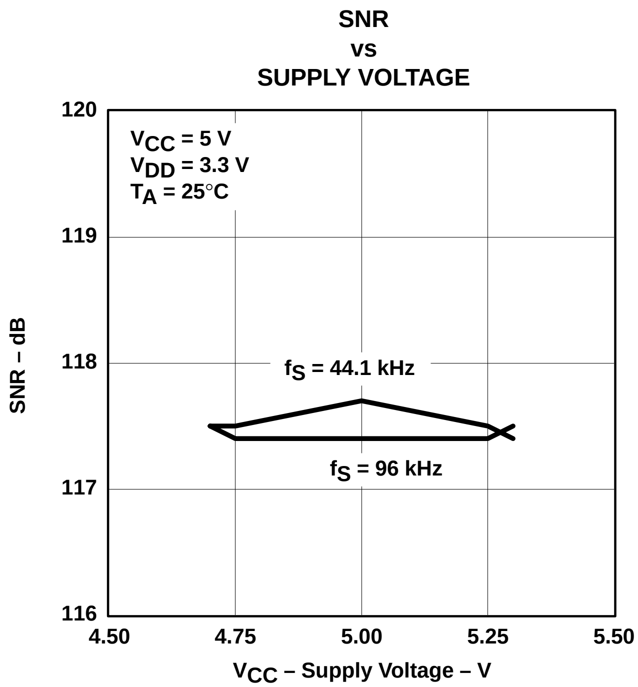


Figure 23

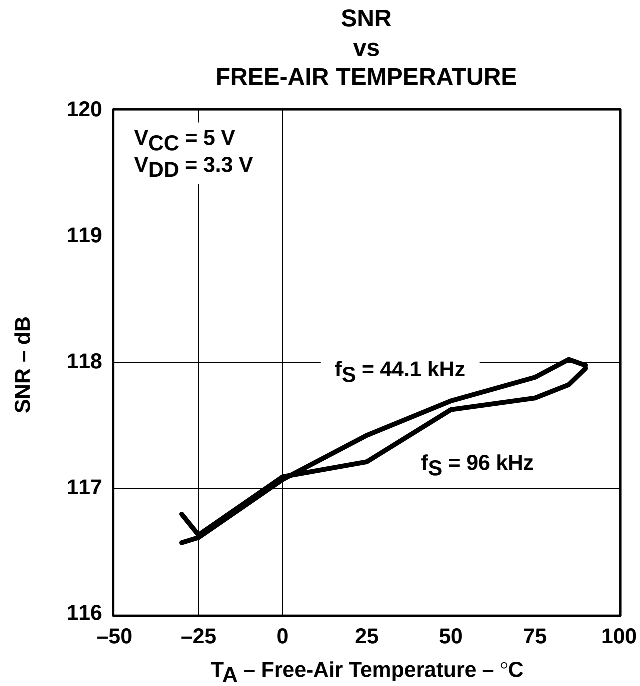


Figure 24

† All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted)

TYPICAL CHARACTERISTICS

analog dynamic performance (continued)

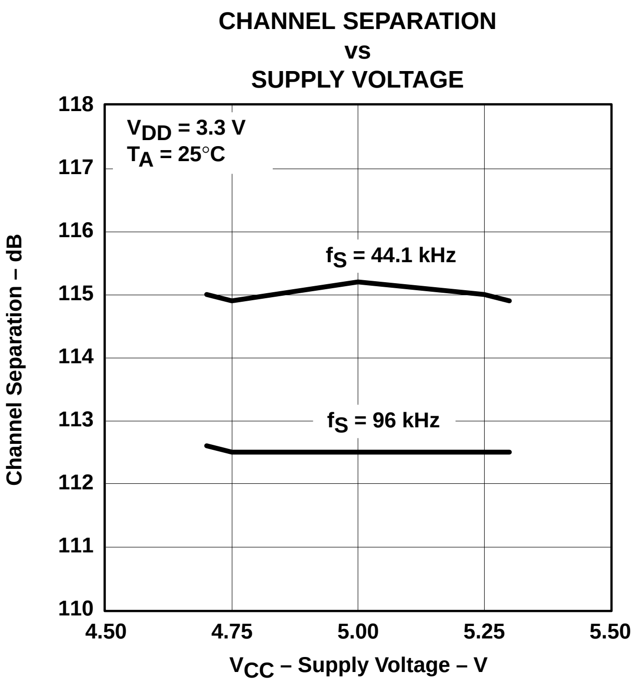


Figure 25

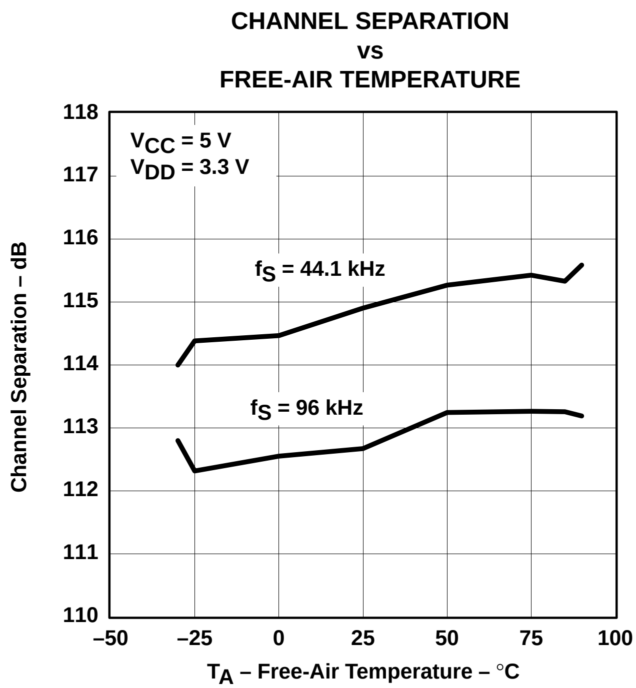


Figure 26

† All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted)

TYPICAL CHARACTERISTICS

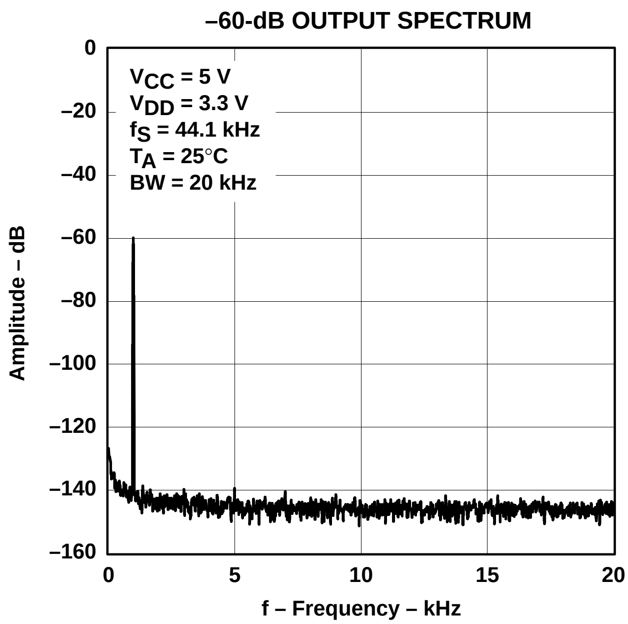


Figure 27

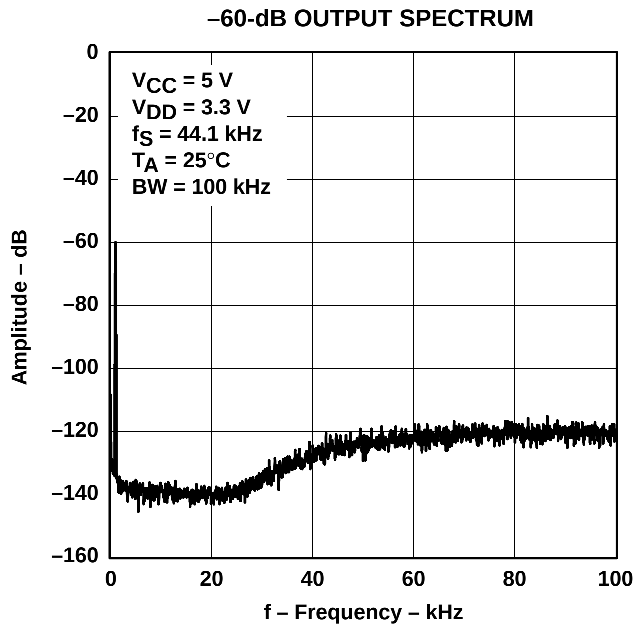


Figure 28

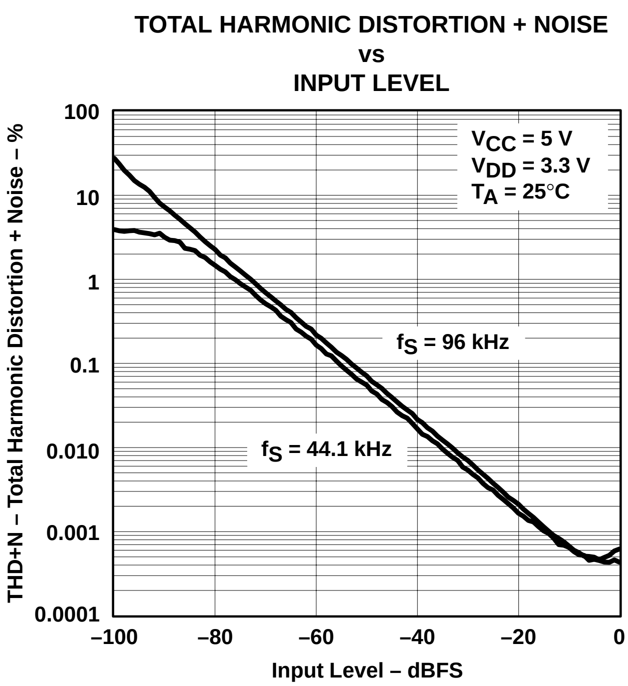


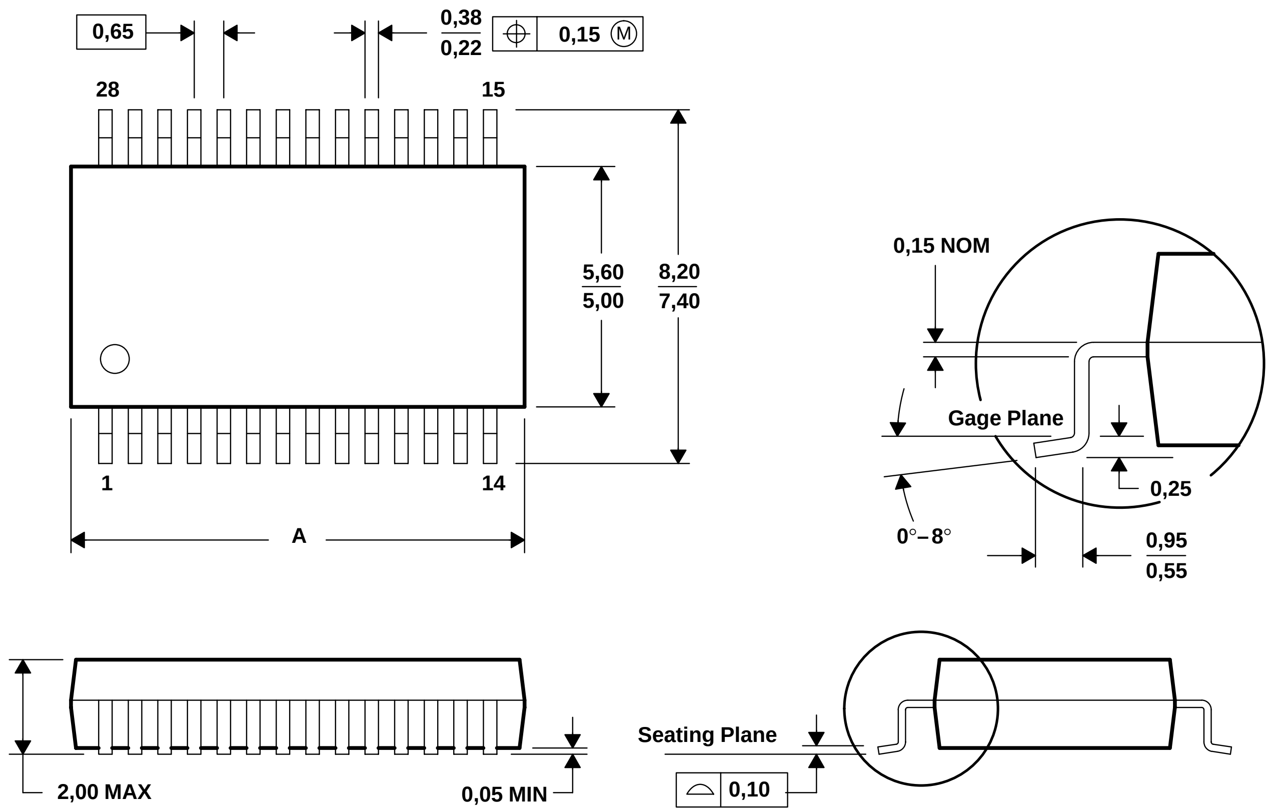
Figure 29

† All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted)

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /D 09/00

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15 mm.
- D. Falls within JEDEC MO-150

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