M41T0

SERIAL REAL-TIME CLOCK

FEATURES SUMMARY

- 2.0 TO 5.5V CLOCK OPERATING VOLTAGE
- COUNTERS FOR SECONDS, MINUTES, HOURS, DAY, DATE, MONTH, YEARS, and CENTURY
- YEAR 2000 COMPLIANT
- I^2C BUS COMPATIBLE (400kHz)
- LOW OPERATING CURRENT OF 130µA
- OPERATING TEMPERATURE OF –40 TO 85°C
- AUTOMATIC LEAP YEAR COMPENSATION
- SPECIAL SOFTWARE PROGRAMMABLE OUTPUT
- OSCILLATOR STOP DETECTION

Figure 1. 8-pin SOIC Packages

SO8 (M)

TSSOP8 3x3 (DS)

TABLE OF CONTENTS

SUMMARY DESCRIPTION

The M41T0 TIMEKEEPER® RAM is a low power Serial TIMEKEEPER with a built-in 32.768kHz oscillator (external crystal controlled). Eight registers are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. Addresses and data are transferred serially via a two-line bi-directional bus. The built-in address register is incremented automatically after each WRITE or READ data byte.

The M41T0 is supplied in 8 lead Plastic Small Outline package.

Figure 2. Logic Diagram

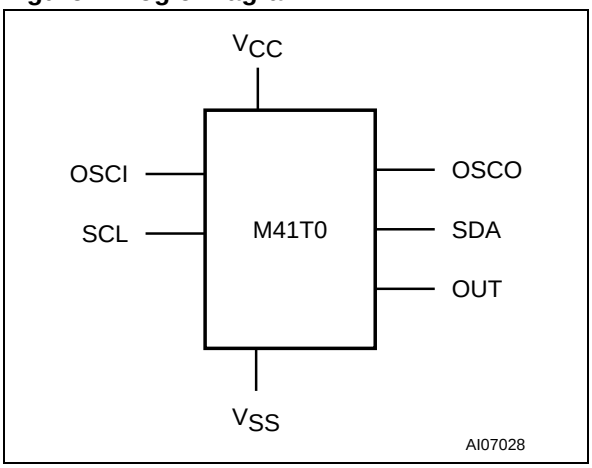
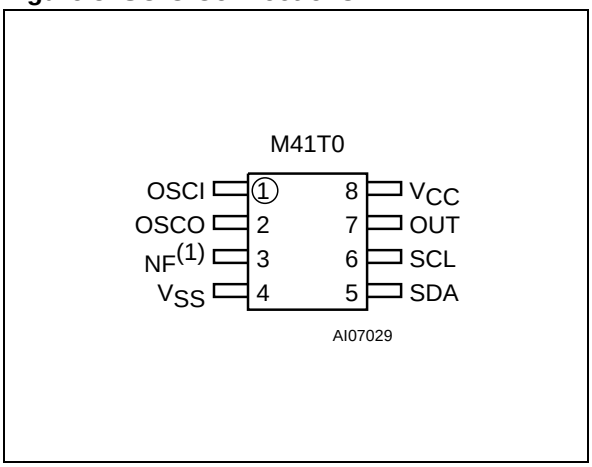


Figure 3. SOIC Connections



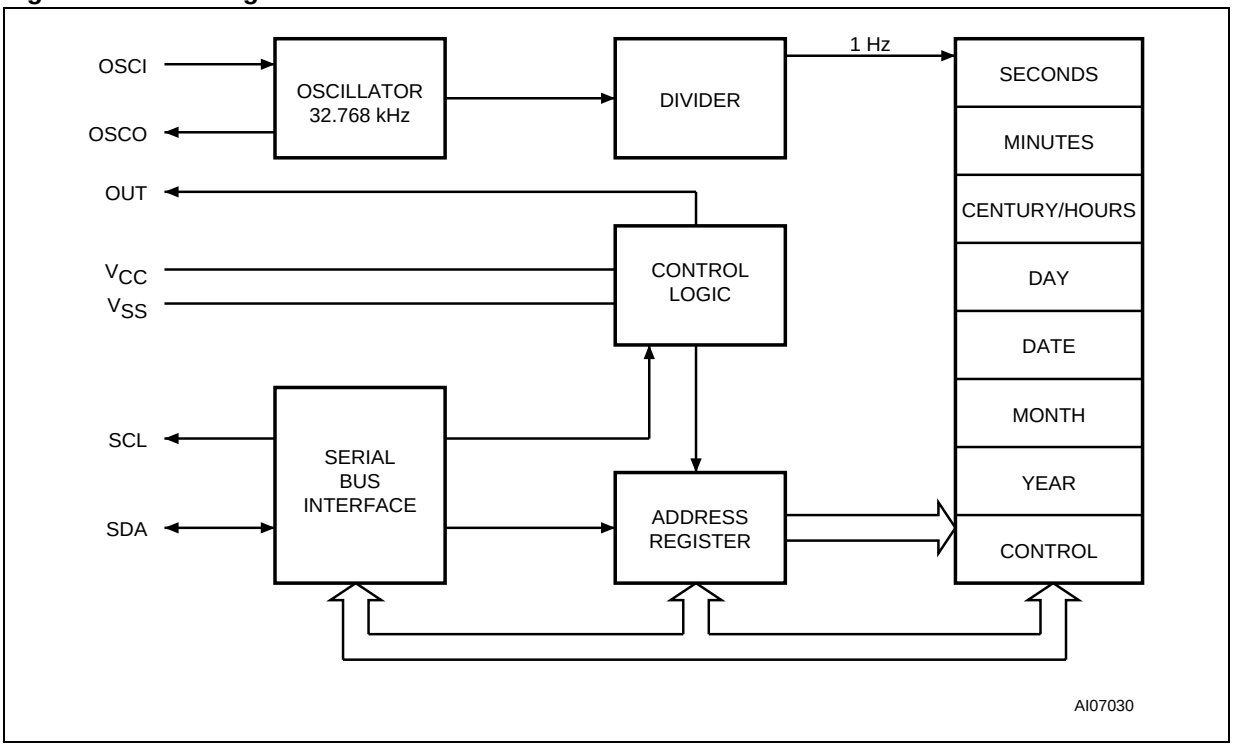
Note: 1. NF pin must be tied to V_{SS}.

Table 1. Signal Names

OSCI	Oscillator Input
OCSO	Oscillator Output
OUT	Output Driver (Open Drain)
SDA	Serial Data Address Input / Output
SCL	Serial Clock
NF(1)	No Function
V_{CC}	Supply Voltage
V_{SS}	Ground

Note: 1. NF pin must be tied to V_{SS}.

Figure 4. Block Diagram



MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–55 to 125	°C
V_{CC}	Supply Voltage	–0.3 to 7	V
T_{SLD}(1)	Lead Solder Temperature for 10 Seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to V_{CC} + 0.3	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: 1. Reflow at peak temperature of 255°C to 260°C for < 30 seconds (total thermal budget not to exceed 180°C for between 90 and 150 seconds).

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. Operating and AC Measurement Conditions

Parameter	M41T0	Unit
Supply Voltage (V_{CC})	2.0 to 5.5	V
Ambient Operating Temperature (T_A)	–40 to 85	°C
Load Capacitance (C_L)	100	pF
Input Rise and Fall Times	≤ 5	ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$	V
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Input/Output Waveform

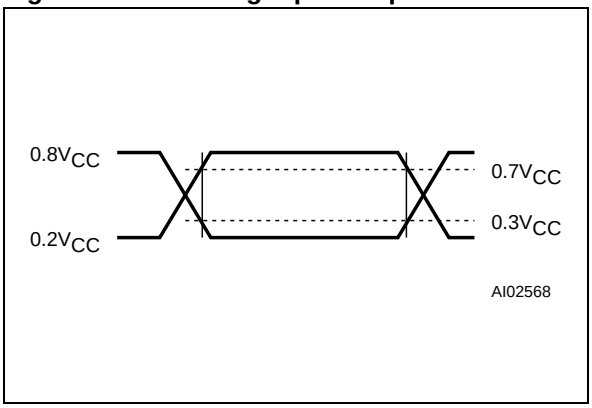


Table 4. Capacitance

Symbol	Parameter(1,2)	Min	Max	Unit
C_{IN}	Input Capacitance (SCL)		7	pF
C_{OUT}(3)	Output Capacitance (SDA, OUT)		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		50	ns

Note: 1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

Table 5. DC Characteristics

Sym	Parameter	Test Condition(1)		Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$				±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$				±1	µA
I_{CC1}	Supply Current	Frequency (SCL) = 400kHz	3.0V		35	55	µA
			5.5V		130	200	µA
I_{CC2}(2)	Supply Current (Standby)	All inputs = V_{CC} – 0.2V Frequency (SCL) = 0Hz	3.0V		0.9	1.2	µA
			5.5V			31	µA
V_{IL}	Input Low Voltage			–0.3		0.3 V_{CC}	V
V_{IH}	Input High Voltage			0.7 V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA				0.4	V
	Output Low Voltage (Open Drain)	I_{OL} = 10mA				0.4	V

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC} = 2.0 to 5.5V (except where noted).
2. At 25°C.

Table 6. Crystal Electrical Characteristics

Symbol	Parameter(1,2)	Min	Typ	Max	Unit
f_O	Resonant Frequency		32.768		kHz
R_S	Series Resistance			60(3)	KΩ
C_L	Load Capacitance		12.5		pF

Note: 1. These values are externally supplied. STMicroelectronics recommends the KDS DT-38: 1TA/1TC252E127, Tuning Fork Type (thru-hole) or the DMX-26S: 1TJS125FH2A212, (SMD) quartz crystal for industrial temperature operations. KDS can be contacted at kouhou@kdsj.co.jp or http://www.kdsj.co.jp for further information on this crystal type.
2. Load capacitors are integrated within the M41T0. Circuit board layout considerations for the 32.768kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.
3. R_S = 40kΩ when $V_{CC} \le 2.5V$.

OPERATION

The M41T0 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 8 bytes contained in the device can then be accessed sequentially in the following order:

1. Seconds Register
2. Minutes Register
3. Century/Hours Register
4. Day Register
5. Date Register
6. Month Register
7. Years Register
8. Control Register

2-Wire Bus Characteristics

This bus is intended for communication between different ICs. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

– Data transfer may be initiated only when the bus is not busy.
– During data transfer, the data line must remain stable whenever the clock line is High. Changes in the data line while the clock line is High will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy. Both data and clock lines remain High.

Start data transfer. A change in the state of the data line, from High to Low, while the clock is High, defines the START condition.

Stop data transfer. A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

Data valid. The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition, a device that gives out a message is called “transmitter”, the receiving device that gets the message is called “receiver”. The device that controls the message is called “master”. The devices that are controlled by the master are called “slaves”.

Acknowledge. Each byte of eight bits is followed by one Acknowledge Bit. This Acknowledge Bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 6. Serial Bus Data Transfer Sequence

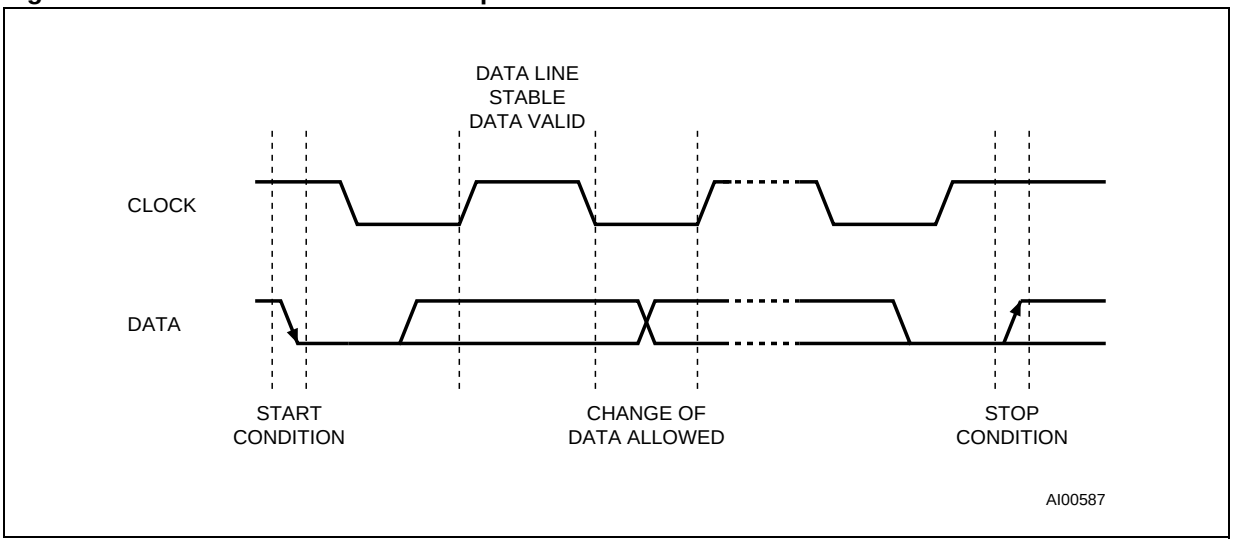


Figure 7. Acknowledgement Sequence

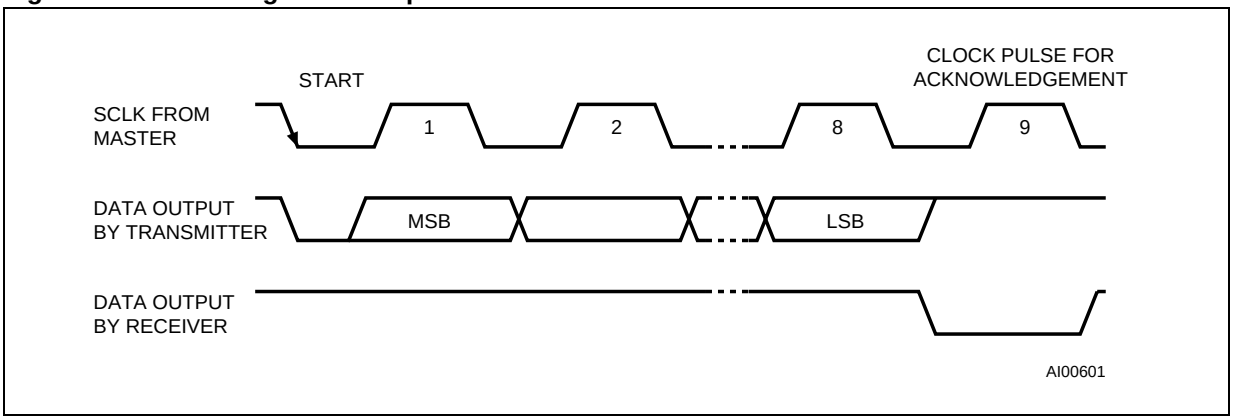
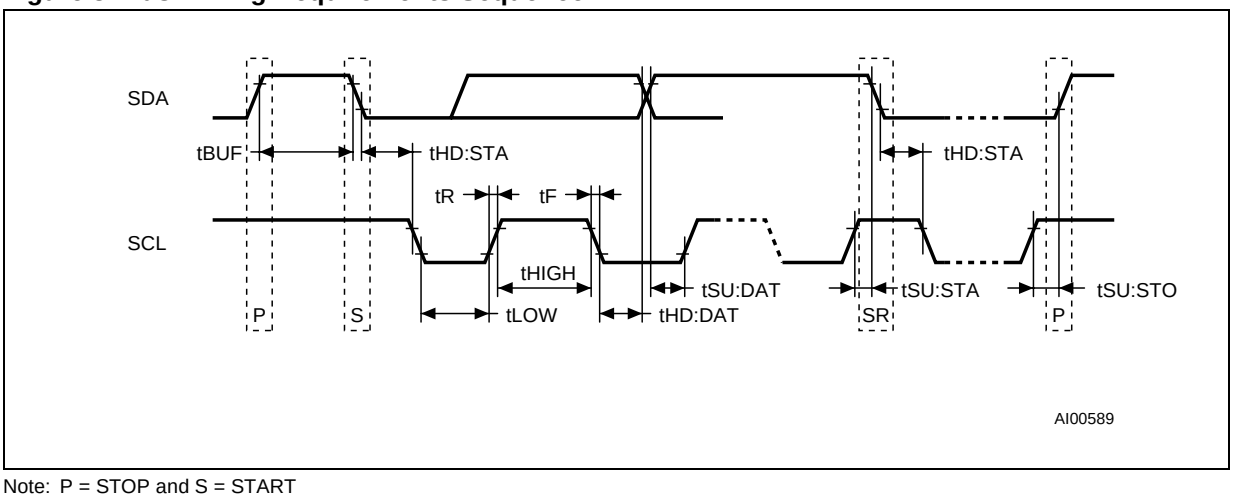


Figure 8. Bus Timing Requirements Sequence



Note: P = STOP and S = START

Table 7. AC Characteristics

Symbol	Parameter[1]	Min	Typ	Max	Unit
f_{SCL}	SCL Clock Frequency	0		400	kHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_R	SDA and SCL Rise Time			300	ns
t_F	SDA and SCL Fall Time			300	ns
$t_{HD:STA}$	START Condition Hold Time (after this period the first clock pulse is generated)	600			ns
$t_{SU:STA}$	START Condition Setup Time (only relevant for a repeated start condition)	600			ns
$t_{SU:DAT}$	Data Setup Time	100			ns
$t_{HD:DAT}$[2]	Data Hold Time	0			µs
$t_{SU:STO}$	STOP Condition Setup Time	600			ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3			µs

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC} = 2.0 to 5.5V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

READ Mode

In this mode, the master reads the M41T0 slave after setting the slave address (see Figure 9.). Following the WRITE Mode Control Bit (R/W = 0) and the Acknowledge Bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ Mode Control Bit (R/W = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an Acknowledge Bit to the slave transmitter. The address pointer is only incremented on reception of an Acknowledge Bit. The M41T0 slave transmitter will now place the data byte at address A_{n+1} on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to A_{n+2}.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ Mode may also be implemented, whereby the master reads the M41T0 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see Figure 11., page 13).

WRITE Mode

In this mode the master transmitter transmits to the M41T0 slave receiver. Bus protocol is shown in Figure 12., page 13. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The M41T0 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte (see Figure 9.).

Figure 9. Slave Address Location

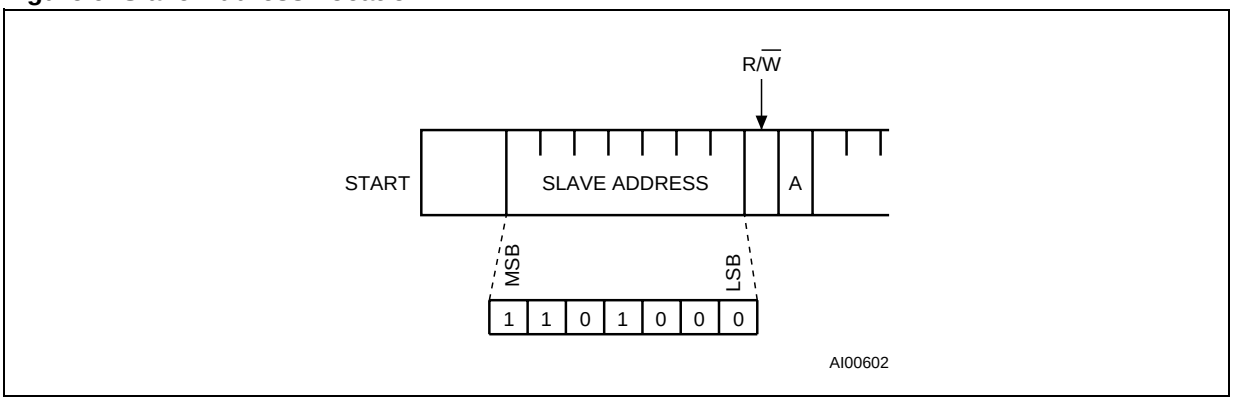


Figure 10. READ Mode Sequence

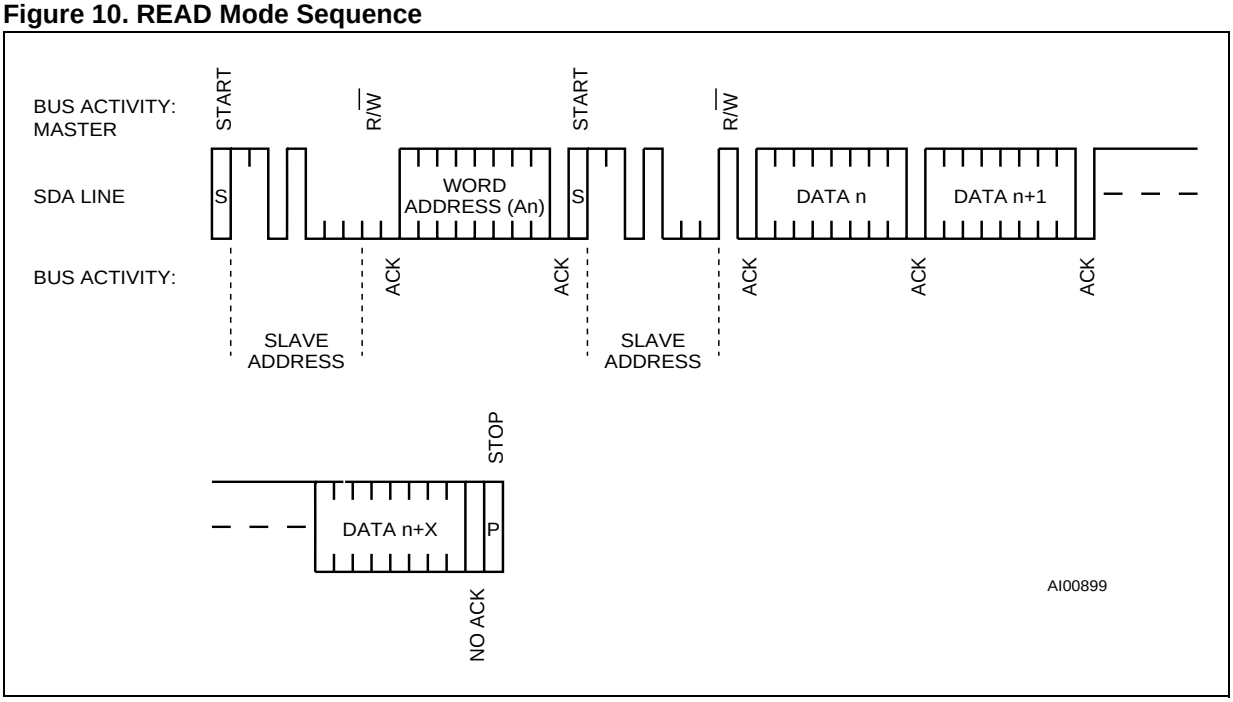


Figure 11. Alternate READ Mode Sequence

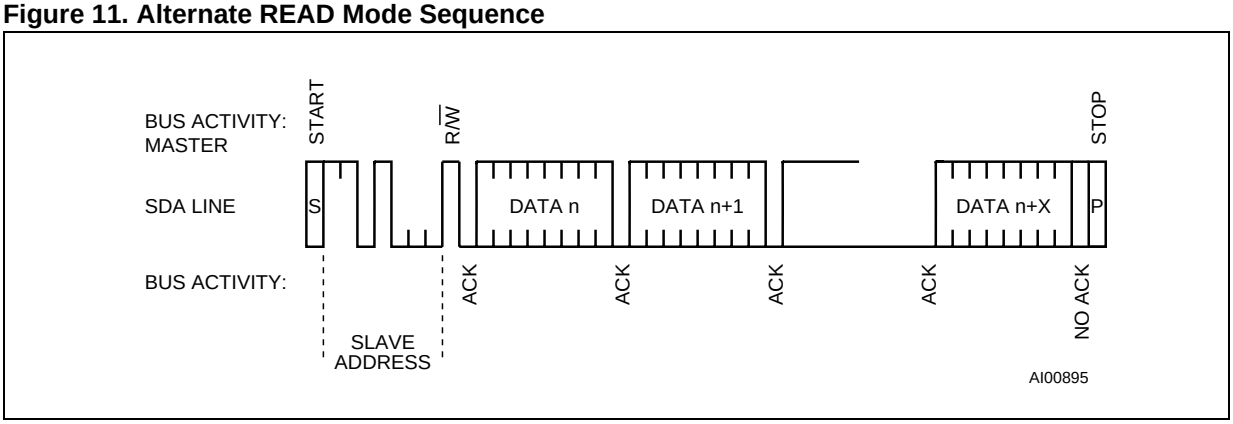
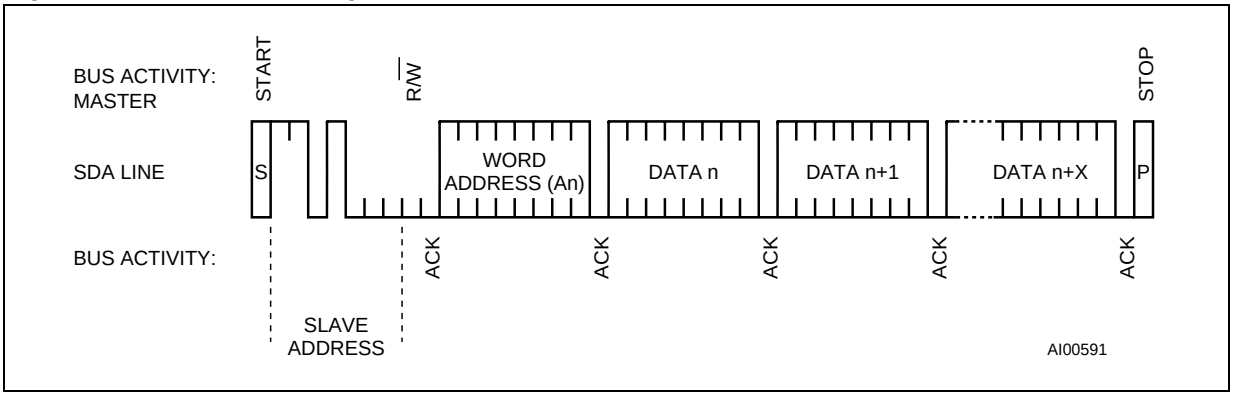


Figure 12. WRITE Mode Sequence



CLOCK OPERATION

The M41T0 is driven by a quartz controlled oscillator with a nominal frequency of 32.768kHz. The accuracy of the Real-Time Clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC. The M41T0 is tested to meet ± 35 ppm with nominal crystal. The eight-byte Clock Register (see Table 8., page 15) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Seconds, Minutes, and Hours are contained within the first three registers. Bits D6 and D7 of Clock Register 2 (Hours Register) contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0', CB will not toggle. Bits D0 through D2 of Register 3 contain the Day (day of week). Registers 4, 5 and 6 contain the Date (day of month), Month and Years. The final register is the Control Register. Bit D7 of Register 0 contains the STOP Bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within four seconds (typically one second).

The seven clock registers may be read one byte at a time, or in a sequential block. The Control Register (Address location 7) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the seven clock addresses are being read. If a clock address is being read, an update of the clock registers will be delayed by 250ms to allow the READ to be completed before the update occurs. This will prevent a transition of data during the READ.

Note: This 250ms delay affects only the clock register update and does not alter the actual clock time.

Output Driver Pin

The OUT pin is an output driver that reflects the contents of D7 of the Control Register. In other words, when D7 of location 7 is a '0' then the OUT pin will be driven low.

Note: The OUT pin is open drain which requires an external pull-up resistor.

Oscillator Stop Detection

If the Oscillator Fail (OF) Bit is internally set to a '1,' this indicates that the oscillator has either stopped, or was stopped for some period of time and can be used to judge the validity of the clock and date data. This bit will be set to '1' any time the oscillator stops. The following conditions can cause the OF Bit to be set:

– The first time power is applied (defaults to a '1' on power-up).
– The voltage present on V_{CC} is insufficient to support oscillation.
– The ST Bit is set to '1.'
– External interference or removal of the crystal.

This bit will remain set to '1' until written to logic '0.'

The oscillator must start and have run for at least 4 seconds before attempting to reset the OF Bit to '0.' This function operates both under normal power and in battery back-up.

Initial Power-on Defaults

Upon initial application of power to the device, the OUT Bit and OF Bit will be set to a '1,' while the ST Bit will be set to '0.' All other Register bits will initially power-on in a random state.

Table 8. Register Map

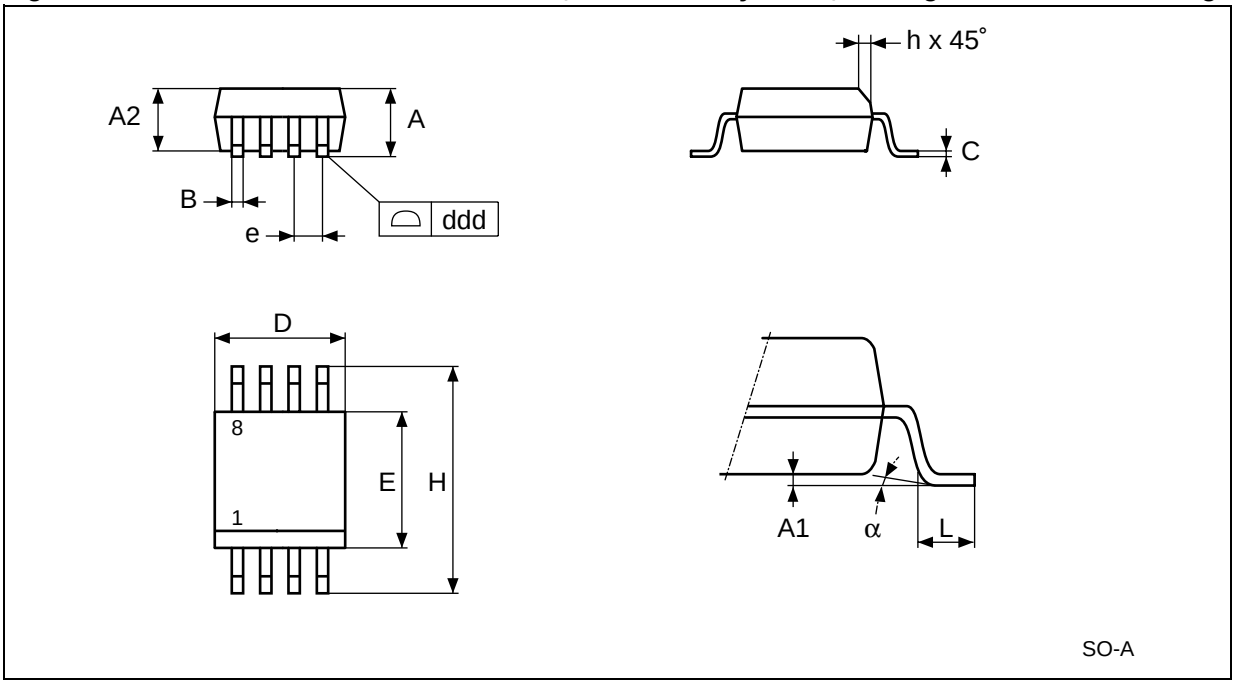
Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST	10 Seconds			Seconds				Seconds	00-59
1	OF	10 Minutes			Minutes				Minutes	00-59
2	CEB (1)	CB	10 Hours		Hours				Century/Hours	0-1/00-23
3	X	X	X	X	X	Day			Day	01-07
4	X	X	10 Date		Date				Date	01-31
5	X	X	X	10 M.	Month				Month	01-12
6	10 Years				Years				Year	00-99
7	OUT	0	X	X	X	X	X	X	Control	

Keys: ST = STOP Bit
OUT = Output level
X = Don't care
0 = Must be set to '0.'
CEB = Century Enable Bit
CB = Century Bit
OF = Oscillator Fail Bit

Note: 1. When CEB is set to '1', CB will toggle from '0' to '1' or from '1' to '0' at the turn of the century (dependent upon the initial value set). When CEB is set to '0', CB will not toggle.

PACKAGE MECHANICAL INFORMATION

Figure 13. SO8 – 8 lead Plastic Small Outline, 150 mils body width, Package Mechanical Drawing

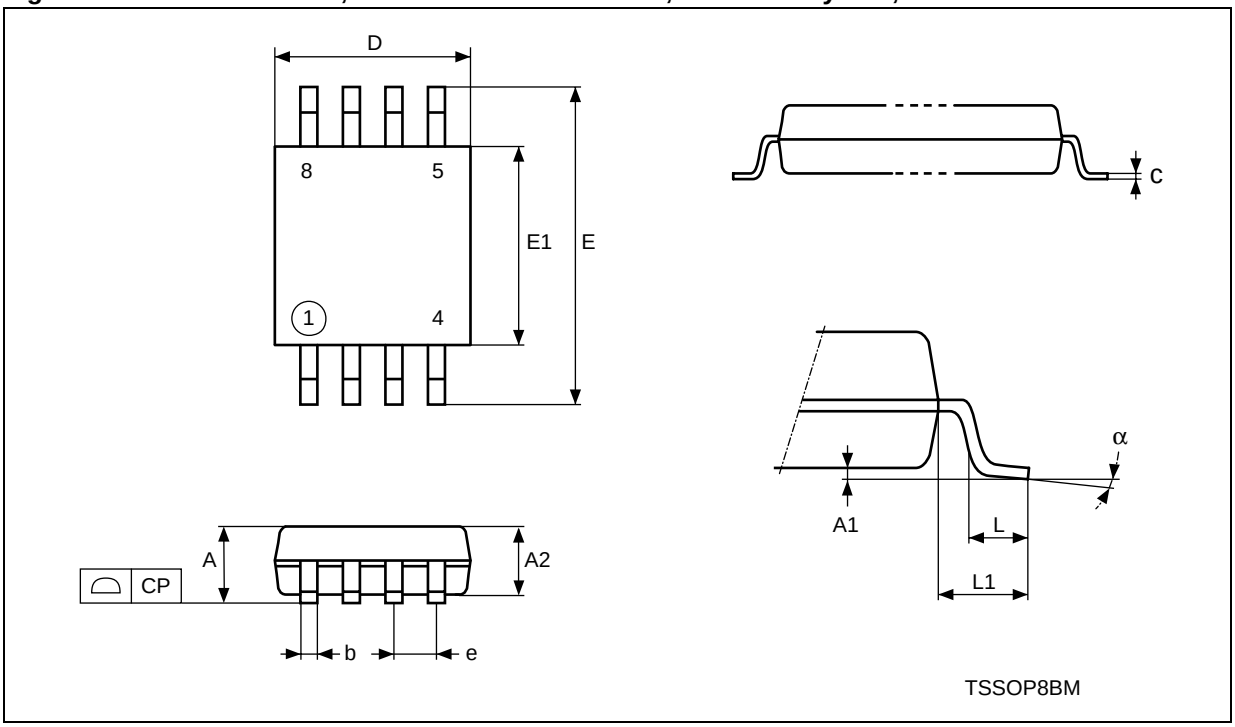


Note: Drawing is not to scale.

Table 9. SO8 – 8-lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	–	1.35	1.75	–	0.053	0.069
A1	–	0.10	0.25	–	0.004	0.010
B	–	0.33	0.51	–	0.013	0.020
C	–	0.19	0.25	–	0.007	0.010
D	–	4.80	5.00	–	0.189	0.197
ddd	–	–	0.10	–	–	0.004
E	–	3.80	4.00	–	0.150	0.157
e	1.27	–	–	0.050	–	–
H	–	5.80	6.20	–	0.228	0.244
h	–	0.25	0.50	–	0.010	0.020
L	–	0.40	0.90	–	0.016	0.035
α	–	0°	8°	–	0°	8°
N	8			8		

Figure 14. TSSOP8 – 8-lead, Thin Shrink Small Outline, 3x3mm body size, Outline



Note: Drawing is not to scale.

Table 10. TSSOP8 – 8-lead, Thin Shrink Small Outline, 3x3mm body size, Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.10	–	–	0.043
A1	–	0.05	0.15	–	0.002	0.006
A2	0.85	0.75	0.95	0.034	0.030	0.037
b	–	0.25	0.40	–	0.010	0.016
c	–	0.13	0.23	–	0.005	0.009
CP	–	–	0.10	–	–	0.004
D	3.00	2.90	3.10	0.118	0.114	0.122
e	0.65	–	–	0.026	–	–
E	4.90	4.65	5.15	0.193	0.183	0.203
E1	3.00	2.90	3.10	0.118	0.114	0.122
L	0.55	0.40	0.70	0.022	0.0160.028	0.030
L1	0.95	–	–	0.037	–	–
α	–	0°	6°	–	0°	6°
N	8			8		

PART NUMBERING

Table 11. Ordering Information Scheme

Example: M41T 0 M 6 T

Device Type

M41T

Supply Voltage and Write Protect Voltage

0 = V_{CC} = 2.0 to 5.5V

Package

M = SO8 (150mils width)

DS = TSSOP8

Temperature Range

6 = –40 to 85°C

Shipping Method

blank = Tubes (Not for New Design - Use E)

E = Lead-Free Package (ECOPACK®), Tubes

F = Lead-Free Package (ECOPACK®), Tape & Reel

T = Tape & Reel (Not for New Design - Use F)

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 12. Document Revision History

Date	Rev. #	Revision Details
February 2003	1.0	First Issue
18-Feb-03	1.1	Add Pb-Free information (Table 2., Table 11.); update package information (Figure 1., Figure 14.; Table 11.)
01-Apr-03	1.2	Fix package outline and data (Figure 1., Figure 14., Table 10., Table 11.)
10-Apr-03	1.3	Revert to previous package (Figure 1., Figure 14., Table 10., Table 11.)
30-Oct-03	1.4	Remove footnote (Table 2.)
30-Jun-2004	2.0	Shipping Method options updated and Note 1 removed from Table 11., Ordering Information Scheme. Datasheet put in new template.
23-Jul-2004	3.0	Content corrected from M41T80 to M41T0.