MAX3232 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH \pm 15-kV ESD PROTECTION

SLLS410I - JANUARY 2000 - REVISED JANUARY 2004

- RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates Up To 250 kbit/s
- Two Drivers and Two Receivers
- Low Supply Current . . . 300 μA Typical
- External Capacitors . . . 4 × 0.1 μF
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Pin-Compatible Device (1 Mbit/s)
 - SNx5C3232
- Applications
 - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment

D, DB, DW, OR PW PACKAGE (TOP VIEW) 16 V_{CC} С1+ Г ∨+ Π 2 15 GND C1− ∏ 3 14∏ DOUT1 C2+ [] 4 13**∏** RIN1 C2- [] 5 12 ROUT1 11 DIN1 V- [] 6 10 DIN2 DOUT2 17 9 ROUT2 RIN2 8

description/ordering information

ORDERING INFORMATION

TA	PACKAG	ΕŤ	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	0010 (D)	Tube of 40	MAX3232CD	1447/0000
	SOIC (D)	Reel of 2500	MAX3232CDR	MAX3232C
	0010 (DIA))	Tube of 40	MAX3232CDW	MANAGOOO
000 1- 7000	SOIC (DW)	Reel of 2000	MAX3232CDWR	MAX3232C
−0°C to 70°C	CCOR (DR)	Tube of 80	MAX3232CDB	MA2020C
	SSOP (DB)	Reel of 2000	MAX3232CDBR	MA3232C
	TSSOP (PW)	Tube of 90	MAX3232CPW	MA20200
		Reel of 2000	MAX3232CPWR	MA3232C
	SOIC (D)	Tube of 40	MAX3232ID	MANAGOO
		Reel of 2500	MAX3232IDR	MAX3232I
	SOIC (DW)	Tube of 40	MAX3232IDW	MAX3232I
–40°C to 85°C	SOIC (DW)	Reel of 2000	MAX3232IDWR	IVIAA3232I
	CCOD (DD)	Tube of 80	MAX3232IDB	MD2020I
	SSOP (DB)	Reel of 2000	MAX3232IDBR	MB3232I
	TSSOR (DW)	Tube of 90	MAX3232IPW	MB3232I
	TSSOP (PW)	Reel of 2000	MAX3232IPWR	IVIDOZOZI

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH \pm 15-kV ESD PROTECTION

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description/ordering information (continued)

The MAX3232 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/ μ s driver output slew rate.

Function Tables

EACH DRIVER

INPUT DIN	OUTPUT DOUT
L	Н
Н	L

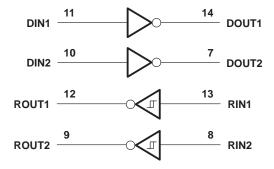
H = high level, L = low level

EACH RECEIVER

INPUT RIN	OUTPUT ROUT
L	Н
Н	L
Open	Н

H = high level, L = low level, Open = input disconnected or connected driver off

logic diagram (positive logic)





3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH \pm 15-kV ESD PROTECTION

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, V+ (see Note 1)	0.3 V to 7 V
Negative output supply voltage range, V- (see Note 1)	0.3 V to –7 V
Supply voltage difference, V+ - V- (see Note 1)	13 V
Input voltage range, V _I : Drivers	–0.3 V to 6 V
Receivers	
Output voltage range, VO: Drivers	
Receivers	0.3 V to V _{CC} + 0.3 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3):	D package 73°C/W
	DB package 82°C/W
	DW package 57°C/W
	PW package 108°C/W
Operating virtual junction temperature, T _J	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

- 2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 4)

				MIN	NOM	MAX	UNIT
	Supply voltage		V _{CC} = 3.3 V	3	3.3	3.6	.,
			$V_{CC} = 5 V$	4.5	5	5.5	V
.,	Driver high-level input voltage	DIN	V _{CC} = 3.3 V	2			V
VIH		DIN	V _{CC} = 5 V	2.4			
VIL	Driver low-level input voltage		DIN			0.8	V
.,	Driver input voltage		DIN	0		5.5	
VI Receiver input voltage			-25		25	٧	
TA	Operating free-air temperature		MAX3232C	0		70	00
			MAX3232I	-40		85	°C

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V $_{CC}$ = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V $_{CC}$ = 5 V \pm 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
ICC	Supply current	No load,	V _{CC} = 3.3 V or 5 V		0.3	1	mA

 \ddagger All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.



WITH ±15-kV ESD PROTECTION SLLS410I – JANUARY 2000 – REVISED JANUARY 2004

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
Vон	High-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND,	DIN = GND	5	5.4		V
VOL	Low-level output voltage	DOUT at R _L = 3 k Ω to GND,	$DIN = V_{CC}$	-5	-5.4		V
lіН	High-level input current	VI = VCC			±0.01	±1	μΑ
Ι _Ι L	Low-level input current	V _I at GND			±0.01	±1	μΑ
la at	Chart singuit autout aumant	V _{CC} = 3.6 V,	VO = 0 V		105	-00	A
los‡	Short-circuit output current	V _{CC} = 5.5 V,	VO = 0 V		±35	±60	mA
r _O	Output resistance	V_{CC} , V+, and V- = 0 V,	V _O = ±2 V	300	10M		Ω

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
	Maximum data rate	C _L = 1000 pF, One DOUT switching,	$R_L = 3 kΩ$, See Figure 1	150	250		kbit/s
t _{sk(p)}	Pulse skew§	C _L = 150 pF to 2500 pF	R _L = 3 kΩ to 7 kΩ, See Figure 2		300		ns
CD(tr)	Slew rate, transition region	$R_L = 3 k\Omega$ to $7 k\Omega$,	C _L = 150 pF to 1000 pF	6		30	1//
SR(tr)	(see Figure 1)	V _{CC} = 3.3 V	C _L = 150 pF to 2500 pF	4		30	V/μs

 $[\]overline{\dagger}$ All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25 ^{\circ}\text{C}$.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V $_{CC}$ = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V $_{CC}$ = 5 V \pm 0.5 V.



^{\$} Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V $_{CC}$ = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V $_{CC}$ = 5 V \pm 0.5 V.

[§] Pulse skew is defined as |tplH - tpHL| of each channel of the same device.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Vон	High-level output voltage	$I_{OH} = -1 \text{ mA}$	V _{CC} -0.6V	V _{CC} -0.1 V		V
VOL	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Parallibrary and any format through a list and to a list and	V _{CC} = 3.3 V		1.5	2.4	.,
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 5 V		1.8	2.4	V
,,	N	V _{CC} = 3.3 V	0.6	1.2		.,
V _{IT} _	Negative-going input threshold voltage	V _{CC} = 5 V	0.8	1.5		V
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.3		V
rį	Input resistance	$V_I = \pm 3 \text{ V to } \pm 25 \text{ V}$	3	5	7	kΩ

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^{\circ}\text{C}$.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.

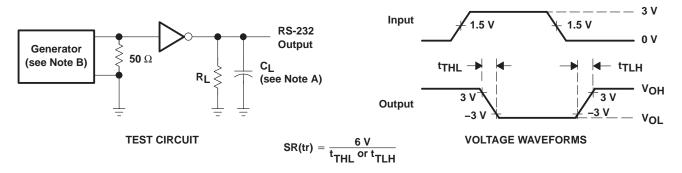
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 3)

	PARAMETER	TEST CONDITIONS	MIN TYP [†] MAX	UNIT
tPLH	Propagation delay time, low- to high-level output	0: 450 = 5	300	ns
tPHL	Propagation delay time, high- to low-level output	C _L = 150 pF	300	ns
tsk(p)	Pulse skew [‡]		300	ns

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^{\circ}\text{C}$.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50~\Omega$, 50% duty cycle, $t_\Gamma \le 10$ ns. $t_f \le 10$ ns.

Figure 1. Driver Slew Rate

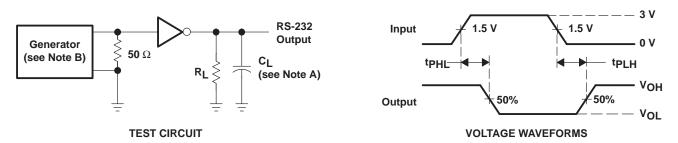


[‡] Pulse skew is defined as |tplH - tpHL| of each channel of the same device.

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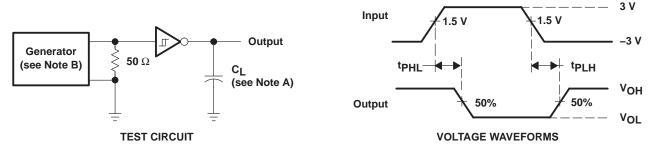
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_\Gamma \le 10$ ns. $t_f \le 10$ ns.

Figure 2. Driver Pulse Skew



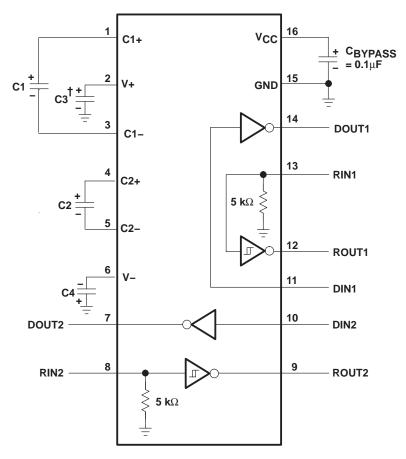
NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50~\Omega$, 50% duty cycle, $t_\Gamma \le 10~\text{ns}$.

Figure 3. Receiver Propagation Delay Times



APPLICATION INFORMATION



 $^\dagger\text{C3}$ can be connected to VCC or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

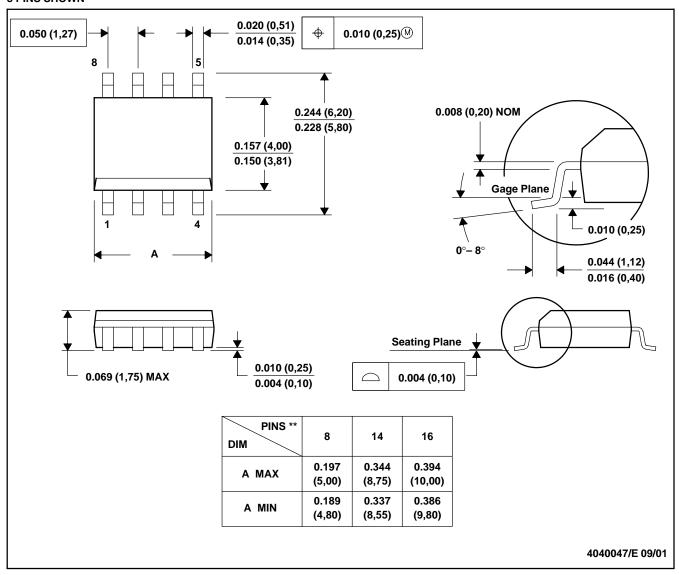
VCC	C1	C2, C3, C4
$\begin{array}{c} \textbf{3.3 V} \pm \textbf{0.3 V} \\ \textbf{5 V} \pm \textbf{0.5 V} \\ \textbf{3 V to 5.5 V} \end{array}$	0.1 μF 0.047 μF 0.1 μF	0.1 μF 0.33 μF 0.47 μF

Figure 4. Typical Operating Circuit and Capacitor Values

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

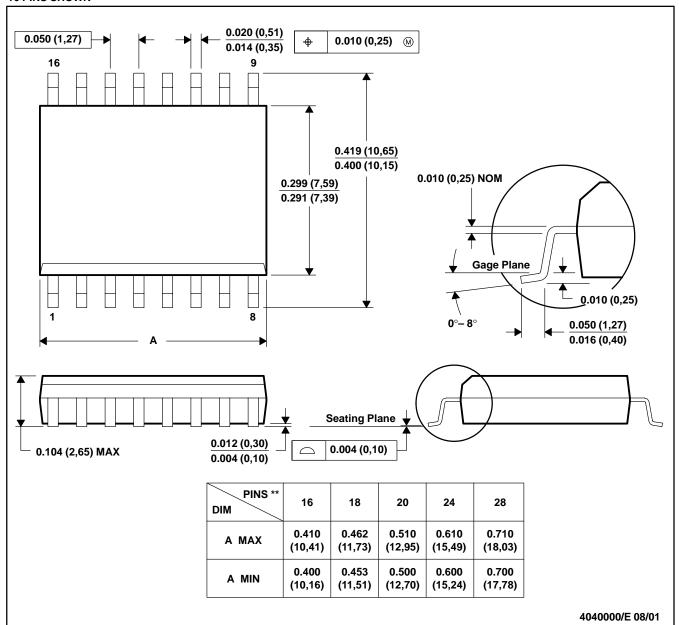
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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