

STATIC RAM CARDS

**8/16-bit Data Bus
Static RAM Card**

Connector Type

Two-piece 68-pin

MF365A-LCDATXX
MF365A-LSDATXX
MF3129-LCDATXX
MF3129-LSDATXX
MF3257-LCDATXX
MF3257-LSDATXX
MF3513-LCDATXX
MF3513-LSDATXX
MF31M1-LCDATXX
MF31M1-LSDATXX
MF32M1-LCDATXX
MF32M1-LSDATXX
MF34M1-LCDATXX
MF34M1-LSDATXX

DESCRIPTION

Mitsubishi's Static RAM cards provide large memory capacities on a device approximately the size of a credit card(85.6mm×54mm×3.3mm). The cards use a 8/16 bit data bus.The devices use a replaceable lithium battery to maintain data. Available in 64K byte-4M byte capacities, Mitsubishi's Static RAM cards are available with a 68-pin, two-piece connector.

- Electrostatic discharge protection to 15kV
- Buffered interface
- 68-pin connector
- 8-bit and 16-bit data width
- Write protect switch
- Battery voltage pin
- LS Type Wide Range operating temperature
Ta= -20 to 70°C

FEATURES

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size

APPLICATIONS

- Office automation
- Computers
- Telecommunications
- Data Communications
- Industrial
- Consumer

PRODUCT LIST

Type name	Item	Memory capacity	Data Bus width(bits)	Attribute memory	Auxiliary battery	Memory organization	Outline drawing	Main battery holder
MF365A-LCDATXX		64KB	8/16	NO	NO	256K bit SRAM×2	68P-003	Screw type
MF3129-LCDATXX		128KB				256K bit SRAM×4		
MF3257-LCDATXX		256KB				1M bit SRAM×2		
MF3513-LCDATXX		512KB				1M bit SRAM×4		
MF31M1-LCDATXX		1MB				1M bit SRAM×8		
MF32M1-LCDATXX		2MB				1M bit SRAM×16		
MF34M1-LCDATXX		4MB				4M bit SRAM×8		
MF365A-LSDATXX		64KB				256K bit SRAM×2		
MF3129-LSDATXX		128KB				256K bit SRAM×4		
MF3257-LSDATXX		256KB				1M bit SRAM×2		
MF3513-LSDATXX		512KB				1M bit SRAM×4		
MF31M1-LSDATXX		1MB				1M bit SRAM×8		
MF32M1-LSDATXX		2MB				1M bit SRAM×16		
MF34M1-LSDATXX		4MB				4M bit SRAM×8		



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PIN ASSIGNMENT

Two-Piece Type (68-pin)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D3	Data I/O	36	CD1#	Card detect 1
3	D4		37	D11	Data I/O
4	D5		38	D12	
5	D6		39	D13	
6	D7		40	D14	
7	CE1#		Card enable 1	41	
8	A10	Address input	42	CE2#	Card enable 2
9	OE#	Output enable	43	NC	No connection
10	A11	Address input	44	NC	
11	A9		45	NC	
12	A8		46	A17	Address input
13	A13		47	A18	
14	A14		48	A19	
15	WE#	Write enable	49	A20	
16	NC	No connection	50	A21	
17	VCC	Power supply voltage	51	VCC	Power supply voltage
18	NC	No connection	52	NC	No connection
19	A16	A16(NC for 64KB type)	53	NC	No connection
20	A15	Address input	54	NC	No connection
21	A12		55	NC	
22	A7		56	NC	
23	A6		57	NC	
24	A5		58	NC	
25	A4		59	NC	
26	A3		60	NC	
27	A2		61	REG#	REG function
28	A1		62	BVD2	Battery voltage detect 2
29	A0		63	BVD1	Battery voltage detect 1
30	D0	Data I/O	64	D8	Data I/O
31	D1		65	D9	
32	D2		66	D10	
33	WP	Write protect	67	CD2#	Card detect 2
34	GND	Ground	68	GND	Ground

WRITE PROTECT MODE (WP)

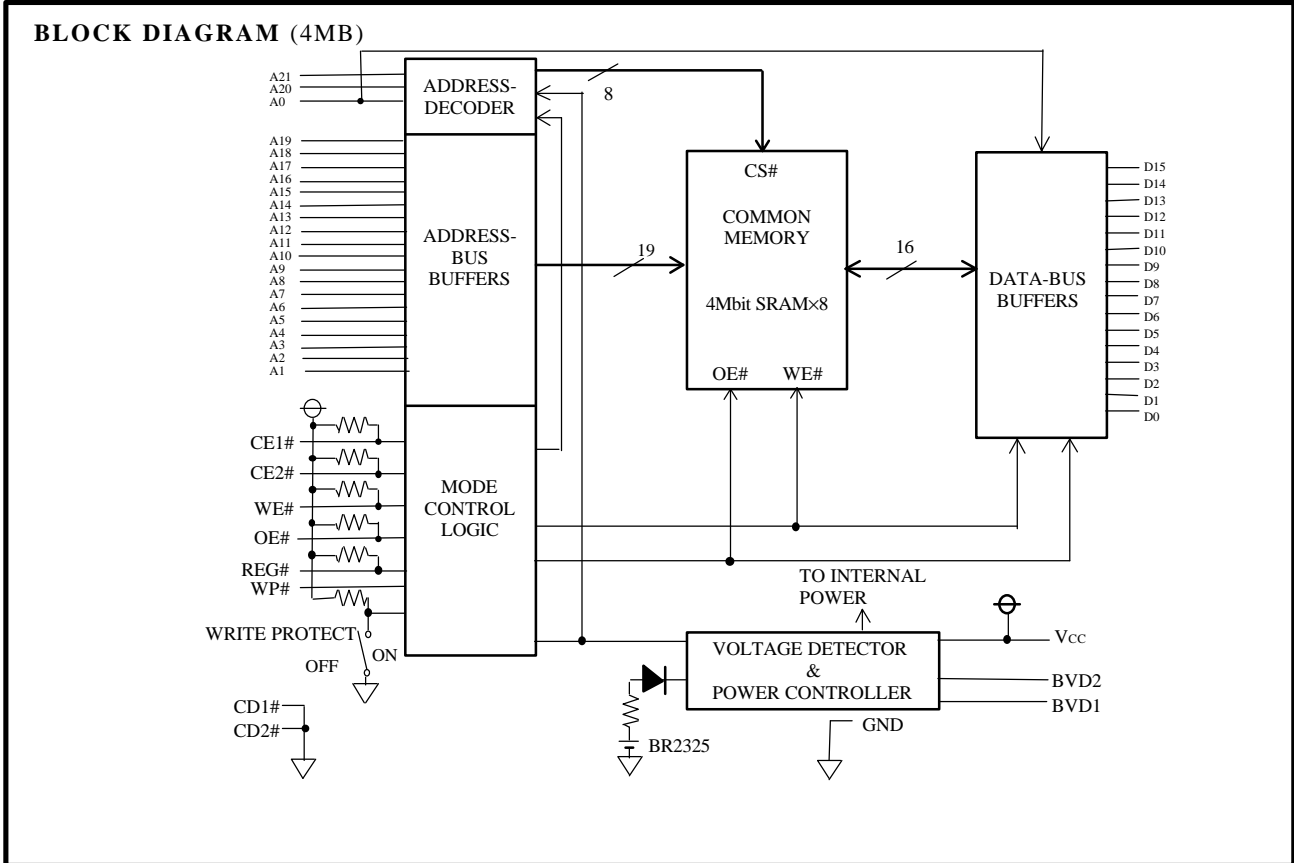
When the write protect switch is switched on, this card goes into a write protect mode that can read but not write data.

In this mode, the WP pin becomes "H" level.

At the shipment the write protect switch is switched off (Normal mode : The card can be written ; WP pin indicates "L" level).

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FUNCTION TABLE

Mode	REG#	CE1#	CE2#	OE#	WE#	A0	I/O (D15~D8)	I/O (D7~D0)	Icc
Standby	X	H	H	X	X	X	High-impedance	High-impedance	Standby
Read A (16bit) common	H	L	L	L	H	X	Odd Byte Data out	Even Byte Data out	Active
Write A (16bit) common	H	L	L	H	L	X	Odd Byte Data in	Even Byte Data in	Active
Read B (8bit) common	H	L	H	L	H	L	High-impedance	Even Byte Data out	Active
	H	L	H	L	H	H	High-impedance	Odd Byte Data out	Active
Write B (8bit) common	H	L	H	H	L	L	High-impedance	Even Byte Data in	Active
	H	L	H	H	L	H	High-impedance	Odd Byte Data in	Active
Read C (8bit) common	H	H	L	L	H	X	Odd Byte Data out	High-impedance	Active
Write C (8bit) common	H	H	L	H	L	X	Odd Byte Data in	High-impedance	Active
Output disable	X	X	X	H	H	X	High-impedance	High-impedance	Active
Read A (16bit) attribute	L	L	L	L	H	X	Data out (unknown)	Data out (FFh)	Active
Read B (8bit) attribute	L	L	H	L	H	L	High-impedance	Data out (FFh)	Active
	L	L	H	L	H	H	High-impedance	Data out (unknown)	Active
Read C (8bit) attribute	L	H	L	L	H	X	Data out (unknown)	High-impedance	Active

Note 1 : H=VIH, L=VIL, X=VIH or VIL

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Supply voltage	With respect to GND	-0.3~6.0	V
Vi	Input voltage		-0.3~VCC+0.3	V
Vo	Output voltage		0~VCC	V
Topr1	Operating temperature 1	Read, Write, Operation	LC series 0~70	°C
			LS series -20~70	°C
Topr2	Operating temperature 2	Data retention	LC series 0~70	°C
			LS series -20~70	°C
Tstg	Storage temperature		-30~80	°C

RECOMMENDED OPERATING CONDITIONS (LC series Ta= 0~55°C, unless otherwise noted) (LS series Ta=-20~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VCC	VCC Supply voltage	4.50	5.0	5.25	V
GND	System ground		0		V
VIH	High input voltage	3.5		VCC	V
VIL	Low input voltage	0		0.8	V

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ELECTRICAL CHARACTERISTICS (LC series Ta= 0~55°C, VCC=4.50~5.25V, unless otherwise noted)
(LS series Ta=-20~70°C, VCC=4.50~5.25V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit	
				Min.	Typ.	Max.		
VOH	High output voltage	IOH=-1.0mA		2.4			V	
VOL	Low output voltage	IOL=1mA				0.4	V	
I _{IH}	High input current	V _I =V _{CC} V				10	μA	
I _{IL}	Low input current	V _I =0V	CE1#, CE2#, WE#, OE#, REG#	-10		-70	μA	
			Other inputs					
IOZH	High output current in off state	CE1#=CE2#=V _{IH} or OE#=V _{IH} WE#=V _{IH} , V _O =V _{CC}				10	μA	
IOZL	Low output current in off state	CE1#=CE2#=V _{IH} or OE#=V _{IH} WE#=V _{IH} , V _O =0V				-10	μA	
ICC 1 • 1	Active supply current 1	CE1#=CE2#=V _{IL} Other inputs V _{IH} or V _{IL} Outputs=open Cycle time=250ns	64KB~1MB	16bit			150	mA
				8bit			110	
			2MB	16bit			160	
				8bit			120	
			4MB	16bit			200	
				8bit			160	
ICC 1 • 2	Active supply current 2	CE1#=CE2# ≤ 0.2V Other inputs ≤ 0.2V or ≥ V _{CC} -0.2V Outputs=open Cycle time=250ns	64KB~1MB	16bit			140	mA
				8bit			100	
			2MB	16bit			150	
				8bit			110	
			4MB	16bit			190	
				8bit			150	
ICC 2 • 1	Standby supply current 1	CE1#=CE2#=V _{IH} Other inputs=V _{IH} or V _{IL}				10	mA	
ICC 2 • 2	Standby supply current 2	CE1#=CE2# ≥ V _{CC} -0.2V Other inputs ≤ 0.2V or ≥ V _{CC} -0.2V	64KB,128KB		0.15	0.30	mA	
			256KB~1MB		0.15	0.45		
			2MB,4MB		0.30	0.65		
VBDET1	Battery detect reference voltage 1*	V _{CC} =5V, Ta=25°C		2.27	2.37	2.47	V	
VBDET2	Battery detect reference voltage 2*	V _{CC} =5V, Ta=25°C		2.55	2.65	2.75	V	

Note 2 : Currents flowing into the IC are taken as positive (unsigned).

3 : Typical values are measured at V_{CC}=5V, Ta=25°C.

*Pin asserted when battery voltage drops below specified level.

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CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
CI	Input capacitance	VI=GND, VI=25mVrms f=1 MHz, Ta=25°C	64KB~2MB		45	pF
			4MB		30	
CO	Output capacitance	VO=GND, VO=25mVrms, f=1 MHz, Ta=25°C	64KB~2MB		45	pF
			4MB		20	

Note 4 : These parameters are not 100% tested.

SWITCHING CHARACTERISTICS

Read Cycle (LC series Ta= 0~55°C, VCC=4.50~5.25V, unless otherwise noted)

(LS series Ta=-20~70°C, VCC=4.50~5.25V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tCR	Read cycle time	200			ns
ta(A)	Address access time			200	ns
ta(CE)	Card enable access time			200	ns
ta(OE)	Output enable access time			100	ns
tdis(CE)	Output disable time (from CE#)			90	ns
tdis(OE)	Output disable time (from OE#)			90	ns
ten(CE)	Output enable time (from CE#)	5			ns
ten(OE)	Output enable time (from OE#)	5			ns
tv(A)	Data valid time (after address change)	0			ns

TIMING REQUIREMENTS

Write Cycle (LC series Ta= 0~55°C, VCC=4.50~5.25V, unless otherwise noted)

(LS series Ta=-20~70°C, VCC=4.50~5.25V, unless otherwise noted)

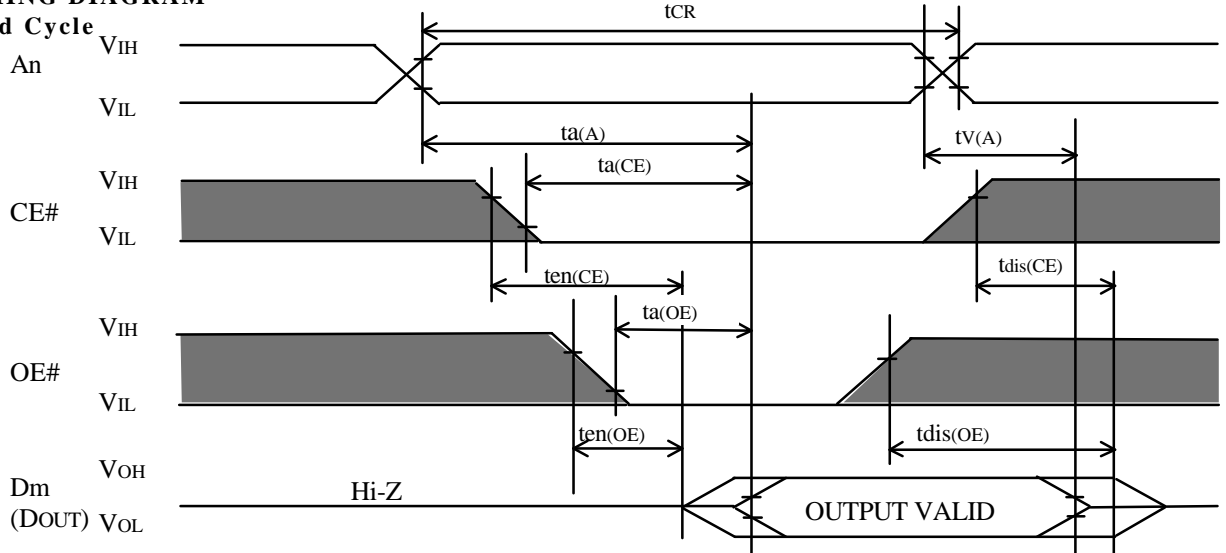
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tCW	Write cycle time	200			ns
tw(WE)	Write pulse width	120			ns
tsu(A)	Address set up time	20			ns
tsu(A-WEH)	Address set up time with respect to WE# high	140			ns
tsu(CE-WEH)	Card enable set up time with respect to WE# high	140			ns
tsu(D-WEH)	Data set up time with respect to WE# high	60			ns
th(D)	Data hold time	30			ns
trec(WE)	Write recovery time	30			ns
tdis(WE)	Output disable time (from WE#)			90	ns
tdis(OE)	Output disable time (from OE#)			90	ns
ten(WE)	Output enable time (from WE#)	5			ns
ten(OE)	Output enable time (from OE#)	5			ns
tsu(OE-WE)	OE# set up time with respect to WE# low	10			ns
th(OE-WE)	OE# hold time with respect to WE# high	10			ns

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TIMING DIAGRAM

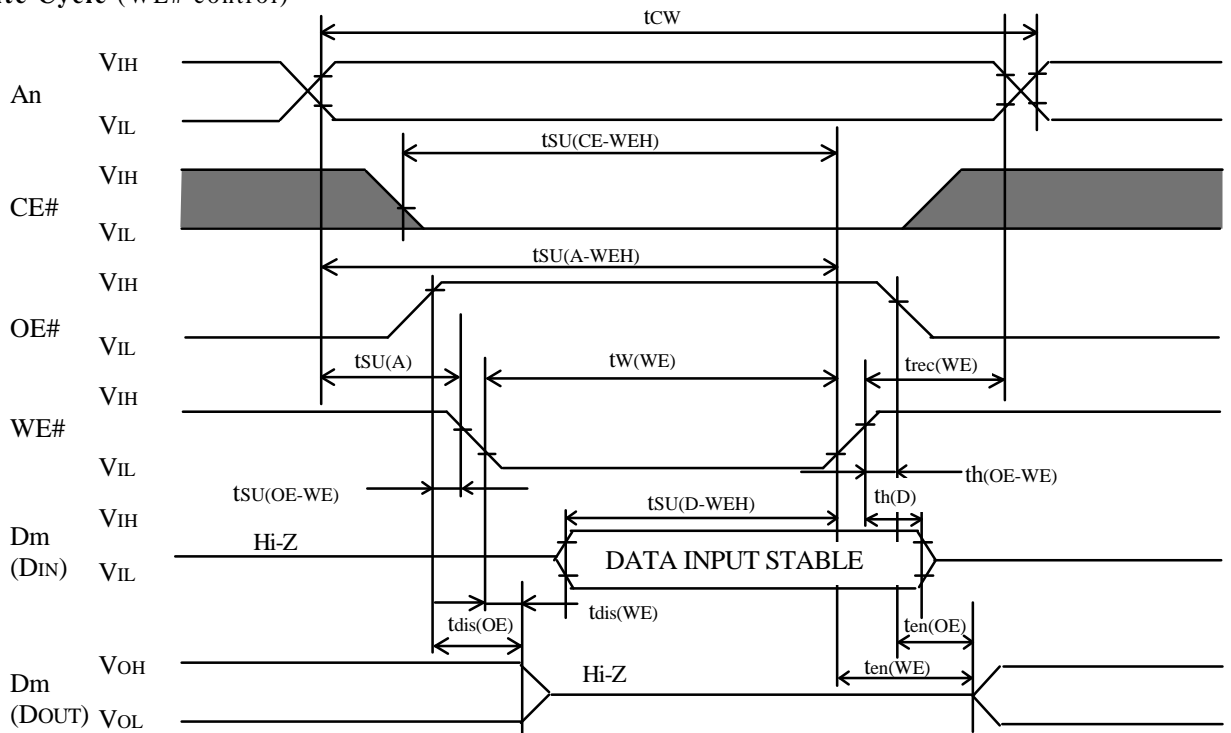
Read Cycle



WE#="H" level
REG#="H" level

Note 5 :  Indicates the don't care input

Write Cycle (WE# control)

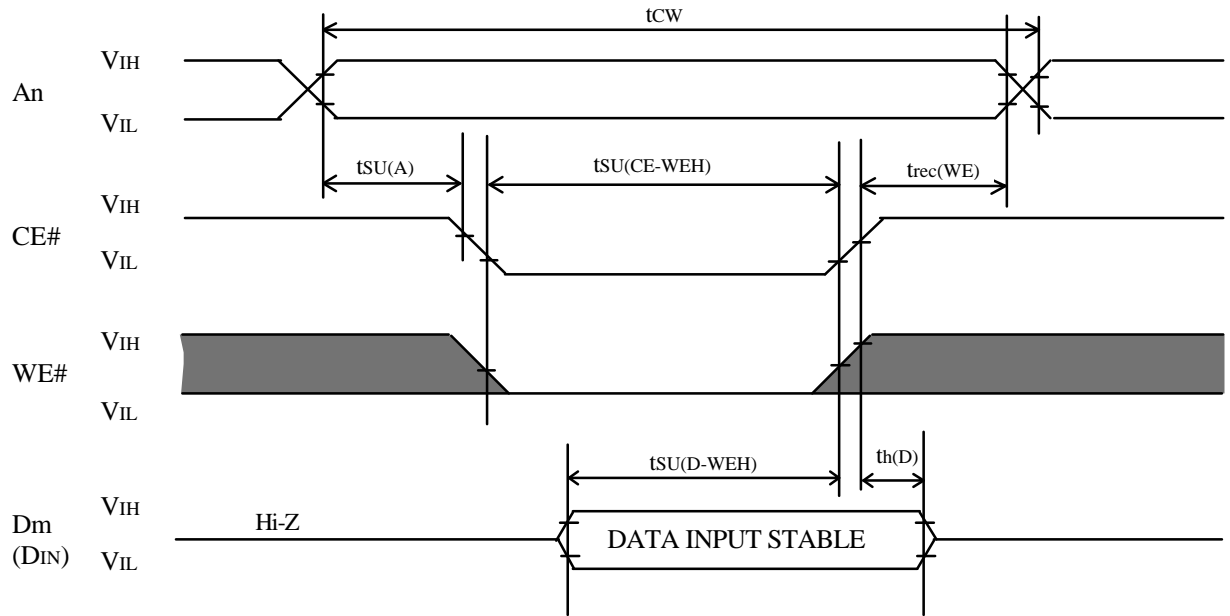


REG#="H" level

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Write Cycle (CE# control)



OE#="H" level
REG#="H" level

SWITCHING CHARACTERISTICS (Attribute)

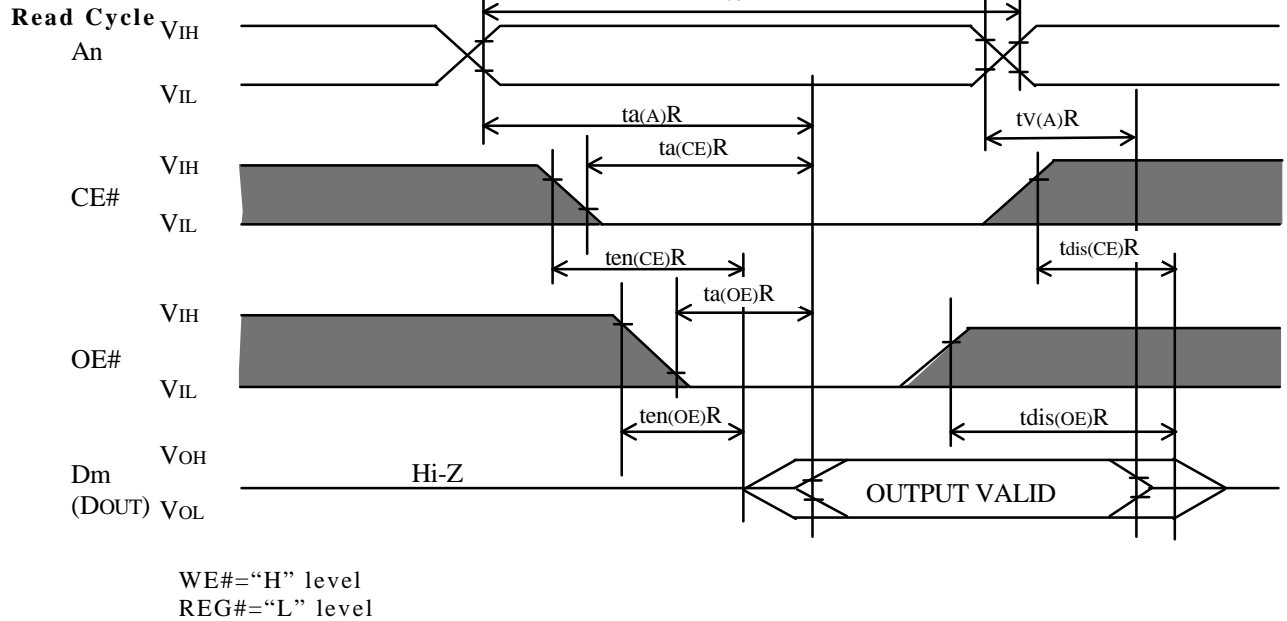
Read Cycle (LC series Ta= 0~55°C, VCC=4.50~5.25V, unless otherwise noted)
(LS series Ta=-20~70°C, VCC=4.50~5.25V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tCRR	Read cycle time	300			ns
ta(A)R	Address access time			300	ns
ta(CE)R	Card enable access time			300	ns
ta(OE)R	Output enable access time			150	ns
tdis(CE)R	Output disable time (from CE#)			100	ns
tdis(OE)R	Output disable time (from OE#)			100	ns
ten(CE)R	Output enable time (from CE#)	5			ns
ten(OE)R	Output enable time (from OE#)	5			ns
tV(A)R	Data valid time after address change	0			ns

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TIMING DIAGRAM (Attribute)



Note 6 : Test Conditions

Input pulse levels : $V_{IL}=0.4V$, $V_{IH}=4.0V$

Input pulse rise, fall time : $t_r=t_f=10ns$

Reference voltage

Input : $V_{IL}=0.8V$, $V_{IH}=3.5V$

Output : $V_{OL}=0.8V$, $V_{OH}=3.0V$

(t_{en} and t_{dis} are measured when output voltage is $\pm 500mV$ from steady state.)

Load : 100pF+1 TTL gate

5pF+1 TTL gate (at t_{en} and t_{dis} measuring)

7 : Writing is executed in overlap of CE# and WE# are "L" level. (only for Common Memory)

8 : Don't apply inverted phase signal externally when Dm pin is in output mode.

9 : CE# is indicated as follows:

Read A/Write A : CE#=CE1#=CE2#

Read B/Write B : CE#=CE1#, CE2#="H" level

Read C/Write C : CE#=CE2#, CE1#="H" level

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ELECTRICAL CHARACTERISTICS

BATTERY BACKUP (LC series Ta= 0~55°C, unless otherwise noted)

(LS series Ta=-20~70°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit	
			Min.	Typ.	Max.		
VBATT	Back-up enable battery voltage	All pins open	2.6			V	
Vi(CE)	Card enable voltage	2.4V ≤ VCC ≤ 5.25V	2.4			V	
		0V ≤ VCC < 2.4V	VCC-0.1	VCC	VCC+0.1		
Icc(BUP)	Battery back-up supply current	All pins open, VBATT=3V, Ta=25°C	64KB			3	μA
			128KB			5	
			256KB			3	
			512KB			5	
			1MB			9	
			2MB			17	
Icc(BUP)	Battery back-up supply current	All pins open, VBATT=3V	4MB			9	μA
			64KB			40	
			128KB			70	
			256KB			100	
			512KB			200	
			1MB			400	
			2MB			800	
			4MB			400	

TIMING REQUIREMENTS (LC series Ta= 0~55°C, unless otherwise noted)

(LS series Ta=-20~70°C, unless otherwise noted)

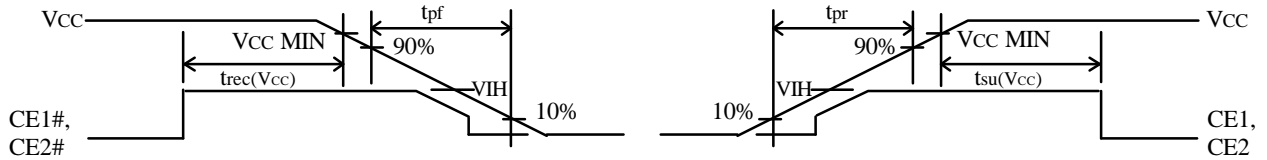
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tpr	Power supply rise time	0.1		300	ms
tpf	Power supply fall time	3		300	ms
tsu(VCC)	Set up time at power on	20			ms
trec(VCC)	Recovery time at power off	1000			ns

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CARD INSERTION/REMOVAL TIMING DIAGRAM

VCC MIN means Minimum Operating Voltage=4.75V.



Note 10: When the card is holding valuable data, the battery must not be removed unless VCC is present.

BATTERY SPECIFICATIONS

A replaceable battery (type BR2325) with a capacity of 165mAH is used:
Estimated battery life when the card is left continuously.

MF365A-LC/LSDATXX	5.9years
MF3129-LC/LSDATXX	3.6years
MF3257-LC/LSDATXX	5.9years
MF3513-LC/LSDATXX	3.6years
MF31M1-LC/LSDATXX	2.0years
MF32M1-LC/LSDATXX	1.1years
MF34M1-LC/LSDATXX	2.0years

Conditions

Temperature : 25°C

Humidity : 60%RH