MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

DESCRIPTION

The MH4M36CJD is an 4M word by 36-bit dynamic RAM module and consists of 8 industry standard 4M X 4 dynamic RAMs in TSOP and 4 industry standard 4M X 1 dynamic RAMs in TSOP.

The ICs are mounted on both sides of small ceracom PC boards and form a convenient 64-pin WDIP package.

FEATURES

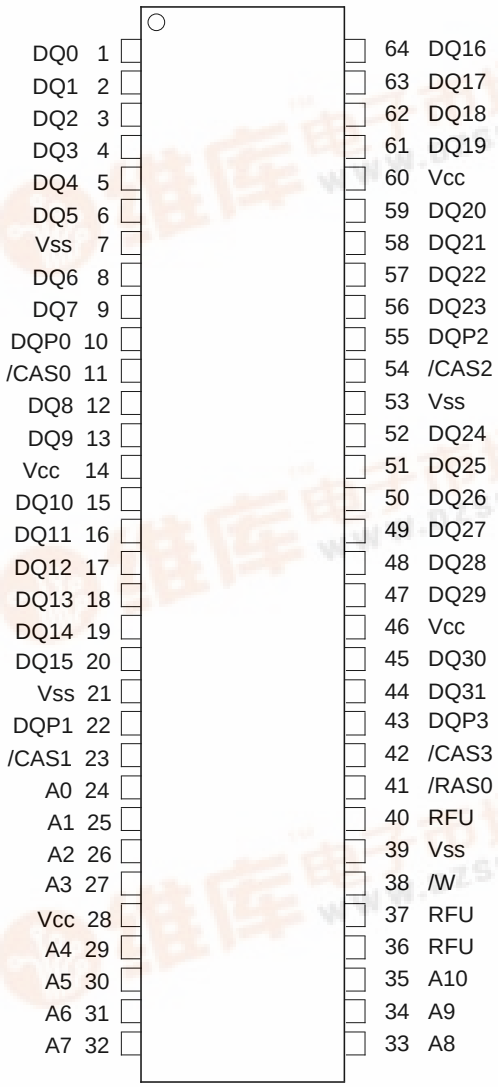
Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
MH4M36CJD-5	50	13	25	13	90	7240
MH4M36CJD-6	60	15	30	15	110	5920
MH4M36CJD-7	70	20	35	20	130	5200

- **Utilizes industry standard 4M X 4 DRAMs in TSOP package and 4M X 1 DRAMs in TSOP package**
- **Single 5V ± 10%supply**
- **Low stand-by power dissipation**
  - **66mW (Max) . . . . . CMOS Input level**
- **Low operating power dissipation**
  - **MH4M36CJD - 5 . . . . . 9.15W (Max)**
  - **MH4M36CJD - 6 . . . . . 7.48W (Max)**
  - **MH4M36CJD - 7 . . . . . 6.51W (Max)**
- **All inputs, output TTL compatible and low capacitance**
- **2048 refresh cycles every 32ms (A_0 ~ A_{10})**
- **Includes 12 0.22uF decoupling capacitors**

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



FUNCTION

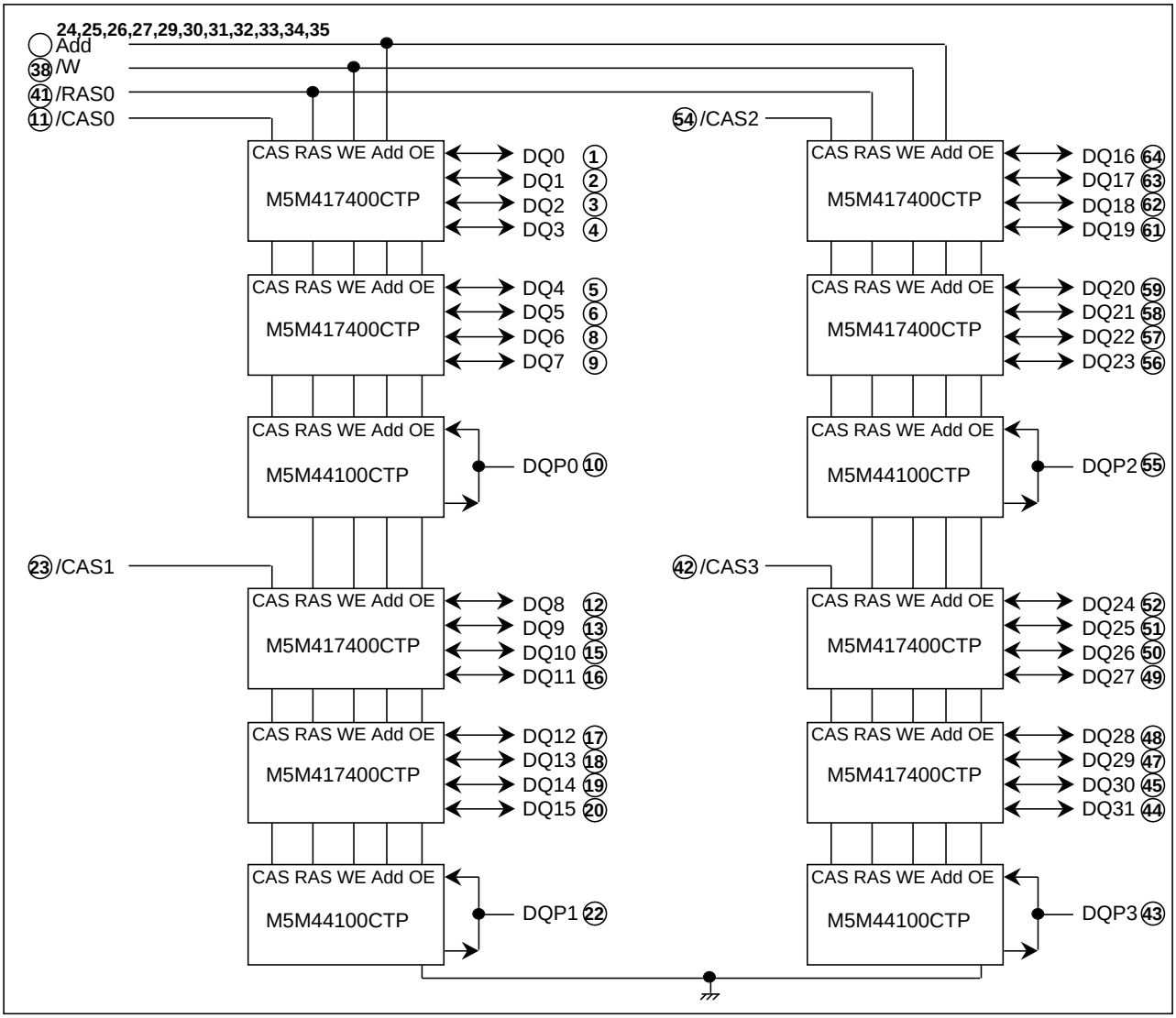
The MH4M36CJD provide, in addition to normal read and write a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	APD	OPN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1 ~ 7	V
VI	Input voltage		-1 ~ 7	V
V0	Output voltage		-1 ~ 7	V
I0	Output current		50	mA
Pd	Power dissipation	Ta=25°C	12	W
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70 °C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1.0		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≤ V_{OUT} ≤ 5.5V	-10		10	uA
I_I	Input current		0V ≤ V_{IN} ≤ 6.0V, Other inputs pins=0V	-120		120	uA
$I_{CC1\ (AV)}$	Average supply current from Vcc operating (Note 3,4)	MH4M36CJD-5	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			1660	mA
		MH4M36CJD-6				1360	
		MH4M36CJD-7				1180	
I_{CC2}	Supply current from Vcc , stand-by		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			24	mA
			$\overline{RAS}$= $\overline{CAS}$ ≥ Vcc -0.5			12	
$I_{CC3\ (AV)}$	Average supply current from Vcc refreshing (Note 3)	MH4M36CJD-5	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			1660	mA
		MH4M36CJD-6				1360	
		MH4M36CJD-7				1180	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	MH4M36CJD-5	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			1060	mA
		MH4M36CJD-6				900	
		MH4M36CJD-7				780	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	MH4M36CJD-5	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			1580	mA
		MH4M36CJD-6				1300	
		MH4M36CJD-7				1140	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc3 (AV) , Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0 ~ 70 °C , Vcc=5V ± 10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I\ (A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz Vi=25mVrms			90	pF
$C_{I\ (\overline{W})}$	Input capacitance, write control input				130	pF
$C_{I\ (\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				130	pF
$C_{I\ (\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				35	pF
$C_{I/O}$	Input/Output capacitance, data ports				20	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted , see notes 5,12,13)

Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$ (Note 6,7)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 6,8)		50		60		70	ns
t_{AA}	Columu address access time (Note 6,9)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (Note 6,10)		30		35		40	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low (Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note 11)	0	13	0	15	0	15	ns

Note 5: An initial pause of 500us is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 32 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assumes that tRCD ≥ tRCD(max) and tASC ≥ tASC(max).
8: Assumes that tRCD ≤ tRCD(max) and tRAD ≤ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
9: Assumes that tRAD ≥ tRAD(max) and tASC ≤ tASC(max).
10: Assumes that tCP ≤ tCP(max) and tASC ≥ tASC(max).
11: tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (| IOUT | ≤ 10 uA) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted See notes 12,13)

Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time		32		32		32	ms
t_{RP}	$\overline{RAS}$ high pulse width	30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note14)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note15)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note16)	0	10	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	13		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low (Note17)	0		0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data (Note18)	13		15		15		ns
t_T	Transition time (Note19)	1	50	1	50	1	50	ns

Note 12: The timing requirements are assumed tT =5ns.
13: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
14: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tH+tASC(min).
15: tRAD(max) is specified as a reference point only. If tRAD ≥ tRAD(max) and tASC ≤ tASC(max), access time is controlled exclusively by tAA.
16: tASC(max) is specified as a reference point only. If tRCD ≥ tRCD(max) and tASC ≥ tASC(max), access time is controlled exclusively by tCAC.
17: Either tDZC or tDZO must be satisfied.
18: Either tCDD or tODD must be satisfied.
19: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ iow pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ iow pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ iow	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ iow	13		15		20		ns
t_{RCS}	Read Setup time after $\overline{CAS}$ high	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ iow (Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ iow (Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	25		30		35		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle

Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ iow pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ iow pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ iow	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ iow	13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ iow	8		10		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ iow	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ iow	13		15		20		ns
t_{WP}	Write pulse width	8		10		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ iow or $\overline{W}$ iow	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ iow or $\overline{W}$ iow	8		10		15		ns

Fast-Page Mode Cycle (Read, Early Write Cycle) (Note 21)

Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	40		45		50		ns
t_{RAS}	$\overline{RAS}$ iow pulse width for read write cycle (Note22)	95	125000	110	125000	125	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note23)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		45		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ iow	53		60		65		ns

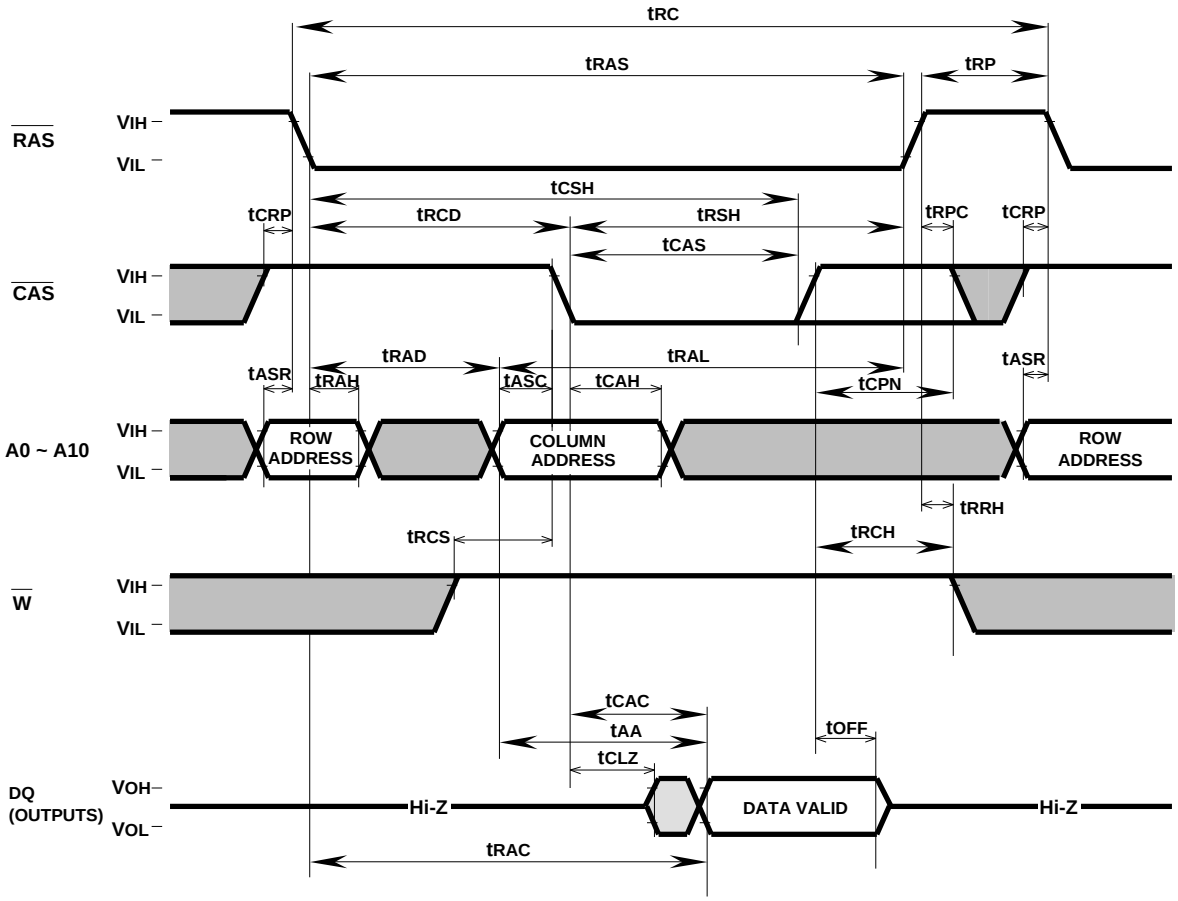
Note 21: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
22: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
23: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 24)

Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 24: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 25)
Read Cycle

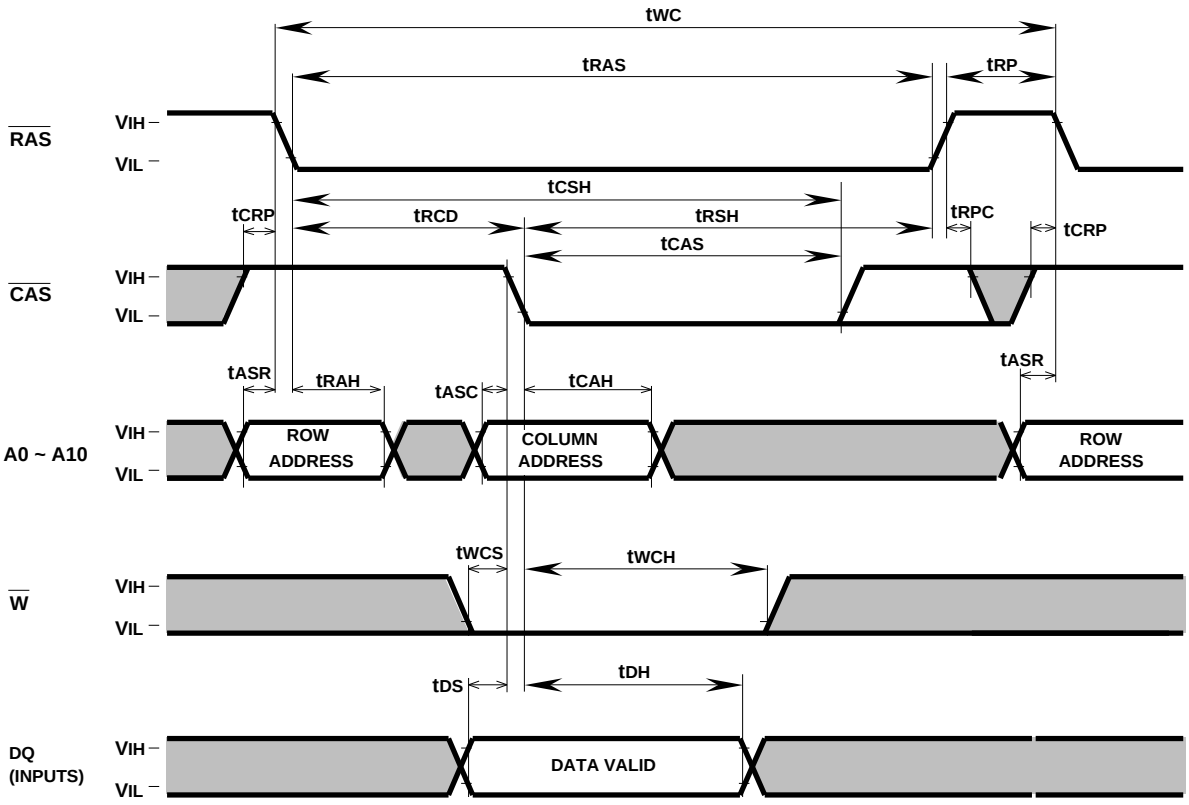


Note 25

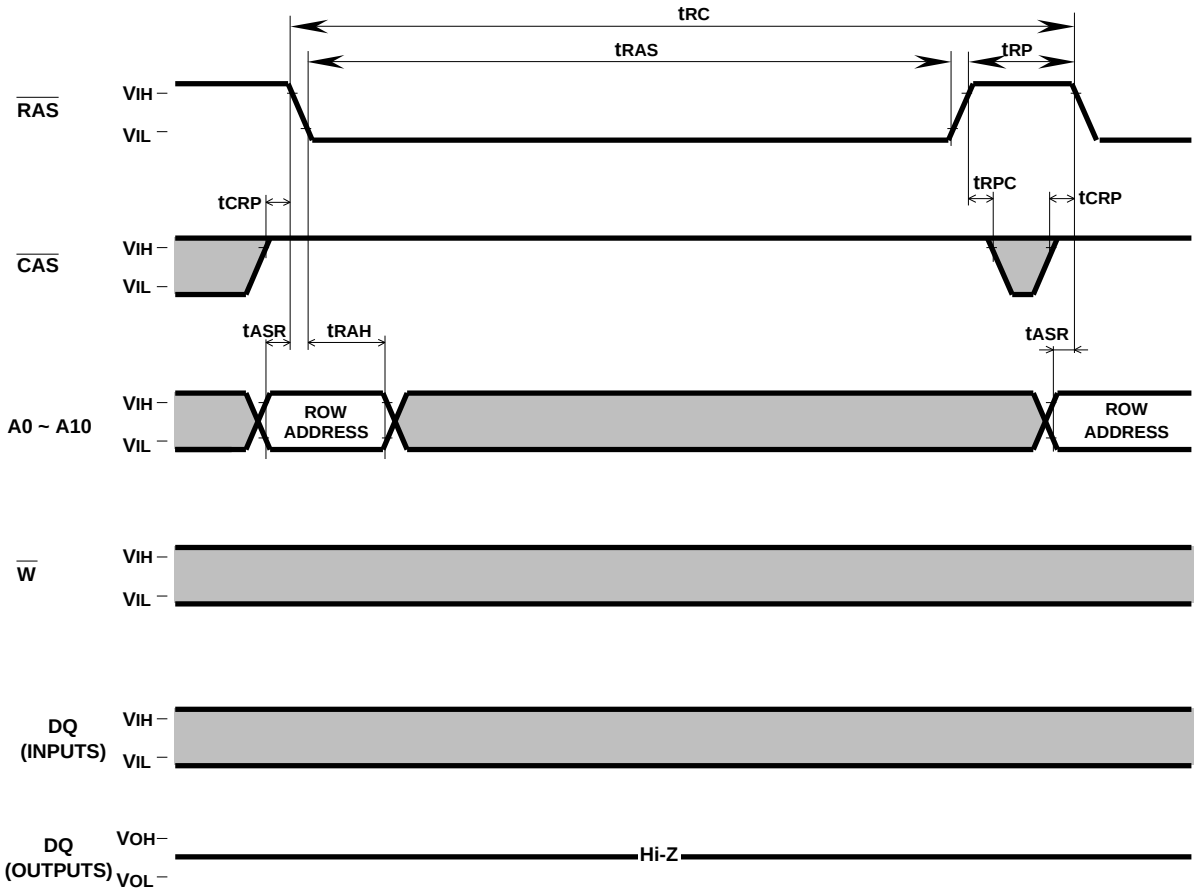
Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

Indicates the invalid output.

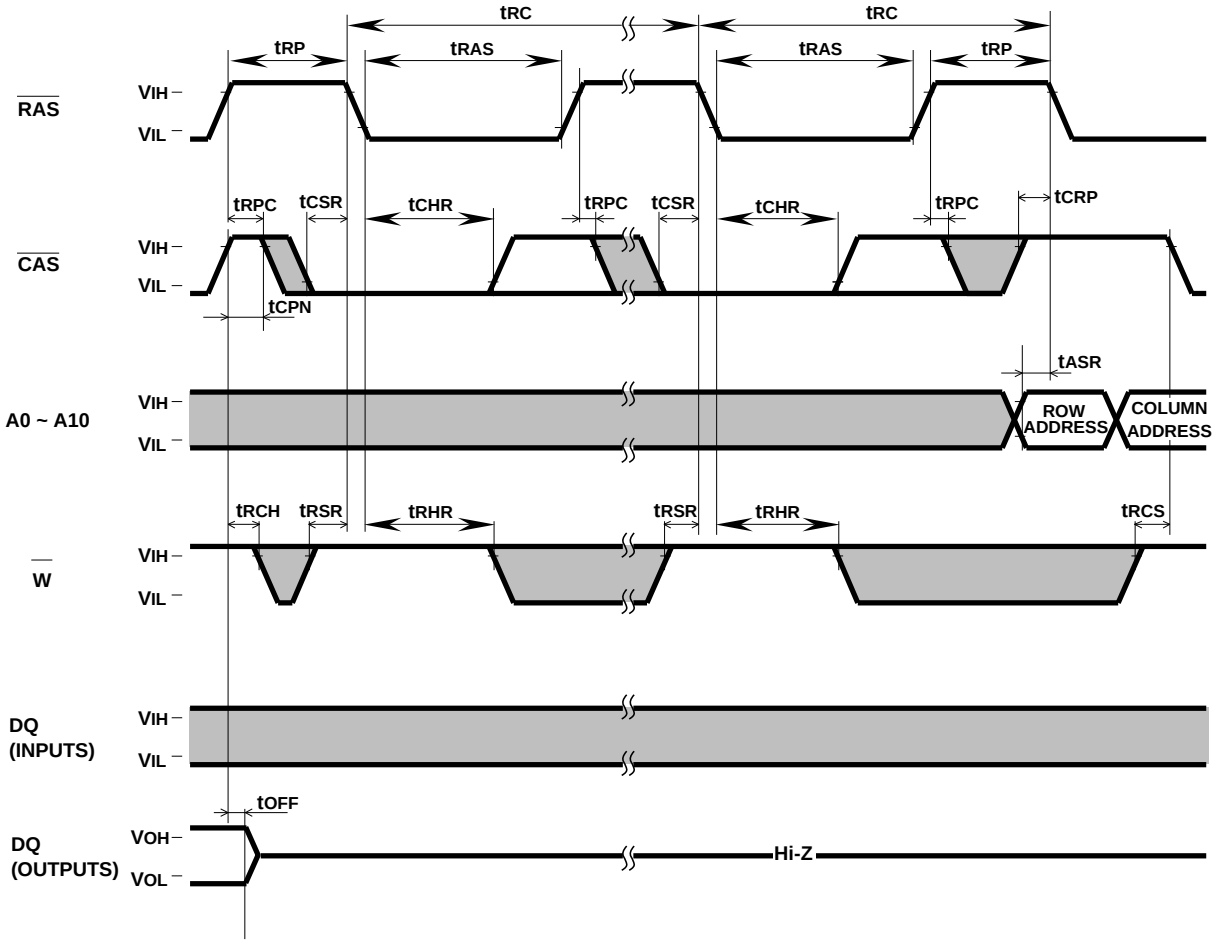
Write Cycle (Early write)



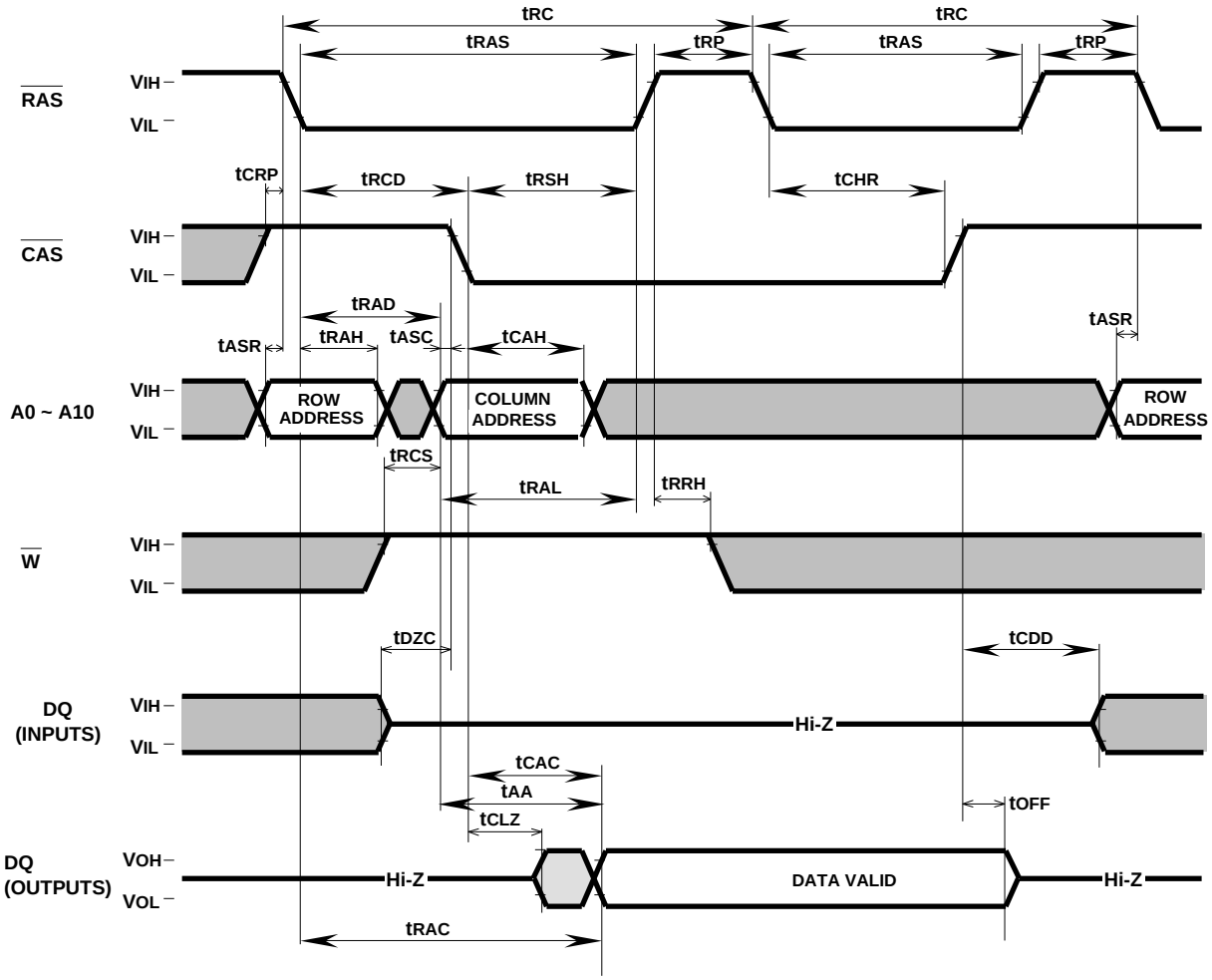
$\overline{\text{RAS}}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

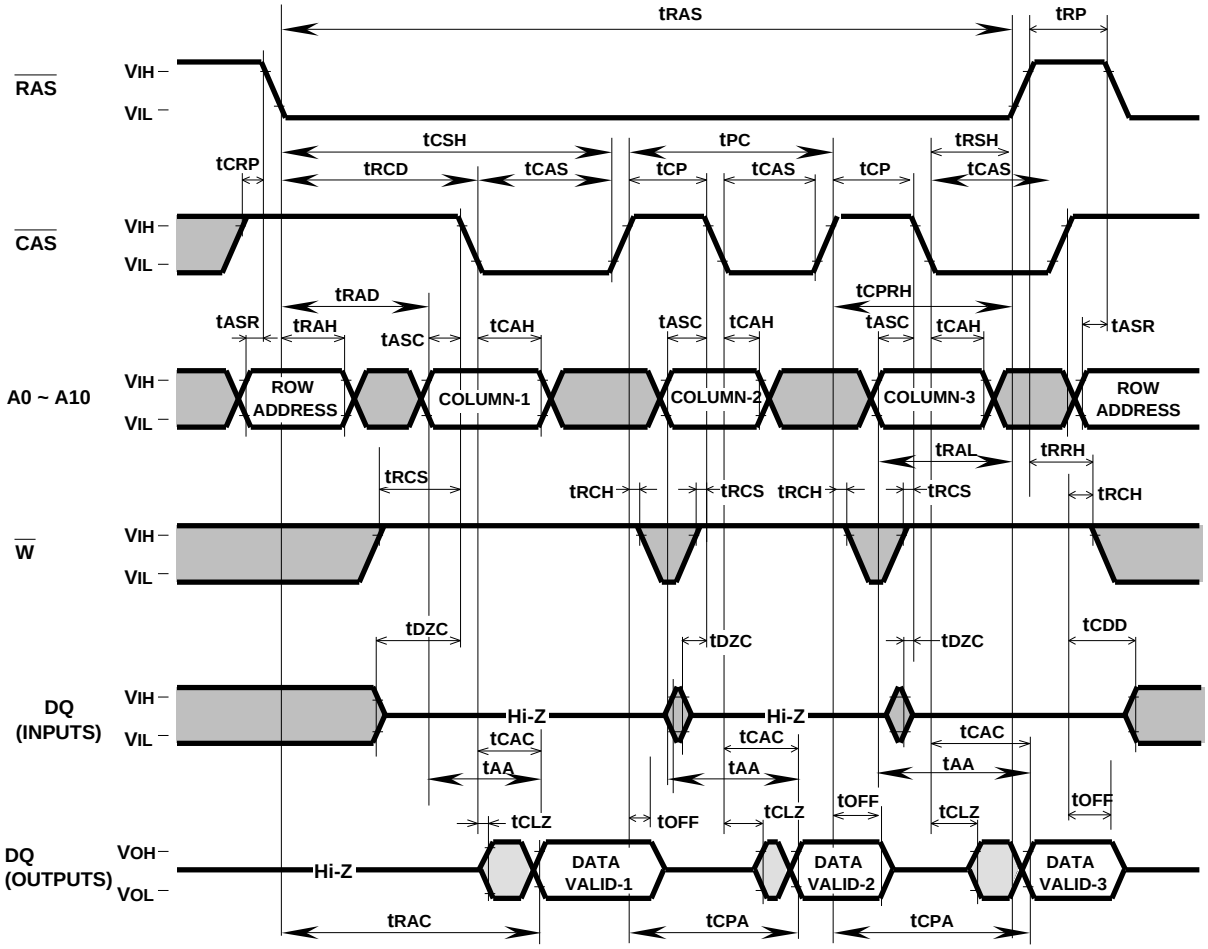


Hidden Refresh Cycle (Read) (Note 26)

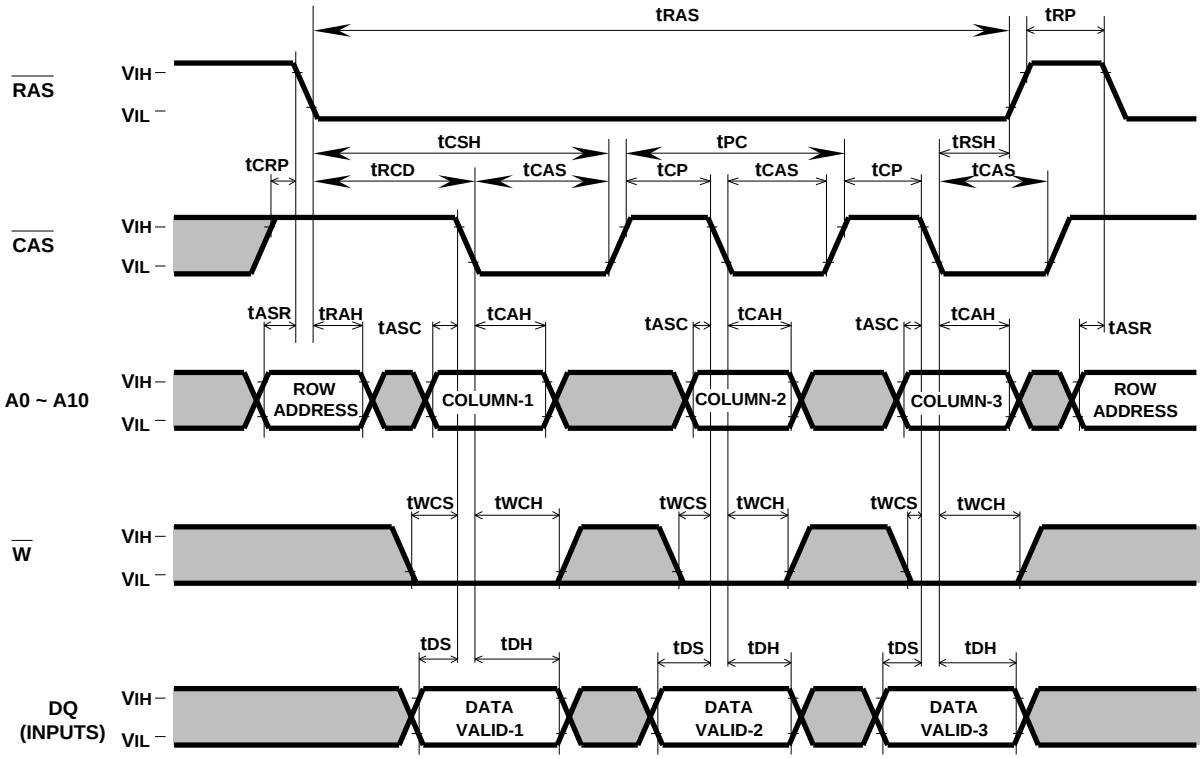


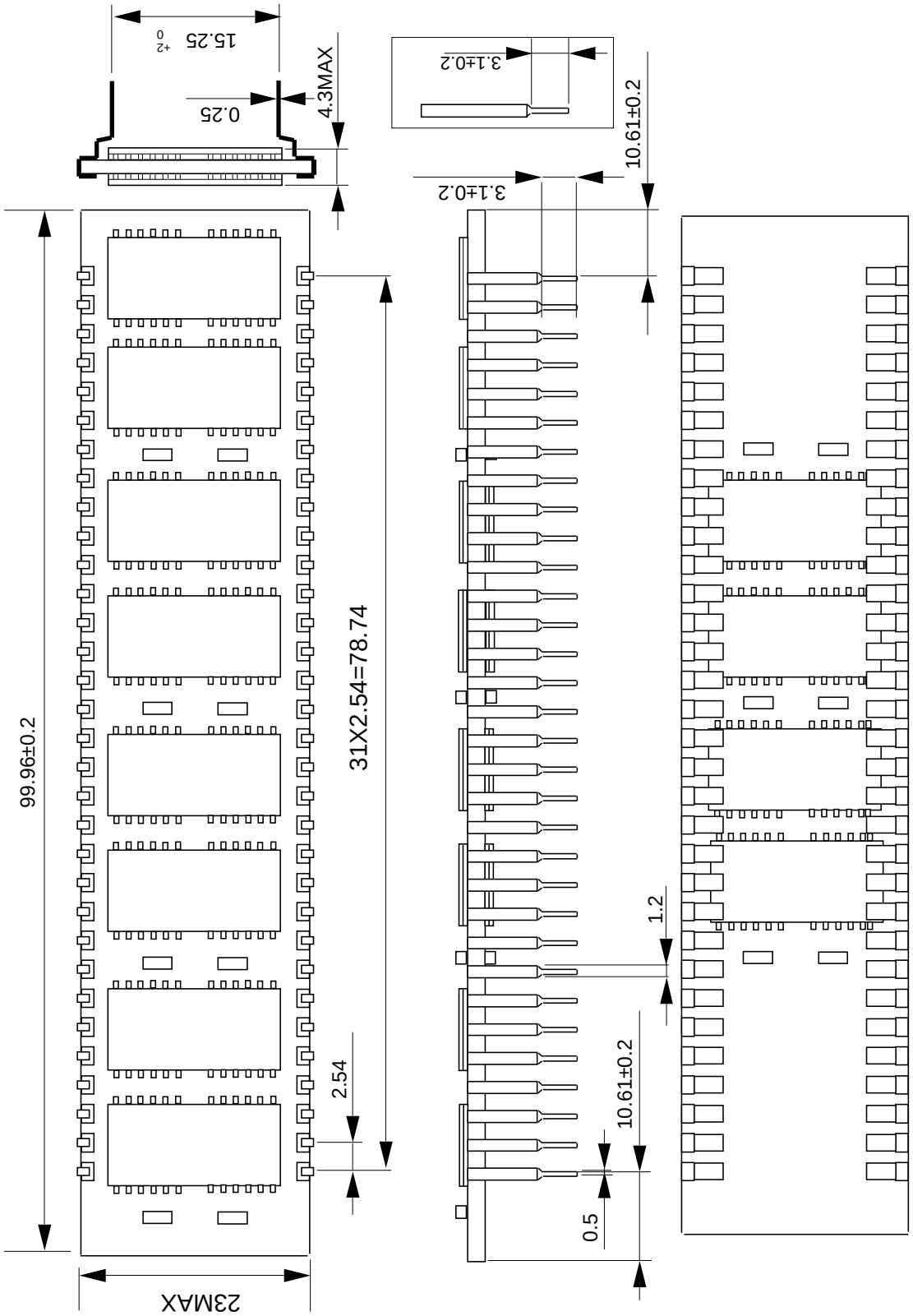
Note 26: Early write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)




15.25 +2 0
0.25
4.3MAX
3.1±0.2
10.61±0.2
3.1±0.2
99.96±0.2
31X2.54=78.74
1.2
2.54
10.61±0.2
0.5
23MAX