FAIRCHILD SEMICONDUCTOR™

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PRELIMINARY

ML4805

Variable Feedforward PFC/PWM Controller Combo

GENERAL DESCRIPTION

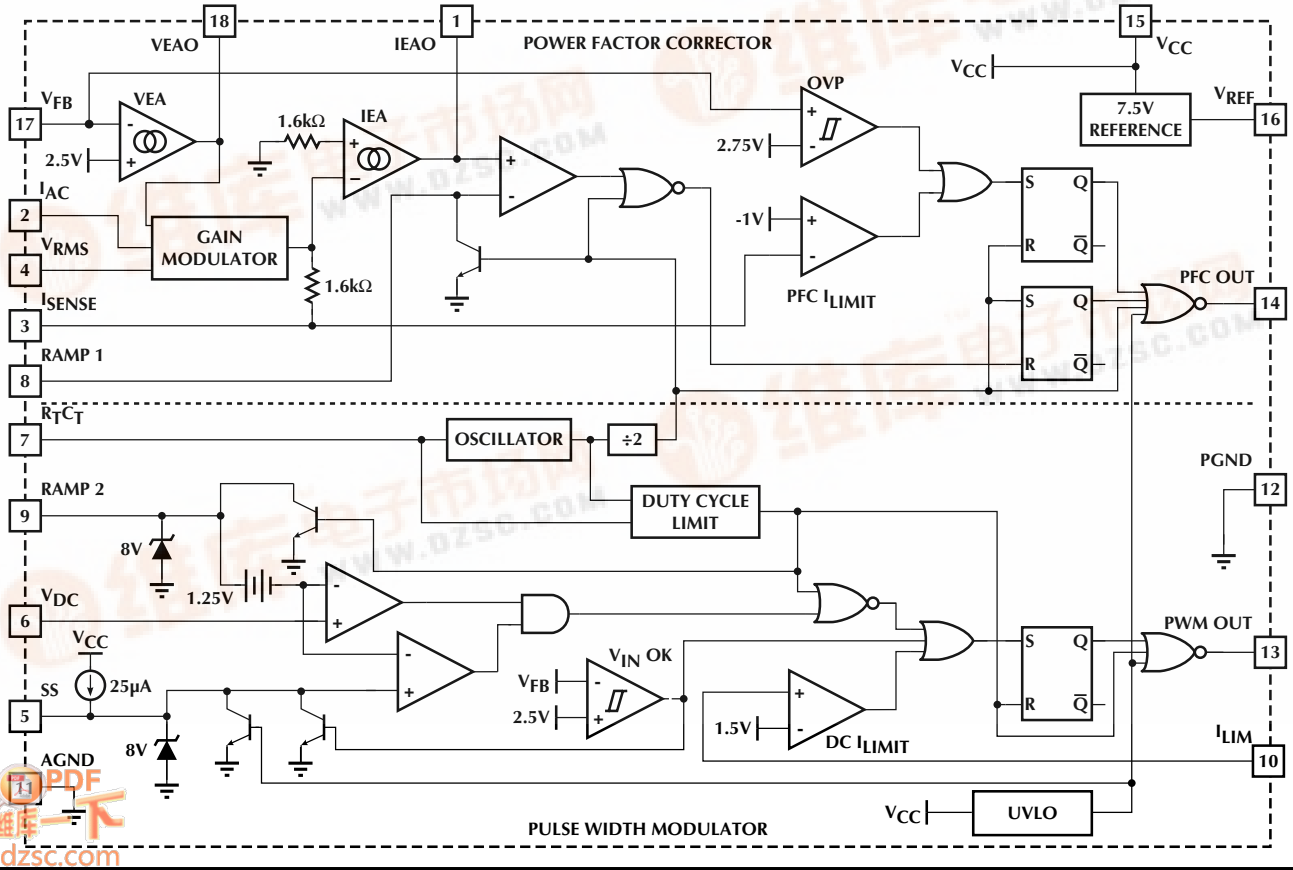
The ML4805 is a controller for power factor corrected, switched mode power supplies. Similar to the ML4801, the ML4805 may be used for voltage mode operation. Key features of this combined PFC and PWM controller are low start-up and operating currents. Power Factor Correction (PFC) allows the use of smaller, lower cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply that fully complies with IEC1000-2-3 specifications. The ML4805 includes circuits for the implementation of a leading edge, average current "boost" type power factor correction and a trailing edge pulse width modulator.

The PFC frequency of the ML4805 is automatically set at half that of the PWM frequency generated by the internal oscillator. This technique allows the user to design with smaller output components while maintaining the optimum operating frequency for the PFC. An over-voltage comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting and input voltage brown-out protection.

FEATURES

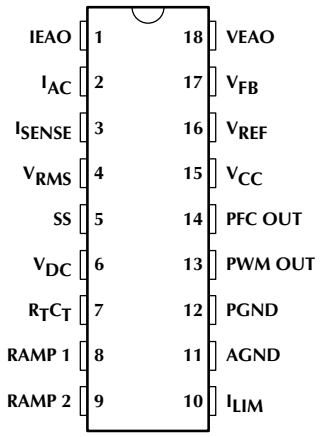
- Internally synchronized PFC and PWM in one IC
- Low start-up current (200µA typ.)
- Low operating current (5.5mA typ.)
- Low total harmonic distortion
- Reduces ripple current in the storage capacitor between the PFC and PWM sections
- Average current continuous boost leading edge PFC
- High efficiency trailing edge PWM optimized for voltage mode operation
- Current fed gain modulator for improved noise immunity
- Brown-out control, overvoltage protection, UVLO, and soft start

BLOCK DIAGRAM



PIN CONFIGURATION

ML4805
18-Pin PDIP (P18)
18-Pin SOIC (S18)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	IEAO	PFC transconductance current error amplifier output
2	I_{AC}	PFC gain control reference input
3	I_{SENSE}	Current sense input to the PFC current limit comparator
4	V_{RMS}	Input for PFC RMS line voltage compensation
5	SS	Connection point for the PWM soft start capacitor
6	V_{DC}	PWM voltage feedback input
7	R_TC_T	Connection for oscillator frequency setting components
8	RAMP 1	PFC ramp input
9	RAMP 2	PWM ramp sense input
10	ILIM	PWM current limit sense input
11	AGND	Analog ground
12	PGND	Power ground
13	PWM OUT	PWM driver output
14	PFC OUT	PFC driver output
15	V_{CC}	Positive supply (connected to an internal shunt regulator).
16	V_{REF}	Buffered output for the internal 7.5V reference
17	V_{FB}	PFC transconductance voltage error amplifier input
18	VEAO	PFC transconductance voltage error amplifier output

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} 18V
I_{SENSE} Voltage ..... -3V to 5V
Voltage on Any Other Pin ..... GND - 0.3V to V_{CC} + 0.3V
I_{REF} 20mA
I_{AC} Input Current 10mA
Peak PFC OUT Current, Source or Sink 500mA
Peak PWM OUT Current, Source or Sink 500mA
PFC OUT, PWM OUT Energy Per Cycle 1.5µJ

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C
Thermal Resistance (θ_{JA})
Plastic DIP ..... 70°C/W
Plastic SOIC ..... 100°C/W

OPERATING CONDITIONS

Temperature Range
ML4805CX ..... 0°C to 70°C
ML4805IX ..... -40°C to 85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 15V, R_T = 29.4kΩ, R_{RAMP1} = 15.4kΩ, C_T = 270pF, C_{RAMP1} = 620pF, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE ERROR AMPLIFIER						
	Input Voltage Range		0		5	V
	Transconductance	$V_{NON\ INV} = V_{INV}$, VEAO = 3.75V	40	65	80	µ℧
	Feedback Reference Voltage		2.43	2.50	2.57	V
	Input Bias Current	Note 2		-0.5	-1.0	µA
	Output High Voltage		6.0	6.7		V
	Output Low Voltage			0.1	0.4	V
	Source Current	ΔV_{IN} = ±0.5V, V_{OUT} = 6V	-40	-70	-150	µA
	Sink Current	ΔV_{IN} = ±0.5V, V_{OUT} = 1.5V	40	70	150	µA
	Open Loop Gain		60	70		dB
	PSRR	11V < V_{CC} < 16.5V	60	70		dB
CURRENT ERROR AMPLIFIER						
	Input Voltage Range		-1.5		2	V
	Transconductance	$V_{NON\ INV} = V_{INV}$, VEAO = 3.75V	60	100	120	µ℧
	Input Offset Voltage		0	8	15	mV
	Input Bias Current			-0.5	-1.0	µA
	Output High Voltage		6.0	6.7		V
	Output Low Voltage			0.65	1.0	V
	Source Current	ΔV_{IN} = ±0.5V, V_{OUT} = 6V	-40	-70	-150	µA
	Sink Current	ΔV_{IN} = ±0.5V, V_{OUT} = 1.5V	40	70	150	µA
	Open Loop Gain		55	65		dB
	PSRR	11V < V_{CC} < 16.5V	60	75		dB

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVP COMPARATOR						
	Threshold Voltage		2.65	2.75	2.85	V
	Hysteresis		175	250	325	mV
PFC I_{LIMIT} COMPARATOR						
	Threshold Voltage		-0.9	-1.0	-1.1	V
	ΔPFC I_{LIMIT} Threshold - Gain Modulator Output		120	220		mV
	Delay to Output			150	300	ns
DC I_{LIMIT} COMPARATOR						
	Threshold Voltage		1.4	1.5	1.6	V
	Input Bias Current			±0.3	±1	µA
	Delay to Output			150	300	ns
V_{IN} OK COMPARATOR						
	Threshold Voltage		2.4	2.5	2.6	V
	Hysteresis		0.8	1.0	1.2	V
GAIN MODULATOR						
	Gain (Note 3)	I_{AC} = 100µA, V_{RMS} = V_{FB} = 0V	0.65	0.85	1.05	
		I_{AC} = 50µA, V_{RMS} = 1V, V_{FB} = 0V	1.90	2.20	2.40	
		I_{AC} = 50µA, V_{RMS} = 1.8V, V_{FB} = 0V	0.90	1.05	1.25	
		I_{AC} = 100µA, V_{RMS} = 3.3V, V_{FB} = 0V	0.20	0.30	0.40	
	Bandwidth	IAC = 100µA		10		MHz
	Output Voltage	I_{AC} = 350µA, V_{RMS} = 1V, V_{FB} = 0V	0.65	0.75	0.85	V
OSCILLATOR						
	Initial Accuracy	T_A = 25ºC	188	200	212	kHz
	Voltage Stability	11V < V_{CC} < 16.5V		1		%
	Temperature Stability			2		%
	Total Variation	Line, Temp	182		218	kHz
	Ramp Valley to Peak Voltage			2.5		V
	PFC Dead Time		350	470	600	ns
	C_T Discharge Current	$V_{RAMP\ 2}$ = 0V, $V_{RAMP\ 1}$ = 2.5V	3.5	5.5	7.5	mA

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
	Output Voltage	T_A = 25ºC, I(V_{REF}) = 1mA	7.4	7.5	7.6	V
	Line Regulation	11V < V_{CC} < 16.5V		10	25	mV
	Load Regulation	1mA < I(V_{REF}) < 10mA		10	20	mV
	Temperature Stability			0.4		%
	Total Variation	Line, Load, Temp	7.35		7.65	V
	Long Term Stability	T_J = 125ºC, 1000 Hours		5	25	mV
PFC						
	Minimum Duty Cycle	V_{IEAO} > 6.7V			0	%
	Maximum Duty Cycle	V_{IEAO} < 1.2V	90	95		%
	Output Low Voltage	I_{OUT} = -20mA		0.4	0.8	V
		I_{OUT} = -100mA		0.7	2.0	V
		I_{OUT} = -10mA, V_{CC} = 9V		0.4	0.8	V
	Output High Voltage	I_{OUT} = 20mA	V_{CC} - 0.8			V
		I_{OUT} = 100mA	V_{CC} - 2.0			V
	Rise/Fall Time	C_L = 1000pF		50		ns
PWM						
DC	Duty Cycle Range		0-44	0-47	0-50	%
V_{OL}	Output Low Voltage	I_{OUT} = -20mA		0.4	0.8	V
		I_{OUT} = -100mA		0.7	2.0	V
		I_{OUT} = -10mA, V_{CC} = 9V		0.4	0.8	V
V_{OH}	Output High Voltage	I_{OUT} = 20mA	V_{CC} - 0. 8			V
		I_{OUT} = 100mA	V_{CC} - 2.0			V
	Rise/Fall Time	C_L = 1000pF		50		ns
SUPPLY						
	Start-up Current	V_{CC} = 12V, C_L = 0		200	350	µA
	Operating Current	V_{CC} = 14V, C_L = 0		5.5	7.0	mA
	Undervoltage Lockout Threshold		12.4	13.0	13.6	V
	Undervoltage Lockout Hysteresis		2.7	3.0	3.3	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Includes all bias currents to other circuits connected to the V_{FB} pin.

Note 3: Gain = K x 5.3V; K = (I_{MULO} - I_{OFFSET}) x I_{AC} x (VEAO - 0.625V)$^{-1}$.

FUNCTIONAL DESCRIPTION

The ML4805 consists of a combined average-current-controlled, continuous boost Power Factor Corrector (PFC) front end and a synchronized Pulse Width Modulator (PWM) back end. It is distinguished from earlier combo controllers by its dramatically reduced start-up and operating currents. The PWM section can be used in either current or voltage mode. In voltage mode, feedforward from the PFC output buss can be used to improve the PWM's line regulation. In either mode, the PWM stage uses conventional trailing-edge duty cycle modulation, while the PFC uses leading-edge modulation. This patented leading/trailing edge modulation technique results in a higher useable PFC error amplifier bandwidth, and can significantly reduce the size of the PFC DC buss capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the reduced ripple on the PFC output capacitor (the PWM input capacitor). The PWM section of the ML4805 runs at twice the frequency of the PFC, which allows the use of smaller PWM output magnetics and filter capacitors while holding down the losses in the PFC stage power components.

In addition to power factor correction, a number of protection features have been built into the ML4805. These include soft-start, PFC over-voltage protection, peak current limiting, brown-out protection, duty cycle limit, and under-voltage lockout.

POWER FACTOR CORRECTION

Power factor correction makes a non-linear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with, and proportional to, the line voltage, so the power factor is unity (one). A common class of non-linear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect which occurs on the input filter capacitor in such a supply causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such a supply presents a power factor to the line of less than one (another way to state this is that it causes significant current harmonics to appear at its input). If the input current drawn by such a supply (or any other non-linear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To maintain the input current of a device drawing power from the AC line in phase with, and proportional to, the input voltage, a way must be found to cause that device to load the line in proportion to the instantaneous line voltage. The PFC section of the ML4805 uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage.

No filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges, at twice line frequency, from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current which the converter draws from the power line matches the instantaneous line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VDC, to allow for a high line of $270VAC_{rms}$. The other condition is that the current which the converter is allowed to draw from the line at any given instant must be proportional to the line voltage. The first of these requirements is satisfied by establishing a suitable voltage control loop for the converter, which sets an average operating current level for a current error amplifier and switching output driver. The second requirement is met by using the rectified AC line voltage to modulate the input of the current control loop. Such modulation causes the current error amplifier to command a power stage current which varies directly with the input voltage. In order to prevent ripple which will necessarily appear at the output of the boost circuit (typically about 10VAC on a 385V DC level), from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC such to be proportional to $1/V_{IN}^2$, which linearizes the transfer function of the system as the AC input voltage varies.

Since the boost converter topology in the ML4805 PFC is of the current-averaging type, no slope compensation is required.

PFC SECTION

Gain Modulator

Figure 1 shows a block diagram of the PFC section of the ML4805. The gain modulator is the heart of the PFC, as it is this circuit block which controls the response of the current loop to line voltage waveform and frequency, rms line voltage, and PFC output voltage. There are three inputs to the gain modulator. These are:

1) A current representing the instantaneous input voltage (amplitude and waveshape) to the PFC. The rectified AC input sine wave is converted to a proportional current via an external resistor and is then fed into the gain modulator at I_{AC}. Sampling current in this way minimizes ground noise, as is required in high power switching power conversion environments. The gain modulator responds linearly to this current.

2) A voltage proportional to the long-term rms AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at V_{RMS}. The gain modulator's output is

FUNCTIONAL DESCRIPTION (Continued)

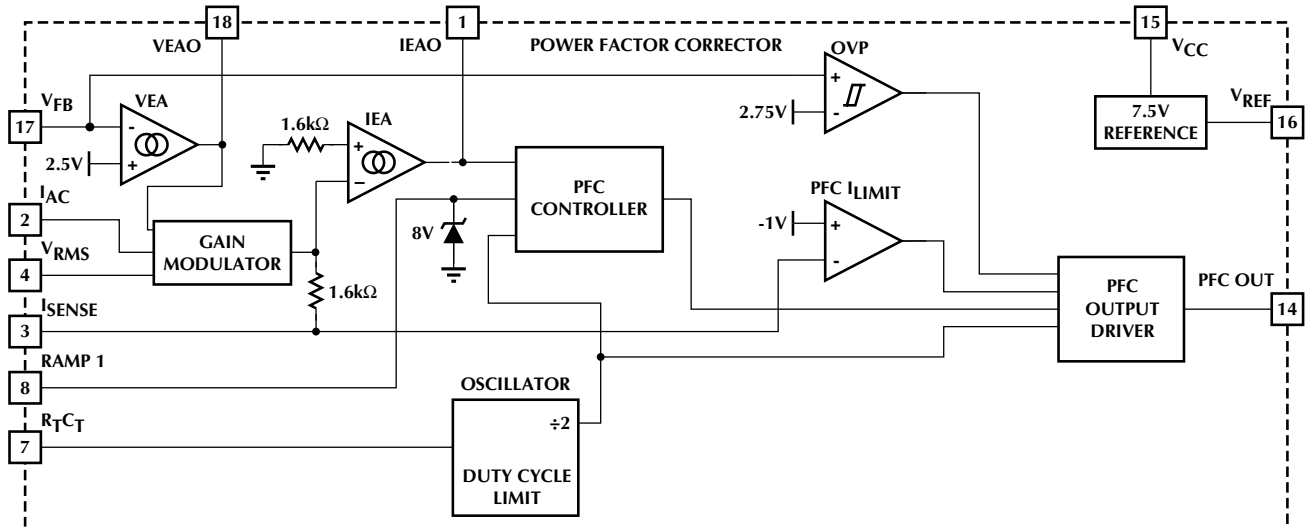


Figure 1. PFC Section Block Diagram

inversely proportional to V_{RMS}^2 (except at unusually low values of V_{RMS} where special gain contouring takes over to limit power dissipation of the circuit components under heavy brownout conditions). The relationship between V_{RMS} and gain is designated as K.

3) The output of the voltage error amplifier, VEAO. The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual-ground (negative) input of the current error amplifier. In this way the gain modulator forms the reference for the current error loop, and ultimately controls the instantaneous current draw of the PFC from the power line. The general form for the output of the gain modulator is:

$$I_{GAINMOD} = \frac{I_{AC} \times VEAO}{V_{RMS}^2} \times 1V$$

More exactly, the output current of the gain modulator is given by:

$$I_{GAINMOD} = K \times (VEAO - 0.625V) \times I_{AC} \quad (1)$$

where K is in units of V^{-1}.

Note that the output current of the gain modulator is limited to ≅ 500µA.

Current Error Amplifier

The current error amplifier's output controls the PFC duty cycle to keep the current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current which results from a negative voltage being impressed upon the I_{SENSE} pin (current into $I_{SENSE} \cong V_{SENSE}/1.6k\Omega$). The negative voltage on I_{SENSE} represents the sum of all currents flowing in the PFC circuit, and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier. In higher power applications, two current transformers are sometimes used, one to monitor the I_D of the boost MOSFET(s) and one to monitor the I_F of the boost diode. As stated above, the inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator will cause the output stage to increase its duty cycle until the voltage on I_{SENSE} is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle will decrease to achieve a less negative voltage on the I_{SENSE} pin.

Cycle-By-Cycle Current Limiter

The I_{SENSE} pin, as well as being a part of the current feedback loop, is a direct input to the cycle-by-cycle current limiter for the PFC section. Should the input voltage at this pin ever be more negative than -1V, the output of the PFC will be disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

FUNCTIONAL DESCRIPTION (Continued)

Overvoltage Protection

The OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load should suddenly change. A resistor divider from the high voltage DC output of the PFC is fed to V_{FB}. When the voltage on V_{FB} exceeds 2.75V, the PFC output driver is shut down. The PWM section will continue to operate. The OVP comparator has 250mV of hysteresis, and the PFC will not restart until the voltage at V_{FB} drops below 2.5V. The OVP trip level should be set at a level where the active and passive external power components and the ML4805 are within their safe operating voltages, but not so low as to interfere with the regular operation of the boost voltage regulation loop.

Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor; an increase in input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 2 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current loop compensation is returned to V_{REF} to produce a soft-start characteristic on the PFC: as the reference voltage comes up from zero volts, it creates a differentiated voltage on IEAO which prevents the PFC from immediately demanding a full duty cycle on its boost converter.

There are two major concerns when compensating the voltage loop error amplifier; stability and transient response. Optimizing interaction between transient response and stability requires that the error amplifier's open-loop crossover frequency should be 1/2 that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency). Rapid perturbations in line or load conditions will cause the input to the voltage error amplifier (V_{FB}) to deviate from its 2.5V (nominal) value. If this happens, the transconductance of the voltage error amplifier will increase significantly. This increases the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with a conventional linear gain characteristic. The current amplifier compensation is similar to that of the voltage error amplifier with the exception of the choice of crossover frequency. The crossover frequency of the current amplifier should be at least 10 times that of the voltage amplifier, to prevent interaction with the voltage loop. It should also be limited to less than 1/6th that of the switching frequency, e.g. 16.7kHz for a 100kHz switching frequency.

There is also a degree of gain contouring applied to the transfer characteristic of the current error amplifier, to increase its speed of response to current-loop perturbations. However, the boost inductor will usually be the dominant factor in overall current loop response. Therefore, this contouring is significantly less marked than that of the voltage error amplifier.

For more information on compensating the current and voltage control loops, see Application Notes 33, 34, and 55. Application Note 16 also contains valuable information for the design of this class of PFC.

Oscillator (R_TC_T)

The oscillator frequency is determined by the values of R_T and C_T, which determine the ramp and off-time of the ML4805's master oscillator:

$$f_{OSC} = \frac{1}{t_{RAMP} + t_{DEADTIME}} \quad (2)$$

The deadtime of the oscillator is derived from the following equation:

$$t_{RAMP} = C_T \times R_T \times \ln\left(\frac{V_{REF} - 1.25}{V_{REF} - 3.75}\right) \quad (3)$$

at V_{REF} = 7.5V:

$$t_{RAMP} = C_T \times R_T \times 0.51$$

The ramp of the oscillator may be determined using:

$$t_{DEADTIME} = \frac{2.5V}{5.5mA} \times C_T = 455 \times C_T \quad (4)$$

The deadtime is so small ($t_{RAMP} >> t_{DEADTIME}$) that the

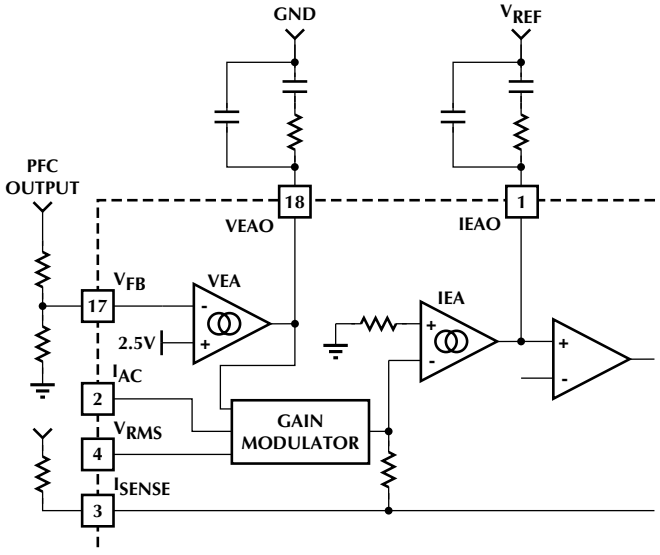


Figure 2. Compensation Network Connections for the Voltage and Current Error Amplifiers

FUNCTIONAL DESCRIPTION (Continued)

operating frequency can typically be approximated by:

$$f_{OSC} = \frac{1}{t_{RAMP}} \quad (5)$$

EXAMPLE:
For the application circuit shown in the data sheet, with the oscillator running at:

$$f_{OSC} = 100kHz = \frac{1}{t_{RAMP}}$$

$$t_{RAMP} = 0.51 \times R_T \times C_T = 1 \times 10^{-5}$$

Solving for R_T x C_T yields 2 x 10^{-4}. Selecting standard components values, C_T = 270pF, and R_T = 36.5kΩ.

PWM SECTION

Pulse Width Modulator

The PWM section of the ML4805 is straightforward, but there are several points which should be noted. Foremost among these is its inherent synchronization to the PFC section of the device. The PWM is capable of current-mode or voltage mode operation. In current-mode applications, the PWM ramp (RAMP 2) is usually derived directly from a current sensing resistor or current transformer in the primary of the output stage, and is thereby representative of the current flowing in the converter's output stage. DC I_{LIMIT}, which provides cycle-by-cycle current limiting, is typically connected to RAMP 2 in such applications. For voltage-mode operation or certain specialized applications, RAMP 2 can be connected to a separate RC timing network to generate a voltage ramp against which V_{DC} will be compared. Under these conditions, the use of voltage feedforward from the PFC buss can assist in line regulation accuracy and response. As in current mode operation, the DC I_{LIMIT} input is used for output stage overcurrent protection.

No voltage error amplifier is included in the PWM stage of the ML4805, as this function is generally performed on the output side of the PWM's isolation boundary. To facilitate the design of optocoupler feedback circuitry, an offset has been built into the PWM's RAMP 2 input which allows V_{DC} to command a zero percent duty cycle for input voltages below 1.25V.

PWM Current Limit

The DC I_{LIMIT} pin is a direct input to the cycle-by-cycle current limiter for the PWM section. Should the input voltage at this pin ever exceed 1.5V, the output of the PWM will be disabled until the output flip-flop is reset by the clock pulse at the start of the next PWM power cycle.

V_{IN} OK Comparator

The V_{IN} OK comparator monitors the DC output of the PFC and inhibits the PWM if this voltage on V_{FB} is less than its nominal 2.5V. Once this voltage reaches 2.5V, which corresponds to the PFC output capacitor being charged to its rated boost voltage, the soft-start commences.

PWM Control (RAMP 2)

When the PWM section is used in current mode, RAMP 2 is generally used as the sampling point for a voltage representing the current in the primary of the PWM's output transformer, derived either by a current sensing resistor or a current transformer. In voltage mode, it is the input for a ramp voltage generated by a second set of timing components (R_{RAMP2}, C_{RAMP2}), which will have a minimum value of zero volts and should have a peak value of approximately 5V. In voltage mode operation, feedforward from the PFC output buss is an excellent way to derive the timing ramp for the PWM stage.

Soft Start

Start-up of the PWM is controlled by the selection of the external capacitor at SS. A current source of 25µA supplies the charging current for the capacitor, and start-up of the PWM begins at 1.25V. Start-up delay can be programmed by the following equation:

$$C_{SS} = t_{DELAY} \times \frac{25\mu A}{1.25V} \quad (6)$$

where C_{SS} is the required soft start capacitance, and t_{DELAY} is the desired start-up delay.

It is important that the time constant of the PWM soft-start allow the PFC time to generate sufficient output power for the PWM section. The PWM start-up delay should be at least 5ms.

Solving for the minimum value of C_{SS}:

$$C_{SS} = 5ms \times \frac{25\mu A}{1.25V} = 100nF$$

In the ML4805, the operating frequency of the PFC section is fixed at 1/2 of the PWM's operating frequency. This is done through the use of a 2:1 digital frequency divider ("T" flip-flop) linking the two functional sections of the IC.

FUNCTIONAL DESCRIPTION (Continued)

Generating V_{CC}

The ML4805 is a voltage-fed part. It requires an external 15V±10% or better Zener shunt voltage regulator, or some other controlled supply, to regulate the voltage supplied to the part at 15V nominal. This allows a low power dissipation while at the same time delivering 13V nominal of gate drive at the PWM OUT and PFC OUT outputs. If using a Zener diode, it is important to limit the current through the Zener to avoid overheating or destroying it. This can be easily done with a single resistor in series with the Vcc pin, returned to a bias supply of typically 18V to 20V. The resistor's value must be chosen to meet the operating current requirement of the ML4805 itself (8.5mA max.) plus the current required by the two gate driver outputs.

EXAMPLE:
With a V_{BIAS} of 20V, a V_{CC} limit of 16.5V (max) and driving a total gate charge of 110nC at 100kHz (1 IRF840 MOSFET and 2 IRF830 MOSFETs), the gate driver current required is:

$$I_{GATEDRIVE} = 100kHz \times 110nC = 11mA$$

$$R_{BIAS} = \frac{20V - 16.5V}{7.5mA + 11mA} = 180\Omega$$

The ML4805 should be locally bypassed with a 10nF and a 1µF ceramic capacitor. In most applications, an electrolytic capacitor of between 100µF and 330µF is also required across the part, both for filtering and as part of the start-up bootstrap circuitry.

LEADING/TRAILING MODULATION

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn on right after the trailing edge of the system clock. The error amplifier output voltage is then compared with the modulating ramp. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned OFF. When the switch is ON, the inductor current will ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 3 shows a typical trailing edge control scheme.

In the case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during the OFF time of the switch. Figure 4 shows a leading edge control scheme.

One of the advantages of this control technique is that it requires only one system clock. Switch 1 (SW1) turns off and switch 2 (SW2) turns on at the same instant to minimize the momentary "no-load" period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using this method.

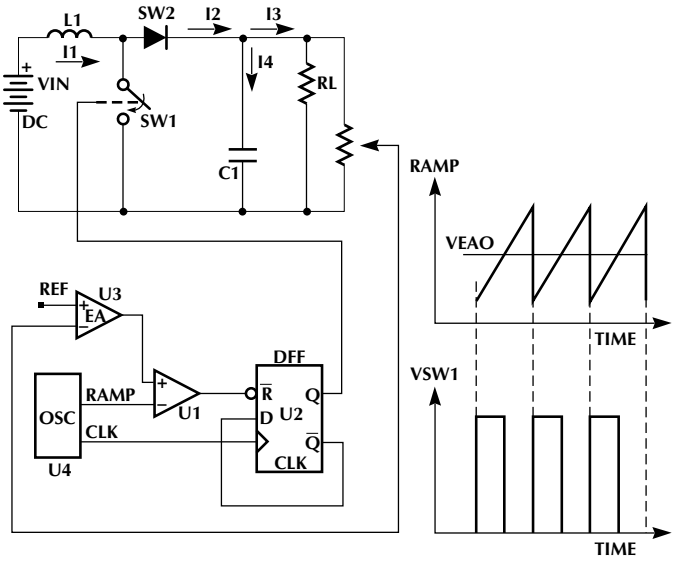


Figure 3. Typical Trailing Edge Control Scheme

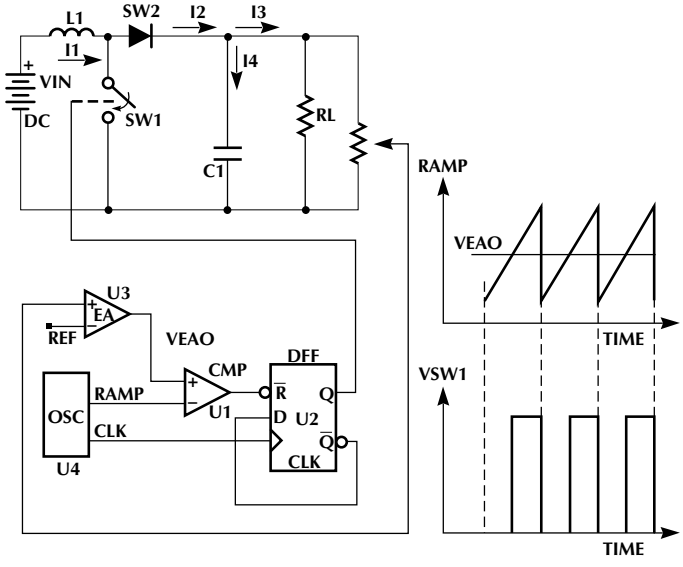


Figure 4. Leading/Trailing Edge Control Scheme

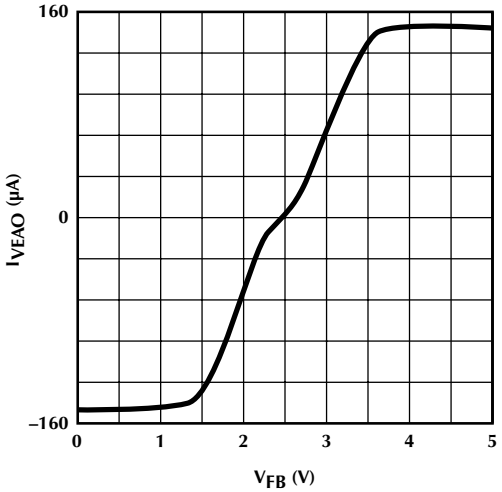


Figure 5. I_{VEAO} vs. V_{FB}

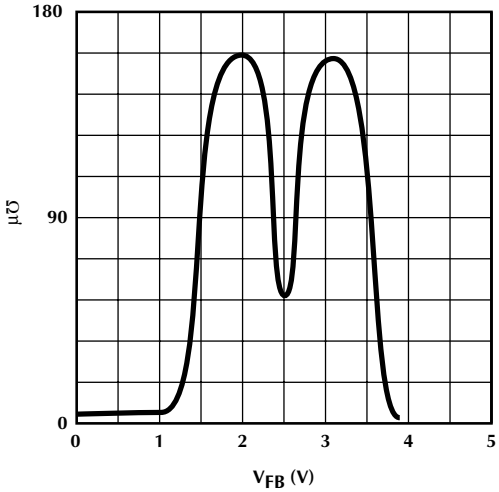


Figure 6. g_M of V_{OTA}

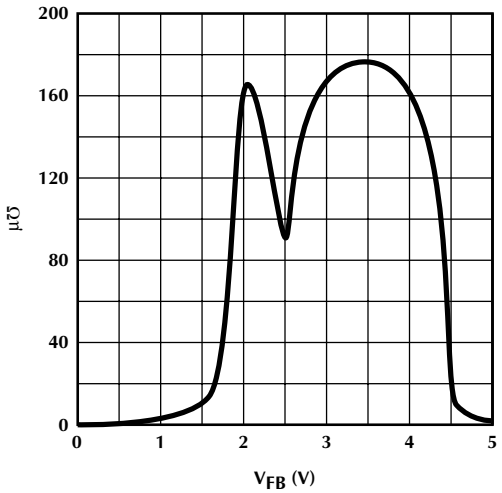


Figure 7. g_M of I_{OTA}

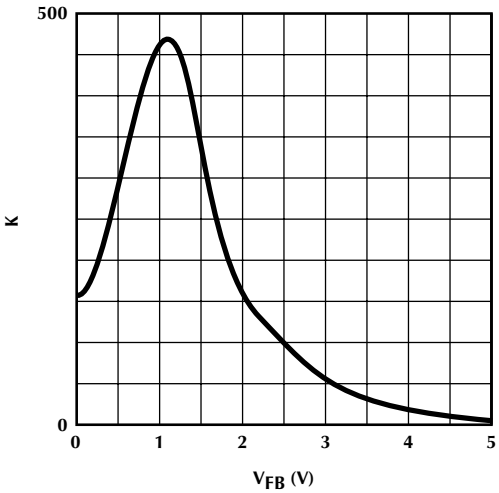
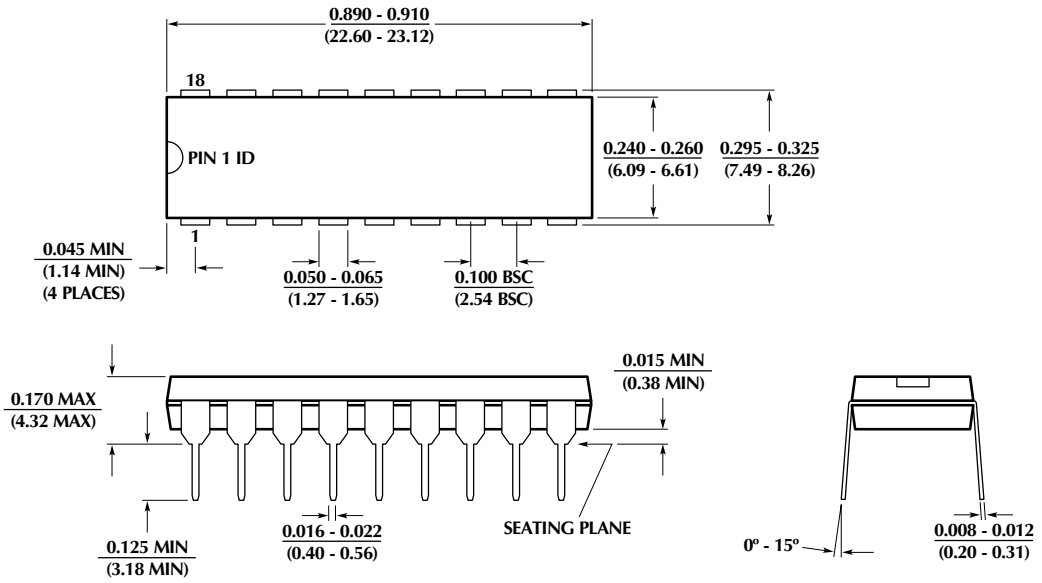


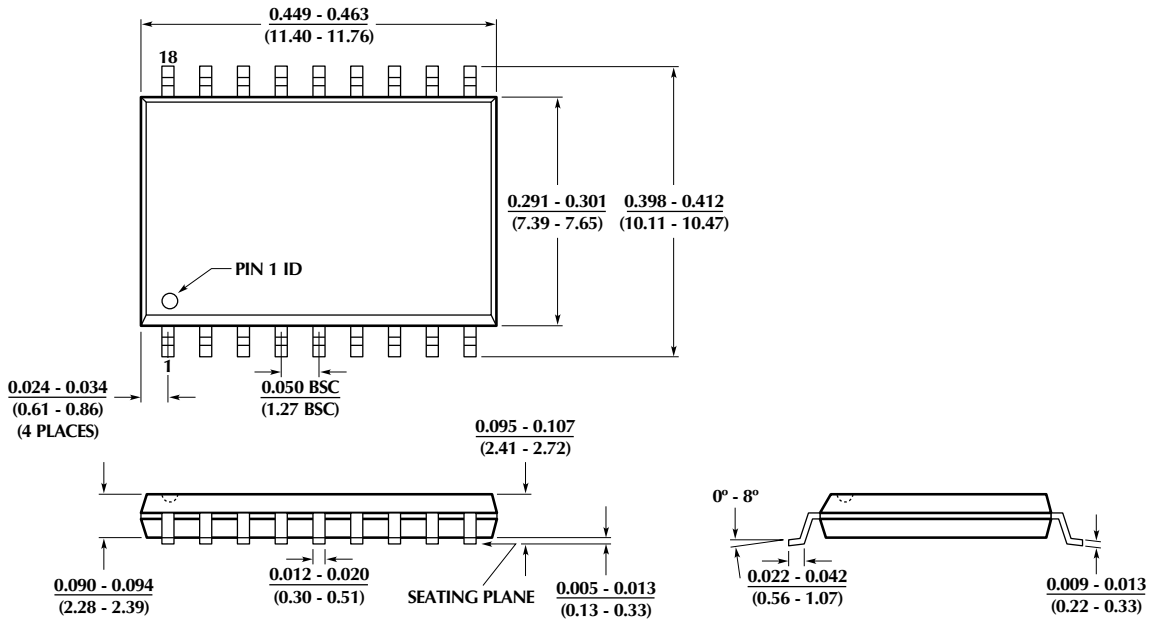
Figure 8. K of Multiplier

PHYSICAL DIMENSIONS inches (millimeters)

Package: P18
18-Pin PDIP



Package: S18
18-Pin SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4805CP	0°C to 70°C	18-Pin Plastic DIP (P18)
ML4805CS	0°C to 70°C	18-Pin Wide SOIC (S18)
ML4805IP	-40°C to 85°C	18-Pin Plastic DIP (P18)
ML4805IS	-40°C to 85°C	18-Pin Wide SOIC (S18)