Regulator+Reset IC
Monolithic IC MM1437

Outline

This IC combines a low saturation 5V regulator, adapted for low power consumption, and a reset function (regulator output monitoring), for which there is significant market need, that uses the built-in 4.2V detection delay circuit.

Features

1. Small input/output voltage difference 0.25V typ.
2. High input voltage 18V max.
3. Internal thermal shutdown circuit.
4. Internal current-limiting circuit.
5. Adjustment-free reset detection voltage 4.2V typ.
6. Easy to set delay time from voltage detection to reset release.

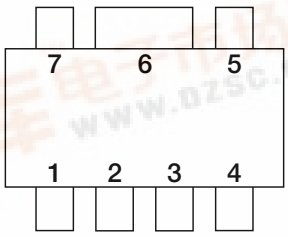
Package

SOP-7
SIP-5

Applications

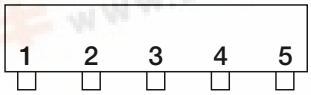
TV, monitors, air conditioners, others.

Pin Assignment



SOP-7

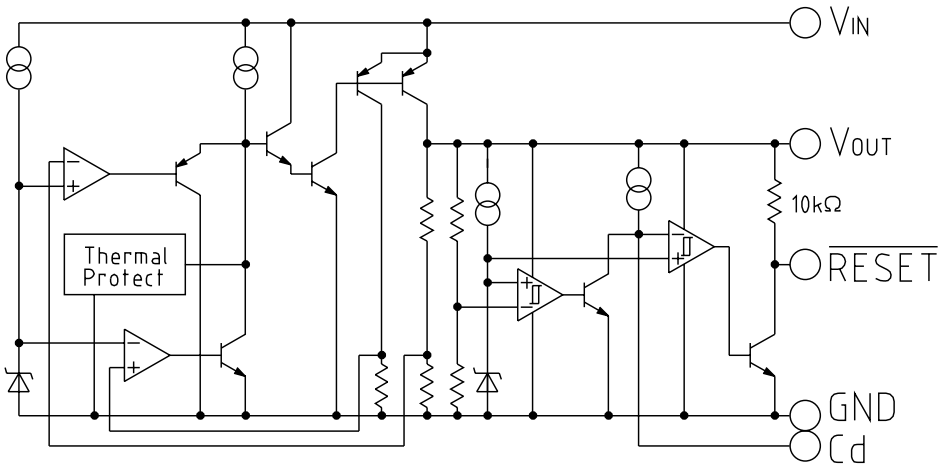
1	GND
2	$\overline{\text{RESET}}$
3	Cd
4	V_{IN}
5	V_{OUT}
6	GND
7	N.C



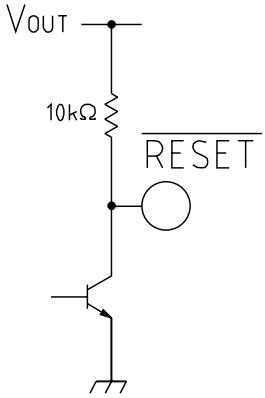
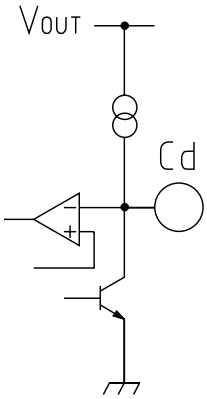
SIP-5

1	$\overline{\text{RESET}}$
2	Cd
3	V_{IN}
4	V_{OUT}
5	GND

Equivalent Circuit Diagram



Pin Description

Pin No.	Pin name	Functions	Equivalent circuit diagram
1 (SOP–7) 5 (SIP–5)	GND	GND pin	
2 (SOP–7) 1 (SIP–5)	$\overline{\text{RESET}}$	Output pin voltage detection output V_{OUT} pin voltage detection output pin $\overline{\text{RESET}}$ pin logic $\overline{\text{RESET}}$: V_{OUT}<Vs → L; V_{OUT}>Vs → H	
3 (SOP–7) 2 (SIP–5)	Cd	Delay time capacitor pin $\overline{\text{RESET}}$ pin output delay time can be set by the capacitance connected to the Cd pin. t_{PLH}= 100000 · C t_{PLH}: transmission delay time [S] C: capacitor value [F]	
4 (SOP–7) 3 (SIP–5)	V_{IN}	Voltage supply input pin	
5 (SOP–7) 4 (SIP–5)	V_{OUT}	Regulator output pin	
6 (SOP–7)	GND	GND pin	
7 (SOP–7)	N.C		

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Operating temperature	T_{OPR}	–20~+85	°C
Storage temperature	T_{STG}	–40~+125	°C
Supply voltage	V_{CC}	–0.3~+18	V
Output current	I_{OUT}	200	mA
Power dissipation	Pd	650*	mW

Note: * When mounted on a 55×20 mm paper phenol board (SOP-7)
When mounted on a 45×45 mm paper phenol board (SIP-5)

Recommended Operating Conditions

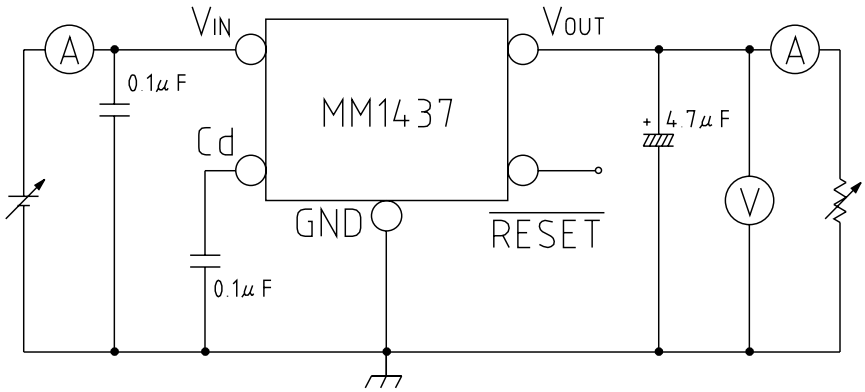
Item	Symbol	Ratings	Unit
Operating temperature	T_{OP}	–20~+85	°C
Output current	I_{OP}	0~150	mA
Operating voltage	V_{OP}	2~16	V

Electrical Characteristics (Except where noted otherwise, Ta=25°C)

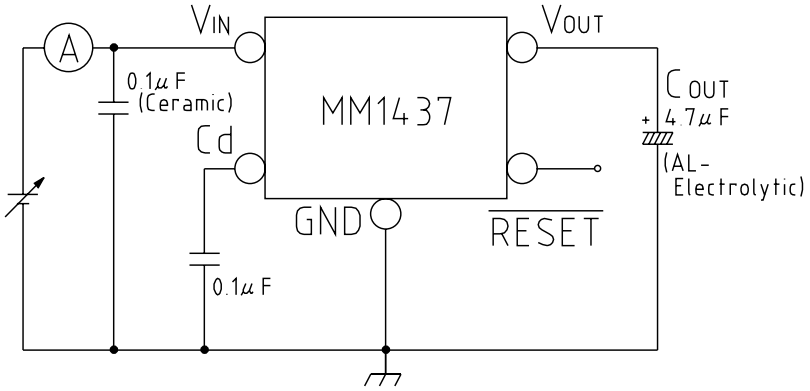
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
No-load input current 1	Iccq1	V_{IN}=6V I_{OUT}=0mA		400	800	µA
No-load input current 2	Iccq2	V_{IN}=4V I_{OUT}=0mA		2.5		mA
Regulator						
Output voltage	V_{OUT}	V_{IN}=6V I_{OUT}=30mA	4.90	5.00	5.10	V
Input-output differential voltage	Vi0	V_{IN}=4.8V I_{OUT}=150 mA		0.25	0.50	V
Line regulation	⊿V1	V_{IN}=6V~10V I_{OUT}=30mA		10	30	mV
Load regulation	⊿V2	V_{IN}=6V I_{OUT}=0~150mA		40	80	mV
Vo temperature coefficient *1	⊿V_{OUT}/⊿T	Tj=–20~+85°C V_{IN}=6V I_{OUT}=30mA		100		ppm/°C
Ripple rejection *1	RR	V_{IN}=6V f=120Hz V_{RIPPLE}=1V_{P-P}, I_{OUT}=30mA	50	60		dB
Output noise voltage *1	Vn	V_{IN}=6V, f=20~80kHz I_{OUT}=30mA		200	400	µVrms
Reset						
Detecting voltage	VS	V_{IN}=H→L	4.03	4.2	4.37	V
Vs temperature coefficient *1	⊿VS/⊿T	Tj=–20~+85°C		100		ppm/°C
Hysteresis voltage	⊿VS	V_{OUT}=H→L→H	25	50	100	mV
Low-level output voltage	V_{OL}	V_{OUT}=3.9V		100	200	mV
$\overline{\text{RESET}}$ delay time	t_{PLH}	Cd=0.1µF	5	10	15	mS
"L" transmission delay time *1	t_{PHL}	Cd=0.1µF		30	90	µS
Threshold operating voltage	V_{OPL}	VOL=0.4V		0.65	0.85	V

Note 1: design guaranteed

Measuring Circuit



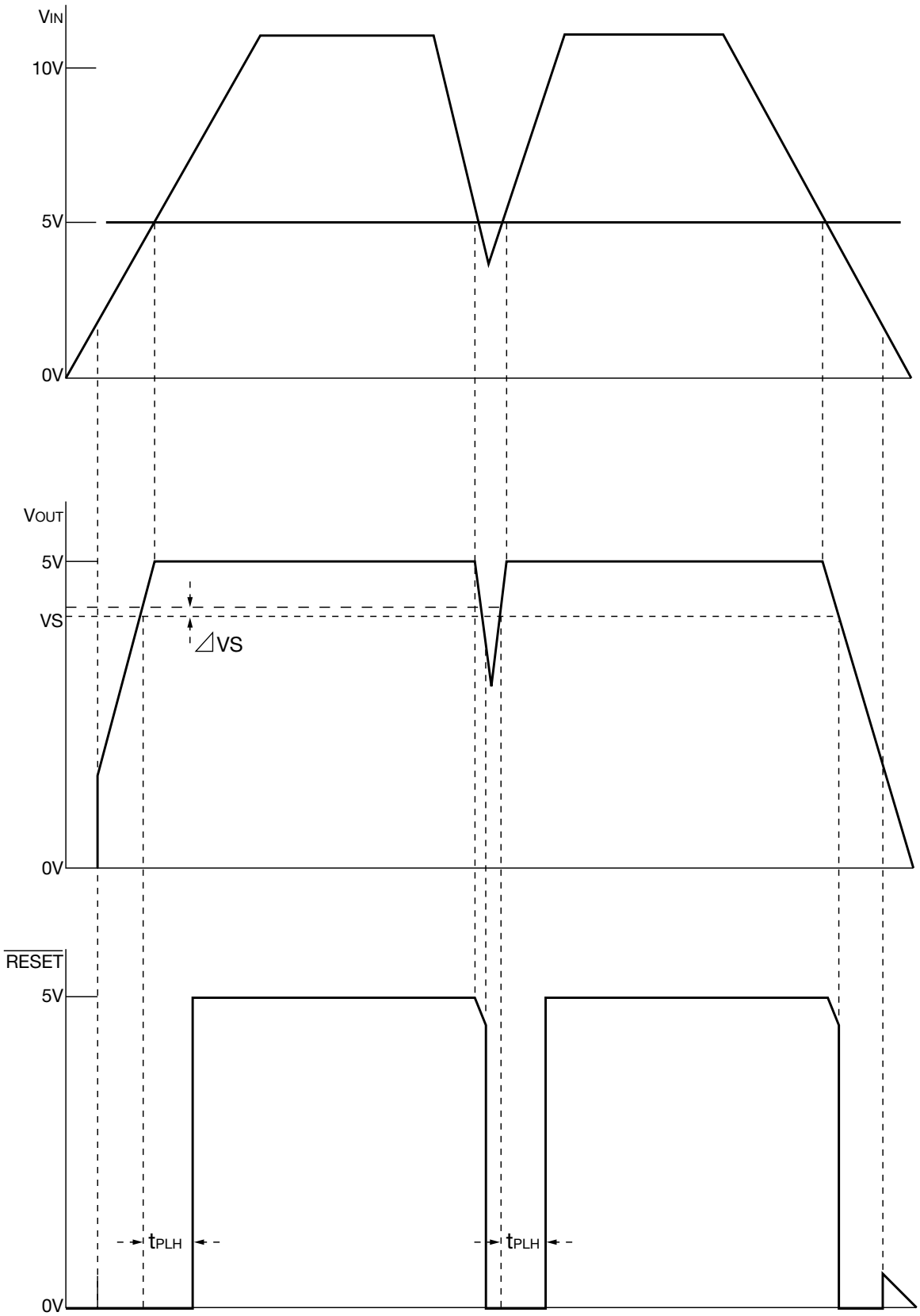
Application Circuit



Note 1 : This regulator is not internally compensated and thus requires an external output-capacitor (C_{OUT}) for stability.

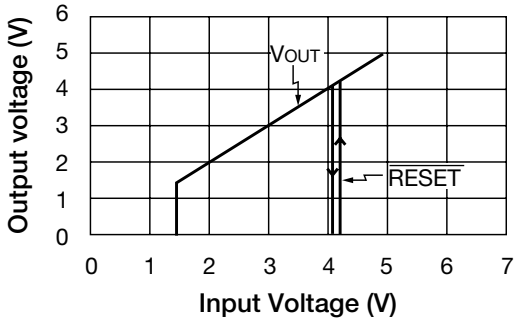
Note 2 : $\overline{\text{RESET}}$-terminal with a built-in pull-up resistance (10kΩ).

Timing Chart

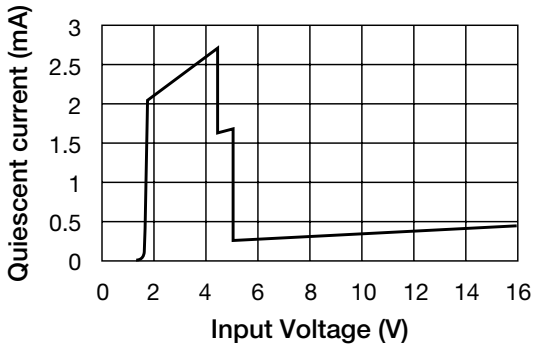


Characteristics

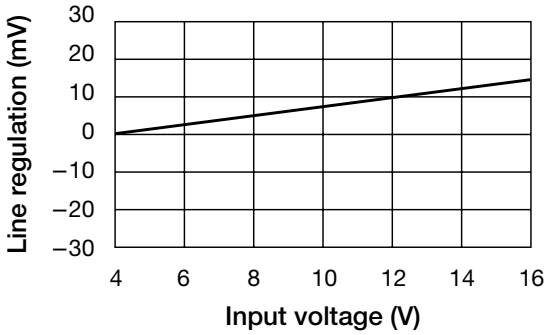
Detection voltage (I_{OUT}=0mA)



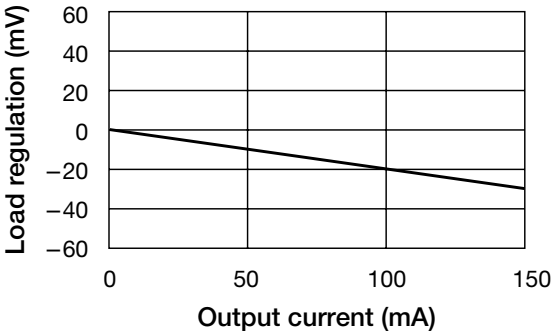
Quiescent current (I_{OUT}=0mA)



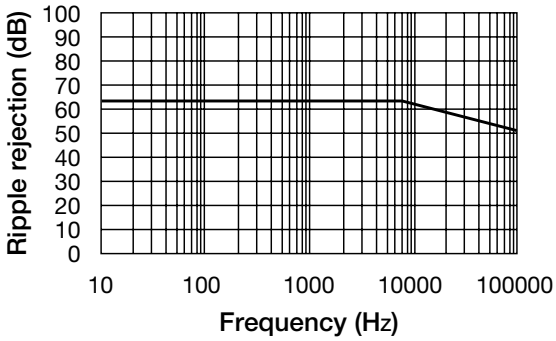
Line regulation



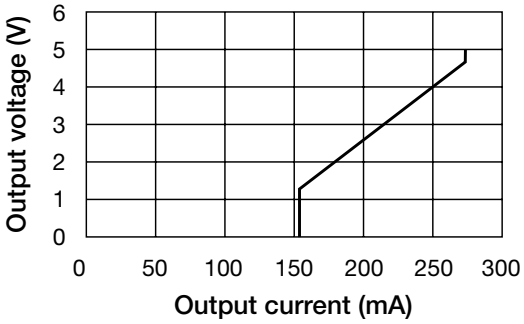
Load regulation



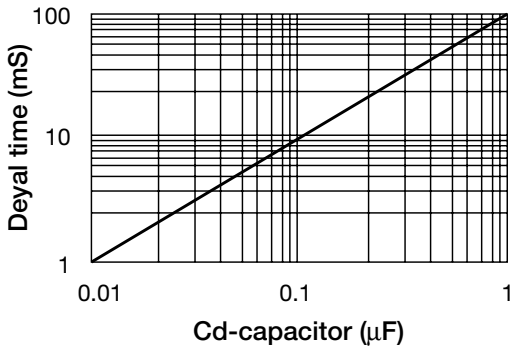
Ripple rejection



Current limit



RESET delay time



Allowable loss