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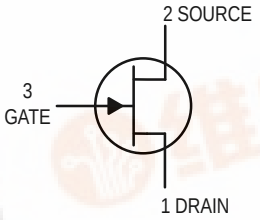
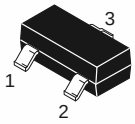
JFET Switching Transistors
N–Channel

MMBF4391LT1
MMBF4392LT1
MMBF4393LT1





CASE 318–08, STYLE 10
SOT–23 (TO–236AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	30	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage	V_{GS}	30	Vdc
Forward Gate Current	$I_{G(f)}$	50	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board(1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

DEVICE MARKING

MMBF4391LT1 = 6J; MMBF4392LT1 = 6K; MMBF4393LT1 = 6G

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate–Source Breakdown Voltage (I_G = 1.0 µAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	—	Vdc
Gate Reverse Current (V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 25°C) (V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 100°C)		I_{GSS}	 — —	 1.0 0.20	 nAdc µAdc
Gate–Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	 MMBF4391LT1 MMBF4392LT1 MMBF4393LT1	$V_{GS(off)}$	 –4.0 –2.0 –0.5	 –10 –5.0 –3.0	Vdc
Off–State Drain Current (V_{DS} = 15 Vdc, V_{GS} = –12 Vdc) (V_{DS} = 15 Vdc, V_{GS} = –12 Vdc, T_A = 100°C)		$I_{D(off)}$	 — —	 1.0 1.0	 nAdc µAdc

1. FR–5 = 1.0 × 0.75 × 0.062 in.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
Zero–Gate–Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	MMBF4391LT1	I_{DSS}	50	150	mAdc
	MMBF4392LT1		25	75	
	MMBF4393LT1		5.0	30	
Drain–Source On–Voltage		$V_{DS(on)}$			Vdc
(I_D = 12 mAdc, V_{GS} = 0)	MMBF4391LT1		—	0.4	
(I_D = 6.0 mAdc, V_{GS} = 0)	MMBF4392LT1		—	0.4	
(I_D = 3.0 mAdc, V_{GS} = 0)	MMBF4393LT1		—	0.4	
Static Drain–Source On–Resistance		$r_{DS(on)}$			Ω
(I_D = 1.0 mAdc, V_{GS} = 0)	MMBF4391LT1		—	30	
	MMBF4392LT1		—	60	
	MMBF4393LT1		—	100	
SMALL–SIGNAL CHARACTERISTICS					
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	14	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 12 Vdc, f = 1.0 MHz)		C_{rss}	—	3.5	pF

TYPICAL CHARACTERISTICS

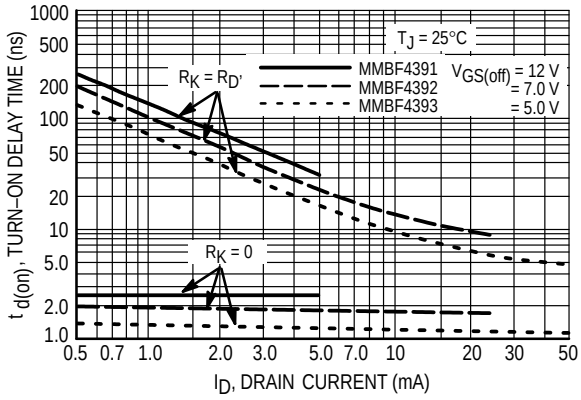


Figure 1. Turn–On Delay Time

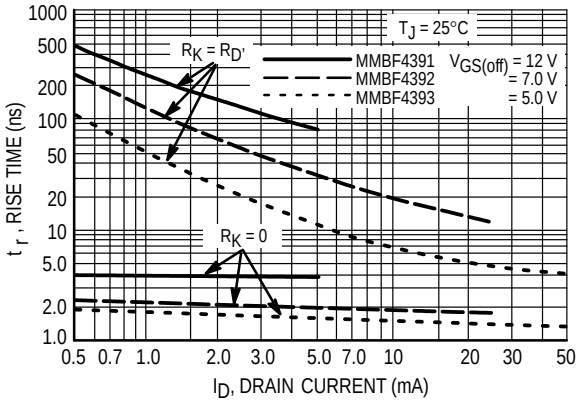


Figure 2. Rise Time

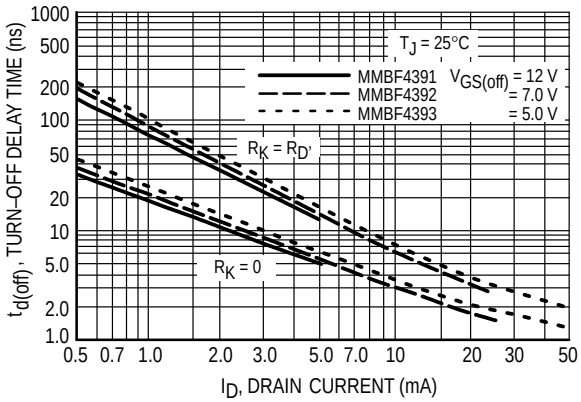


Figure 3. Turn–Off Delay Time

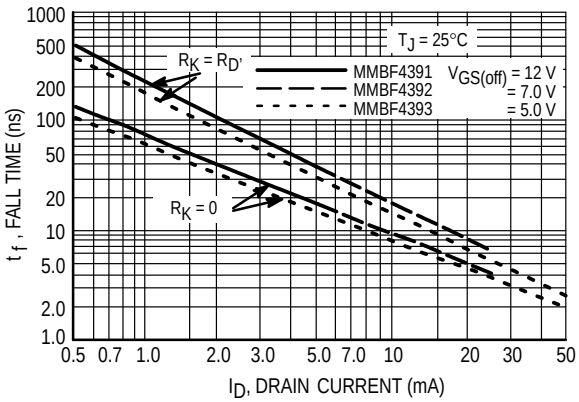


Figure 4. Fall Time

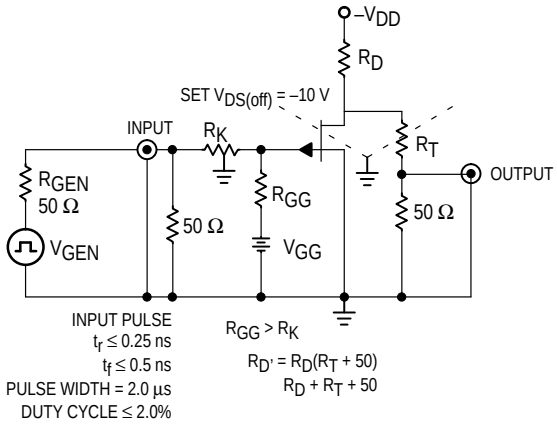


Figure 5. Switching Time Test Circuit

NOTE 1

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($-V_{GG}$). The Drain–Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{rss}) of Gate–Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn–on interval, Gate–Source Capacitance (C_{gs}) discharges through the series combination of R_{Gen} and R_K. C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R'_D) and Drain–Source Resistance (r_{DS}). During the turn–off, this charge flow is reversed.

Predicting turn–on time is somewhat difficult as the channel resistance r_{DS} is a function of the gate–source voltage. While C_{gs} discharges, V_{GS} approaches zero and r_{DS} decreases. Since C_{gd} discharges through r_{DS}, turn–on time is non–linear. During turn–off, the situation is reversed with r_{DS} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to $R_{D'}$ which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2) $R_K = 0$ (low impedance) the driving source impedance is that of the generator.

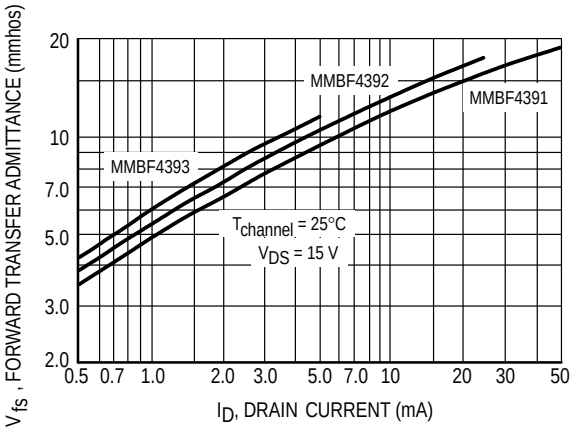


Figure 6. Typical Forward Transfer Admittance

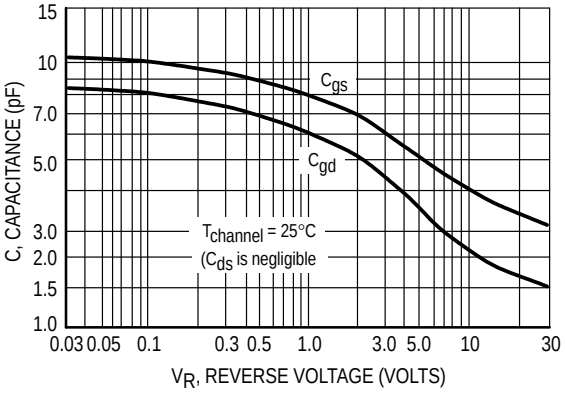


Figure 7. Typical Capacitance

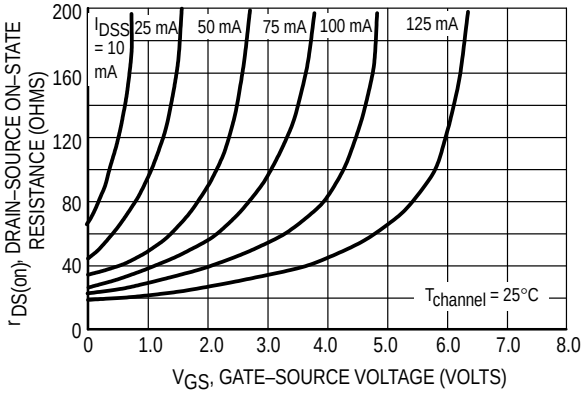


Figure 8. Effect of Gate–Source Voltage on Drain–Source Resistance

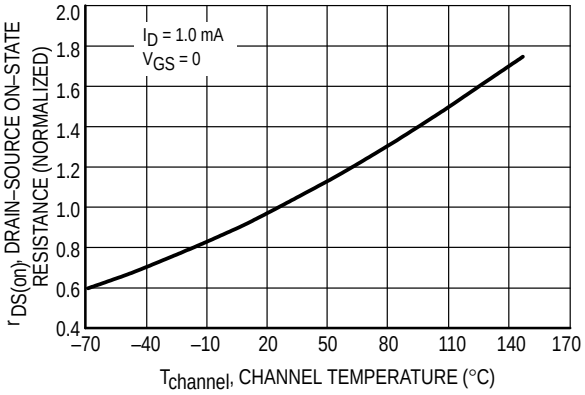


Figure 9. Effect of Temperature on Drain–Source On–State Resistance

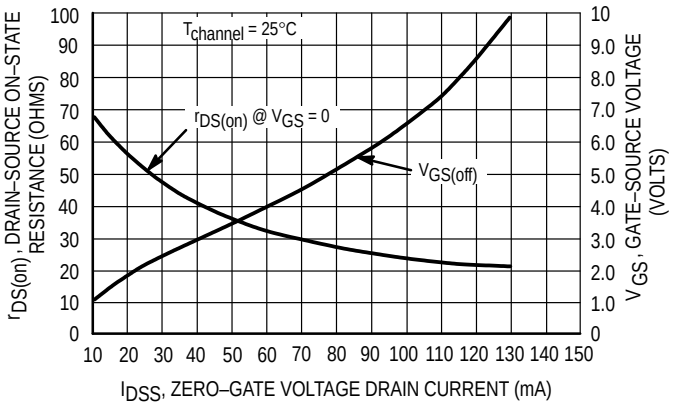


Figure 10. Effect of I_{DSS} on Drain–Source Resistance and Gate–Source Voltage

NOTE 2

The Zero–Gate–Voltage Drain Current (I_{DSS}) is the principle determinant of other J–FET characteristics. Figure 10 shows the relationship of Gate–Source Off Voltage ($V_{GS(off)}$) and Drain–Source On Resistance ($r_{DS(on)}$) to I_{DSS}. Most of the devices will be within ±10% of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

For example:

Unknown

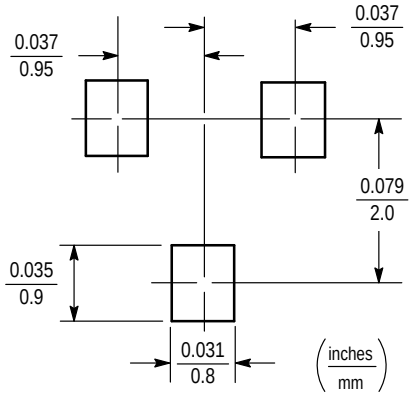
$r_{DS(on)}$ and V_{GS} range for an MMBF4392

The electrical characteristics table indicates that an MMBF4392 has an I_{DSS} range of 25 to 75 mA. Figure 10 shows $r_{DS(on)}$ = 52 Ohms for I_{DSS} = 25 mA and 30 Ohms for I_{DSS} = 75 mA. The corresponding V_{GS} values are 2.2 volts and 4.8 volts.

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

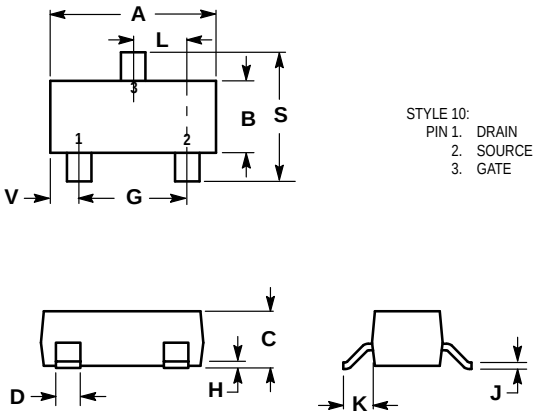
SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS



STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

CASE 318–08
ISSUE AE
SOT–23 (TO–236AB)

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