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List of Sections

Section 1. General Description 43

Section 2. System Memory Map 51

Section 3. Chip Configuration Module (CCM) 89

Section 4. Signal Description. 107

Section 5. Reset Controller Module. 129

Section 6. M•CORE M210 Central Processor Unit (CPU) 143

Section 7. Interrupt Controller Module 153

Section 8. Static Random-Access Memory (SRAM). 175

Section 9. Non-Volatile Memory FLASH (CMFR). 179

Section 10. Clock Module. 221

Section 11. Ports Module 247

Section 12. Edge Port Module (EPORT) 261

Section 13. Watchdog Timer Module 271

Section 14. Programmable Interrupt Timer Modules (PIT1 and PIT2) 281

Section 15. Timer Modules (TIM1 and TIM2). 293

Freescale Semiconductor, Inc.

List of Sections

Section 16. Serial Communications Interface Modules (SCI1 and SCI2) 329

Section 17. Serial Peripheral Interface Module (SPI) 371

Section 18. Queued Analog-to-Digital Converter (QADC) 399

Section 19. External Bus Interface Module (EBI) 503

Section 20. Chip Select Module 521

Section 21. JTAG Test Access Port and OnCE 533

Section 22. Electrical Specifications 585

Section 23. Mechanical Specifications 609

Section 24. Ordering Information 615

Freescale Semiconductor, Inc.

Table of Contents

Section 1. General Description

1.1 Contents 43
1.2 Introduction 43
1.3 Features 44
1.4 Block Diagram 48

Section 2. System Memory Map

2.1 Contents 51
2.2 Introduction 51
2.3 Address Map 52
2.4 Register Map 54

Section 3. Chip Configuration Module (CCM)

3.1 Contents 89
3.2 Introduction 90
3.3 Features 90
3.4 Modes of Operation 90
3.4.1 Master Mode 91
3.4.2 Single-Chip Mode 91
3.4.3 Emulation Mode 91
3.4.4 Factory Access Slave Test (FAST) Mode 91
3.5 Block Diagram 92
3.6 Signal Descriptions 92

Freescale Semiconductor, Inc.

Table of Contents

3.7 Memory Map and Registers 93
3.7.1 Programming Model 93
3.7.2 Memory Map 94
3.7.3 Register Descriptions 94
3.7.3.1 Chip Configuration Register 94
3.7.3.2 Reset Configuration Register 97
3.7.3.3 Chip Identification Register 99
3.7.3.4 Chip Test Register 100
3.8 Functional Description 100
3.8.1 Reset Configuration 101
3.8.2 Chip Mode Selection 103
3.8.3 Boot Device Selection 103
3.8.4 Output Pad Strength Configuration 105
3.8.5 Clock Mode Selection 105
3.8.6 Internal FLASH Configuration 106
3.9 Reset 106
3.10 Interrupts 106

Section 4. Signal Description

4.1 Contents 107
4.2 Introduction 109
4.3 Package Pinout Summary 110
4.4 MMC2107 Specific Implementation Signal Issues 120
4.4.1 $\overline{\text{RSTOUT}}$ Signal Functions 120
4.4.2 $\overline{\text{INT}}$ Signal Functions 121
4.5 Signal Descriptions 121
4.5.1 Reset Signals 121
4.5.1.1 Reset In ($\overline{\text{RESET}}$) 121
4.5.1.2 Reset Out ($\overline{\text{RSTOUT}}$) 121
4.5.2 Phase-Lock Loop (PLL) and Clock Signals 122
4.5.2.1 External Clock In (EXTAL) 122
4.5.2.2 Crystal (XTAL) 122
4.5.2.3 Clock Out (CLKOUT) 122
4.5.2.4 Synthesizer Power (V_{DDSYN} and V_{SSSYN}) 122

Freescale Semiconductor, Inc.

4.5.3 External Memory Interface Signals 122
4.5.3.1 Data Bus (D[31:0]) 122
4.5.3.2 Show Cycle Strobe ($\overline{\text{SHS}}$) 123
4.5.3.3 Transfer Acknowledge ($\overline{\text{TA}}$) 123
4.5.3.4 Transfer Error Acknowledge ($\overline{\text{TEA}}$) 123
4.5.3.5 Emulation Mode Chip Selects (CSE[1:0]) 123
4.5.3.6 Transfer Code (TC[2:0]) 123
4.5.3.7 Read/Write (R/$\overline{\text{W}}$) 123
4.5.3.8 Address Bus ($\overline{\text{A}}$[22:0]) 124
4.5.3.9 Enable Byte ($\overline{\text{EB}}$[3:0]) 124
4.5.3.10 Chip Select ($\overline{\text{CS}}$[3:0]) 124
4.5.3.11 Output Enable ($\overline{\text{OE}}$) 124
4.5.4 Edge Port Signals 124
4.5.4.1 External Interrupts ($\overline{\text{INT}}$[7:6]) 124
4.5.4.2 External Interrupts ($\overline{\text{INT}}$[5:2]) 124
4.5.4.3 External Interrupts ($\overline{\text{INT}}$[1:0]) 125
4.5.5 Serial Peripheral Interface Module Signals 125
4.5.5.1 Master Out/Slave In (MOSI) 125
4.5.5.2 Master In/Slave Out (MISO) 125
4.5.5.3 Serial Clock ($\overline{\text{SCK}}$) 125
4.5.5.4 Slave Select ($\overline{\text{SS}}$) 125
4.5.6 Serial Communications Interface Module Signals 125
4.5.6.1 Receive Data (RXD1 and RXD2) 125
4.5.6.2 Transmit Data (TXD1 and TXD2) 126
4.5.7 Timer Signals (ICOC1[3:0] and ICOC2[3:0]) 126
4.5.8 Analog-to-Digital Converter Signals 126
4.5.8.1 Analog Inputs (PQA[4:3], PQA[1:0], and PQB[3:0]) 126
4.5.8.2 Analog Reference (V_{RH} and V_{RL}) 126
4.5.8.3 Analog Supply (V_{DDA} and V_{SSA}) 126
4.5.8.4 Positive Supply (V_{DDH}) 126
4.5.9 Debug and Emulation Support Signals 127
4.5.9.1 Test Reset ($\overline{\text{TRST}}$) 127
4.5.9.2 Test Clock (TCLK) 127
4.5.9.3 Test Mode Select (TMS) 127
4.5.9.4 Test Data Input (TDI) 127
4.5.9.5 Test Data Output (TDO) 127
4.5.9.6 Debug Event ($\overline{\text{DE}}$) 127

Freescale Semiconductor, Inc.

4.5.10 Test Signal (TEST) 128
4.5.11 Power and Ground Signals 128
4.5.11.1 Power for FLASH Erase/Program (V_{PP}) 128
4.5.11.2 Power and Ground for FLASH Array (V_{DDF} and V_{SSF}) 128
4.5.11.3 Standby Power (V_{STBY}) 128
4.5.11.4 Positive Supply (V_{DD}) 128
4.5.11.5 Ground (V_{SS}) 128

Section 5. Reset Controller Module

5.1 Contents 129
5.2 Introduction 130
5.3 Features 130
5.4 Block Diagram 131
5.5 Signals 131
5.6 Memory Map and Registers 132
5.6.1 Reset Control Register 133
5.6.2 Reset Status Register 134
5.6.3 Reset Test Register 135
5.7 Functional Description 136
5.7.1 Reset Sources 136
5.7.1.1 Power-On Reset 137
5.7.1.2 External Reset 137
5.7.1.3 Watchdog Timer Reset 137
5.7.1.4 Loss of Clock Reset 137
5.7.1.5 Loss of Lock Reset 138
5.7.1.6 Software Reset 138
5.7.2 Reset Control Flow 138
5.7.2.1 Synchronous Reset Requests 138
5.7.2.2 Internal Reset Request 140
5.7.2.3 Power-On Reset 140
5.7.3 Concurrent Resets 140
5.7.3.1 Reset Flow 140
5.7.3.2 Reset Status Flags 141
5.8 Interrupts 141

Freescale Semiconductor, Inc.

Section 6. M•CORE M210 Central Processor Unit (CPU)

6.1 Contents 143
6.2 Introduction 143
6.3 Features 144
6.4 Microarchitecture Summary 145
6.5 Programming Model 147
6.6 Data Format Summary 149
6.7 Operand Addressing Capabilities 150
6.8 Instruction Set Overview 150

Section 7. Interrupt Controller Module

7.1 Contents 153
7.2 Introduction 154
7.3 Features 154
7.4 Low-Power Mode Operation 154
7.5 Block Diagram 155
7.6 External Signals 155
7.7 Memory Map and Registers 155
7.7.1 Memory Map 156
7.7.2 Registers 157
7.7.2.1 Interrupt Control Register 157
7.7.2.2 Interrupt Status Register 159
7.7.2.3 Interrupt Force Registers 160
7.7.2.4 Interrupt Pending Register 162
7.7.2.5 Normal Interrupt Enable Register 163
7.7.2.6 Normal Interrupt Pending Register 164
7.7.2.7 Fast Interrupt Enable Register 165
7.7.2.8 Fast Interrupt Pending Register 166
7.7.2.9 Priority Level Select Registers 167
7.8 Functional Description 167
7.8.1 Interrupt Sources and Prioritization 168
7.8.2 Fast and Normal Interrupt Requests 168
7.8.3 Autovectored and Vectored Interrupt Requests 169

Freescale Semiconductor, Inc.

7.8.4 Interrupt Configuration 171
7.8.4.1 M•CORE Processor Configuration 171
7.8.4.2 Interrupt Controller Configuration 171
7.8.4.3 Interrupt Source Configuration 172
7.8.5 Interrupts 172

Section 8. Static Random-Access Memory (SRAM)

8.1 Contents 175
8.2 Introduction 175
8.3 Modes of Operation 175
8.4 Low-Power Modes 176
8.5 Standby Power Supply Pin (V_{STBY}) 176
8.6 Standby Operation 176
8.7 Reset Operation 177
8.8 Interrupts 177

Section 9. Non-Volatile Memory FLASH (CMFR)

9.1 Contents 179
9.2 Introduction 180
9.3 Features 181
9.4 Modes of Operation 182
9.4.1 Stop Mode 182
9.4.2 Disabled Mode 182
9.5 Block Diagram 183
9.6 Glossary of Terms 185
9.7 Registers and Memory Map 186
9.7.1 Control Registers 187
9.7.1.1 CMFR Module Configuration Register 188
9.7.1.2 CMFR Module Test Register 193
9.7.1.3 CMFR High-Voltage Control Register 196
9.7.2 Array Addressing 203
9.7.2.1 Read Page Buffers 203
9.7.2.2 Program Page Buffers 204

Freescale Semiconductor, Inc.

9.8 Functional Description 205
9.8.1 Master Reset 205
9.8.2 Register Read and Write Operation 205
9.8.3 Array Read Operation 205
9.8.4 Programming 206
9.8.4.1 Program Sequence 207
9.8.4.2 Program Margin Reads 211
9.8.4.3 Programming Shadow Information. 212
9.8.4.4 Program Pulse-Width and Amplitude Modulation 213
9.8.4.5 Overprogramming 213
9.8.5 Erasing 214
9.8.5.1 Erase Sequence 215
9.8.5.2 Erase Margin Reads 218
9.8.5.3 Erasing Shadow Information Words. 219
9.8.6 Erase Pulse Amplitude and Width Modulation 219
9.8.7 Emulation Operation. 220
9.9 Master Reset 220
9.10 Interrupts. 220

Section 10. Clock Module

10.1 Contents 221
10.2 Introduction 222
10.3 Features 222
10.4 Modes of Operation 223
10.4.1 Normal PLL Mode 223
10.4.2 1:1 PLL Mode 223
10.4.3 External Clock Mode 223
10.4.4 Low-Power Options 223
10.4.4.1 Wait and Doze Modes 223
10.4.4.2 Stop Mode 224
10.5 Block Diagram 224
10.6 Signal Descriptions 225
10.6.1 EXTAL 225
10.6.2 XTAL 225
10.6.3 CLKOUT 225

Freescale Semiconductor, Inc.

Table of Contents

10.6.4 V_{DDSYN} and V_{SSSYN} 225
10.6.5 RSTOUT 226
10.7 Memory Map and Registers 226
10.7.1 Module Memory Map 226
10.7.2 Register Descriptions 227
10.7.2.1 Synthesizer Control Register 227
10.7.2.2 Synthesizer Status Register 230
10.7.2.3 Synthesizer Test Register 233
10.7.2.4 Synthesizer Test Register 2 234
10.8 Functional Description 235
10.8.1 System Clock Modes 235
10.8.2 System Clocks Generation 236
10.8.3 PLL Lock Detection 236
10.8.3.1 PLL Loss of Lock Conditions 238
10.8.3.2 PLL Loss of Lock Reset 238
10.8.4 Loss of Clock Detection 238
10.8.4.1 Alternate Clock Selection 239
10.8.4.2 Loss-of-Clock Reset 242
10.8.5 Clock Operation During Reset 243
10.8.6 PLL Operation 243
10.8.6.1 Phase and Frequency Detector (PFD) 245
10.8.6.2 Charge Pump/Loop Filter 245
10.8.6.3 Voltage Control Output (VCO) 246
10.8.6.4 Multiplication Factor Divider (MFD) 246
10.9 Reset 246
10.10 Interrupts 246

Section 11. Ports Module

11.1 Contents 247
11.2 Introduction 248
11.3 Signals 249
11.4 Memory Map and Registers 249
11.4.1 Memory Map 250
11.4.2 Register Descriptions 251
11.4.2.1 Port Output Data Registers 251
11.4.2.2 Port Data Direction Registers 252

Freescale Semiconductor, Inc.

11.4.2.3 Port Pin Data/Set Data Registers 253
11.4.2.4 Port Clear Output Data Registers 254
11.4.2.5 Port C/D Pin Assignment Register 255
11.4.2.6 Port E Pin Assignment Register 256
11.5 Functional Description 257
11.5.1 Pin Functions 258
11.5.2 Port Digital I/O Timing 259
11.6 Interrupts 259

Section 12. Edge Port Module (EPORT)

12.1 Contents 261
12.2 Introduction 261
12.3 Low-Power Mode Operation 262
12.3.1 Wait and Doze Modes 262
12.3.2 Stop Mode 263
12.4 Interrupt/General-Purpose I/O Pin Descriptions 263
12.5 Memory Map and Registers 263
12.5.1 Memory Map 263
12.5.2 Registers 264
12.5.2.1 EPORT Pin Assignment Register 264
12.5.2.2 EPORT Data Direction Register 266
12.5.2.3 Edge Port Interrupt Enable Register 267
12.5.2.4 Edge Port Data Register 268
12.5.2.5 Edge Port Pin Data Register 268
12.5.2.6 Edge Port Flag Register 269

Section 13. Watchdog Timer Module

13.1 Contents 271
13.2 Introduction 271
13.3 Modes of Operation 272
13.3.1 Wait Mode 272
13.3.2 Doze Mode 272
13.3.3 Stop Mode 272
13.3.4 Debug Mode 272

Freescale Semiconductor, Inc.

13.4 Block Diagram 273
13.5 Signals 273
13.6 Memory Map and Registers 274
13.6.1 Memory Map 274
13.6.2 Registers 274
13.6.2.1 Watchdog Control Register 275
13.6.2.2 Watchdog Modulus Register 277
13.6.2.3 Watchdog Count Register 278
13.6.2.4 Watchdog Service Register 279

Section 14. Programmable Interrupt Timer Modules (PIT1 and PIT2)

14.1 Contents 281
14.2 Introduction 282
14.3 Block Diagram 282
14.4 Modes of Operation 283
14.4.1 Wait Mode 283
14.4.2 Doze Mode 283
14.4.3 Stop Mode 283
14.4.4 Debug Mode 283
14.5 Signals 283
14.6 Memory Map and Registers 284
14.6.1 Memory Map 284
14.6.2 Registers 284
14.6.2.1 PIT Control and Status Register 285
14.6.2.2 PIT Modulus Register 288
14.6.2.3 PIT Count Register 289
14.7 Functional Description 290
14.7.1 Set-and-Forget Timer Operation 290
14.7.2 Free-Running Timer Operation 291
14.7.3 Timeout Specifications 291
14.8 Interrupt Operation 292

Freescale Semiconductor, Inc.

Section 15. Timer Modules (TIM1 and TIM2)

15.1 Contents 293
15.2 Introduction 295
15.3 Features 295
15.4 Block Diagram 296
15.5 Modes of Operation 297
15.5.1 Supervisor and User Modes 297
15.5.2 Run Mode 297
15.5.3 Stop Mode 297
15.5.4 Wait, Doze, and Debug Modes 297
15.5.5 Test Mode 297
15.6 Signal Description 298
15.6.1 ICOC[2:0] 298
15.6.2 ICOC3 298
15.7 Memory Map and Registers 298
15.7.1 Timer Input Capture/Output Compare Select Register 300
15.7.2 Timer Compare Force Register 301
15.7.3 Timer Output Compare 3 Mask Register 302
15.7.4 Timer Output Compare 3 Data Register 303
15.7.5 Timer Counter Registers 304
15.7.6 Timer System Control Register 1 305
15.7.7 Timer Toggle-On-Overflow Register 306
15.7.8 Timer Control Register 1 307
15.7.9 Timer Control Register 2 308
15.7.10 Timer Interrupt Enable Register 309
15.7.11 Timer System Control Register 2 310
15.7.12 Timer Flag Register 1 312
15.7.13 Timer Flag Register 2 313
15.7.14 Timer Channel Registers 314
15.7.15 Pulse Accumulator Control Register 315
15.7.16 Pulse Accumulator Flag Register 317
15.7.17 Pulse Accumulator Counter Registers 318
15.7.18 Timer Port Data Register 319
15.7.19 Timer Port Data Direction Register 320
15.7.20 Timer Test Register 321

Freescale Semiconductor, Inc.

Table of Contents

15.8 Functional Description 321
15.8.1 Prescaler 321
15.8.2 Input Capture 321
15.8.3 Output Compare 322
15.8.4 Pulse Accumulator 323
15.8.4.1 Event Counter Mode 323
15.8.4.2 Gated Time Accumulation Mode 324
15.8.5 General-Purpose I/O Ports 325
15.9 Reset 326
15.10 Interrupts 326
15.10.1 Timer Channel Interrupts (CxF) 326
15.10.2 Pulse Accumulator Overflow (PAOVF) 327
15.10.3 Pulse Accumulator Input (PAIF) 327
15.10.4 Timer Overflow (TOF) 327

Section 16. Serial Communications Interface Modules (SCI1 and SCI2)

16.1 Contents 329
16.2 Introduction 330
16.3 Features 331
16.4 Block Diagram 332
16.5 Modes of Operation 333
16.5.1 Doze Mode 333
16.5.2 Stop Mode 333
16.6 Signal Description 334
16.6.1 RXD 334
16.6.2 TXD 334
16.7 Memory Map and Registers 334
16.7.1 SCI Baud Rate Registers 336
16.7.2 SCI Control Register 1 337
16.7.3 SCI Control Register 2 340
16.7.4 SCI Status Register 1 342
16.7.5 SCI Status Register 2 344
16.7.6 SCI Data Registers 345
16.7.7 SCI Pullup and Reduced Drive Register 346

Freescale Semiconductor, Inc.

16.7.8 SCI Port Data Register 347
16.7.9 SCI Data Direction Register 348
16.8 Functional Description 349
16.9 Data Format 349
16.10 Baud Rate Generation 350
16.11 Transmitter 351
16.11.1 Frame Length 352
16.11.2 Transmitting a Frame 353
16.11.3 Break Frames 355
16.11.4 Idle Frames 355
16.12 Receiver 356
16.12.1 Frame Length 356
16.12.2 Receiving a Frame 356
16.12.3 Data Sampling 357
16.12.4 Framing Errors 362
16.12.5 Baud Rate Tolerance 362
16.12.5.1 Slow Data Tolerance 363
16.12.5.2 Fast Data Tolerance 364
16.12.6 Receiver Wakeup 365
16.12.6.1 Idle Input Line Wakeup (WAKE = 0) 365
16.12.6.2 Address Mark Wakeup (WAKE = 1) 365
16.13 Single-Wire Operation 366
16.14 Loop Operation 367
16.15 I/O Ports 368
16.16 Reset 369
16.17 Interrupts 369
16.17.1 Transmit Data Register Empty 369
16.17.2 Transmission Complete 369
16.17.3 Receive Data Register Full 370
16.17.4 Idle Receiver Input 370
16.17.5 Overrun 370

Freescale Semiconductor, Inc.

Table of Contents

Section 17. Serial Peripheral Interface Module (SPI)

17.1 Contents 371
17.2 Introduction 372
17.3 Features 372
17.4 Modes of Operation 373
17.5 Block Diagram 373
17.6 Signal Description 374
17.6.1 MISO (Master In/Slave Out) 374
17.6.2 MOSI (Master Out/Slave In) 374
17.6.3 SCK (Serial Clock) 375
17.6.4 SS (Slave Select) 375
17.7 Memory Map and Registers 375
17.7.1 SPI Control Register 1 376
17.7.2 SPI Control Register 2 378
17.7.3 SPI Baud Rate Register 379
17.7.4 SPI Status Register 381
17.7.5 SPI Data Register 382
17.7.6 SPI Pullup and Reduced Drive Register 383
17.7.7 SPI Port Data Register 384
17.7.8 SPI Port Data Direction Register 385
17.8 Functional Description 386
17.8.1 Master Mode 387
17.8.2 Slave Mode 387
17.8.3 Transmission Formats 388
17.8.3.1 Transfer Format When CPHA = 1 388
17.8.3.2 Transfer Format When CPHA = 0 390
17.8.4 SPI Baud Rate Generation 393
17.8.5 Slave-Select Output 393
17.8.6 Bidirectional Mode 394
17.8.7 Error Conditions 395
17.8.7.1 Write Collision Error 395
17.8.7.2 Mode Fault Error 395
17.8.8 Low-Power Mode Options 396
17.8.8.1 Run Mode 396
17.8.8.2 Doze Mode 396
17.8.8.3 Stop Mode 396

Freescale Semiconductor, Inc.

17.9 Reset 397
17.10 Interrupts. 397
17.10.1 SPI Interrupt Flag (SPIF) 397
17.10.2 Mode Fault (MODF) Flag 397

Section 18. Queued Analog-to-Digital Converter (QADC)

18.1 Contents 399
18.2 Introduction. 401
18.3 Features 402
18.4 Block Diagram 403
18.5 Modes of Operation 404
18.5.1 Debug Mode. 404
18.5.2 Stop Mode 405
18.6 Signals 405
18.6.1 Port QA Pin Functions 406
18.6.1.1 Port QA Analog Input Pins. 406
18.6.1.2 Port QA Digital Input/Output Pins 407
18.6.2 Port QB Pin Functions 407
18.6.2.1 Port QB Analog Input Pins. 407
18.6.2.2 Port QB Digital Input Pins 407
18.6.3 External Trigger Input Pins. 408
18.6.4 Multiplexed Address Output Pins 408
18.6.5 Multiplexed Analog Input Pins 409
18.6.6 Voltage Reference Pins 409
18.6.7 Dedicated Analog Supply Pins. 409
18.7 Memory Map. 409
18.8 Register Descriptions 411
18.8.1 QADC Module Configuration Register 411
18.8.2 QADC Test Register. 412
18.8.3 Port Data Registers 412
18.8.4 Port QA Data Direction Register 414

Freescale Semiconductor, Inc.

Table of Contents

18.8.5 Control Registers 416
18.8.5.1 Control Register 0 416
18.8.5.2 Control Register 1 419
18.8.5.3 QADC Control Register 2 422
18.8.6 Status Registers 427
18.8.6.1 QADC Status Register 0 427
18.8.6.2 QADC Status Register 1 436
18.8.7 Conversion Command Word Table 437
18.8.8 Result Registers 441
18.8.8.1 Right-Justified Unsigned Result Register 441
18.8.8.2 Left-Justified Signed Result Register 442
18.8.8.3 Left-Justified Unsigned Result Register 442

18.9 Functional Description 443
18.9.1 QADC Bus Accessing 443
18.9.2 External Multiplexing 443
18.9.2.1 External Multiplexing Operation 443
18.9.2.2 Module Version Options 444
18.9.2.3 External Multiplexed Address Configuration 446
18.9.3 Analog Subsystem 446
18.9.3.1 Analog-to-Digital Converter Operation 446
18.9.3.2 Conversion Cycle Times 446
18.9.3.3 Channel Decode and Multiplexer 448
18.9.3.4 Sample Buffer 448
18.9.3.5 Digital-to-Analog Converter (DAC) Array 449
18.9.3.6 Comparator 449
18.9.3.7 Bias 449
18.9.3.8 Successive-Approximation Register 449
18.9.3.9 State Machine 450

18.10 Digital Control 450
18.10.1 Queue Priority Timing Examples 450
18.10.1.1 Queue Priority 451
18.10.1.2 Queue Priority Schemes 453
18.10.2 Boundary Conditions 465
18.10.3 Scan Modes 466
18.10.4 Disabled Mode 467
18.10.5 Reserved Mode 467

Freescale Semiconductor, Inc.

18.10.6 Single-Scan Modes 467
18.10.6.1 Software-Initiated Single-Scan Mode 468
18.10.6.2 External Trigger Single-Scan Mode 469
18.10.6.3 External Gated Single-Scan Mode 470
18.10.6.4 Interval Timer Single-Scan Mode 470
18.10.7 Continuous-Scan Modes 472
18.10.7.1 Software-Initiated Continuous-Scan Mode 473
18.10.7.2 External Trigger Continuous-Scan Mode 474
18.10.7.3 External Gated Continuous-Scan Mode 474
18.10.7.4 Periodic Timer Continuous-Scan Mode 475
18.10.8 QADC Clock (QCLK) Generation 476
18.10.9 Periodic/Interval Timer 480
18.10.10 Conversion Command Word Table 481
18.10.11 Result Word Table 485
18.11 Pin Connection Considerations 486
18.11.1 Analog Reference Pins 486
18.11.2 Analog Power Pins 486
18.11.3 Conversion Timing Schemes 488
18.11.4 Analog Supply Filtering and Grounding 490
18.11.5 Accommodating Positive/Negative Stress Conditions 494
18.11.6 Analog Input Considerations 495
18.11.7 Analog Input Pins 497
18.11.7.1 Settling Time for the External Circuit 498
18.11.7.2 Error Resulting from Leakage 499
18.12 Interrupts 500
18.12.1 Interrupt Operation 500
18.12.2 Interrupt Sources 501

Section 19. External Bus Interface Module (EBI)

19.1 Contents 503
19.2 Introduction 504
19.3 Signal Descriptions 505
19.3.1 Data Bus (D[31:0]) 506
19.3.2 Show Cycle Strobe ($\overline{\text{SHS}}$) 506
19.3.3 Transfer Acknowledge ($\overline{\text{TA}}$) 506
19.3.4 Transfer Error Acknowledge ($\overline{\text{TEA}}$) 506

Freescale Semiconductor, Inc.

Table of Contents

19.3.5 Emulation Mode Chip Selects (CSE[1:0]) 506
19.3.6 Transfer Code (TC[2:0]) 506
19.3.7 Read/Write (R/W) 507
19.3.8 Address Bus (A[22:0]) 507
19.3.9 Enable Byte (EB[3:0]) 507
19.3.10 Chip Selects (CS[3:0]) 507
19.3.11 Output Enable (OE) 507
19.3.12 Transfer Size (TSIZ[1:0]) 507
19.3.13 Processor Status (PSTAT[3:0]) 507
19.4 Memory Map and Registers 508
19.5 Operand Transfer 508
19.6 Enable Byte Pins (EB[3:0]) 510
19.7 Bus Master Cycles 510
19.7.1 Read Cycles 511
19.7.1.1 State 1 (X1) 512
19.7.1.2 Optional Wait States (X2W) 512
19.7.1.3 State 2 (X2) 512
19.7.2 Write Cycles 513
19.7.2.1 State 1 (X1) 514
19.7.2.2 Optional Wait States (X2W) 514
19.7.2.3 State 2 (X2) 514
19.8 Bus Exception Operation 516
19.8.1 Transfer Error Termination 516
19.8.2 Transfer Abort Termination 516
19.9 Emulation Support 516
19.9.1 Emulation Chip-Selects (CSE[1:0]) 516
19.9.2 Internal Data Transfer Display (Show Cycles) 517
19.9.3 Show Strobe (SHS) 518
19.10 Bus Monitor 519
19.11 Interrupts 520

Section 20. Chip Select Module

20.1 Contents 521
20.2 Introduction 521
20.3 Features 522

Freescale Semiconductor, Inc.

20.4 Block Diagram 523
20.5 Signals 524
20.6 Memory Map and Registers 524
20.6.1 Memory Map 524
20.6.2 Registers 525
20.7 Functional Description 530
20.8 Interrupts. 531

Section 21. JTAG Test Access Port and OnCE

21.1 Contents 533
21.2 Introduction 535
21.3 Top-Level Test Access Port (TAP) 537
21.3.1 Test Clock (TCLK) 538
21.3.2 Test Mode Select (TMS) 538
21.3.3 Test Data Input (TDI) 538
21.3.4 Test Data Output (TDO) 538
21.3.5 Test Reset ($\overline{\text{TRST}}$) 538
21.3.6 Debug Event ($\overline{\text{DE}}$) 538
21.4 Top-Level TAP Controller 540
21.5 Instruction Shift Register. 541
21.5.1 EXTEST Instruction 541
21.5.2 IDCODE Instruction 542
21.5.3 SAMPLE/PRELOAD Instruction 543
21.5.4 ENABLE_MCU_ONCE Instruction 543
21.5.5 HIGHZ Instruction. 544
21.5.6 CLAMP Instruction 544
21.5.7 BYPASS Instruction 544
21.6 IDCODE Register 545
21.7 Bypass Register 546
21.8 Boundary SCAN Register 546
21.9 Restrictions 546
21.10 Non-Scan Chain Operation. 547
21.11 Boundary Scan 547
21.12 Low-Level TAP (OnCE) Module 553

Freescale Semiconductor, Inc.

Table of Contents

21.13 Signal Descriptions 555
21.13.1 Debug Serial Input (TDI) 555
21.13.2 Debug Serial Clock (TCLK) 555
21.13.3 Debug Serial Output (TDO) 555
21.13.4 Debug Mode Select (TMS) 556
21.13.5 Test Reset (TRST) 556
21.13.6 Debug Event (DE) 556
21.14 Functional Description 556
21.14.1 Operation 557
21.14.2 OnCE Controller and Serial Interface 558
21.14.3 OnCE Interface Signals 559
21.14.3.1 Internal Debug Request Input (IDR) 559
21.14.3.2 CPU Debug Request (DBGRQ) 560
21.14.3.3 CPU Debug Acknowledge (DBGACK) 560
21.14.3.4 CPU Breakpoint Request (BRKRQ) 560
21.14.3.5 CPU Address, Attributes (ADDR, ATTR) 560
21.14.3.6 CPU Status (PSTAT) 560
21.14.3.7 OnCE Debug Output (DEBUG) 560
21.14.4 OnCE Controller Registers 561
21.14.4.1 OnCE Command Register 561
21.14.4.2 OnCE Control Register 564
21.14.4.3 OnCE Status Register 568
21.14.5 OnCE Decoder (ODEC) 570
21.14.6 Memory Breakpoint Logic 570
21.14.6.1 Memory Address Latch (MAL) 571
21.14.6.2 Breakpoint Address Base Registers 571
21.14.7 Breakpoint Address Mask Registers 571
21.14.7.1 Breakpoint Address Comparators 572
21.14.7.2 Memory Breakpoint Counters 572
21.14.8 OnCE Trace Logic 572
21.14.8.1 OnCE Trace Counter 573
21.14.8.2 Trace Operation 574
21.14.9 Methods of Entering Debug Mode 574
21.14.9.1 Debug Request During RESET 574
21.14.9.2 Debug Request During Normal Activity 575
21.14.9.3 Debug Request During Stop, Doze, or Wait Mode 575
21.14.9.4 Software Request During Normal Activity 575

Freescale Semiconductor, Inc.

21.14.10 Enabling OnCE Trace Mode 575
21.14.11 Enabling OnCE Memory Breakpoints. 576
21.14.12 Pipeline Information and Write-Back Bus Register 576
21.14.12.1 Program Counter Register 577
21.14.12.2 Instruction Register 577
21.14.12.3 Control State Register 577
21.14.12.4 Writeback Bus Register 579
21.14.12.5 Processor Status Register 579
21.14.13 Instruction Address FIFO Buffer (PC FIFO) 580
21.14.14 Reserved Test Control Registers 581
21.14.15 Serial Protocol 581
21.14.16 OnCE Commands 582
21.14.17 Target Site Debug System Requirements 582
21.14.18 Interface Connector for JTAG/OnCE Serial Port 582

Section 22. Electrical Specifications

22.1 Contents 585
22.2 Introduction 585
22.3 Absolute Maximum Ratings 586
22.4 Thermal Characteristics 587
22.5 Power Dissipation 587
22.6 Electrostatic Discharge (ESD) Protection 587
22.7 DC Electrical Specifications 588
22.8 PLL Electrical Specifications. 590
22.9 QADC Electrical Characteristics 591
22.10 FLASH Memory Characteristics 594
22.11 External Interface Timing Characteristics 596
22.12 Reset and Configuration Override Timing 601
22.13 SPI Timing Characteristics 602
22.14 OnCE, JTAG, and Boundary Scan Timing 605

Freescale Semiconductor, Inc.

Table of Contents

Section 23. Mechanical Specifications

23.1 Contents 609
23.2 Introduction 609
23.3 Bond Pins 610
23.4 Package Information for the 144-Pin LQFP 611
23.5 Package Information for the 100-Pin LQFP 611
23.6 144-Pin LQFP Mechanical Drawing 612
23.7 100-Pin LQFP Mechanical Drawing 613

Section 24. Ordering Information

24.1 Contents 615
24.2 Introduction 615
24.3 MC Order Numbers 615

Freescale Semiconductor, Inc.

List of Figures

Figure	Title	Page
1-1	Block Diagram	49
2-1	Address Map	52
2-2	Register Summary	54
3-1	Chip Configuration Module Block Diagram	92
3-2	Chip Configuration Register (CCR)	94
3-3	Reset Configuration Register (RCON)	97
3-4	Chip Identification Register (CIR)	99
3-5	Chip Test Register (CTR)	100
4-1	144-Pin LQFP Assignments	115
4-2	100-Pin LQFP Assignments	116
5-1	Reset Controller Block Diagram	131
5-2	Reset Control Register (RCR)	133
5-3	Reset Status Register (RSR)	134
5-4	Reset Test Register (RTR)	135
5-5	Reset Control Flow	139
6-1	M•CORE Processor Block Diagram	145
6-2	Programming Model	147
6-3	Data Organization in Memory	149
6-4	Data Organization in Registers	149
7-1	Interrupt Controller Block Diagram	155
7-2	Interrupt Control Register (ICR)	157
7-3	Interrupt Status Register (ISR)	159
7-4	Interrupt Force Register High (IFRH)	160
7-5	Interrupt Force Register Low (IFRL)	161

Freescale Semiconductor, Inc.

List of Figures

Figure	Title	Page
7-6	Interrupt Pending Register (IPR)	162
7-7	Normal Interrupt Enable Register (NIER)	163
7-8	Normal Interrupt Pending Register (NIPR)	164
7-9	Fast Interrupt Enable Register (FIER)	165
7-10	Fast Interrupt Pending Register (FIPR)	166
7-11	Priority Level Select Registers (PLSR0–PLSR39)	167
9-1	CMFR 128-Kbyte Block Diagram	183
9-2	CMFR Array and Control Register Addressing	186
9-3	CMFR Module Configuration Register (CMFRMCR)	188
9-4	CMFR Module Test Register (CMFRMTR)	193
9-5	CMFR High-Voltage Control Register (CMFRCTL)	196
9-6	Pulse Status Timing	197
9-7	FLASH Programming Flowchart	209
9-8	Program State Diagram	210
9-9	FLASH Erasing Flowchart	216
9-10	Erase State Diagram	217
10-1	Clock Module Block Diagram	224
10-2	Synthesizer Control Register (SYNCR)	227
10-3	Synthesizer Status Register (SYNSR)	230
10-4	Synthesizer Test Register (SYNTR)	233
10-5	Synthesizer Test Register 2 (SYNTR2)	234
10-6	Lock Detect Sequence	237
10-7	PLL Block Diagram	244
10-8	Crystal Oscillator Example	244
11-1	Ports Module Block Diagram	248
11-2	Port Output Data Registers (PORTx)	251
11-3	Port Data Direction Registers (DDRx)	252
11-4	Port Pin Data/Set Data Registers (PORTxP/SETx)	253
11-5	Port Clear Output Data Registers (CLRx)	254
11-6	Port C, D, I7, and I6 Pin Assignment Register (PCDPAR)	255
11-7	Port E Pin Assignment Register (PEPAR)	256

Freescale Semiconductor, Inc.

Figure	Title	Page
11-8	Digital Input Timing	259
11-9	Digital Output Timing	259
12-1	EPORT Block Diagram	262
12-2	EPORT Pin Assignment Register (EPPAR)	264
12-3	EPORT Data Direction Register (EPDDR)	266
12-4	EPORT Port Interrupt Enable Register (EPIER)	267
12-5	EPORT Port Data Register (EPDR)	268
12-6	EPORT Port Pin Data Register (EPPDR)	268
12-7	EPORT Port Flag Register (EPFR)	269
13-1	Watchdog Timer Block Diagram	273
13-2	Watchdog Control Register (WCR)	275
13-3	Watchdog Modulus Register (WMR)	277
13-4	Watchdog Count Register (WCNTR)	278
13-5	Watchdog Service Register (WSR)	279
14-1	PIT Block Diagram	282
14-2	PIT Control and Status Register (PCSR)	285
14-3	PIT Modulus Register (PMR)	288
14-4	PIT Count Register (PCNTR)	289
14-5	Counter Reloading from the Modulus Latch	290
14-6	Counter in Free-Running Mode	291
15-1	Timer Block Diagram	296
15-2	Timer Input Capture/Output Compare Select Register (TIMIOS)	300
15-3	Timer Compare Force Register (TIMCFORC)	301
15-4	Timer Output Compare 3 Mask Register (TIMOC3M)	302
15-5	Timer Output Compare 3 Data Register (TIMOC3D)	303
15-6	Timer Counter Register High (TIMCNTH)	304
15-7	Timer Counter Register Low (TIMCNTL)	304
15-8	Timer System Control Register (TIMSCR1)	305
15-9	Fast Clear Flag Logic	306
15-10	Timer Toggle-On-Overflow Register (TIMTOV)	306
15-11	Timer Control Register 1 (TIMCTL1)	307

Freescale Semiconductor, Inc.

List of Figures

Figure	Title	Page
15-12	Timer Control Register 2 (TIMCTL2)	308
15-13	Timer Interrupt Enable Register (TIMIE)	309
15-14	Timer System Control Register 2 (TIMSCR2)	310
15-15	Timer Flag Register 1 (TIMFLG1)	312
15-16	Timer Flag Register 2 (TIMFLG2)	313
15-17	Timer Channel [0:3] Register High (TIMCxH)	314
15-18	Timer Channel [0:3] Register Low (TIMCxL)	314
15-19	Pulse Accumulator Control Register (TIMPACTL)	315
15-20	Pulse Accumulator Flag Register (TIMPAFLG)	317
15-21	Pulse Accumulator Counter Register High (TIMPACNTH)	318
15-22	Pulse Accumulator Counter Register Low (TIMPACNTL)	318
15-23	Timer Port Data Register (TIMPORT)	319
15-24	Timer Port Data Direction Register (TIMDDR)	320
15-25	Timer Test Register (TIMTST)	321
15-26	Channel 3 Output Compare/Pulse Accumulator Logic	324
16-1	SCI Block Diagram	332
16-2	SCI Baud Rate Register High (SCIBDH)	336
16-3	SCI Baud Rate Register Low (SCIBDL)	336
16-4	SCI Control Register 1 (SCICR1)	337
16-5	SCI Control Register 2 (SCICR2)	340
16-6	SCI Status Register 1 (SCISR1)	342
16-7	SCI Status Register 2 (SCISR2)	344
16-8	SCI Data Register High (SCIDRH)	345
16-9	SCI Data Register Low (SCIDRL)	345
16-10	SCI Pullup and Reduced Drive Register (SCIPURD)	346
16-11	SCI Port Data Register (SCIPORT)	347
16-12	SCI Data Direction Register (SCIDDR)	348
16-13	SCI Data Formats	349
16-14	Transmitter Block Diagram	351
16-15	SCI Receiver Block Diagram	356
16-16	Receiver Data Sampling	357
16-17	Start Bit Search Example 1	359
16-18	Start Bit Search Example 2	360

Freescale Semiconductor, Inc.

Figure	Title	Page
16-19	Start Bit Search Example 3	360
16-20	Start Bit Search Example 4	361
16-21	Start Bit Search Example 5	361
16-22	Start Bit Search Example 6	362
16-23	Slow Data	363
16-24	Fast Data	364
16-25	Single-Wire Operation (LOOPS = 1, RSRC = 1)	366
16-26	Loop Operation (LOOPS = 1, RSRC = 0)	367
17-1	SPI Block Diagram	373
17-2	SPI Control Register 1 (SPICR1)	376
17-3	SPI Control Register 2 (SPICR2)	378
17-4	SPI Baud Rate Register (SPIBR)	379
17-5	SPI Status Register (SPISR)	381
17-6	SPI Data Register (SPIDR)	382
17-7	SPI Pullup and Reduced Drive Register (SPIPURD)	383
17-8	SPI Port Data Register (SPIPORT)	384
17-9	SPI Port Data Direction Register (SPIDDR)	385
17-10	Full-Duplex Operation	386
17-11	SPI Clock Format 1 (CPHA = 1)	389
17-12	SPI Clock Format 0 (CPHA = 0)	391
17-13	Transmission Error Due to Master/Slave Clock Skew	392
18-1	QADC Block Diagram	403
18-2	QADC Input and Output Signals	406
18-3	QADC Module Configuration Register (QADCMCR)	411
18-4	QADC Test Register (QADCTEST)	412
18-5	QADC Port QA Data Register (PORTQA)	413
18-6	QADC Port QB Data Register (PORTQB)	413
18-7	QADC Port QA Data Direction Register (DDRQA)	415
18-8	QADC Control Register 0 (QACR0)	416
18-9	QADC Control Register 1 (QACR1)	419
18-10	QADC Control Register 2 (QACR2)	422
18-11	QADC Status Register 0 (QASR0)	427
18-12	Queue Status Transition	435
18-13	QADC Status Register 1 (QASR1)	436

Freescale Semiconductor, Inc.

List of Figures

Figure	Title	Page
18-14	Conversion Command Word Table (CCW)	437
18-15	Right-Justified Unsigned Result Register (RJURR)	441
18-16	Left-Justified Signed Result Register (LJSRR)	442
18-17	Left-Justified Unsigned Result Register (LJURR)	442
18-18	External Multiplexing Configuration	445
18-19	QADC Analog Subsystem Block Diagram	447
18-20	Conversion Timing	447
18-21	Bypass Mode Conversion Timing	448
18-22	QADC Queue Operation with Pause	452
18-23	CCW Priority Situation 1	455
18-24	CCW Priority Situation 2	456
18-25	CCW Priority Situation 3	457
18-26	CCW Priority Situation 4	457
18-27	CCW Priority Situation 5	458
18-28	CCW Priority Situation 6	459
18-29	CCW Priority Situation 7	459
18-30	CCW Priority Situation 8	460
18-31	CCW Priority Situation 9	460
18-32	CCW Priority Situation 10	461
18-33	CCW Priority Situation 11	461
18-34	CCW Freeze Situation 12	462
18-35	CCW Freeze Situation 13	462
18-36	CCW Freeze Situation 14	463
18-37	CCW Freeze Situation 15	463
18-38	CCW Freeze Situation 16	463
18-39	CCW Freeze Situation 17	464
18-40	CCW Freeze Situation 18	464
18-41	CCW Freeze Situation 19	464
18-42	QADC Clock Subsystem Functions	477
18-43	QADC Clock Programmability Examples	479
18-44	QADC Conversion Queue Operation	482
18-45	Equivalent Analog Input Circuitry	487
18-46	Errors Resulting from Clipping	488
18-47	External Positive Edge Trigger Mode Timing With Pause	489
18-48	Gated Mode, Single Scan Timing	491

Freescale Semiconductor, Inc.

Figure	Title	Page
18-49	Gated Mode, Continuous Scan Timing	491
18-50	Star-Ground at the Point of Power Supply Origin	493
18-51	Input Pin Subjected to Negative Stress	494
18-52	Input Pin Subjected to Positive Stress	494
18-53	External Multiplexing of Analog Signal Sources	496
18-54	Electrical Model of an A/D Input Pin	497
19-1	Read Cycle Flowchart	511
19-2	Write Cycle Flowchart	513
19-3	Master Mode — 1-Clock Read and Write Cycle	515
19-4	Master Mode — 2-Clock Read and Write Cycle	515
19-5	Internal (Show) Cycle Followed by External 1-Clock Read	518
19-6	Internal (Show) Cycle Followed by External 1-Clock Write	519
20-1	Chip Select Block Diagram	523
20-2	Chip Select Control Register 0 (CSCR0)	525
20-3	Chip Select Control Register 1 (CSCR1)	526
20-4	Chip Select Control Register 2 (CSCR2)	526
20-5	Chip Select Control Register 3 (CSCR3)	527
21-1	Top-Level Tap Module and Low-Level (OnCE) TAP Module	536
21-2	Top-Level TAP Controller State Machine	540
21-3	IDCODE Register Bit Specification	545
21-4	OnCE Block Diagram	553
21-5	Low-Level (OnCE) Tap Module Data Registers (DRs)	554
21-6	OnCE Controller	557
21-7	OnCE Controller and Serial Interface	559
21-8	OnCE Command Register (OCMR)	562
21-9	OnCE Control Register (OCR)	564
21-10	OnCE Status Register (OSR)	568
21-11	OnCE Memory Breakpoint Logic	570
21-12	OnCE Trace Logic Block Diagram	573
21-13	CPU Scan Chain Register (CPUSCR)	576

Freescale Semiconductor, Inc.

List of Figures

Figure	Title	Page
21-14	Control State Register (CTL)	578
21-15	OnCE PC FIFO	580
21-16	Recommended Connector Interface to JTAG/OnCE Port	583
22-1	V_{PP} versus Programming Time	595
22-2	V_{PP} versus Programming Pulses	595
22-3	CLKOUT Timing	597
22-4	Clock Read/Write Cycle Timing	598
22-5	Read/Write Cycle Timing with Wait States	599
22-6	Show Cycle Timing	600
22-7	$\overline{\text{RESET}}$ and Configuration Override Timing	601
22-8	SPI Timing Diagram	603
22-9	Test Clock Input Timing	605
22-10	Boundary Scan (JTAG) Timing	606
22-11	Test Access Port Timing	606
22-12	$\overline{\text{TRST}}$ Timing	606
22-13	Debug Event Pin Timing	607

Freescale Semiconductor, Inc.

List of Tables

Table	Title	Page
2-1	Register Address Location Map	53
3-1	Signal Properties	92
3-2	Write-Once Bits Read/Write Accessibility	93
3-3	Chip Configuration Module Memory Map	94
3-4	Chip Configuration Mode Selection	95
3-5	Bus Monitor Timeout Values	97
3-6	Reset Configuration Pin States During Reset	101
3-7	Configuration During Reset	102
3-8	Chip Configuration Mode Selection	103
3-9	Chip Select $\overline{CS0}$ Configuration Encoding	104
3-10	Boot Device Selection	104
3-11	Output Pad Driver Strength Selection	105
3-12	Clock Mode Selection	105
3-13	Internal FLASH Configuration	106
4-1	Package Pinouts	110
4-2	Signal Descriptions	117
5-1	Reset Controller Signal Properties	131
5-2	Reset Controller Module Memory Map	132
5-3	Reset Source Summary	136
6-1	M•CORE Instruction Set	150
7-1	Interrupt Controller Module Memory Map	156
7-2	MASK Encoding	158
7-3	Priority Select Encoding	167
7-4	Fast Interrupt Vector Number	170

Freescale Semiconductor, Inc.

List of Tables

Table	Title	Page
7-5	Vector Table Mapping	170
7-6	Interrupt Source Assignment	172
9-1	Non-Volatile Memory FLASH Memory Map	187
9-2	Negative Voltage Modulation	194
9-3	Drain Amplitude Modulation (GDB = 0)	195
9-4	System Clock Range	198
9-5	Clock Period Exponent and Pulse Width Range	199
9-6	Determining SCLKR[2:0], CLKPE[1:0], and CLKPM[6:0]	200
9-7	Program Interlock State Descriptions	210
9-8	Results of Programming Margin Read	212
9-9	Required Programming Algorithm	213
9-10	Erase Interlock State Descriptions	217
9-11	Required Erase Algorithm	219
10-1	Signal Properties	225
10-2	Clock Module Memory Map	226
10-3	System Frequency Multiplier of the Reference Frequency in Normal PLL Mode	228
10-4	STPMD[1:0] Operation in Stop Mode	230
10-5	System Clock Modes	231
10-6	Clock-Out and Clock-In Relationships	235
10-7	Loss of Clock Summary	239
10-8	Stop Mode Operation	240
10-9	Charge Pump Current and MFD in Normal Mode Operation	245
11-1	I/O Port Module Memory Map	250
11-2	PEPAR Reset Values	256
11-3	Ports A–I Supported Pin Functions	258
12-1	Edge Port Module Memory Map	263
12-2	EPPAx Field Settings	265
13-1	Watchdog Timer Module Memory Map	274

Freescale Semiconductor, Inc.

Table	Title	Page
14-1	Programmable Interrupt Timer Modules Memory Map	284
14-2	Prescaler Select Encoding	286
14-3	PIT Interrupt Requests	292
15-1	Signal Properties	298
15-2	Timer Modules Memory Map	299
15-3	Output Compare Action Selection	307
15-4	Input Capture Edge Selection	308
15-5	Prescaler Selection	311
15-6	Clock Selection	316
15-7	TIMPORT I/O Function	325
15-8	Timer Interrupt Requests	326
16-1	Signal Properties	334
16-2	Serial Communications Interface Module Memory Map	335
16-3	SCI Normal, Loop, and Single-Wire Mode Pin Configurations	338
16-4	Example Baud Rates (System Clock = 33 MHz)	350
16-5	Example 10-Bit and 11-Bit Frames	352
16-6	Start Bit Verification	358
16-7	Data Bit Recovery	358
16-8	Stop Bit Recovery	359
16-9	SCI Port Control Summary	368
16-10	SCI Interrupt Request Sources	369
17-1	Signal Properties	374
17-2	SPI Memory Map	375
17-3	SS Pin I/O Configurations	377
17-4	Bidirectional Pin Configurations	378
17-5	SPI Baud Rate Selection (33-MHz Module Clock)	380
17-6	SPI Port Summary	384
17-7	Normal Mode and Bidirectional Mode	394
17-8	SPI Interrupt Request Sources	397

Freescale Semiconductor, Inc.

List of Tables

Table	Title	Page
18-1	Multiplexed Analog Input Channels	409
18-2	QADC Memory Map	410
18-3	Prescaler Clock High Times	417
18-4	Prescaler Clock Low Times	418
18-5	Queue 1 Operating Modes	420
18-6	Queue 2 Operating Modes	423
18-7	Pause Response	429
18-8	Queue Status	433
18-9	Input Sample Times	439
18-10	Non-Multiplexed Channel Assignments and Pin Designations	440
18-11	Multiplexed Channel Assignments and Pin Designations	440
18-12	Analog Input Channels	444
18-13	Trigger Events	454
18-14	Status Bits	454
18-15	QADC Clock Programmability	479
18-16	External Circuit Settling Time to 1/2 LSB (10-Bit Conversions)	499
18-17	Error Resulting From Input Leakage (I_{Off})	500
18-18	QADC Status Flags and Interrupt Sources	500
19-1	Signal Properties	505
19-2	Data Transfer Cases	509
19-3	EB[3:0] Assertion Encoding	510
19-4	Emulation Mode Chip-Select Summary	517
20-1	Signal Properties	524
20-2	Chip Select Memory Map	524
20-3	Chip Select Wait States Encoding	529
20-4	Chip Select Address Range Encoding	531
21-1	JTAG Instructions	542
21-2	List of Pins Not Scanned in JTAG Mode	548
21-3	Boundary-Scan Register Definition	549
21-4	OnCE Register Addressing	563

Freescale Semiconductor, Inc.

Table	Title	Page
21-5	Sequential Control Field Settings	565
21-6	Memory Breakpoint Control Field Settings	567
21-7	Processor Mode Field Settings	569
22-1	Absolute Maximum Ratings	586
22-2	Thermal Characteristics	587
22-3	ESD Protection Characteristics	587
22-4	DC Electrical Specifications	588
22-5	PLL Electrical Specifications	590
22-6	QADC Absolute Maximum Ratings	591
22-7	QADC Electrical Specifications	592
22-8	QADC Conversion Specifications	593
22-9	FLASH Program and Erase Characteristics	594
22-10	FLASH EEPROM Module Life Characteristics	594
22-11	External Interface Timing Characteristics	596
22-12	Reset and Configuration Override Timing	601
22-13	SPI Timing Characteristics	602
22-14	OnCE, JTAG, and Boundary Scan Timing	605
24-1	MC Order Numbers	615

Freescale Semiconductor, Inc.

List of Tables

Freescale Semiconductor, Inc.

Section 1. General Description

1.1 Contents

1.2 Introduction 43
1.3 Features 44
1.4 Block Diagram 48

1.2 Introduction

The MMC2107 is the first member of a family of general-purpose microcontrollers (MCU) based on the M•CORE™ M210 central processor unit (CPU).

As a low-voltage part, the MMC2107 operates at voltages between 2.7 volts and 3.6 volts. It is particularly suited for use in battery-powered applications. The operating frequency is up to a maximum of 33 MHz over a temperature range of –40°C to 85°C.

Available packages are 100-pin low-profile quad flat pack (LQFP) or a 144-pin LQFP for applications requiring the full external memory interface support or a large number of general-purpose inputs/outputs (GPIO).

™M•CORE is a trademark of Motorola, Inc.

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1.3 Features

Features of the MMC2107 include:

- M•CORE M210 integer processor:
  - 32-bit reduced instruction set computer (RISC) architecture
  - Low power and high performance
- OnCE™ debug support
- On-chip 128-Kbyte FLASH:
  - Motorola's one transistor, CDR MoneT(1) FLASH bit cell
  - Page mode (2111) read access
  - External V_{PP} required for programming
  - 16-K block size
- On-chip, 8-Kbyte static random-access memory (SRAM):
  - One clock per access (including bytes, half-words, and words)
  - Byte, half-word (16 bits), and word (32 bits) read/write accesses
  - Standby power supply support
- Serial peripheral interface (SPI):
  - Master mode and slave mode
  - Wired-OR mode
  - Slave select output
  - Mode fault error flag with CPU interrupt capability
  - Double-buffered operation
  - Serial clock with programmable polarity and phase
  - Control of SPI operation during wait mode
  - Reduced drive control

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™OnCE is a trademark of Motorola, Inc.

1. CDR MoneT designates the Motorola one-transistor bitcell.

- Two serial communications interfaces (SCI):
  - Full-duplex operation
  - Standard mark/space non-return-to-zero (NRZ) format
  - 13-bit baud rate selection
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver
  - Separate receiver and transmitter CPU interrupt requests
  - Programmable transmitter output polarity
  - Two receiver wakeup methods (idle line and address mark)
  - Interrupt-driven operation with eight flags
  - Receiver framing error detection
  - Hardware parity checking
  - 1/16 bit-time noise detection
  - General-purpose input/output port
- Two timers:
  - Four 16-bit input capture/output compare channels
  - 16-bit architecture
  - 16-bit pulse accumulator
  - Pulse widths variable from microseconds to seconds
  - Prescaler
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - Timer port pullups enabled on reset
- Queued analog-to-digital converter (QADC):
  - Eight analog input channels
  - 10-bit resolution ±2 counts accuracy
  - Minimum 7 µs conversion time
  - Internal sample and hold
  - Programmable input sample time for various source impedances
  - Two conversion command queues with a total of 64 entries
  - Subqueues possible using pause mechanism
  - Queue complete and pause software interrupts available on both queues

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- Queue pointers indicate current location for each queue
- Automated queue modes initiated by:
  - External edge trigger and gated trigger
  - Periodic/interval timer, within queued analog-to-digital converter (QADC) module {queue1 and queue2}
  - Software command
- Single-scan or continuous-scan of queues
- Output data readable in three formats:
  - Right-justified unsigned
  - Left-justified signed
  - Left-justified unsigned
- Unused analog channels can be used as digital input/output (I/O)
- Minimum pin set configuration implemented

• Interrupt controller:
- Up to 40 interrupt sources
- 32 unique programmable priority levels for each interrupt source
- Independent enable/disable of pending interrupts based on priority level
- Select normal or fast interrupt request for each priority level
- Fast interrupt requests always have priority over normal interrupts.
- Ability to mask interrupts at and below a defined priority level
- Ability to select between autovectored or vectored interrupt requests
- Vectored interrupts generated based on priority level
- Ability to generate a separate vector number for normal and fast interrupts
- Ability for software to self-schedule interrupts
- Software visibility of pending interrupts and interrupt signals to core
- Asynchronous operation to support wakeup from low-power modes

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- External interrupts supported:
  - Rising/falling edge select
  - Low-level sensitive
  - Ability for software generation of external interrupt event
  - General-purpose input/output support
- Periodic interval timer:
  - 16-bit counter
  - Selectable as free running or count down
- Watchdog timer:
  - 16-bit counter
  - Low-power mode support
- Phase-lock loop (PLL):
  - Reference crystal from 2 to 10 MHz
  - Low-power modes supported
  - Separate clock-out signal
- Reset:
  - Separate reset in and reset out signals
  - Six sources of reset:
    Power-on reset (POR)
    External
    Software
    Watchdog
    Loss of clock
    Loss of lock
  - Status flag indication of source of last reset
- Chip configurations:
  - Support for single-chip, master, emulation, and test modes
  - System configuration during reset
  - Bus monitor
  - Configurable output pad drive strength control

Freescale Semiconductor, Inc.

- General-purpose input/output (GPIO):
  - Up to 72 bits of GPIO
  - Coherent 32-bit control
  - Bit manipulation supported via set/clear functions
  - Unused peripheral pins may be used as extra GPIO.
  - Reduced drive control
- M•CORE to IPbus interface:
  - Complete interfacing between the M•CORE bus and the IPbus peripheral bus
  - Minimum of three clocks for peripheral bus access
  - Data alignment and data width conversion between the M•CORE 32-bit data bus and the IPbus peripheral data buses
- External interface:
  - Provides for direct support of asynchronous random-access memory (RAM), read-only memory (ROM), and FLASH
  - Support interfacing to 16-bit and 32-bit data buses
  - 32-bit external bidirectional data bus
  - 23-bit address bus
  - Four chip selects
  - Byte/write enables
  - Ability to boot from internal or external memories
  - Internal bus activity is visible via show-cycle mode
  - Special chip selects support replacement of GPIO with external logic (port replacement logic)
  - Emulation of internal page mode FLASH support
- Joint Test Action Group (JTAG) support for system-level board testing

1.4 Block Diagram

The basic structure of the MMC2107 is shown in **Figure 1-1**.

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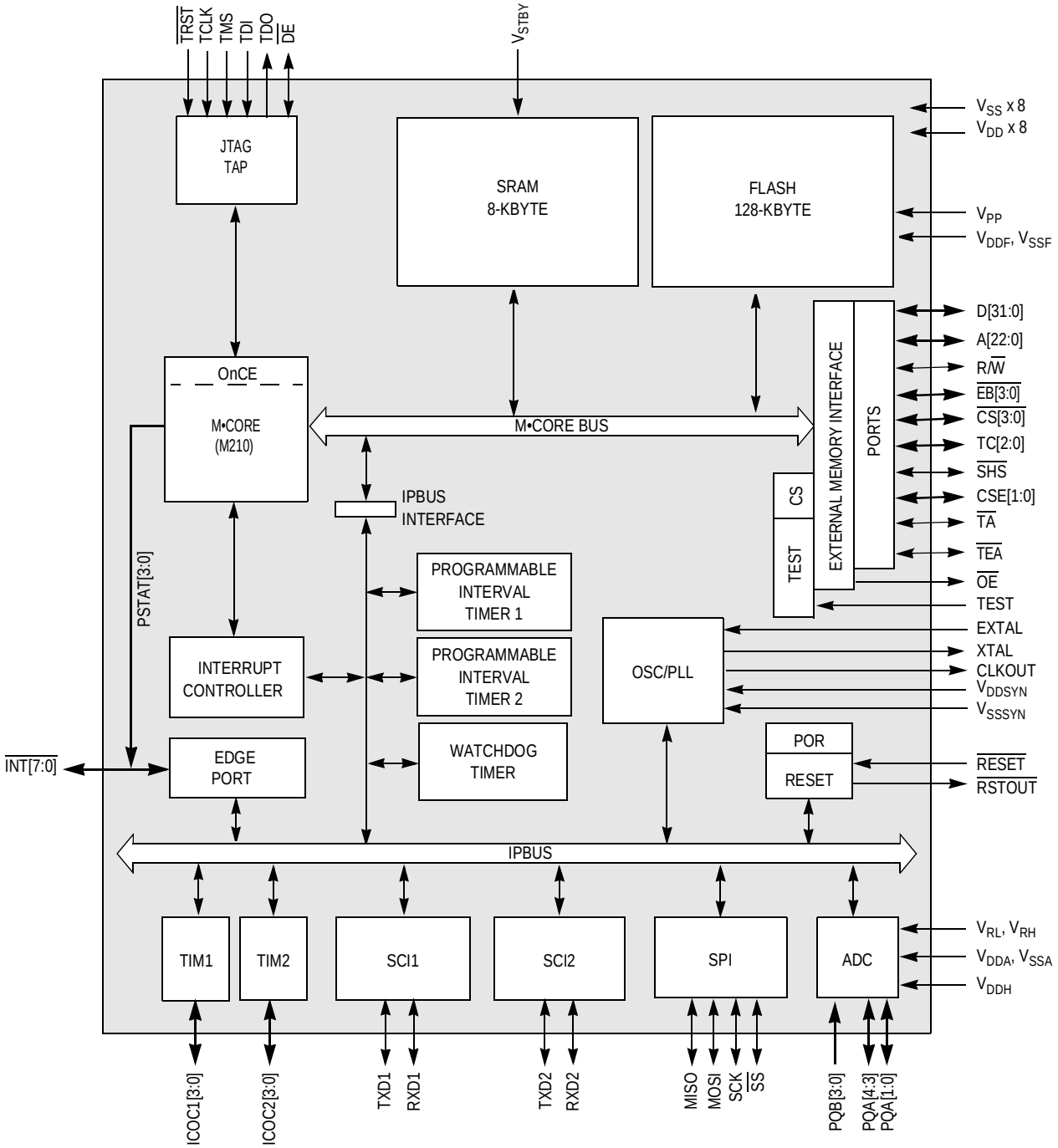

Figure 1-1. Block Diagram

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General Description

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Section 2. System Memory Map

2.1 Contents

2.2 Introduction 51
2.3 Address Map. 52
2.4 Register Map 54

2.2 Introduction

The address map, shown in **Figure 2-1**, includes:

- 128 Kbytes of internal FLASH
- 8 Kbytes of internal static random-access memory (SRAM)
- Internal memory mapped registers
- External address space

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2.3 Address Map

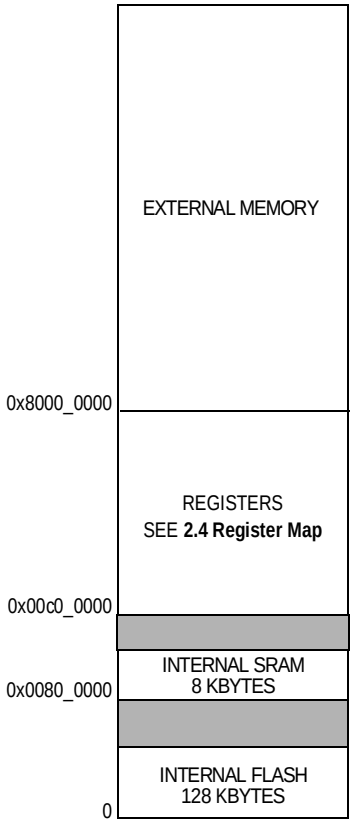

Figure 2-1. Address Map

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Table 2-1. Register Address Location Map[1]

Base Address (Hex)	Usage
0x00c0_0000	Ports[2] (PORTS)
0x00c1_0000	Chip configuration (CCM)
0x00c2_0000	Chip selects (CS)
0x00c3_0000	Clocks (CLOCK)
0x00c4_0000	Reset (RESET)
0x00c5_0000	Interrupt controller (INTC)
0x00c6_0000	Edge port (EPORT)
0x00c7_0000	Watchdog timer (WDT)
0x00c8_0000	Programmable interrupt timer 1 (PIT1)
0x00c9_0000	Programmable interrupt timer 2 (PIT2)
0x00ca_0000	Queued analog-to-digital converter (QADC)
0x00cb_0000	Serial peripheral interface (SPI)
0x00cc_0000	Serial communications interface 1 (SCI1)
0x00cd_0000	Serial communications interface 2 (SCI2)
0x00ce_0000	Timer 1 (TIM1)
0x00cf_0000	Timer 2 (TIM2)
0x00d0_0000	FLASH registers (CMFR)

1. See module sections for details of how much of each block is being decoded. Accesses to addresses outside the module memory maps (and also the reserved area 0x00d1_0000–0x7fff_ffff) will not be responded to and will result in a bus monitor transfer error exception.
2. The port register space is mirrored/repeated in the 64-Kbyte block. This allows the full 64-Kbyte block to be decoded and used to execute an external access to a port replacement unit in emulation mode.

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2.4 Register Map

Address	Register Name		Bit Number							
Ports (PORTS)										
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0000	Port A Output Data Register (PORTA) See page 251.	Read: Write:	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0001	Port B Output Data Register (PORTB) See page 251.	Read: Write:	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0002	Port C Output Data Register (PORTC) See page 251.	Read: Write:	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0003	Port D Output Data Register (PORTD) See page 251.	Read: Write:	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0004	Port E Output Data Register (PORTE) See page 251.	Read: Write:	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0
		Reset :	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0005	Port F Output Data Register (PORTF) See page 251.	Read: Write:	PORTF7	PORTF6	PORTF5	PORTF4	PORTF3	PORTF2	PORTF1	PORTF0
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0006	Port G Output Data Register (PORTG) See page 251.	Read: Write:	PORTG7	PORTG6	PORTG5	PORTG4	PORTG3	PORTG2	PORTG1	PORTG0
		Reset:	1	1	1	1	1	1	1	1

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 1 of 34)

Freescale Semiconductor, Inc.

Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0007	Port H Output Data Register (PORTH) See page 251.	Read: Write:	PORTH7	PORTH6	PORTH5	PORTH4	PORTH3	PORTH2	PORTH1	PORTH0
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0008	Port I Output Data Register (PORTI) See page 251.	Read: Write:	PORTI7	PORTI6	PORTI5	PORTI4	PORTI3	PORTI2	PORTI1	PORTI0
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0009 ↓ 0x00c0_000b	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_000c	Port A Data Direction Register (DDRA) See page 252.	Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_000d	Port B Data Direction Register (DDRB) See page 252.	Read: Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_000e	Port C Data Direction Register (DDRC) See page 252.	Read: Write:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_000f	Port D Data Direction Register (DDRD) See page 252.	Read: Write:	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0010	Port E Data Direction Register (DDRE) See page 252.	Read: Write:	DDRE7	DDRE6	DDRE5	DDRE4	DDRE3	DDRE2	DDRE1	DDRE0
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 2 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0011	Port F Data Direction Register (DDRF) See page 252.	Read: Write:	DDRF7	DDRF6	DDRF5	DDRF4	DDRF3	DDRF2	DDRF1	DDRF0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0012	Port G Data Direction Register (DDRG) See page 252.	Read: Write:	DDRG7	DDRG6	DDRG5	DDRG4	DDRG3	DDRG2	DDRG1	DDRG0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0013	Port H Data Direction Register (DDRH) See page 252.	Read: Write:	DDRH7	DDRH6	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0014	Port I Data Direction Register (DDRI) See page 252.	Read: Write:	DDRI7	DDRI6	DDRI5	DDRI4	DDRI3	DDRI2	DDRI1	DDRI0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0015 ↓ 0x00c0_0017	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0018	Port A Pin Data/Set Data Register (PORTAP/SETA) See page 253.	Read:	PORTAP7	PORTAP6	PORTAP5	PORTAP4	PORTAP3	PORTAP2	PORTAP1	PORTAP0
		Write:	SETA7	SETA6	SETA5	SETA4	SETA3	SETA2	SETA1	SETA0
		Reset:	P	P	P	P	P	P	P	P
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0019	Port B Pin Data/Set Data Register (PORTBP/SETB) See page 253.	Read:	PORTBP7	PORTBP6	PORTBP5	PORTBP4	PORTBP3	PORTBP2	PORTBP1	PORTBP0
		Write:	SETB7	SETB6	SETB5	SETB4	SETB3	SETB2	SETB1	SETB0
		Reset:	P	P	P	P	P	P	P	P
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_001a	Port C Pin Data/Set Data Register (PORTCP/SETC) See page 253.	Read:	PORTCP7	PORTCP6	PORTCP5	PORTCP4	PORTCP3	PORTCP2	PORTCP1	PORTCP0
		Write:	SETC7	SETC6	SETC5	SETC4	SETC3	SETC2	SETC1	SETC0
		Reset:	P	P	P	P	P	P	P	P

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 3 of 34)

Freescale Semiconductor, Inc.

Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_001b	Port D Pin Data/Set Data Register (PORTDP/SETD) See page 253.	Read:	PORTDP7	PORTDP6	PORTDP5	PORTDP4	PORTDP3	PORTDP2	PORTDP1	PORTDP0
		Write:	SETD7	SETD6	SETD5	SETD4	SETD3	SETD2	SETD1	SETD0
		Reset:	P	P	P	P	P	P	P	P
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_001c	Port E Pin Data/Set Data Register (PORTEP/SETE) See page 253.	Read:	PORTEP7	PORTEP6	PORTEP5	PORTEP4	PORTEP3	PORTEP2	PORTEP1	PORTEP0
		Write:	SETE7	SETE6	SETE5	SETE4	SETE3	SETE2	SETE1	SETE0
		Reset:	P	P	P	P	P	P	P	P
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_001d	Port F Pin Data/Set Data Register (PORTFP/SETF) See page 253.	Read:	PORTFP7	PORTFP6	PORTFP5	PORTFP4	PORTFP3	PORTFP2	PORTFP1	PORTFP0
		Write:	SETF7	SETF6	SETF5	SETF4	SETF3	SETF2	SETF1	SETF0
		Reset:	P	P	P	P	P	P	P	P
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_001e	Port G Pin Data/Set Data Register (PORTGP/SETG) See page 253.	Read:	PORTGP7	PORTGP6	PORTGP5	PORTGP4	PORTGP3	PORTGP2	PORTGP1	PORTGP0
		Write:	SETG7	SETG6	SETG5	SETG4	SETG3	SETG2	SETG1	SETG0
		Reset:	P	P	P	P	P	P	P	P
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_001f	Port H Pin Data/Set Data Register (PORTHP/SETH) See page 253.	Read:	PORTHP7	PORTHP6	PORTHP5	PORTHP4	PORTHP3	PORTHP2	PORTHP1	PORTHP0
		Write:	SETH7	SETH6	SETH5	SETH4	SETH3	SETH2	SETH1	SETH0
		Reset:	P	P	P	P	P	P	P	P
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0020	Port I Pin Data/Set Data Register (PORTIP/SETI) See page 253.	Read:	PORTIP7	PORTIP6	PORTIP5	PORTIP4	PORTIP3	PORTIP2	PORTIP1	PORTIP0
		Write:	SETI7	SETI6	SETI5	SETI4	SETI3	SETI2	SETI1	SETI0
		Reset:	P	P	P	P	P	P	P	P
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0021 ↓ 0x00c0_0023	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0024	Port A Clear Output Data Register (CLRA) See page 254.	Read:	0	0	0	0	0	0	0	0
		Write:	CLRA7	CLRA6	CLRA5	CLRA4	CLRA3	CLRA2	CLRA1	CLRA0
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 4 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0025	Port B Clear Output Data Register (CLRB) See page 254.	Read:	0	0	0	0	0	0	0	0
		Write:	CLRB7	CLRB6	CLRB5	CLRB4	CLRB3	CLRB2	CLRB1	CLRB0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0026	Port C Clear Output Data Register (CLRC) See page 254.	Read:	0	0	0	0	0	0	0	0
		Write:	CLRC7	CLRC6	CLRC5	CLRC4	CLRC3	CLRC2	CLRC1	CLRC0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0027	Port D Clear Output Data Register (CLRD) See page 254.	Read:	0	0	0	0	0	0	0	0
		Write:	CLRD7	CLRD6	CLRD5	CLRD4	CLRD3	CLRD2	CLRD1	CLRD0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0028	Port E Clear Output Data Register (CLRE) See page 254.	Read:	0	0	0	0	0	0	0	0
		Write:	CLRE7	CLRE6	CLRE5	CLRE4	CLRE3	CLRE2	CLRE1	CLRE0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0029	Port F Clear Output Data Register (CLRF) See page 254.	Read:	0	0	0	0	0	0	0	0
		Write:	CLRF7	CLRF6	CLRF5	CLRF4	CLRF3	CLRF2	CLRF1	CLRF0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_002a	Port G Clear Output Data Register (CLRG) See page 254.	Read:	0	0	0	0	0	0	0	0
		Write:	CLRG7	CLRG6	CLRG5	CLRG4	CLRG3	CLRG2	CLRG1	CLRG0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_002b	Port H Clear Output Data Register (CLRH) See page 254.	Read:	0	0	0	0	0	0	0	0
		Write:	CLRH7	CLRH6	CLRH5	CLRH4	CLRH3	CLRH2	CLRH1	CLRH0
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 5 of 34)

Freescale Semiconductor, Inc.

Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_002c	Port I Clear Output Data Register (CLRI) See page 254.	Read:	0	0	0	0	0	0	0	0
		Write:	CLRI7	CLRI6	CLRI5	CLRI4	CLRI3	CLRI2	CLRI1	CLRI0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_002d ↓ 0x00c0_002f	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0030	Port C/D Pin Assignment Register (PCDPAR) See page 255.	Read:	PCDPA	0	0	0	0	0	0	0
		Write:								
		Reset:	See note	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0031	Port E Pin Assignment Register (PEPAR) See page 256.	Read:	PEPA7	PEPA6	PEPA5	PEPA4	PEPA3	PEPA2	PEPA1	PEPA0
		Write:								
		Reset:	Reset state determined during reset configuration as shown in **Table 11-2. PEPAR Reset Values**.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0032 ↓ 0x00c0_003f	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c0_0040 ↓ 0x00c0_ffff	Reserved		Ports register space (block of 0x00c0_0000 through 0x00c0_oo3f) is mirrored/repeated.							

Note: Reset state determined during reset configuration. PCDPA = 1 except in single-chip mode or when an external boot device is selected with a 16-bit port size in master mode.

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 6 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
Chip Configuration Module (CCM)										
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c1_0000 0x00c1_0001	Chip Configuration Register (CCR) See page 94.	Read:	LOAD	0	SHEN	EMINT	0	MODE2	MODE1	MODE0
		Write:								
		Reset:	Note 1	0	Note 2	Note 2	0	Note 1	Note 1	Note 1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	SZEN	PSTEN	SHINT	BME	BMD	BMT1	BMT0
		Write:								
		Reset:	0	Note 3	Note 2	0	1	0	0	0
0x00c1_0002	Reserved		Bit 7	6	5	4	3	2	1	Bit 0
			Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
0x00c1_0003	Reserved		Bit 7	6	5	4	3	2	1	Bit 0
			Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c1_0004 0x00c1_0005	Reset Configuration Register (RCON) See page 97.	Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	1 RPLLSEL	1 RPLLREF	0 RLOAD	0	1 BOOTPS	0 BOOTSEL	0	0 MODE
		Write:								
		Reset:	1	1	0	0	1	0	0	0

Notes:
1. Determined during reset configuration
2. 0 for all configurations except emulation mode, 1 for emulation mode
3. 0 for all configurations except emulation and master modes, 1 for emulation and master modes

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 7 of 34)

Freescale Semiconductor, Inc.

Address	Register Name		Bit Number							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c1_0006 0x00c1_0007	Chip Identification Register (CIR) See page 99.	Read:	0 PIN7	0 PIN6	0 PIN5	1 PIN4	0 PIN3	1 PIN2	1 PIN1	1 PIN0
		Write:								
		Reset:	0	0	0	1	0	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0 PRN7	0 PRN6	0 PRN5	0 PRN4	0 PRN3	0 PRN2	0 PRN1	0 PRN0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c1_0008 0x00c1_0009	Chip Test Register (CTR) See page 100.	Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c1_000a 0x00c1_000b	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c1_000c ↓ 0x00c1_000f	Unimplemented		Access results in the module generating an access termination transfer error.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c1_0010 ↓ 0x00c1_ffff	Unimplemented		Access results in a bus monitor timeout generating an access termination transfer error.							

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 8 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
Chip Selects (CS)										
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c2_0000 0x00c2_0001	Chip Select Control Register 0 (CSCR0) See page 525.	Read: Write:	SO	RO	PS	WWS	WE	WS2	WS1	WS0
		Reset:	0	0	See note	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	0	0	0	0	0	TAEN	CSEN
		Write:								
		Reset:	0	0	0	0	0	0	1	See note
			Note: Reset state determined during reset configuration.							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c2_0002 0x00c2_0003	Chip Select Control Register 1 (CSCR1) See page 526.	Read: Write:	SO	RO	PS	WWS	WE	WS2	WS1	WS0
		Reset:	0	0	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	0	0	0	0	0	TAEN	CSEN
		Write:								
		Reset:	0	0	0	0	0	0	1	See note
			Note: Reset state determined during reset configuration							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c2_0004 0x00c2_0005	Chip Select Control Register 2 (CSCR2) See page 526.	Read: Write:	SO	RO	PS	WWS	WE	WS2	WS1	WS0
		Reset:	0	0	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	0	0	0	0	0	TAEN	CSEN
		Write:								
		Reset:	0	0	0	0	0	0	1	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 9 of 34)

Freescale Semiconductor, Inc.

Address	Register Name		Bit Number							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c2_0006 0x00c2_0007	Chip Select Control Register 3 (CSCR3) See page 527.	Read: Write:	SO	RO	PS	WWS	WE	WS2	WS1	WS0
		Reset:	0	0	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	0	0	0	0	0	TAEN	CSEN
		Write:								
		Reset:	0	0	0	0	0	0	1	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c2_0008 ↓ 0x00c2_ffff	Unimplemented		Access results in a bus monitor timeout generating an access termination transfer error.							

Clocks (CLOCK)

			Bit 15	14	13	12	11	10	9	Bit 8
0x00c3_0000 0x00c3_0001	Synthesizer Control Register (SYNCR) See page 227.	Read: Write:	LOLRE	MFD2	MFD1	MFD0	LOCRE	RFD2	RFD1	RFD0
		Reset:	0	0	1	0	0	0	0	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	LOCEN	DISCLK	FWKUP	RSVD4	STMPD1	STMPD0	RSVD1	RSVD0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c3_0002	Synthesizer Status Register (SYNSR) See page 230.	Read:	PLLMODE	PLLSEL	PLLREF	LOCKS	LOCK	LOCS	0	0
		Write:								
		Reset:	Note 1	Note 1	Note 1	Note 2	Note 2	0	0	0

Notes:
1. Reset state determined during reset configuration
2. See the LOCKS and LOCK bit descriptions.

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 10 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c3_0003	Synthesizer Test Register (SYNTR) See page 233.	Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 31	30	29	28	27	26	25	Bit 24
0x00c3_0004 0x00c3_0005 0x00c3_0006 0x00c3_0007	Synthesizer Test Register 2 (SYNTR2) See page 234.	Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 23	22	21	20	19	18	17	Bit 16
		Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
		Read:	0	0	0	0	0	0	RSVD9	RSVD8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	RSVD7	RSVD6	RSVD5	RSVD4	RSVD3	RSVD2	RSVD2	RSVD0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c3_0008 ↓ 0x00c3_ffff	Unimplemented		Access results in a bus monitor timeout generating an access termination transfer error.							

Reset (RESET)

			Bit 7	6	5	4	3	2	1	Bit 0
0x00c4_0000	Reset Control Register (RCR) See page 133.	Read:	SOFTRST	FRC-RSTOUT	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 11 of 34)

Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c4_0001	Reset Status Register (RSR) See page 134.	Read:	0	0	SOFT	WDR	POR	EXT	LOC	LOL
		Write:								
		Reset:	0	0	Reset dependent					
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c4_0002	Reset Test Register (RTR) See page 135.	Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c4_0003	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c4_0004 ↓ 0x00c4_ffff	Unimplemented		Access results in a bus monitor timeout generating an access termination transfer error.							

Interrupt Controller (INTC)

			Bit 15	14	13	12	11	10	9	Bit 8
0x00c5_0000 0x00c5_0001	Interrupt Control Register (ICR) See page 157.	Read:	AE	FVE	ME	MFI	0	0	0	0
		Write:								
		Reset:	1	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	0	0	MASK4	MASK3	MASK2	MASK1	MASK0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c5_0002 0x00c5_0003	Interrupt Status Register (ISR) See page 159.	Read:	0	0	0	0	0	0	INT	FINT
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	VEC6	VEC5	VEC4	VEC3	VEC2	VEC1	VEC0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 12 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
			Bit 31	30	29	28	27	26	25	Bit 24
0x00c5_0004 0x00c5_0005 0x00c5_0006 0x00c5_0007	Interrupt Force Register High (IFRH) See page 160.	Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 23	22	21	20	19	18	17	Bit 16
		Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
		Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	IF39	IF38	IF37	IF36	IF35	IF34	IF33	IF32
		Reset:	0	0	0	0	0	0	0	0
			Bit 31	30	29	28	27	26	25	Bit 24
0x00c5_0008 0x00c5_0009 0x00c5_000a 0x00c5_000b	Interrupt Force Register Low (IFRL) See page 161.	Read: Write:	IF31	IF30	IF29	IF28	IF27	IF26	IF25	IF24
		Reset:	0	0	0	0	0	0	0	0
			Bit 23	22	21	20	19	18	17	Bit 16
		Read: Write:	IF23	IF22	IF21	IF20	IF19	IF18	IF17	IF16
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
		Read: Write:	IF15	IF14	IF13	IF12	IF11	IF10	IF9	IF8
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	IF7	IF6	IF5	IF4	IF3	IF2	IF1	IF0
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 13 of 34)

Freescale Semiconductor, Inc.

Address	Register Name		Bit Number							
			Bit 31	30	29	28	27	26	25	Bit 24
0x00c5_000c 0x00c5_000d 0x00c5_000e 0x00c5_000f	Interrupt Pending Register (IPR) See page 162.	Read:	IP31	IP30	IP29	IP28	IP27	IP26	IP25	IP24
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 23	22	21	20	19	18	17	Bit 16
		Read:	IP23	IP22	IP21	IP20	IP19	IP18	IP17	IP16
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
		Read:	IP15	IP14	IP13	IP12	IP11	IP10	IP9	IP8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 31	30	29	28	27	26	25	Bit 24
0x00c5_0010 0x00c5_0011 0x00c5_0012 0x00c5_0013	Normal Interrupt Enable Register (NIER) See page 163.	Read: Write:	NIE31	NIE30	NIE29	NIE28	NIE27	NIE26	NIE25	NIE24
		Reset:	0	0	0	0	0	0	0	0
			Bit 23	22	21	20	19	18	17	Bit 16
		Read: Write:	NIE23	NIE22	NIE21	NIE20	NIE19	NIE18	NIE17	NIE16
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
		Read: Write:	NIE15	NIE14	NIE13	NIE12	NIE11	NIE10	NIE9	NIE8
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	NIE7	NIE6	NIE5	NIE4	NIE3	NIE2	NIE1	NIE0
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 14 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
			Bit 31	30	29	28	27	26	25	Bit 24
0x00c5_0014 0x00c5_0015 0x00c5_0016 0x00c5_0017	Normal Interrupt Pending Register (NIPR) See page 164.	Read:	NIP31	NIP30	NIP29	NIP28	NIP27	NIP26	NIP25	NIP24
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 23	22	21	20	19	18	17	Bit 16
		Read:	NIP23	NIP22	NIP21	NIP20	NIP19	NIP18	NIP17	NIP16
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
		Read:	NIP15	NIP14	NIP13	NIP12	NIP11	NIP10	NIP9	NIP8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	NIP7	NIP6	NIP5	NIP4	NIP3	NIP2	NIP1	NIP0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 31	30	29	28	27	26	25	Bit 24
0x00c5_0018 0x00c5_0019 0x00c5_001a 0x00c5_001b	Fast Interrupt Enable Register (FIER) See page 165.	Read: Write:	FIE31	FIE30	FIE29	FIE28	FIE27	FIE26	FIE25	FIE24
		Reset:	0	0	0	0	0	0	0	0
			Bit 23	22	21	20	19	18	17	Bit 16
		Read: Write:	FIE23	FIE22	FIE21	FIE20	FIE19	FIE18	FIE17	FIE16
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
		Read: Write:	FIE15	FIE14	FIE13	FIE12	FIE11	FIE10	FIE9	FIE8
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	FIE7	FIE6	FIE5	FIE4	FIE3	FIE2	FIE1	FIE0
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 15 of 34)

Freescale Semiconductor, Inc.

Address	Register Name		Bit Number							
			Bit 31	30	29	28	27	26	25	Bit 24
0x00c5_001c 0x00c5_001d 0x00c5_001e 0x00c5_001f	Fast Interrupt Pending Register (FIPR) See page 166.	Read:	FIP31	FIP30	FIP29	FIP28	FIP27	FIP26	FIP25	FIP24
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 23	22	21	20	19	18	17	Bit 16
		Read:	FIP23	FIP22	FIP21	FIP20	FIP19	FIP18	FIP17	FIP16
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
		Read:	FIP15	FIP14	FIP13	FIP12	FIP11	FIP10	FIP9	FIP8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	FIP7	FIP6	FIP5	FIP4	FIP3	FIP2	FIP1	FIP0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c5_0040 through 0x00c5_0067	Priority Level Select Registers (PLSR39—PLSR0) See page 167.	Read:	0	0	0	PLS4	PLS3	PLS2	PLS1	PLS0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c5_0068 ↓ 0x00c5_007f	Unimplemented		Access results in the module generating an access termination transfer error.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c5_0080 ↓ 0x00c5_ffff	Unimplemented		Access results in a bus monitor timeout generating an access termination transfer error.							

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 16 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
Edge Port (EPORT)										
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c6_0000 0x00c6_0001	EPORT Pin Assignment Register (EPPAR) See page 264.	Read: Write:	EPPA7		EPPA6		EPPA5		EPPA4	
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	EPPA3		EPPA2		EPPA1		EPPA0	
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0002	EPORT Data Direction Register (EPDDR) See page 266.	Read: Write:	EPDD7	EPDD6	EPDD5	EPDD4	EPDD3	EPDD2	EPDD1	EPDD0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0003	EPORT Port Interrupt Enable Register (EPIER) See page 267.	Read: Write:	EPIE7	EPIE6	EPIE5	EPIE4	EPIE3	EPIE2	EPIE1	EPIE0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0004	EPORT Port Data Register (EPDR) See page 268.	Read: Write:	EPD7	EPD6	EPD5	EPD4	EPD3	EPD2	EPD1	EPD0
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0005	EPORT Port Pin Data Register (EPPDR) See page 268.	Read: Write:	EPPD7	EPPD6	EPPD5	EPPD4	EPPD3	EPPD2	EPPD1	EPPD0
		Reset:	P	P	P	P	P	P	P	P
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0006	EPORT Port Flag Regiser (EPFR) See page 269.	Read: Write:	EPF7	EPF6	EPF5	EPF4	EPF3	EPF2	EPF1	EPF0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0007	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 17 of 34)

Address	Register Name	Bit Number							
		Bit 7	6	5	4	3	2	1	Bit 0
0x00c6_0008 ↓ 0x00c6_ffff	Unimplemented	Access results in a bus monitor timeout generating an access termination transfer error.							

Watchdog Timer (WDT)

			Bit 15	14	13	12	11	10	9	Bit 8
0x00c7_0000 0x00c7_0001	Watchdog Control Register (WCR) See page 275.	Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	0	0	0	WAIT	DOZE	DBG	EN
		Write:								
		Reset:	0	0	0	0	1	1	1	1
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c7_0002 0x00c7_0003	Watchdog Modulus Register (WMR) See page 277.	Read:	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c7_0004 0x00c7_0005	Watchdog Count Register (WCNTR) See page 278.	Read:	WC15	WC14	WC13	WC12	WC11	WC10	WC9	WC8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0
		Write:								
		Reset:	1	1	1	1	1	1	1	1

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 18 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c7_0006 0x00c7_0007	Watchdog Service Register (WSR) See page 279.	Read: Write:	WS15	WS14	WS13	WS12	WS11	WS10	WS9	WS8
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	WS7	WS6	WS5	WS4	WS3	WS2	WS1	WS0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c7_0008 ↓ 0x00c7_ffff	Unimplemented		Access results in a bus monitor timeout generating an access termination transfer error.							

Programmable Interrupt Timer 1 (PIT1) and Programming Interrupt Timer 2 (PIT2)

Note: Addresses for PIT1 are at 0x00c8_#### and addresses for PIT2 are at 0x00c9_####.

			Bit 15	14	13	12	11	10	9	Bit 8
0x00c8_0000 0x00c8_0001 0x00c9_0000 0x00c9_0001	PIT Control and Status Register (PCSR) See page 285.	Read: Write:	0	0	0	0	PRE3	PRE2	PRE1	PRE0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	0	PDOZE	PDBG	OVW	PIE	PIF	RLD	EN
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c8_0002 0x00c8_0003 0x00c9_0002 0x00c9_0003	PIT Modulus Register (PMR) See page 288.	Read: Write:	PM15	PM14	PM13	PM12	PM11	PM10	PM9	PM8
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0
		Reset:	1	1	1	1	1	1	1	1

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 19 of 34)

Freescale Semiconductor, Inc.

Address	Register Name		Bit Number							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00c8_0004 0x00c8_0005 0x00c9_0004 0x00c9_0005	PIT Count Register (PCNTR) See page 289.	Read:	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00c8_0006 ↓ 0x00c8_0007	Unimplemented		Access results in the module generating an access termination transfer error.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ca_0008 ↓ 0x00ca_ffff	Unimplemented		Access results in a bus monitor timeout generating an access termination transfer error.							

Queued Analog-to-Digital Converter (QADC)

			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0000 0x00ca_0001	QADC Module Configuration Register (QADCMCR) See page 411.	Read:	QSTOP	QDBG	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	SUPV	0	0	0	0	0	0	0
		Write:								
		Reset:	1	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0002 0x00ca_0003	QADC Test Register (QADCTEST) See page 412.		Access results in the module generating an access termination transfer error if not in test mode.							
			Bit 7	6	5	4	3	2	1	Bit 0
			Access results in the module generating an access termination transfer error if not in test mode.							

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 20 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
0x00ca_0004 0x00ca_0005	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
			Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ca_0006	QADC Port A Data Register (PORTQA) See page 413.	Read:	0	0	0	PQA4	PQA3	0	PQA1	PQA0
		Write:								
		Reset:	0	0	0	P	P	0	P	P
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ca_0007	QADC Port B Data Register (PORTQB) See page 413.	Read:	0	0	0	0	PQB3	PQB2	PQB1	PQB0
		Write:								
		Reset:	0	0	0	0	P	P	P	P
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0008 0x00ca_0009	QADC Port A Data Direction Register (DDRQA) See page 415.	Read:	0	0	0	DDQA4	DDQA3	0	DDQA1	DDQA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_000a 0x00ca_000b	QADC Control Register 0 (QACR0) See page 416.	Read:	MUX	0	0	TRG	0	0	0	PSH8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	PSH7	PSH6	PSH5	PSH4	PSA	PSL2	PSL1	PSL0
		Write:								
		Reset:	0	0	1	1	0	1	1	1

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 21 of 34)

Freescale Semiconductor, Inc.

Address	Register Name		Bit Number							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_000c 0x00ca_000d	QADC Control Register 1 (QACR1) See page 419.	Read:	CIE1	PIE1	0	MQ112	MQ111	MQ110	MQ19	MQ18
		Write:			SSE1					
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_000e 0x00ca_000f	QADC Control Register 2 (QACR2) See page 422.	Read:	CIE2	PIE2	0	MQ212	MQ211	MQ210	MQ29	MQ28
		Write:			SSE2					
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	RESUME	BQ26	BQ25	BQ24	BQ23	BQ22	BQ21	BQ20
		Write:								
		Reset:	0	1	1	1	1	1	1	1
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0010 0x00ca_0011	QADC Status Register 0 (QASR0) See page 427.	Read:	CF1	PF1	CF2	PF2	TOR1	TOR2	QS9	QS8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	QS7	QS6	CWP5	CWP4	CWP3	CWP2	CWP1	CWP0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 22 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0012 0x00ca_0013	QADC Status Register 1 (QASR1) See page 436.	Read:	0	0	CWPQ15	CWPQ14	CWPQ13	CWPQ12	CWPQ11	CWPQ10
		Write:								
		Reset:	0	0	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	0	CWPQ25	CWPQ24	CWPQ23	CWPQ22	CWPQ21	CWPQ20
		Write:								
		Reset:	0	0	1	1	1	1	1	1
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ca_0014 ↓ 0x00ca_01ff	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0200 0x00ca_027e	Conversion Command Word Register (CCW) See page 437.	Read:	0	0	0	0	0	0	P	BYP
		Write:								
		Reset:	0	0	0	0	0	0	U	U
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	IST1	IST0	CHAN5	CHAN4	CHAN3	CHAN2	CHAN1	CHAN0
		Reset:	U	U	U	U	U	U	U	U
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0280 0x00ca_02fe	Right-Justified Unsigned Result Register (RJURR) See page 441.	Read:	0	0	0	0	0	0	RESULT	
		Write:								
		Reset:	0	0	0	0	0	0		
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	RESULT							
		Reset:								

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 23 of 34)

Freescale Semiconductor, Inc.

Address	Register Name		Bit Number							
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0300 0x00ca_037e	Left-Justified Signed Result Register (LJSRR) See page 442.	Read: Write:	S	RESULT						
		Reset:								
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	RESULT		0	0	0	0	0	0
		Reset:			0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ca_0380 0x00ca_03fe	Left-Justified Unsigned Result Register (LJURR) See page 442.	Read: Write:	RESULT							
		Reset:								
			Bit 7	6	5	4	3	2	1	Bit 0
		Read: Write:	RESULT		0	0	0	0	0	0
		Reset:			0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ca_0400 ↓ 0x00ca_ffff	Unimplemented		Access results in a bus monitor timeout generating an access termination transfer error.							

Serial Peripheral Interface (SPI)

			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0000	SPI Control Register 1 (SPICR1) See page 376.	Read: Write:	SPIE	SPE	SWOM	MSTR	CPOL	CPHA	SSOE	LSBFE
		Reset:	0	0	0	0	0	1	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0001	SPI Control Register 2 (SPICR2) See page 378.	Read: Write:	0	0	0	0	0	0	SPISDOZ	SPC0
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 24 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0002	SPI Baud Rate Register (SPIBR) See page 379.	Read:	0	SPPR6	SPPR5	SPPR4	0	SPR2	SPR1	SPR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0003	SPI Status Register (SPISR) See page 381.	Read:	SPIF	WCOL	0	MODF	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0004	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0005	SPI Data Register (SPIDR) See page 382.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0006	SPI Pullup and Reduced Drive Register (SPIPURD) See page 383.	Read:	0	0	RSVD5	RDPSP	0	0	RSVD1	PUPSP
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0007	SPI Port Data Register (SPIPORT) See page 384.	Read:	RSVD7	RSVD6	RSVD5	RSVD4	PORTSP3	PORTSP2	PORTSP1	PORTSP0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0008	SPI Port Data Direction Register (SPIDDR) See page 385.	Read:	RSVD7	RSVD6	RSVD5	RSVD4	DDRSP3	DDRSP2	DDRSP1	DDRSP0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0009 ↓ 0x00cb_000f	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 25 of 34)

Address	Register Name	Bit Number							
		Bit 7	6	5	4	3	2	1	Bit 0
0x00cb_0010 ↓ 0x00cb_ffff	Unimplemented	Access results in a bus monitor timeout generating an access termination transfer error.							

Serial Communications Interface 1 (SCI1) and Serial Communications Interface 2 (SCI2)

Note: Addresses for SCI1 are at 0x00cc_#### and addresses for SCI2 are at 0x00cd_####.

Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x00cc_0000 0x00cd_0000	SCI Baud Rate Register High (SCIBDH) See page 336.	Read:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
0x00cc_0001 0x00cd_0001	SCI Baud Rate Register Low (SCIBDL) See page 336.	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
		Reset:	0	0	0	0	0	1	0	0
0x00cc_0002 0x00cd_0002	SCI Control Register 1 (SCICR1) See page 337.	Read:	LOOPS	WOMS	RSRC	M	WAKE	ILT	PE	PT
		Write:								
		Reset:	0	0	0	0	0	0	0	0
0x00cc_0003 0x00cd_0003	SCI Control Register 2 (SCICR2) See page 340.	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
		Reset:	0	0	0	0	0	0	0	0
0x00cc_0004 0x00cd_0004	SCI Status Register 1 (SCISR1) See page 342.	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
		Reset:	1	1	0	0	0	0	0	0
0x00cc_0005 0x00cd_0005	SCI Status Register 2 (SCISR2) See page 344.	Read:	0	0	0	0	0	0	0	RAF
		Write:								
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 26 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cc_0006 0x00cd_0006	SCI Data Register High (SCIDRH) See page 345.	Read:	R8	T8	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cc_0007 0x00cd_0007	SCI Data Register Low (SCIDRL) See page 345.	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cc_0008 0x00cd_0008	SCI Pullup and Reduced Drive Register (SCIPURD) See page 346.	Read:	SCISDOZ	0	RSVD5	RDPSCI	0	0	RSVD1	PUPSCI
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cc_0009 0x00cd_0009	SCI Port Data Register (SCIPORT) See page 347.	Read:	RSVD7	RSVD6	RSVD5	RSVD4	RSVD3	RSVD2	PORTSC1	PORTSC0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cc_000a 0x00cd_000a	SCI Data Direction Register (SCIDDR) See page 348.	Read:	RSVD7	RSVD6	RSVD5	RSVD4	RSVD3	RSVD2	DDRSC1	DDRSC0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cc_000b ↓ 0x00cc_000f 0x00cd_000b ↓ 0x00cd_000f	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00cc_0010 ↓ 0x00cc_ffff 0x00cd_0010 ↓ 0x00cd_ffff	Unimplemented		Access results in a bus monitor timeout generating an access termination transfer error.							

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 27 of 34)

Address	Register Name		Bit Number							
Timer 1 (TIM1) and Timer 2 (TIM2)										
Note: Addresses for TIM1 are at 0x00ce_#### and addresses for TIM2 are at 0x00cf_####.										
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0000 0x00cf_0000	Timer Input Capture/ Output Compare Select Register (TIMIOS) See page 300.	Read:	0	0	0	0	IOS3	IOS2	IOS1	IOS0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0001 0x00cf_0001	Timer Compare Force Register (TIMCFORC) See page 301.	Read:	0	0	0	0	0	0	0	0
		Write:					FOC3	FOC2	FOC1	FOC0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0002 0x00cf_0002	Timer Output Compare 3 Mask Register (TIMOC3M) See page 302.	Read:	0	0	0	0	OC3M3	OC3M2	OC3M1	OC3M0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0003 0x00cf_0003	Timer Output Compare 3 Data Register (TIMOC3D) See page 303.	Read:	0	0	0	0	OC3D3	OC3D2	OC3D1	OC3D0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0004 0x00cf_0004	Timer Counter Register High (TIMCNTH) See page 304.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0005 0x00cf_0005	Timer Counter Register Low (TIMCNTL) See page 304.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0006 0x00cf_0006	Timer System Control Register 1 (TIMSCR1) See page 305.	Read:	TIMEN	0	0	TFFCA	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 28 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0007 0x00cf_0007	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
0x00ce_0008 0x00cf_0008	Timer Toggle on Overflow Register (TIMTOV) See page 306.	Read:	0	0	0	0	TOV3	TOV2	TOV1	TOV0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
0x00ce_0009 0x00cf_0009	Timer Control Register 1 (TIMCTL1) See page 307.	Read:	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
0x00ce_000a 0x00cf_000a	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
0x00ce_000b 0x00cf_000b	Timer Control Register 2 (TIMCTL2) See page 308.	Read:	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG10
		Write:								
		Reset:	0	0	0	0	0	0	0	0
0x00ce_000c 0x00cf_000c	Timer Interrupt Enable Register (TIMIE) See page 309.	Read:	0	0	0	0	C3I	C2I	C1I	C0I
		Write:								
		Reset:	0	0	0	0	0	0	0	0
0x00ce_000d 0x00cf_000d	Timer System Control Register 2 (TIMSCR2) See page 310.	Read:	TOI	0	PUPT	RDPT	TCRE	PR2	PR1	PR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
0x00ce_000e 0x00cf_000e	Timer Flag Register 1 (TIMFLG1) See page 312.	Read:	0	0	0	0	C3F	C2F	C1F	C0F
		Write:								
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 29 of 34)

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Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_000f 0x00cf_000f	Timer Flag Register 2 (TIMFLG2) See page 313.	Read:	TOF	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ce_0010 0x00cf_0010	Timer Channel 0 Register High (TIMC0H) See page 314.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0011 0x00cf_0011	Timer Channel 0 Register Low (TIMC0L) See page 314.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ce_0012 0x00cf_0012	Timer Channel 1 Register High (TIMC1H) See page 314.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0013 0x00cf_0013	Timer Channel 1 Register Low (TIMC1L) See page 314.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ce_0014 0x00cf_0014	Timer Channel 2 Register High (TIMC2H) See page 314.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0015 0x00cf_0015	Timer Channel 2 Register Low (TIMC2L) See page 314.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ce_0016 0x00cf_0016	Timer Channel 3 Register High (TIMC3H) See page 314.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 30 of 34)

Freescale Semiconductor, Inc.

System Memory Map

Address	Register Name		Bit Number							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0017 0x00cf_0017	Timer Channel 3 Register Low (TIMC3L) See page 314.	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0018 0x00cf_0018	Pulse Accumulator Control Register (TIMPACTL) See page 315.	Read: Write:	0	PAE	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0019 0x00cf_0019	Pulse Accumulator Flag Register (TIMPAFLG) See page 317.	Read: Write:	0	0	0	0	0	0	PAOVF	PAIF
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
0x00ce_001a 0x00cf_001a	Pulse Accumulator Counter Register High (TIMPACNTH) See page 318.	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_001b 0x00cf_001b	Pulse Accumulator Counter Register Low (TIMPACNTL) See page 318.	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_001c 0x00cf_001c	Reserved		Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.							
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_001d 0x00cf_001d	Timer Port Data Register (TIMPORT) See page 319.	Read: Write:	0	0	0	0	PORTT3	PORTT2	PORTT1	PORTT0
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_001e 0x00cf_001e	Timer Port Data Direction Register (TIMDDR) See page 320.	Read: Write:	0	0	0	0	DDRT3	DDRT2	DDRT1	DDRT0
		Reset:	0	0	0	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 31 of 34)

Freescale Semiconductor, Inc.

Address	Register Name	Bit Number							
		Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_001f 0x00cf_001f	Timer Test Register (TIMTST) See page 321.	Read: 0	0	0	0	0	0	0	0
		Write:							
		Reset: 0	0	0	0	0	0	0	0
		Bit 7	6	5	4	3	2	1	Bit 0
0x00ce_0020 ↓ 0x00ce_ffff 0x00cf_0030 ↓ 0x00cf_ffff	Unimplemented	Access results in the module generating an access termination transfer error.							

Non-Volatile Memory FLASH (CMFR)

Address	Register Name	Bit Number							
		Bit 31	30	29	28	27	26	25	Bit 24
0x00d0_0000 0x00d0_0001 0x00d0_0002 0x00d0_0003	CMFR Module Configuration Register (CMFRMCR) See page 188.	Read: FSTOP	FDBG	0	EME	SIE	LOCKCTL	DIS	RSVD24
		Write:							
		Reset: 0	0	0	Note 1	0	0	Note 1	0
		Bit 23	22	21	20	19	18	17	Bit 16
		Read: SUPV7	SUPV6	SUPV5	SUPV4	SUPV3	SUPV2	SUPV1	SUPV0
		Write:							
		Reset: 1	1	1	1	1	1	1	1
		Bit 15	14	13	12	11	10	9	Bit 8
		Read: DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
		Write:							
		Reset: 0	0	0	0	0	0	0	0
		Bit 7	6	5	4	3	2	1	Bit 0
		Read: PROTECT7	PROTECT6	PROTECT5	PROTECT4	PROTECT3	PROTECT2	PROTECT1	PROTECT0
		Write:							
		Reset: 1	1	1	1	1	1	1	1

Notes:
1. Reset state is defined by reset override.

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 32 of 34)

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System Memory Map

Address	Register Name		Bit Number							
			Bit 31	30	29	28	27	26	25	Bit 24
0x00d0_0004 0x00d0_0005 0x00d0_0006 0x00d0_0007	CMFR Module Test Register (CMFRMTR) See page 193.	Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:								
			Bit 23	22	21	20	19	18	17	Bit 16
		Read:	0	0	0	0	0	0	0	0
		Write:								
		Reset:								
			Bit 15	14	13	12	11	10	9	Bit 8
		Read:	0	0	0	0	NVR	PAWS2	PAWS1	PAWS0
		Write:								
		Reset:					0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	RSVD6	GDB	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 31	30	29	28	27	26	25	Bit 24
0x00d0_0008 0x00d0_0009 0x00d0_000a 0x00d0_000b	CMFR High-Voltage Control Register (CMFRCTL) See page 196.	Read:	HVS	0	SCLKR2	SCLKR1	SCLKR0	0	CLKPE1	CLKPE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 23	22	21	20	19	18	17	Bit 16
		Read:	0	CLKPM6	CLKPM5	CLKPM4	CLKPM3	CLKPM2	CLKPM1	CLKPM0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 15	14	13	12	11	10	9	Bit 8
		Read:	BLOCK7	BLOCK6	BLOCK5	BLOCK4	BLOCK3	BLOCK2	BLOCK1	BLOCK0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			Bit 7	6	5	4	3	2	1	Bit 0
		Read:	0	RSVD6	1	0	0	ERASE	SES	EHV
		Write:								
		Reset:	0	0	1	0	0	0	0	0

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 33 of 34)

Freescale Semiconductor, Inc.

Address	Register Name	Bit Number							
		Bit 7	6	5	4	3	2	1	Bit 0
0x00d0_000c ↓ 0x00d0_001c	Unimplemented	Access results in the module generating an access termination transfer error.							
		Bit 7	6	5	4	3	2	1	Bit 0
0x00d0_001d ↓ 0x7fff_ffff	Unimplemented	Access results in a bus monitor timeout generating an access termination transfer error.							

P = Current pin state U = Unaffected = Writes have no effect and the access terminates without a transfer error exception.

Figure 2-2. Register Summary (Sheet 34 of 34)

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System Memory Map

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Section 3. Chip Configuration Module (CCM)

3.1 Contents

3.2 Introduction 90
3.3 Features 90
3.4 Modes of Operation 90
3.4.1 Master Mode 91
3.4.2 Single-Chip Mode 91
3.4.3 Emulation Mode 91
3.4.4 Factory Access Slave Test (FAST) Mode 91
3.5 Block Diagram 92
3.6 Signal Descriptions 92
3.7 Memory Map and Registers 93
3.7.1 Programming Model 93
3.7.2 Memory Map 94
3.7.3 Register Descriptions 94
3.7.3.1 Chip Configuration Register 94
3.7.3.2 Reset Configuration Register 97
3.7.3.3 Chip Identification Register 99
3.7.3.4 Chip Test Register 100
3.8 Functional Description 100
3.8.1 Reset Configuration 101
3.8.2 Chip Mode Selection 103
3.8.3 Boot Device Selection 103
3.8.4 Output Pad Strength Configuration 105
3.8.5 Clock Mode Selection 105
3.8.6 Internal FLASH Configuration 106
3.9 Reset 106
3.10 Interrupts 106

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3.2 Introduction

The chip configuration module (CCM) controls the chip configuration and mode of operation.

3.3 Features

The CCM performs these operations.

- Selects the chip operating mode:
  - Master mode
  - Single-chip mode
  - Emulation mode
  - Factory access slave test (FAST) mode for factory test only
- Selects external clock or phase-lock loop (PLL) mode with internal or external reference
- Selects output pad strength
- Selects boot device
- Selects module configuration
- Selects bus monitor configuration

3.4 Modes of Operation

The CCM configures the chip for four modes of operation:

- Master mode
- Single-chip mode
- Emulation mode
- FAST mode for factory test only

The operating mode is determined at reset and cannot be changed thereafter.

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3.4.1 Master Mode

In master mode, the internal central processor unit (CPU) can access external memories and peripherals. Full master mode functionality requires the bonding out of the optional pins. The external bus consists of a 32-bit data bus and 23 address lines. Available bus control signals include R/$\overline{W}$, TC[2:0], TSIZ[1:0], $\overline{TA}$, $\overline{TEA}$, $\overline{OE}$, and $\overline{EB}$[3:0]. Up to four chip selects can be programmed to select and control external devices and to provide bus cycle termination. When interfacing to 16-bit ports, the ports C and D pins and $\overline{EB}$[3:2] can be configured as general-purpose input/output (I/O).

3.4.2 Single-Chip Mode

In single-chip mode, all memory is internal to the chip. External bus pins are configured as digital I/O.

3.4.3 Emulation Mode

Emulation mode supports external port replacement logic. All ports are emulated and all primary pin functions are enabled. Since the full external bus must be visible to support the external port replacement logic, the emulation mode pin configuration resembles master mode. Full emulation mode functionality requires bonding out the optional pins. Emulation mode chip selects are provided to give additional information about the bus cycle. Also, the signal $\overline{SHS}$ is provided as a strobe for capturing addresses and data during show cycles.

3.4.4 Factory Access Slave Test (FAST) Mode

FAST mode is for factory test only.

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3.5 Block Diagram

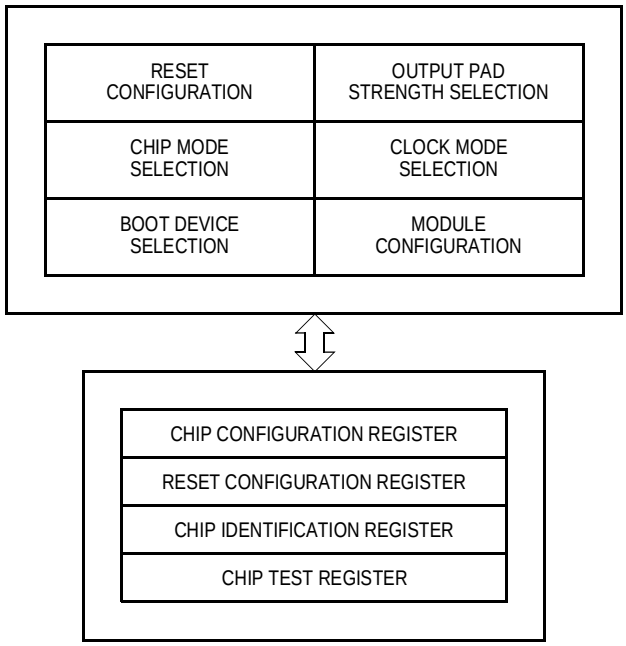

Figure 3-1. Chip Configuration Module Block Diagram

3.6 Signal Descriptions

Table 3-1 provides an overview of the CCM signals. For more detailed information, refer to **Section 4. Signal Description**.

Table 3-1. Signal Properties

Name	Function	Reset State
$\overline{\text{RCON}}$	Reset configuration select	Internal weak pullup device
V_{DDSYN}	Clock mode select	—
D[31:16]	Reset configuration overrides	—

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3.7 Memory Map and Registers

This subsection provides a description of the memory map and registers.

3.7.1 Programming Model

The CCM programming model consists of these registers:

- The chip configuration register (CCR) controls the main chip configuration.
- The reset configuration register (RCON) indicates the default chip configuration.
- The chip identification register (CIR) contains a unique part number.
- The chip test register (CTR) contains chip-specific test functions.

Some control register bits are implemented as write-once bits. These bits are always readable, but once the bit has been written, additional writes have no effect, except during debug mode and test operations.

Some write-once bits and test bits can be read and written while in debug mode or test mode. When debug or test mode is exited, the chip configuration module resumes operation based on the current register values. If a write to a write-once register bit occurs while in debug or test mode, the register bit remains writable on exit from debug or test mode. **Table 3-2** shows the accessibility of write-once bits.

Table 3-2. Write-Once Bits Read/Write Accessibility

Configuration	Read/Write Access
All configurations	Read-always
Debug operation (all modes)	Write-always
Test operation (all modes)	Write-always
Master mode	Write-once
Single-chip mode	Write-once
FAST mode	Write-once
Emulation mode	Write-once

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3.7.2 Memory Map

Table 3-3. Chip Configuration Module Memory Map

Address	Bits 31–16	Bits 15–0	Access(1)
0x00c1_0000	Chip configuration register (CCR)	Reserved(2)	S
0x00c1_0004	Reset configuration register (RCON)	Chip identification register (CIR)	S
0x00c1_0008	Chip test register (CTR)	Reserved(2)	S
0x00c1_000c	Unimplemented(3)		—

1. S = CPU supervisor mode access only. User mode accesses to supervisor only addresses have no effect and result in a cycle termination transfer error.
2. Writing to reserved addresses has no effect; reading returns 0s.
3. Accessing an unimplemented address has no effect and causes a cycle termination transfer error.

3.7.3 Register Descriptions

The following subsection describes the CCM registers.

3.7.3.1 Chip Configuration Register

Address: 0x00c1_0000 and 0x00c1_0001

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	LOAD	0	SHEN	EMINT	0	MODE2	MODE1	MODE0
Write:								
Reset:	Note 1	0	Note 2	Note 2	0	Note 1	Note 1	Note 1

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	SZEN	PSTEN	SHINT	BME	BMD	BMT1	BMT0
Write:								
Reset:	0	Note 3	Note 2	0	1	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Notes:
1. Determined during reset configuration
2. 0 for all configurations except emulation mode, 1 for emulation mode
3. 0 for all configurations except emulation and master modes, 1 for emulation and master modes

Figure 3-2. Chip Configuration Register (CCR)

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LOAD — Pad Driver Load Bit

The LOAD bit selects full or default drive strength for selected pad output drivers. For maximum capacitive load, set the LOAD bit to select full drive strength. For reduced power consumption, clear the LOAD bit to select default drive strength.

1 = Full drive strength
0 = Default drive strength

Table 3-2 shows the read/write accessibility of this write-once bit.

SHEN — Show Cycle Enable Bit

The SHEN bit enables the external memory interface to drive the external bus during internal transfer operations.

1 = Show cycles enabled
0 = Show cycles disabled

In emulation mode, the SHEN bit is read-only. In all other modes, it is a read/write bit.

EMINT — Emulate Internal Address Space Bit

The EMINT bit enables chip select 1 (CS1) to decode the internal memory address space.

1 = CS1 decodes internal memory address space.
0 = CS1 decodes external memory address space.

The EMINT bit is read-always but can be written only in emulation mode.

MODE[2:0] — Chip Configuration Mode Field

This read-only field reflects the chip configuration mode, as shown in **Table 3-4**.

Table 3-4. Chip Configuration Mode Selection

MODE[2:0]	Chip Configuration Mode
111	Master mode
110	Single-chip mode
10X	FAST mode
0XX	Emulation mode

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SZEN — TSIZ[1:0] Enable Bits

This read/write bit enables the TSIZ[1:0] function of the external pins.

1 = TSIZ[1:0] function enabled
0 = TSIZ[1:0] function disabled

PSTEN — PSTAT[3:0] Signal Enable Bits

This read/write bit enables the PSTAT[3:0] function of the external pins.

1 = PSTAT[3:0] function enabled
0 = PSTAT[3:0] function disabled

SHINT — Show Interrupt Bit

The SHINT bit allows visibility to any active interrupt request to the processor. If the SHINT bit is set, the $\overline{\text{RSTOUT}}$ pin is the OR of the fast and normal interrupt signals.

1 = Internal requests reflected on $\overline{\text{RSTOUT}}$ pin
0 = Normal $\overline{\text{RSTOUT}}$ pin function

The SHINT bit is read/write always.

NOTE: *The FRCRSTOUT function in the reset controller has a higher priority than the SHINT function.*

BME — Bus Monitor External Enable Bit

The BME bit enables the bus monitor to operate during external bus cycles.

1 = Bus monitor enabled on external bus cycles
0 = Bus monitor disabled on external bus cycles

Table 3-2 shows the read/write accessibility of this write-once bit.

BMD — Bus Monitor Debug Mode Bit

The BMD bit controls how the bus monitor responds during debug mode.

1 = Bus monitor enabled in debug mode
0 = Bus monitor disabled in debug mode

This bit is read/write always.

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BMT[1:0] — Bus Monitor Timing Field

The BMT field selects the timeout time for the bus monitor as shown in **Table 3-5**.

Table 3-5. Bus Monitor Timeout Values

BMT[1:0]	Timeout Period (in System Clocks)
00	64
01	32
10	16
11	8

Table 3-2 shows the read/write accessibility of these write-once bits.

3.7.3.2 Reset Configuration Register

The reset configuration register (RCON) is a read-only register; writing to RCON has no effect. At reset, RCON determines the default operation of certain chip functions. All default functions defined by the RCON values may be overridden during reset configuration only if the external RCON pin is asserted.

Address: 0x00c1_0004 and 0x00c1_0005

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	1 RPLLSEL	1 RPLLREF	0 RLOAD	0	1 BOOTPS	0 BOOTSEL	0	0 MODE
Write:								
Reset:	1	1	0	0	1	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 3-3. Reset Configuration Register (RCON)

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RPLLSEL — PLL Mode Select Bit

When the PLL is enabled, the read-only RPLLSEL bit reflects the default PLL mode.

1 = Normal PLL mode
0 = 1:1 PLL mode

The default PLL mode can be overridden during reset configuration. If the default mode is overridden, the PLLSEL bit in the clock module SYNSR reflects the PLL mode.

RPLLREF — PLL Reference Bit

When the PLL is enabled in normal PLL mode, the read-only RPLLREF bit reflects the default PLL reference.

1 = Crystal oscillator is PLL reference.
0 = External clock is PLL reference.

The default PLL reference can be overridden during reset configuration. If the default mode is overridden, the PLLREF bit in the clock module SYNSR reflects the PLL reference.

RLOAD — Pad Driver Load Bit

The read-only RLOAD bit reflects the pad driver strength configuration.

1 = Full drive strength
0 = Default drive strength

The default function of the pad driver strength can be overridden during reset configuration. If the default mode is overridden, the LOAD bit in CCR reflects the pad driver strength configuration.

BOOTPS — Boot Port Size Bit

If the boot device is configured to be external, the read-only BOOTPS bit reflects the default selection for the boot port size.

1 = Boot device uses 32-bit port.
0 = Boot device uses 16-bit port.

The default function of the boot port size can be overridden during reset configuration. If the default mode is overridden, the PS bit in CSCR0 reflects the boot device port size configuration.

BOOTSEL — Boot Select Bit

This read-only bit reflects the default selection for the boot device.

1 = Boot from external boot device
0 = Boot from internal boot device

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The default function of the boot select can be overridden during reset configuration. If the default mode is overridden, the CSEN bit in CSCR0 bit reflects the boot device configuration.

MODE — Chip Configuration Mode Bit

The read-only MODE bit reflects the default chip configuration mode.
1 = Master mode
0 = Single-chip mode

The default mode can be overridden during reset configuration. If the default mode is overridden, the MODE0 bit in CCR reflects the mode configuration.

3.7.3.3 Chip Identification Register

The chip identification register (CIR) is a read-only register; writing to CIR has no effect.

Address: 0x00c1_0006 and 0x00c1_0007

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0 PIN7	0 PIN6	0 PIN5	1 PIN4	0 PIN3	1 PIN2	1 PIN1	1 PIN0
Write:								
Reset:	0	0	0	1	0	1	1	1

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0 PRN7	0 PRN6	0 PRN5	0 PRN4	0 PRN3	0 PRN2	0 PRN1	0 PRN0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 3-4. Chip Identification Register (CIR)

PIN[7:0] — Part Identification Number Field

This read-only field contains a unique identification number for the part.

PRN[7:0] — Part Revision Number Field

This read-only field contains the full-layer mask revision number. This number is increased by one for each new full-layer mask set of this part. The revision numbers are assigned in chronological order.

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3.7.3.4 Chip Test Register

The chip test register (CTR) is reserved for factory testing.

NOTE: *To safeguard against unintentionally activating test logic, write $0000 to the lock-out test features. Setting any bit in CTR may lead to unpredictable results.*

Address: 0x00c1_0008 and 0x00c1_0009

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 3-5. Chip Test Register (CTR)

3.8 Functional Description

Six functions are defined within the chip configuration module:

1. Reset configuration
2. Chip mode selection
3. Boot device selection
4. Output pad strength configuration
5. Clock mode selection
6. Module configuration

These functions are described here.

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3.8.1 Reset Configuration

During reset, the pins for the reset override functions are immediately configured to known states, even if the clock source is not present. **Table 3-6** shows the states of the external pins while in reset.

Table 3-6. Reset Configuration Pin States During Reset

Pin	Pin Function[1]	I/O	Output State	Input State
D[28, 26, 23:21, 19:16], PA[4, 2], PB[7:5, 3:0]	Digital I/O or primary function	Input	—	Must be driven by external logic
$\overline{\text{RCON}}$	$\overline{\text{RCON}}$ function for all modes[2]	Input	—	Internal weak pullup device
V_{DDSYN}	Not affected	Input	—	Must be driven by external logic

1. If the external $\overline{\text{RCON}}$ pin is not asserted during reset, pin functions are determined by the default operation mode defined in the RCON register. If the external $\overline{\text{RCON}}$ pin is asserted, pin functions are determined by the chip operation mode defined by the override values driven on the external data bus pins.
2. During reset, the external $\overline{\text{RCON}}$ pin assumes its $\overline{\text{RCON}}$ pin function, but this pin changes to the function defined by the chip operation mode immediately after reset. See **Table 3-7**.

If the $\overline{\text{RCON}}$ pin is not asserted during reset, the chip configuration and the reset configuration pin functions after reset are determined by RCON or fixed defaults, regardless of the states of the external data pins. The internal configuration signals are driven to levels specified by the RCON register's reset state for default module configuration.

If the external $\overline{\text{RCON}}$ pin is asserted during reset, then various chip functions, including the reset configuration pin functions after reset, are configured according to the levels driven onto the external data pins. (See **Table 3-7**.) The internal configuration signals are driven to reflect the levels on the external configuration pins to allow for module configuration.

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Table 3-7. Configuration During Reset(1)

Pin(s) Affected	Default Configuration	Override Pins in Reset(2),(3)	Function
D[31:0], $\overline{SHS}$, $\overline{TA}$, $\overline{TEA}$, CSE[1:0], TC[2:0], $\overline{OE}$, A[22:0], $\overline{EB}$[3:0], $\overline{CS}$[3:0]	V_{DD}, V_{DD}, RCON0	**D[26,17:16]**	**Chip Mode Selected**
		111	Master mode
		110	Single-chip mode
		10X	FAST mode
		0XX	Emulation mode
$\overline{CS}$[1:0]	RCON[3:2]	**D[19:18]**	**Boot Device**
		X0	Internal with 32-bit port
		01	External with 16-bit port
		11	External with 32-bit port
All output pins	RCON5	**D21**	**Output Pad Drive Strength**
		0	Default strength
		1	Full strength
Clock mode	V_{DDSYN}, RCON[7:6]	**V_{DDSYN}, D[23:22]**	**Clock Mode**
		0XX	External clock mode (PLL disabled)
		10X	1:1 PLL mode
		110	Normal PLL mode with external clock reference
		111	Normal PLL mode w/crystal oscillator reference
Internal FLASH configuration	V_{DD}	**D28**	**Module Configuration**
		1	Internal FLASH enabled
		0	Internal FLASH disabled

1. Modifying the default configurations is possible only if the external $\overline{RCON}$ pin is asserted.
2. The D[31:29, 27, 25:24, 20, 15:0] pins do not affect reset configuration.
3. The external reset override circuitry drives the data bus pins with the override values while $\overline{RSTOUT}$ is asserted. It must stop driving the data bus pins within one CLKOUT cycle after $\overline{RSTOUT}$ is negated. To prevent contention with the external reset override circuitry, the reset override pins are forced to inputs during reset and do not become outputs until at least one CLKOUT cycle after $\overline{RSTOUT}$ is negated.

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3.8.2 Chip Mode Selection

The chip mode is selected during reset and reflected in the MODE field of the chip configuration register (CCR). Once reset is exited, the operating mode cannot be changed. **Table 3-8** shows the mode selection during reset configuration.

Table 3-8. Chip Configuration Mode Selection(1)

Chip Configuration Mode	CCR Register MODE Field		
	MODE2	MODE1	MODE0
Master mode	D26 driven high	D17 driven high	D16 driven high
Single-chip mode	D26 driven high	D17 driven high	D16 driven low
FAST mode	D26 driven high	D17 driven low	D16 don't care
Emulation mode	D26 driven low	D17 don't care	D16 don't care

1. Modifying the default configurations is possible only if the external $\overline{\text{RCON}}$ pin is asserted.

During reset, certain module configurations depend on whether emulation mode is active as determined by the state of the internal emulation signal.

3.8.3 Boot Device Selection

During reset configuration, the $\overline{\text{CS0}}$ chip select pin is optionally configured to select an external boot device. In this case, the CSEN bit in CSCR0 is set, enabling $\overline{\text{CS0}}$ after reset. $\overline{\text{CS0}}$ will be asserted for the initial boot fetch accessed from address 0x0. It is assumed that the reset vector loaded from address 0x0 causes the CPU to start executing from external memory space decoded by $\overline{\text{CS0}}$. Also, the PS bit is configured for either a 16-bit or 32-bit port size depending on the external boot device. See **Table 3-9**.

In emulation mode, the $\overline{\text{CS1}}$ chip select pin is optionally configured for emulating an internal memory. In emulation mode and booting from internal memory, the CSEN bit in CSCR1 is set, enabling $\overline{\text{CS1}}$ after reset.

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Table 3-9. Chip Select $\overline{CS0}$ Configuration Encoding

Chip Select $\overline{CS0}$ Control	CSCR0 Register		CSCR1 Register
	CSEN Bit	PS Bit	CSEN Bit
Chip select disabled (32-bit port size)	0	1	1(1)
Chip select enabled with 16-bit port size	1	0	0
Chip select enabled with 32-bit port size	1	1	0

1. CSCR1 CSEN is initially set only in emulation mode when booting from internal memory and is cleared otherwise.

Once reset is exited, the states of the CSEN and PS bits in CSCR0 and the CSEN bit in CSCR1 remain, but can be modified by software.

NOTE: *When booting externally, the D28 pin should be driven low during reset configuration to disable the internal FLASH located at address 0x0 so that no conflict exists with the external boot device.*

The boot device selection during reset configuration is summarized in **Table 3-10**.

Table 3-10. Boot Device Selection(1)

Boot Device Selection	CSCR0 Register		CSCR1 Register
	CSEN Bit	PS Bit	CSEN Bit
Internal boot device; default 32-bit port	D18 driven low	D19 don't care	D18 driven low
External boot device with 16-bit port	D18 driven high	D19 driven low	D18 driven high
External boot device with 32-bit port	D18 driven high	D19 driven high	D18 driven high

1. Modifying the default configurations is possible only if the external $\overline{RCON}$ pin is asserted.

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3.8.4 Output Pad Strength Configuration

Output pad strength is determined during reset configuration as shown in **Table 3-11**. Once reset is exited, the output pad strength configuration can be changed by programming the LOAD bit of the chip configuration register.

Table 3-11. Output Pad Driver Strength Selection(1)

Optional Pin Function Selection	CCR Register LOAD Bit
Output pads configured for default strength	D21 driven low
Output pads configured for full strength	D2 driven high

1. Modifying the default configurations is possible only if the external $\overline{\text{RCON}}$ pin is asserted low.

3.8.5 Clock Mode Selection

The clock mode is selected during reset and reflected in the PLLMODE, PLLSEL, and PLLREF bits of SYNSR. Once reset is exited, the clock mode cannot be changed.

Table 3-12 summarizes clock mode selection during reset configuration.

Table 3-12. Clock Mode Selection(1)

Clock Mode	Synthesizer Status Register (SYNSR)		
	MODE Bit	PLLSEL Bit	PLLREF Bit
External clock mode; PLL disabled	V_{DDSYN} driven low	D23 don't care	D22 don't care
1:1 PLL mode	V_{DDSYN} driven high	D23 driven low	D22 don't care
Normal PLL mode; external clock reference	V_{DDSYN} driven high	D23 driven high	D22 driven low
Normal PLL mode; crystal oscillator reference	V_{DDSYN} driven high	D23 driven high	D22 driven high

1. Modifying the default configurations is possible only if the external $\overline{\text{RCON}}$ pin is asserted low.

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3.8.6 Internal FLASH Configuration

During reset configuration, the D28 pin controls whether or not the internal FLASH is enabled or disabled as shown in **Table 3-13**.

Table 3-13. Internal FLASH Configuration(1)

Internal FLASH Configuration	External D28 State
Internal FLASH enabled	D28 pin driven high
Internal FLASH disabled	D28 pin driven low

1. Modifying the default configurations is possible only if the external $\overline{\text{RCON}}$ pin is asserted low.

3.9 Reset

Reset initializes CCM registers to a known startup state as described in **3.7 Memory Map and Registers**. The CCM controls chip configuration at reset as described in **3.8 Functional Description**.

3.10 Interrupts

The CCM does not generate interrupt requests.

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Section 4. Signal Description

4.1 Contents

4.2 Introduction 109
4.3 Package Pinout Summary 110
4.4 MMC2107 Specific Implementation Signal Issues 120
4.4.1 RSTOUT Signal Functions 120
4.4.2 INT Signal Functions 121
4.5 Signal Descriptions 121
4.5.1 Reset Signals 121
4.5.1.1 Reset In (RESET) 121
4.5.1.2 Reset Out (RSTOUT) 121
4.5.2 Phase-Lock Loop (PLL) and Clock Signals 122
4.5.2.1 External Clock In (EXTAL) 122
4.5.2.2 Crystal (XTAL) 122
4.5.2.3 Clock Out (CLKOUT) 122
4.5.2.4 Synthesizer Power (V_{DDSYN} and V_{SSSYN}) 122
4.5.3 External Memory Interface Signals 122
4.5.3.1 Data Bus (D[31:0]) 122
4.5.3.2 Show Cycle Strobe (SHS) 123
4.5.3.3 Transfer Acknowledge (TA) 123
4.5.3.4 Transfer Error Acknowledge (TEA) 123
4.5.3.5 Emulation Mode Chip Selects (CSE[1:0]) 123
4.5.3.6 Transfer Code (TC[2:0]) 123
4.5.3.7 Read/Write (R/W) 123
4.5.3.8 Address Bus (A[22:0]) 124
4.5.3.9 Enable Byte (EB[3:0]) 124
4.5.3.10 Chip Select (CS[3:0]) 124
4.5.3.11 Output Enable (OE) 124

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4.5.4 Edge Port Signals 124
4.5.4.1 External Interrupts ($\overline{\text{INT}}$[7:6]) 124
4.5.4.2 External Interrupts ($\overline{\text{INT}}$[5:2]) 124
4.5.4.3 External Interrupts (INT[1:0]) 125
4.5.5 Serial Peripheral Interface Module Signals 125
4.5.5.1 Master Out/Slave In (MOSI) 125
4.5.5.2 Master In/Slave Out (MISO) 125
4.5.5.3 Serial Clock ($\overline{\text{SCK}}$) 125
4.5.5.4 Slave Select ($\overline{\text{SS}}$) 125
4.5.6 Serial Communications Interface Module Signals 125
4.5.6.1 Receive Data (RXD1 and RXD2) 125
4.5.6.2 Transmit Data (TXD1 and TXD2) 126
4.5.7 Timer Signals (ICOC1[3:0] and ICOC2[3:0]) 126
4.5.8 Analog-to-Digital Converter Signals 126
4.5.8.1 Analog Inputs (PQA[4:3], PQA[1:0], and PQB[3:0]) 126
4.5.8.2 Analog Reference (V_{RH} and V_{RL}) 126
4.5.8.3 Analog Supply (V_{DDA} and V_{SSA}) 126
4.5.8.4 Positive Supply (V_{DDH}) 126
4.5.9 Debug and Emulation Support Signals 127
4.5.9.1 Test Reset ($\overline{\text{TRST}}$) 127
4.5.9.2 Test Clock (TCLK) 127
4.5.9.3 Test Mode Select (TMS) 127
4.5.9.4 Test Data Input (TDI) 127
4.5.9.5 Test Data Output (TDO) 127
4.5.9.6 Debug Event ($\overline{\text{DE}}$) 127
4.5.10 Test Signal (TEST) 128
4.5.11 Power and Ground Signals 128
4.5.11.1 Power for FLASH Erase/Program (V_{PP}) 128
4.5.11.2 Power and Ground for FLASH Array (V_{DDF} and V_{SSF}) 128
4.5.11.3 Standby Power (V_{STBY}) 128
4.5.11.4 Positive Supply (V_{DD}) 128
4.5.11.5 Ground (V_{SS}) 128

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4.2 Introduction

The MMC2107 is available in two packages:

- 100-pin Joint-Electron Device Engineering Council (JEDEC) low-profile quad flat pack (LQFP) — The 100-pin device is a minimum pin set for single-chip mode implementation.
- 144-pin JEDEC LQFP — The 144-pin implementation includes 44 optional pins as a bond-out option to:
  - Accommodate an expanded set of features
  - Allow expansion of the number of general-purpose input/output (I/O)
  - Utilize off-chip memory
  - Provide enhanced support for development purposes

The optional group of pins includes:

- 23 address output lines
- Four chip selects
- Two emulation chip selects
- Four byte/write enables
- Read/write (R/$\overline{W}$) signal
- Output enable signal
- Three transfer code signals
- Six power/ground pins

NOTE: *The optional pins are either all present or none of them are present.*

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4.3 Package Pinout Summary

Refer to:

- **Table 4-1** for a summary of the pinouts for both packages
- **Figure 4-1** and **Figure 4-2** for a pictorial view of the pinouts
- **Table 4-2** for a brief description of each signal

Table 4-1. Package Pinouts (Sheet 1 of 5)

Pin Number		Pin Name
144-Pin Package	100-Pin Package	
1	1	D30 / PA6
2	2	D29 / PA5
3	3	D28 / PA4
4	4	D27 / PA3
5	5	D26 / PA2
6	—	A11
7	6	D25 / PA1
8	—	V_{SS}
9	—	V_{DD}
10	7	D24 / PA0
11	—	A10
12	8	D23 / PB7
13	—	A9
14	—	A8
15	9	D22 / PB6
16	10	D21 / PB5
17	11	D20 / PB4
18	12	V_{SS}
19	13	V_{DD}
20	14	D19 / PB3
21	15	D18 / PB2
22	16	D17 / PB1
23	—	A7
24	—	A6

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Table 4-1. Package Pinouts (Sheet 2 of 5)

Pin Number		Pin Name
144-Pin Package	100-Pin Package	
25	17	D16 / PB0
26	—	A5
27	18	D15 / PC7
28	—	A4
29	—	A3
30	19	D14 / PC6
31	20	D13 / PC5
32	21	V_{SS}
33	22	V_{DD}
34	23	D12 / PC4
35	24	D11 / PC3
36	25	D10 / PC2
37	26	D9 / PC1
38	27	D8 / PC0
39	28	D7 / PD7
40	29	D6 / PD6
41	30	D5 / PD5
42	31	D4 / PD4
43	32	D3 / PD3
44	—	V_{SS}
45	—	V_{DD}
46	33	D2 / PD2
47	—	A2
48	34	D1 / PD1
49	—	A1
50	—	A0
51	35	D0 / PD0
52	36	ICOC23
53	37	ICOC22
54	38	ICOC21
55	39	ICOC20

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Table 4-1. Package Pinouts (Sheet 3 of 5)

Pin Number		Pin Name
144-Pin Package	100-Pin Package	
56	40	ICOC13
57	41	ICOC12
58	42	ICOC11
59	—	R/$\overline{W}$
60	—	CSE1
61	43	ICOC10
62	—	CSE0
63	44	TEST
64	—	V_{SS}
65	—	V_{DD}
66	45	TXD2
67	—	TC2
68	46	RXD2
69	47	TXD1
70	48	RXD1
71	49	$\overline{INT0}$
72	50	$\overline{INT1}$
73	51	V_{SSF}
74	52	V_{DDF}
75	53	$\overline{INT2}$
76	54	V_{SS}
77	55	V_{DD}
78	—	TC1
79	56	$\overline{INT3}$
80	—	TC0
81	—	$\overline{CS3}$
82	57	INT4
83	—	$\overline{CS2}$
84	58	$\overline{INT5}$
85	—	$\overline{CS1}$

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Table 4-1. Package Pinouts (Sheet 4 of 5)

Pin Number		Pin Name
144-Pin Package	100-Pin Package	
86	—	$\overline{CS0}$
87	59	V_{PP}
88	60	$\overline{INT6}$
89	61	$\overline{INT7}$
90	62	MOSI
91	63	MISO
92	64	V_{STBY}
93	65	SCK
94	66	$\overline{SS}$
95	—	$\overline{OE}$
96	—	$\overline{EB3}$
97	67	$\overline{SHS}$ / PE7
98	—	$\overline{EB2}$
99	68	$\overline{TA}$ / PE6
100	—	$\overline{EB1}$
101	—	$\overline{EB0}$
102	69	$\overline{TEA}$ / PE5
103	70	V_{DDH}
104	71	PQB3
105	72	PQB2
106	73	PQB1
107	74	PQB0
108	75	PQA4
109	76	PQA3
110	77	PQA1
111	78	PQA0
112	79	V_{RL}
113	80	V_{RH}
114	81	V_{SSA}
115	82	V_{DDA}

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Table 4-1. Package Pinouts (Sheet 5 of 5)

Pin Number		Pin Name
144-Pin Package	100-Pin Package	
116	—	A22
117	—	A21
118	83	$\overline{\text{RESET}}$
119	—	A20
120	84	$\overline{\text{RSTOUT}}$
121	—	A19
122	—	A18
123	85	V_{DDSYN}
124	86	XTAL
125	87	EXTAL
126	88	V_{SSSYN}
127	89	V_{SS}
128	90	CLKOUT
129	91	V_{DD}
130	92	TCLK
131	—	A17
132	—	A16
133	93	TDI
134	—	A15
135	94	TDO
136	—	A14
137	—	A13
138	95	TMS
139	—	A12
140	96	V_{SS}
141	97	V_{DD}
142	98	$\overline{\text{TRST}}$
143	99	$\overline{\text{DE}}$
144	100	D31 / PA7

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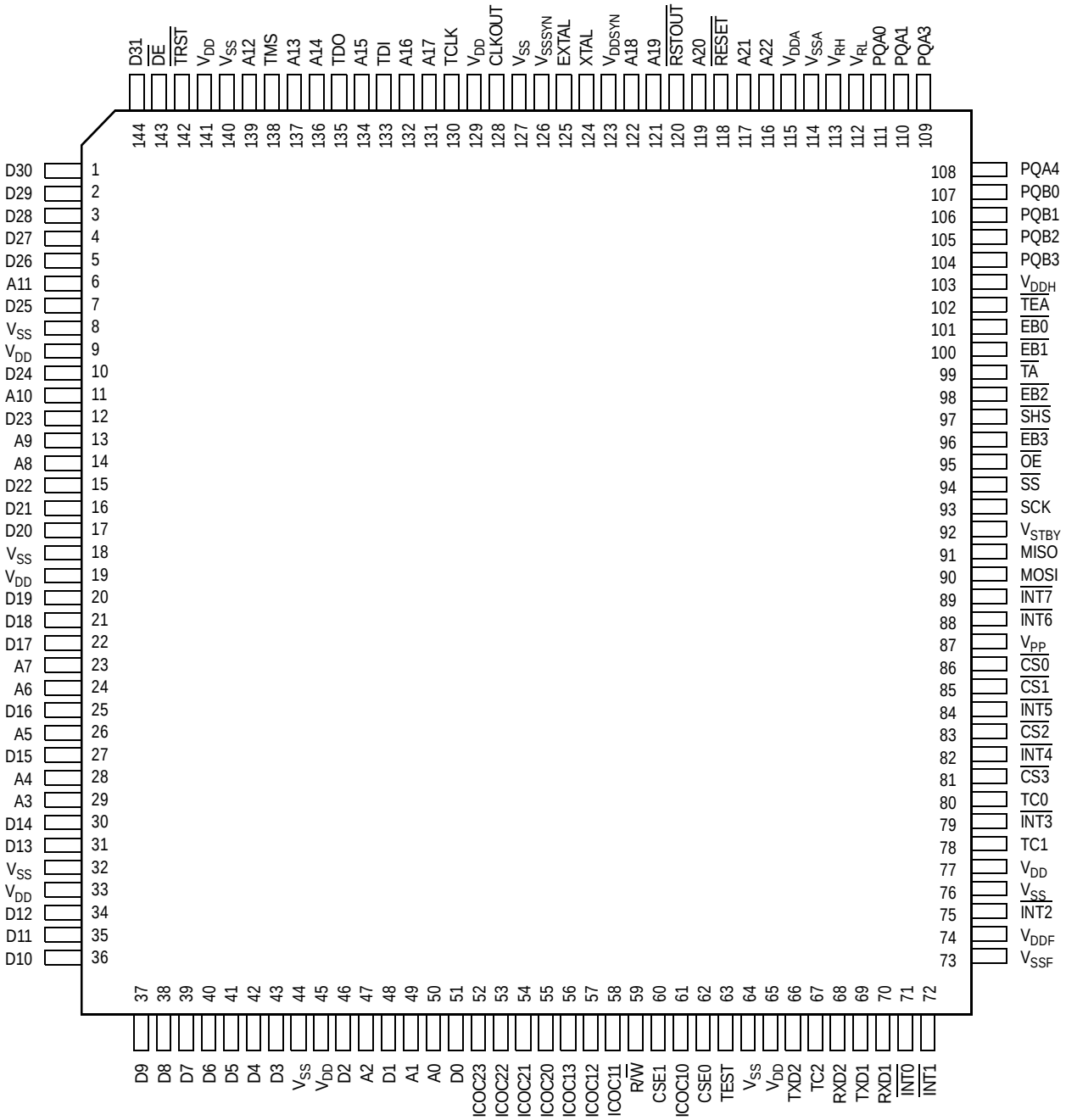

Figure 4-1. 144-Pin LQFP Assignments

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Signal Description

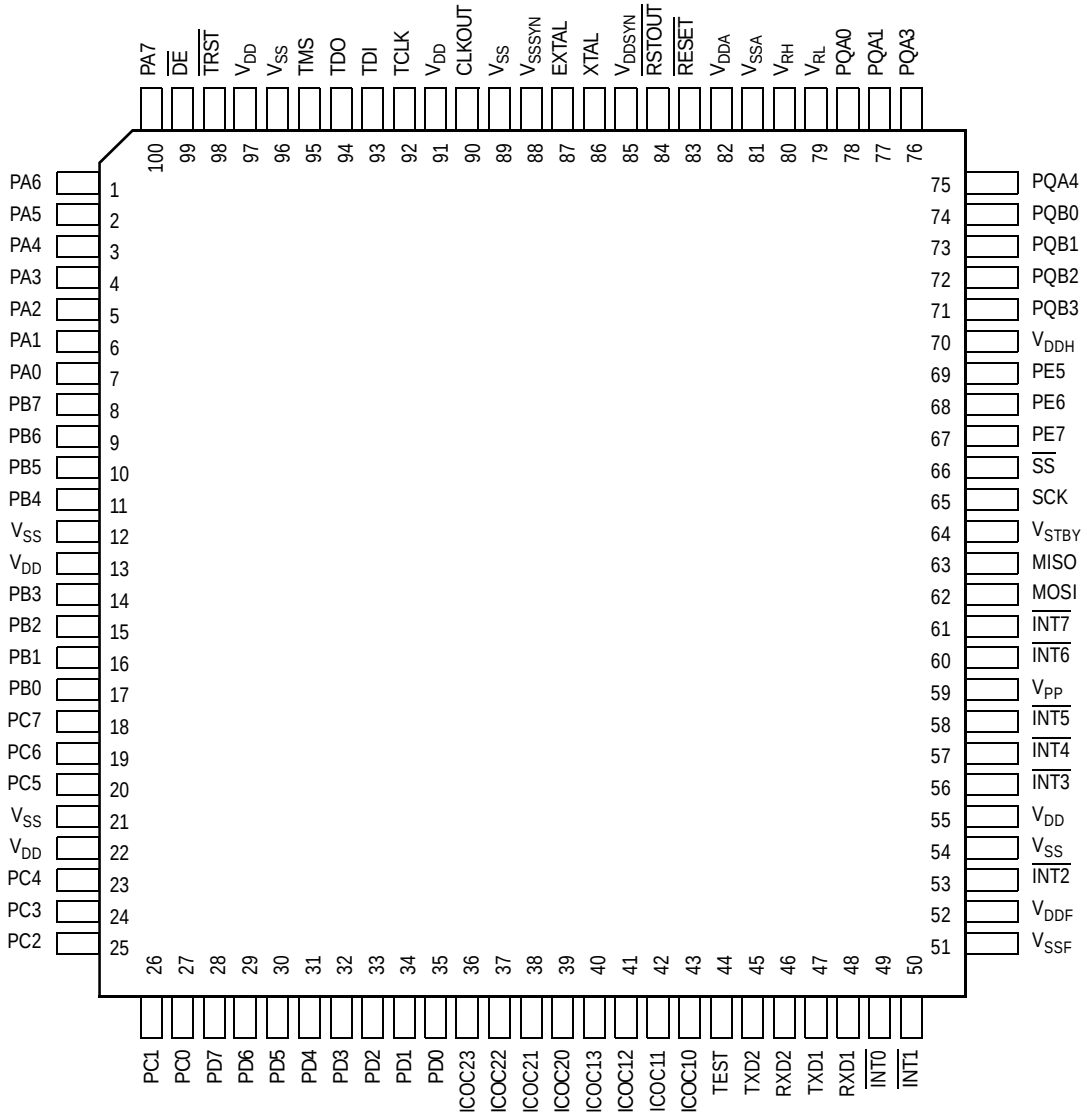

Figure 4-2. 100-Pin LQFP Assignments

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Table 4-2. Signal Descriptions (Sheet 1 of 3)

Name[1]	Alternate	Qty.	Dir.	Input Hyst.	Input Sync.[2]	Drive Strength Control[3]	Pullup[4]	Output Driver (ST/OD/SP)[5]
Reset								
$\overline{\text{RESET}}$	—	1	I/O[6]	Y	Y	—	Pullup	—
$\overline{\text{RSTOUT}}$	$\overline{\text{SHOWINT}}$	1	I/O[6]	—	—	LOAD	—	ST
Clock								
EXTAL	—	1	I	N	N	—	—	SP
XTAL	—	1	O	—	—	—	—	SP
CLKOUT	—	1	I/O[6]	—	—	LOAD	—	ST
V_{DDSYN}	—	1	I	—	—	—	—	—
V_{SSSYN}	—	1	I	—	—	—	—	—
External Memory Interface and Ports								
D[31:0]	PA[7:0], PB[7:0] PC[7:0], PD[7:0]	32	I/O	Y	Y	LOAD	—	ST
$\overline{\text{SHS}}$	$\overline{\text{RCON}}$ / PE7	1	I/O	Y	Y	LOAD	Pullup	ST
$\overline{\text{TA}}$	PE6	1	I/O	Y	Y	LOAD	Pullup	ST
TEA	PE5	1	I/O	Y	Y	LOAD	Pullup	ST
CSE[1:0]	PE[4:3]	2	I/O	Y	Y	LOAD	Pullup	ST
TC[2:0]	PE[2:0]	3	I/O	Y	Y	LOAD	Pullup	ST
R/$\overline{\text{W}}$	PF7	1	I/O	Y	Y	LOAD	Pullup	ST
A[22:0]	PF[6:0], PG[7:0] PH[7:0]	23	I/O	Y	Y	LOAD	Pullup	ST
$\overline{\text{EB[3:0]}}$	PI[7:4]	4	I/O	Y	Y	LOAD	Pullup	ST
$\overline{\text{CS[3:0]}}$	PI[3:0]	4	I/O	Y	Y	LOAD	Pullup	ST
$\overline{\text{OE}}$	—	1	I/O[6]	—	—	LOAD	—	ST
Edge Port								
$\overline{\text{INT[7:6]}}$	TSIZ[1:0] / GPIO	2	I/O	Y	Y	LOAD	—	—
$\overline{\text{INT[5:2]}}$	PSTAT[3:0] / GPIO	4	I/O	Y	Y	LOAD	—	—
$\overline{\text{INT[1:0]}}$	GPIO	2	I/O	Y	Y	LOAD	—	—

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Signal Description

Table 4-2. Signal Descriptions (Sheet 2 of 3)

Name[1]	Alternate	Qty.	Dir.	Input Hyst.	Input Sync.[2]	Drive Strength Control[3]	Pullup[4]	Output Driver (ST/OD/SP)[5]
Serial Peripheral Interface (SPI)								
MOSI	GPIO	1	I/O	Y	Y	RDPSP0	Pullup[4]	ST / OD[7]
MISO	GPIO	1	I/O	Y	Y	RDPSP0	Pullup[4]	ST / OD[7]
SCK	GPIO	1	I/O	Y	Y	RDPSP0	Pullup[4]	ST / OD[7]
$\overline{SS}$	GPIO	1	I/O	Y	Y	RDPSP0	Pullup[4]	ST / OD[7]
Serial Communication Interface (SCI1 and SCI2)								
TXD1	GPIO	1	I/O	Y	Y	RDPSCI0	Pullup[4]	ST / OD[7]
RXD1	GPIO	1	I/O	Y	Y	RDPSCI0	Pullup[4]	ST / OD[7]
TXD2	GPIO	1	I/O	Y	Y	RDPSCI0	Pullup[4]	ST / OD[7]
RXD2	GPIO	1	I/O	Y	Y	RDPSCI0	Pullup[4]	ST / OD[7]
Timer 1 and Timer 2								
ICOC13	IC / OC / PAI / GPIO	1	I/O	Y	Y	RDPT	Pullup[4]	ST
ICOC1[2:0]	IC / OC / GPIO	3	I/O	Y	Y	RDPT	Pullup[4]	ST
ICOC23	IC / OC / PAI / GPIO	1	I/O	Y	Y	RDPT	Pullup[4]	ST
ICOC2[2:0]	IC / OC / GPIO	3	I/O	Y	Y	RDPT	Pullup[4]	ST
Queued Analog-to-Digital Converter (QADC)								
PQA4–PQA3, PQA1–PQA0	GPIO	4	I/O	Y	Y	—	—	ST
PQB[3:0]	GPI	4	I	Y	Y	—	—	—
V_{RH}	—	1	I	—	—	—	—	—
V_{RL}	—	1	I	—	—	—	—	—
V_{DDA}	—	1	I	—	—	—	—	—
V_{SSA}	—	1	I	—	—	—	—	—
V_{DDH}	—	1	I	—	—	—	—	—

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Table 4-2. Signal Descriptions (Sheet 3 of 3)

Name[1]	Alternate	Qty.	Dir.	Input Hyst.	Input Sync.[2]	Drive Strength Control[3]	Pullup[4]	Output Driver (ST/OD/SP)[5]
Debug and JTAG Test Port Control								
$\overline{\text{TRST}}$	—	1	I	Y	N	—	Pullup	—
TCLK	—	1	I	Y	N	—	Pullup	—
TMS	—	1	I	Y	N	—	Pullup	—
TDI	—	1	I	Y	N	—	Pullup	—
TDO	—	1	O[8]	—	—	LOAD	—	ST
$\overline{\text{DE}}$	—	1	I/O	Y	N	LOAD	Pullup	OD
Test								
TEST	—	1	I	Y	N	—	—	—
Power Supplies								
V_{PP}	—	1	I	—	—	—	—	—
V_{DDF}	—	1	I	—	—	—	—	—
V_{SSF}	—	1	I	—	—	—	—	—
V_{STBY}	—	1	I	—	—	—	—	—
V_{DD}	—	5	I	—	—	—	—	—
V_{SS}	—	5	I	—	—	—	—	—
V_{DD}	—	3	I	—	—	—	—	—
V_{SS}	—	3	I	—	—	—	—	—
Total		100						
Total with optional pins		144						

1. Shaded signals are for optional bond-out for 144-pin package.
2. Synchronized input used only if signal configured as a digital I/O. $\overline{\text{RESET}}$ signal is always synchronized, except in low-power stop mode.
3. LOAD (chip configuration register bit), RDPSP0 (SPIPURD register bit in SPI), RDPSCI0 (SCIPURD register bit in both SCIs), RDPT (TIMSCR2 register bit in both timers)
4. All pullups are disconnected when the signal is programmed as an output.
5. Output driver type: ST = standard, OD = standard driver with open-drain pulldown option selected, SP = special
6. Digital input function for $\overline{\text{RSTOUT}}$, CLKOUT, $\overline{\text{OE}}$, and digital output function for $\overline{\text{RESET}}$ used only for JTAG boundary scan
7. Open-drain and pullup function selectable via programmer's model in module configuration registers
8. Three-state output with no input function

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4.4 MMC2107 Specific Implementation Signal Issues

Most modules are designed to allow expanded capabilities if all the module signals to the pads are implemented. This subsection discusses how these modules are implemented on the MMC2107.

4.4.1 $\overline{\text{RSTOUT}}$ Signal Functions

The $\overline{\text{RSTOUT}}$ signal has these multiple functions:

- Whenever the internal system reset is asserted, the $\overline{\text{RSTOUT}}$ signal will always be asserted to indicate the reset condition to the system.
- If the internal reset is not asserted, then setting the FRCRSTOUT bit in the reset control register will assert the $\overline{\text{RSTOUT}}$ signal for as long as the FRCRSTOUT bit is set.
- If the internal reset is not asserted and the FRCRSTOUT bit is not set, then setting the SHOWINT bit in the chip configuration register will reflect internal interrupt requests out to the $\overline{\text{RSTOUT}}$ signal.
- If the internal reset is not asserted and the FR$\overline{\text{CRSTOUT}}$ bit is not set and the SHOWINT bit is not set, then the $\overline{\text{RSTOUT}}$ signal will be negated to indicate to the system that there is no reset condition.

CAUTION: *External logic used to drive reset configuration data during reset needs to be considered when using the $\overline{\text{RSTOUT}}$ signal for a function other than an indication of reset.*

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4.4.2 $\overline{\text{INT}}$ Signal Functions

The $\overline{\text{INT}}$ signals have these multiple functions:

- If the SZEN bit in the chip configuration register is set, then $\overline{\text{INT}}$[7:6] will be used to reflect the state of the TSIZ[1:0] signals from the M•CORE.
- If the PSTEN bit in the chip configuration register is set, then $\overline{\text{INT}}$[5:2] will be used to reflect the state of the PSTAT[3:0] signals from the M•CORE.

NOTE: *If the SZEN or PSTEN bits are set during emulation mode, then the corresponding edge port $\overline{\text{INT}}$ functions are lost and will not be emulated externally.*

The default reset values for PUPSCI1 and PUPSCI0 will be 0. Thus, the pullup function is disabled by default.

4.5 Signal Descriptions

This subsection provides a brief description of the signals. For more detailed information, reference the module section.

4.5.1 Reset Signals

These signals are used to either reset the chip or as a reset indication.

4.5.1.1 Reset In ($\overline{\text{RESET}}$)

This active-low input signal is used as an external reset request.

4.5.1.2 Reset Out ($\overline{\text{RSTOUT}}$)

This active-low output signal is an indication that the internal reset controller has reset the chip. When $\overline{\text{RSTOUT}}$ is active, the user may drive override options on the data bus. $\overline{\text{RSTOUT}}$ is three-stated in phase-lock loop (PLL) test mode.

$\overline{\text{RSTOUT}}$ may also be used to reflect an indication of an internal interrupt request.

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4.5.2 Phase-Lock Loop (PLL) and Clock Signals

These signals are used to support the on-chip clock generation circuitry.

4.5.2.1 External Clock In (EXTAL)

This input signal is always driven by an external clock input except when used as a connection to the external crystal when the internal oscillator circuit is used. The clock source is configured during reset.

4.5.2.2 Crystal (XTAL)

This output signal is used as a connection to the external crystal when the internal oscillator circuit is used. XTAL should be grounded when using an external clock input.

4.5.2.3 Clock Out (CLKOUT)

This output signal reflects the internal system clock.

4.5.2.4 Synthesizer Power (V_{DDSYN} and V_{SSSYN})

These are dedicated quiet power and ground supply signals for the frequency synthesizer circuit.

4.5.3 External Memory Interface Signals

In addition to the function stated here, these signals can be configured as discrete I/O signals also.

4.5.3.1 Data Bus (D[31:0])

These three-state bidirectional signals provide the general-purpose data path between the microcontroller unit (MCU) and all other devices.

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4.5.3.2 Show Cycle Strobe ($\overline{SHS}$)

This output signal is used in emulation mode as a strobe for capturing addresses, controls, and data during show cycles. This signal is also used as $\overline{RCON}$.

NOTE: *This input signal, used only during reset, indicates whether the states on the external signals affect the chip configuration.*

4.5.3.3 Transfer Acknowledge ($\overline{TA}$)

This signal indicates that the external data transfer is complete. During a read cycle, when the processor recognizes $\overline{TA}$, it latches the data and then terminates the bus cycle. During a write cycle, when the processor recognizes $\overline{TA}$, the bus cycle is terminated. This signal is an input in master and emulation modes.

4.5.3.4 Transfer Error Acknowledge ($\overline{TEA}$)

This signal indicates an error condition exists for the bus transfer. The bus cycle is terminated and the central processor unit (CPU) begins execution of the access error exception. This signal is an input in master and emulation modes.

4.5.3.5 Emulation Mode Chip Selects (CSE[1:0])

These output signals provide information for development support.

4.5.3.6 Transfer Code (TC[2:0])

These output signals indicate the data transfer code for the current bus cycle.

4.5.3.7 Read/Write (R/$\overline{W}$)

This output signal indicates the direction of the data transfer on the bus. A logic 1 indicates a read from a slave device and a logic 0 indicates a write to a slave device.

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4.5.3.8 Address Bus (A[22:0])

These output signals provide the address for the current bus transfer.

4.5.3.9 Enable Byte ($\overline{EB}$[3:0])

These output signals indicate which byte of data is valid during external cycles.

4.5.3.10 Chip Select ($\overline{CS}$[3:0])

These output signals select external devices for external bus transactions.

4.5.3.11 Output Enable ($\overline{OE}$)

This output signal indicates when an external device can drive data during external read cycles.

4.5.4 Edge Port Signals

These signals are used by the edge port module.

4.5.4.1 External Interrupts ($\overline{INT}$[7:6])

These bidirectional signals function as either external interrupt sources or GPIO. Also, these signals may be used to reflect the internal TSIZ[1:0] signals and externally to provide an indication of the M•CORE transfer size.

4.5.4.2 External Interrupts ($\overline{INT}$[5:2])

These bidirectional signals function as either external interrupt sources or GPIO. Also, these signals may be used to reflect the internal PSTAT[3:0] signals and externally to provide an indication of the M•CORE processor status.

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4.5.4.3 External Interrupts ($\overline{INT[1:0]}$)

These bidirectional signals function as either external interrupt sources or GPIO.

4.5.5 Serial Peripheral Interface Module Signals

These signals are used by the SPI module and may also be configured to be discrete I/O signals.

4.5.5.1 Master Out/Slave In (MOSI)

This signal is the serial data output from the SPI in master mode and the serial data input in slave mode.

4.5.5.2 Master In/Slave Out (MISO)

This signal is the serial data input to the SPI in master mode and the serial data output in slave mode.

4.5.5.3 Serial Clock (SCK)

The serial clock synchronizes data transmissions between master and slave devices. SCK is an output if the SPI is configured as a master and SCK is an input if the SPI is configured as a slave.

4.5.5.4 Slave Select ($\overline{SS}$)

This I/O signal is the peripheral chip select signal in master mode and is an active-low slave select in slave mode.

4.5.6 Serial Communications Interface Module Signals

These signals are used by the two SCI modules.

4.5.6.1 Receive Data (RXD1 and RXD2)

These signals are used for the SCI receiver data input and are also available for GPIO when not configured for receiver operation.

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4.5.6.2 Transmit Data (TXD1 and TXD2)

These signals are used for the SCI transmitter data output and are also available for GPIO when not configured for transmitter operation.

4.5.7 Timer Signals (ICOC1[3:0] and ICOC2[3:0])

These signals provide the external interface to the timer functions. They may be configured as general-purpose I/O if the timer output function is not needed. The default state at reset is general-purpose input.

4.5.8 Analog-to-Digital Converter Signals

These signals are used by the analog-to-digital converter (QADC) module.

4.5.8.1 Analog Inputs (PQA[4:3], PQA[1:0], and PQB[3:0])

These signals provide the analog inputs to the QADC. The PQA signals may also be used as general-purpose digital I/O. The PQB signals may also be used as general-purpose digital inputs.

4.5.8.2 Analog Reference (V_{RH} and V_{RL})

These signals serve as the high (V_{RH}) and low (V_{RL}) reference potentials for the analog converter.

4.5.8.3 Analog Supply (V_{DDA} and V_{SSA})

These dedicated power supply signals isolate the sensitive analog circuitry from the normal levels of noise present on the digital power supply.

4.5.8.4 Positive Supply (V_{DDH})

This signal supplies positive power to the ESD structures in the QADC pads.

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4.5.9 Debug and Emulation Support Signals

These signals are used as the interface to the on-chip JTAG (Joint Test Action Group) controller and also to interface to the OnCE logic.

4.5.9.1 Test Reset ($\overline{TRST}$)

This active-low input signal is used to initialize the JTAG and OnCE logic asynchronously.

4.5.9.2 Test Clock (TCLK)

This input signal is the test clock used to synchronize the JTAG and OnCE logic.

4.5.9.3 Test Mode Select (TMS)

This input signal is used to sequence the JTAG state machine. TMS is sampled on the rising edge of TCLK.

4.5.9.4 Test Data Input (TDI)

This input signal is the serial input for test instructions and data. TDI is sampled on the rising edge of TCLK.

4.5.9.5 Test Data Output (TDO)

This output signal is the serial output for test instructions and data. TDO is three-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.

4.5.9.6 Debug Event ($\overline{DE}$)

This is a bidirectional, active-low signal. As an output, this signal will be asserted for three system clocks, synchronous to the rising CLKOUT edge, to acknowledge that the CPU has entered debug mode as a result of a debug request or a breakpoint condition. As an input, this signal provides multiple functions.

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4.5.10 Test Signal (TEST)

This input signal (TEST) is reserved for factory testing only and should be connected to V_{SS} to prevent unintentional activation of test functions.

4.5.11 Power and Ground Signals

These signals provide system power and ground to the chip. Multiple signals are provided for adequate current capability. All power supply signals must have adequate bypass capacitance for high-frequency noise suppression.

4.5.11.1 Power for FLASH Erase/Program (V_{PP})

This signal supplies an isolated power for FLASH program and erase operations.

4.5.11.2 Power and Ground for FLASH Array (V_{DDF} and V_{SSF})

These signals supply an isolated power and ground to the FLASH array.

4.5.11.3 Standby Power (V_{STBY})

This signal is used to provide standby voltage to the RAM array if V_{DD} is lost.

4.5.11.4 Positive Supply (V_{DD})

This signal supplies positive power to the core logic and I/O pads.

4.5.11.5 Ground (V_{SS})

This signal is the negative supply (ground) to the chip.

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Section 5. Reset Controller Module

5.1 Contents

5.2 Introduction 130
5.3 Features 130
5.4 Block Diagram 131
5.5 Signals 131
5.6 Memory Map and Registers 132
5.6.1 Reset Control Register 133
5.6.2 Reset Status Register 134
5.6.3 Reset Test Register 135
5.7 Functional Description 136
5.7.1 Reset Sources 136
5.7.1.1 Power-On Reset 137
5.7.1.2 External Reset 137
5.7.1.3 Watchdog Timer Reset 137
5.7.1.4 Loss of Clock Reset 137
5.7.1.5 Loss of Lock Reset 138
5.7.1.6 Software Reset 138
5.7.2 Reset Control Flow 138
5.7.2.1 Synchronous Reset Requests 138
5.7.2.2 Internal Reset Request 140
5.7.2.3 Power-On Reset 140
5.7.3 Concurrent Resets 140
5.7.3.1 Reset Flow 140
5.7.3.2 Reset Status Flags 141
5.8 Interrupts 141

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5.2 Introduction

The reset controller is provided to:

- Determine the cause of reset
- Assert the appropriate reset signals to the system
- Keep a history of what caused the reset

5.3 Features

Features of the reset controller module include:

- Six sources of reset:
  - External
  - Power-on reset (POR)
  - Watchdog timer
  - Phase-lock loop (PLL) loss of lock
  - PLL loss of clock
  - Software
- Software can assert external $\overline{\text{RSTOUT}}$ pin independent of chip reset state.
- Software readable status flags indicating the cause of the last reset

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5.4 Block Diagram

Figure 5-1 shows the structure of the reset controller.

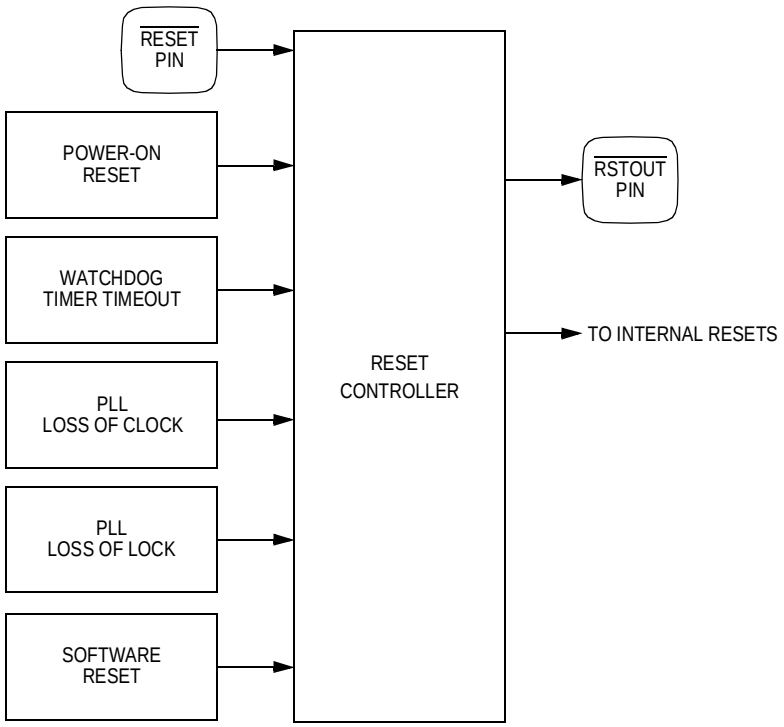

Figure 5-1. Reset Controller Block Diagram

5.5 Signals

See **Table 5-1** for an overview of the reset controller signal properties. For additional information, refer to **Section 4. Signal Description**.

Table 5-1. Reset Controller Signal Properties

Name	Alternate	Direction	Input Hysteresis	Input Synchronization	Pullup(1)
$\overline{\text{RESET}}$ pin	—	I	Y	Y(2)	Y
$\overline{\text{RSTOUT}}$ pin	$\overline{\text{SHOWINT}}$	O	—	—	—

1. Pullups are disconnected from pins configured as outputs.
2. $\overline{\text{RESET}}$ is always synchronized except when in low-power stop mode.

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5.6 Memory Map and Registers

The reset controller programming model consists of the following registers:

- Reset control register (RCR) — Selects interrupt controller functions
- Reset status register (RSR) — Reflects the state of the last reset source
- Reset test register (RTR) — Used only for factory test

Table 5-2. Reset Controller Module Memory Map

Address	Bits 7–0	Access[1]
0x000c4_0000	Reset control register (RCR)	S/U
0x000c4_0001	Reset status register (RSR)	S/U
0x000c4_0002	Reset test register (RTR)	S/U
0x000c4_0003	Reserved[2]	—

1. S/U = CPU supervisor or user mode access. User mode accesses to supervisor only addresses have no effect and result in a a cycle termination transfer error.
2. Within the specified module memory map, accessing reserved addresses does not generate a bus error exception. Reads of reserved addresses return 0s and writes have no effect.

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5.6.1 Reset Control Register

The reset control register (RCR) allows software control for requesting a reset or for independently asserting the external $\overline{\text{RSTOUT}}$ pin. RCR is read/write always.

Address: 0x000c4_0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SOFTRST	FRC-RSTOUT	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 5-2. Reset Control Register (RCR)

SOFTRST — Software Reset Request Bit

The SOFTRST bit allows software to request a reset. Note that the reset caused by setting this bit clears this bit.

1 = Request software reset
0 = No software reset request

FRCRSTOUT — Force $\overline{\text{RSTOUT}}$ Pin Bit

The FRCRSTOUT bit allows software to assert or negate the external $\overline{\text{RSTOUT}}$ pin.

1 = Assert the $\overline{\text{RSTOUT}}$ pin.
0 = Do not assert the $\overline{\text{RSTOUT}}$ pin.

CAUTION: *External logic driving reset configuration data during reset needs to be considered when asserting the $\overline{\text{RSTOUT}}$ pin when setting FRCRSTOUT.*

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5.6.2 Reset Status Register

The reset status register (RSR) contains a status bit for every reset source. When reset is entered, the cause of the reset condition is latched along with a value of 0 for the other reset sources that were not pending at the time of the reset condition. These values are then reflected in the RSR. One or more status bits may be set at the same time. The cause of any subsequent reset is also recorded in the register, overwriting status from the previous reset condition.

RSR can be read at any time. Writing to RSR has no effect.

Address: 0x000c4_0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	SOFT	WDR	POR	EXT	LOC	LOL
Write:								
Reset:	0	0	Reset dependent					

= Writes have no effect and the access terminates without a transfer error exception.

Figure 5-3. Reset Status Register (RSR)

SOFT— Software Reset Flag

SOFT indicates that the last reset was caused by software.
1 = Last reset caused by software
0 = No software reset

WDR — Watchdog Timer Reset Flag

WDR indicates that the last reset was caused by a watchdog timer timeout.
1 = Last reset caused by watchdog timer timeout
0 = No watchdog timer timeout reset

POR — Power-On Reset Flag

POR indicates that the last reset was caused by a power-on reset.
1 = Last reset caused by power-on reset
0 = Last reset not caused by power-on reset

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EXT — External Reset Flag

EXT indicates that the last reset was caused by an external device asserting the external $\overline{\text{RESET}}$ pin.

1 = Last reset state caused by external device asserting the external $\overline{\text{RESET}}$ pin
0 = No external reset

LOC — Loss of Clock Reset Flag

LOC indicates that the last reset state was caused by a loss of clock detected by the loss of clock circuit.

1 = Last reset caused by loss of clock
0 = No loss of clock reset

LOL — Loss of Lock Reset Flag

LOL indicates that the last reset state was caused by a loss of lock detected by the PLL circuit.

1 = Last reset caused by loss of lock
0 = No loss of lock

5.6.3 Reset Test Register

The reset test register (RTR) is used only for factory testing.

This register is read-only when not in test mode.

Address: 0x000c4_0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 5-4. Reset Test Register (RTR)

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5.7 Functional Description

This subsection provides a functional description of the MMC2107 reset controller module.

5.7.1 Reset Sources

Table 5-3 defines the sources of reset and the signals driven by the reset controller.

Table 5-3. Reset Source Summary

Source	Type
Power on	Asynchronous
External $\overline{\text{RESET}}$ pin (not stop mode)	Synchronous
External $\overline{\text{RESET}}$ pin (during stop mode)	Asynchronous
Watchdog timer	Synchronous
Loss of clock	Asynchronous
Loss of lock	Asynchronous
Software	Synchronous

To protect data integrity, a synchronous reset source is not acted upon by the reset control logic until the end of the current bus cycle. Reset is then asserted on the next rising edge of the system clock after the cycle is terminated. Whenever the reset control logic must synchronize reset to the end of the bus cycle, the internal bus monitor is automatically enabled regardless of the BME bit setting in the chip configuration register (CCR). Then if the current bus cycle is not terminated normally, the bus monitor terminates the cycle based on the length of time programmed in the BMT field of CCR.

Internal single-byte, half-word, or word writes are guaranteed to complete without data corruption when a synchronous reset occurs. External writes, including word writes to 16-bit ports, are also guaranteed to complete.

Asynchronous reset sources usually indicate a catastrophic failure. Therefore, the reset control logic does not wait for the current bus cycle to complete. Reset is asserted immediately to the system.

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5.7.1.1 Power-On Reset

At power-up, the reset controller asserts $\overline{\text{RSTOUT}}$. $\overline{\text{RSTOUT}}$ continues to be asserted until V_{DD} has reached a minimum acceptable level and, if a PLL clock mode is selected, until the PLL achieves phase lock. Then after approximately another 512 cycles, $\overline{\text{RSTOUT}}$ is negated and the part begins operation.

5.7.1.2 External Reset

Asserting the external $\overline{\text{RESET}}$ pin for at least four rising CLKOUT edges causes the external reset request to be recognized and latched. The bus monitor is enabled and the current bus cycle is completed. The reset controller asserts $\overline{\text{RSTOUT}}$ for approximately 512 cycles after the $\overline{\text{RESET}}$ pin is negated and the PLL has acquired lock. The part then exits reset and begins operation.

In low-power stop mode, the system clocks are stopped. Asserting the external $\overline{\text{RESET}}$ pin during stop mode causes an external reset to be recognized.

5.7.1.3 Watchdog Timer Reset

A watchdog timer timeout causes the watchdog timer reset request to be recognized and latched. The bus monitor is enabled and the current bus cycle is completed. If the $\overline{\text{RESET}}$ pin is negated and the PLL has acquired lock, the reset controller asserts $\overline{\text{RSTOUT}}$ for approximately 512 cycles. Then the part exits reset and begins operation.

5.7.1.4 Loss of Clock Reset

This reset condition occurs in PLL clock mode when the LOCRE bit in SYNCR is set and either the PLL reference or the PLL fails. The reset controller asserts $\overline{\text{RSTOUT}}$ for approximately 512 cycles after the PLL has acquired lock. The part then exits reset and begins operation.

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5.7.1.5 Loss of Lock Reset

This reset condition occurs in PLL clock mode when the LOLRE bit in SYNCR is set and the PLL loses lock. The reset controller asserts RSTOUT for approximately 512 cycles after the PLL has acquired lock. The part then exits reset and begins operation.

5.7.1.6 Software Reset

A software reset occurs when the SOFTRST bit is set. If the RESET pin is negated and the PLL has acquired lock, the reset controller asserts RSTOUT for approximately 512 cycles. Then the part exits reset and begins operation.

5.7.2 Reset Control Flow

Figure 5-5 shows the reset logic control flow. In the flow description that follows, there are references in parentheses to the control state box numbers in the figure. All cycle counts given are approximate.

5.7.2.1 Synchronous Reset Requests

If either the external RESET pin is asserted by an external device for at least four rising CLKOUT edges (3), or the watchdog timer times out, or software requests a reset, the reset control logic latches the reset request internally and enables the bus monitor (5). When the current bus cycle is completed (6), RSTOUT is asserted (7). The reset control logic waits until the RESET pin is negated (8) and for the PLL to attain lock (9, 9A) before waiting 512 CLKOUT cycles (10). The reset control logic may latch the configuration according to the RCON pin level (11, 11A) before negating RSTOUT (12).

If the external RESET pin is asserted by an external device for at least four rising CLKOUT edges during the 512 count (10) or during the wait for PLL lock (9A), the reset flow switches to (8) and waits for the RESET pin to be negated before continuing.

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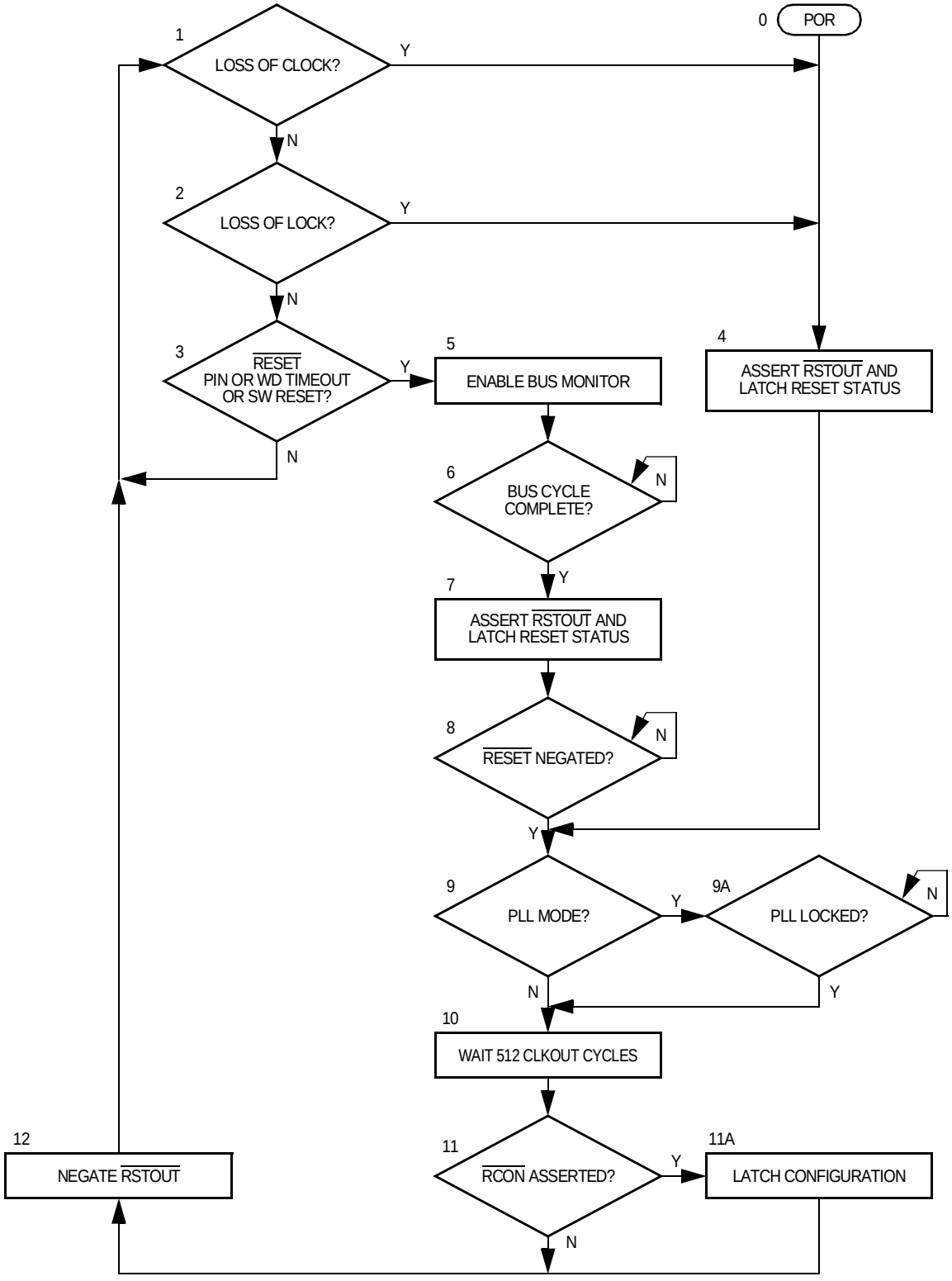

Figure 5-5. Reset Control Flow

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5.7.2.2 Internal Reset Request

If reset is asserted by an asynchronous internal reset source, such as loss of clock (1) or loss of lock (2), the reset control logic asserts RSTOUT (4). The reset control logic waits for the PLL to attain lock (9, 9A) before waiting 512 CLKOUT cycles (10). Then the reset control logic may latch the configuration according to the RCON pin level (11, 11A) before negating RSTOUT (12).

If a loss of lock occurs during the 512 count (10), the reset flow switches to (9A) and waits for the PLL to lock before continuing.

5.7.2.3 Power-On Reset

When the reset sequence is initiated by power-on reset (0), the same reset sequence is followed as for the other asynchronous reset sources.

5.7.3 Concurrent Resets

This subsection describes the concurrent resets.

5.7.3.1 Reset Flow

If a power-on reset condition is detected during any reset sequence, the power-on reset sequence starts immediately (0).

If the external RESET pin is asserted for at least four rising CLKOUT edges while waiting for PLL lock or the 512 cycles, the external reset is recognized. Reset processing switches to wait for the external RESET pin to negate (8).

If a loss of clock or loss of lock condition is detected while waiting for the current bus cycle to complete (5, 6) for an external reset request, the cycle is terminated. The reset status bits are latched (7) and reset processing waits for the external RESET pin to negate (8).

If a loss of clock or loss of lock condition is detected during the 512-cycle wait, the reset sequence continues after a PLL lock (9, 9A).

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5.7.3.2 Reset Status Flags

For a power-on reset, the POR bit in RSR is set, and the SOFT, WDR, EXT, LOC, and LOL bits are cleared even if another type of reset condition is detected during the reset sequence for the POR.

If a loss of clock or loss of lock condition is detected while waiting for the current bus cycle to complete (5, 6) for an external reset request, the EXT bit along with the LOC and/or LOL bits are set.

5.8 Interrupts

The reset controller does not generate interrupt requests.

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Section 6. M•CORE M210 Central Processor Unit (CPU)

6.1 Contents

6.2 Introduction 143
6.3 Features 144
6.4 Microarchitecture Summary 145
6.5 Programming Model 147
6.6 Data Format Summary 149
6.7 Operand Addressing Capabilities 150
6.8 Instruction Set Overview 150

6.2 Introduction

The M•CORE M210 central processor unit (CPU) architecture is one of the most compact, full 32-bit core implementations available. The pipelined reduced instruction set computer (RISC) execution unit uses 16-bit instructions to achieve maximum speed and code efficiency, while conserving on-chip memory resources. The instruction set is designed to support high-level language implementation. A non-intrusive resident debugging system supports product development and in-situ testing. The M•CORE technology library also encompasses a full complement of on-chip peripheral modules designed specifically for embedded control applications.

Total system power consumption is determined by all the system components, rather than the processor core alone. In particular, memory power consumption (both on-chip and external) is a dominant factor in total power consumption of the core plus memory subsystem. With this in mind, the M•CORE instruction set architecture trades absolute performance capability for reduced total energy consumption. This is accomplished while maintaining an acceptably high level of performance at a given clock frequency.

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The streamlined execution engine uses many of the same performance enhancements and implementation techniques incorporated in desktop RISC processors. A strictly defined load/store architecture minimizes control complexity. Use of a fixed, 16-bit instruction encoding significantly lowers the memory bandwidth needed to sustain a high rate of instruction execution, and careful selection of the instruction set allows the code density and overall memory efficiency of the M•CORE architecture to surpass those of complex instruction set computer (CISC) architectures.

These factors reduce system energy consumption significantly, and the fully static M•CORE design uses other techniques to reduce it even more. The core uses dynamic clock management to automatically power-down internal functions that are not in use on a clock-by-clock basis. It also incorporates three power-conservation operating modes, which are invoked via dedicated instructions.

6.3 Features

The main features of the M•CORE are:

- 32-bit load/store RISC architecture
- Fixed 16-bit instruction length
- 16 entry, 32-bit general-purpose register file
- Efficient 4-stage execution pipeline, hidden from application software
- Single-cycle execution for most instructions, 2-cycle branches and memory accesses
- Support for byte/half-word/word memory access
- Fast interrupt support, with 16 entry user-controlled alternate register file
- Vectored and autovectored interrupt support
- On-chip emulation support
- Full static design for minimal power consumption

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6.4 Microarchitecture Summary

Figure 6-1 is a block diagram of the M•CORE processor.

The processor utilizes a 4-stage pipeline for instruction execution. The instruction fetch, instruction decode/register file read, execute, and register file writeback stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The execution unit consists of a 32-bit arithmetic/logic unit, a 32-bit barrel shifter, a find-first-one unit, result feed-forward hardware, and miscellaneous support hardware for multiplication, division, and multiple-register loads and stores.

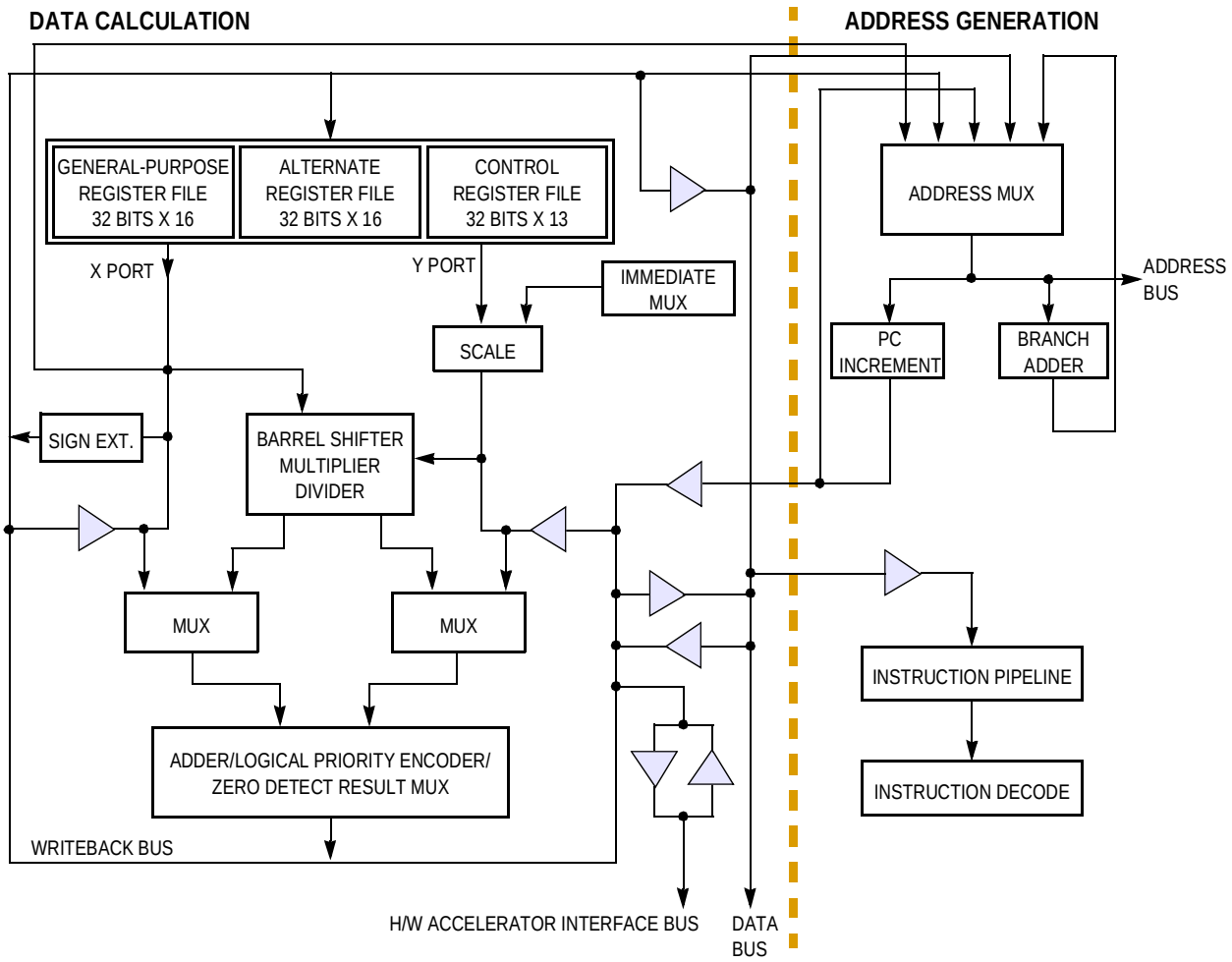

Figure 6-1. M•CORE Processor Block Diagram

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Arithmetic and logical operations are executed in a single cycle. Multiplication is implemented with a 2-bit per clock, overlapped-scan, modified Booth algorithm with early-out capability, to reduce execution time for operations with small multipliers. Divide is implemented with a 1-bit per clock early-in algorithm. The find-first-one unit operates in a single clock cycle.

The program counter unit incorporates a dedicated branch address adder to minimize delays during change of flow operations. Branch target addresses are calculated in parallel with branch instruction decode. Taken branches and jumps require only two clocks; branches which are not taken execute in a single clock.

Memory load and store operations are provided for 8-bit (byte), 16-bit (half-word), and 32-bit (word) data, with automatic zero extension for byte and half-word load operations. These instructions can execute in as few as two clock cycles. Load and store multiple register instructions allow low overhead context save and restore operations. These instructions can execute in (N+1) clock cycles, where N is the number of registers to transfer.

A condition code/carry (C) bit is provided for condition testing and for use in implementing arithmetic and logical operations with operands/results greater than 32 bits. The C bit is typically set by explicit test/comparison operations, not as a side-effect of normal instruction operation. Exceptions to this rule occur for specialized operations where it is desirable to combine condition setting with actual computation.

The processor uses autovectors for both normal and fast interrupt requests. Fast interrupts take precedence over normal interrupts. Both types have dedicated exception shadow registers. For service requests of either kind, an automatic vector is generated when the request is made.

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6.5 Programming Model

Figure 6-2 shows the M•CORE programming model. The model is defined differently for supervisor and user privilege modes. By convention, in both modes R15 serves as the link register for subroutine calls. R0 is typically used as stack pointer.

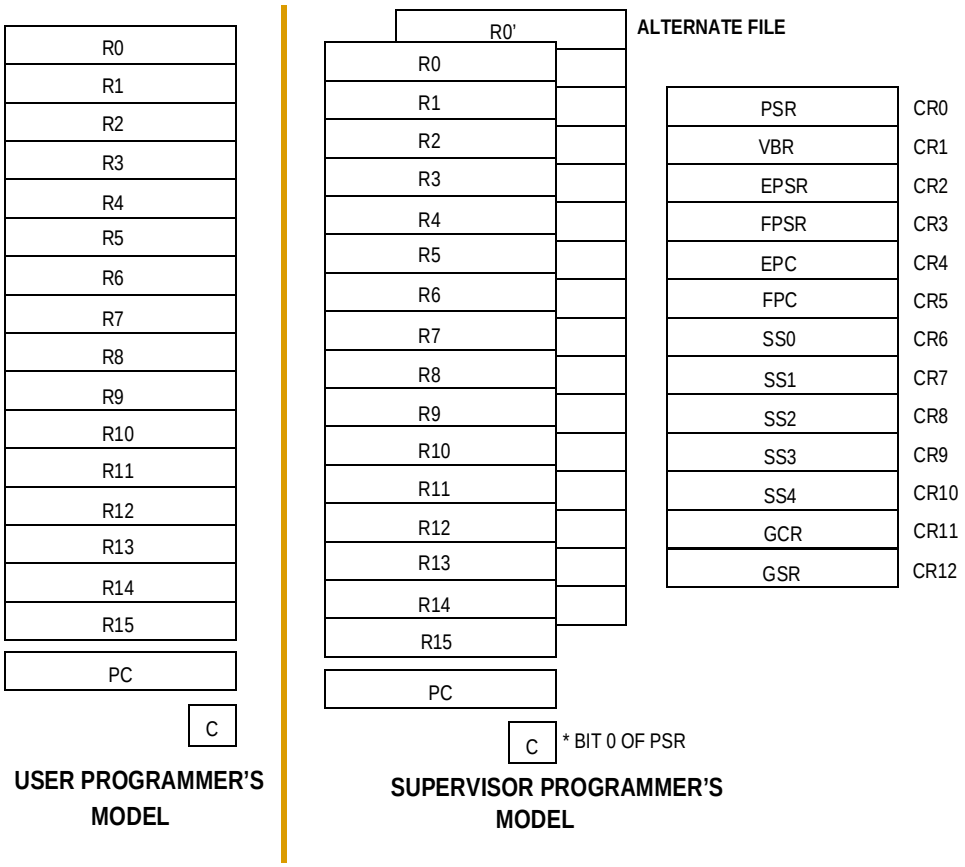

Figure 6-2. Programming Model

The user programming model consists of 16 general-purpose 32-bit registers (R[15:0]), the 32-bit PC, and the C bit. The C bit is implemented as bit 0 of the processor status register (PSR) and is the only portion of the PSR accessible in the user model.

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The supervisor programming model consists of the user model plus 16 additional 32-bit general-purpose registers (R[15:0]', or the alternate file), the entire PSR, and a set of status/control registers (CR[12:0]). Setting the S bit in the PSR enables supervisor mode operation.

The alternate file allows very low overhead context switching for real-time event handling. While the alternate file is enabled, general-purpose operands are accessed from it.

The vector base register (VBR) determines the base address of the exception vector table. Exception shadow registers EPC and EPSR are used to save the states of the program counter and PSR, respectively, when an exception occurs. Shadow registers FPC and FPSR save the states of the program counter and PSR, respectively, when an exception occurs.

Scratch registers (SS[4:0]) are used to handle exception events.

The global control (GCR) and status (GSR) registers can be used for a variety of system monitoring tasks.

The supervisor programming model includes the PSR, which contains operation control and status information. In addition, a set of exception shadow registers is provided to save the state of the PSR and the program counter at the time an exception occurs. A separate set of shadow registers is provided for fast interrupt support to minimize context saving overhead.

Five scratch registers are provided for supervisor software use in handling exception events. A single register is provided to alter the base address of the exception vector table. Two registers are provided for global control and status.

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6.6 Data Format Summary

The operand data formats supported by the integer unit are standard two's-complement data formats. The operand size for each instruction is either explicitly encoded in the instruction (load/store instructions) or implicitly defined by the instruction operation (index operations, byte extraction). Typically, instructions operate on all 32 bits of the source operand(s) and generate a 32-bit result.

Memory is viewed from a big-endian byte ordering perspective. The most significant byte (byte 0) of word 0 is located at address 0. Bits are numbered within a word starting with bit 31 as the most significant bit.

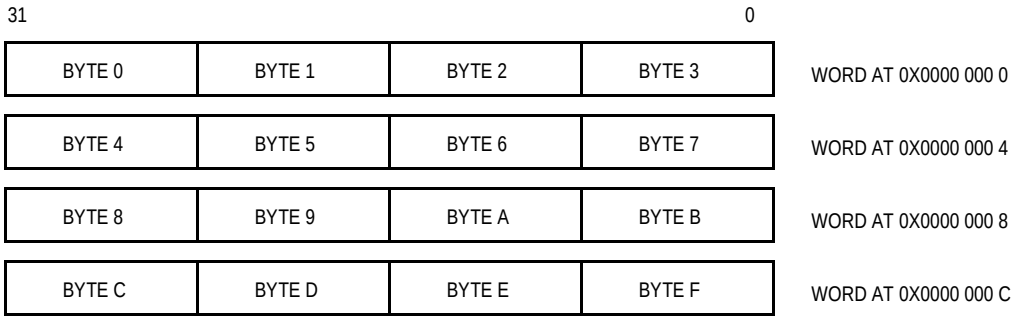

Figure 6-3. Data Organization in Memory

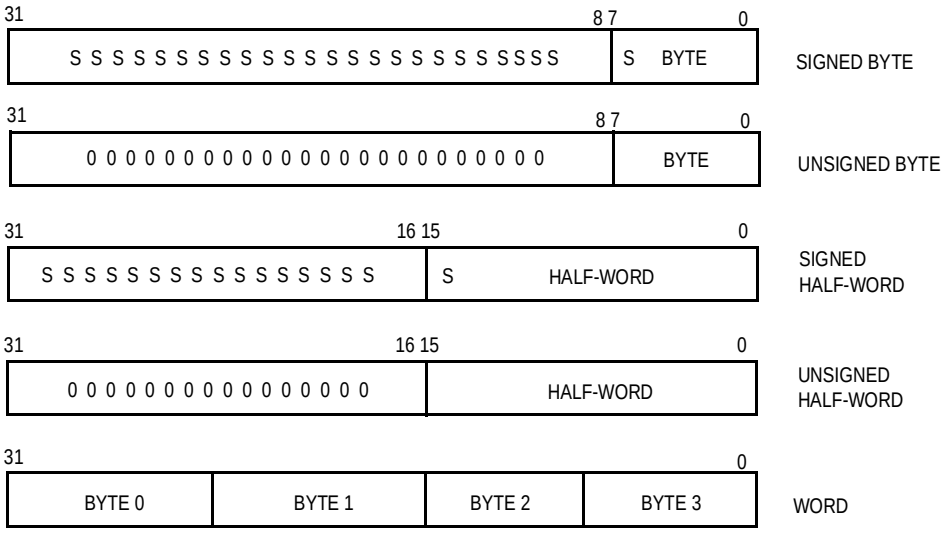

Figure 6-4. Data Organization in Registers

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6.7 Operand Addressing Capabilities

M•CORE accesses all memory operands through load and store instructions, transferring data between the general-purpose registers and memory. Register-plus-four-bit scaled displacement addressing mode is used for load and store instructions addressing byte, half-word, and word data.

Load and store multiple instructions allow a subset of the 16 general-purpose registers to be transferred to or from a base address pointed to by register R0 (the default stack pointer by convention).

Load and store register quadrant instructions use register indirect addressing to transfer a register quadrant to or from memory.

6.8 Instruction Set Overview

The instruction set is tailored to support high-level languages and is optimized for those instructions most commonly executed. A standard set of arithmetic and logical instructions is provided, as well as instruction support for bit operations, byte extraction, data movement, control flow modification, and a small set of conditionally executed instructions which can be useful in eliminating short conditional branches.

Table 6-1 is an alphabetized listing of the M•CORE instruction set. Refer to the *M•CORE Reference Manual* (Motorola document order number MCORERM/AD) for more details on instruction operation.

Table 6-1. M•CORE Instruction Set (Sheet 1 of 3)

Mnemonic	Description
ABS	Absolute Value
ADDC	Add with C Bit
ADDI	Add Immediate
ADDU	Add Unsigned
AND	Logical AND
ANDI	Logical AND Immediate
ANDN	AND NOT
ASR	Arithmetic Shift Right
ASRC	Arithmetic Shift Right, Update C Bit

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Table 6-1. M•CORE Instruction Set (Sheet 2 of 3)

Mnemonic	Description
BCLRI	Bit Clear Immediate
BF	Branch on Condition False
BGENI	Bit Generate Immediate
BGENR	Bit Generate Register
BKPT	Breakpoint
BMASKI	Bit Mask Immediate
BR	Branch
BREV	Bit Reverse
BSETI	Bit Set Immediate
BSR	Branch to Subroutine
BT	Branch on Condition True
BTSTI	Bit Test Immediate
CLRF	Clear Register on Condition False
CLRT	Clear Register on Condition True
CMPHS	Compare Higher or Same
CMPLT	Compare Less Than
CMPLTI	Compare Less Than Immediate
CMPNE	Compare Not Equal
CMPNEI	Compare Not Equal Immediate
DECF	Decrement on Condition False
DECGT	Decrement Register and Set Condition if Result Greater Than Zero
DECLT	Decrement Register and Set Condition if Result Less Than Zero
DECNE	Decrement Register and Set Condition if Result Not Equal to Zero
DECT	Decrement on Condition True
DIVS	Divide Signed Integer
DIVU	Divide Unsigned Integer
DOZE	Doze
FF1	Find First One
INCF	Increment on Condition False
INCT	Increment on Condition True
IXH	Index Half-Word
IXW	Index Word
JMP	Jump
JMPI	Jump Indirect
JSR	Jump to Subroutine
JSRI	Jump to Subroutine Indirect
LD.[BHW]	Load
LDM	Load Multiple Registers
LDQ	Load Register Quadrant
LOOPT	Decrement with C-Bit Update and Branch if Condition True
LRW	Load Relative Word
LSL, LSR	Logical Shift Left and Right
LSLC, LSRC	Logical Shift Left and Right, Update C Bit
LSLI, LSRI	Logical Shift Left and Right by Immediate

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Table 6-1. M•CORE Instruction Set (Sheet 3 of 3)

Mnemonic	Description
MFCR MOV MOVI MOVF MOVT MTCR MULT MVC MVCV	Move from Control Register Move Move Immediate Move on Condition False Move on Condition True Move to Control Register Multiply Move C Bit to Register Move Inverted C Bit to Register
NOT	Logical Complement
OR	Logical Inclusive-OR
ROTLI RSUB RSUBI RTE RFI	Rotate Left by Immediate Reverse Subtract Reverse Subtract Immediate Return from Exception Return from Interrupt
SEXTB SEXTH ST.[BHW] STM STQ STOP SUBC SUBU SUBI SYNC	Sign-Extend Byte Sign-Extend Half-Word Store Store Multiple Registers Store Register Quadrant Stop Subtract with C Bit Subtract Subtract Immediate Synchronize
TRAP TST TSTNBZ	Trap Test Operands Test for No Byte Equal Zero
WAIT	Wait
XOR XSR XTRB0 XTRB1 XTRB2 XTRB3	Exclusive OR Extended Shift Right Extract Byte 0 Extract Byte 1 Extract Byte 2 Extract Byte 3
ZEXTB ZEXTH	Zero-Extend Byte Zero-Extend Half-Word

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Section 7. Interrupt Controller Module

7.1 Contents

7.2 Introduction 154
7.3 Features 154
7.4 Low-Power Mode Operation 154
7.5 Block Diagram 155
7.6 External Signals 155
7.7 Memory Map and Registers 155
7.7.1 Memory Map 156
7.7.2 Registers 157
7.7.2.1 Interrupt Control Register 157
7.7.2.2 Interrupt Status Register 159
7.7.2.3 Interrupt Force Registers 160
7.7.2.4 Interrupt Pending Register 162
7.7.2.5 Normal Interrupt Enable Register 163
7.7.2.6 Normal Interrupt Pending Register 164
7.7.2.7 Fast Interrupt Enable Register 165
7.7.2.8 Fast Interrupt Pending Register 166
7.7.2.9 Priority Level Select Registers 167
7.8 Functional Description 167
7.8.1 Interrupt Sources and Prioritization 168
7.8.2 Fast and Normal Interrupt Requests 168
7.8.3 Autovectored and Vectored Interrupt Requests 169
7.8.4 Interrupt Configuration 171
7.8.4.1 M•CORE Processor Configuration 171
7.8.4.2 Interrupt Controller Configuration 171
7.8.4.3 Interrupt Source Configuration 172
7.8.5 Interrupts 172

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7.2 Introduction

The interrupt controller collects requests from multiple interrupt sources and provides an interface to the processor core interrupt logic.

7.3 Features

Features of the interrupt controller module include:

- Up to 40 interrupt sources
- 32 unique programmable priority levels for each interrupt source
- Independent enable/disable of pending interrupts based on priority level
- Select normal or fast interrupt request for each priority level
- Fast interrupt requests always have priority over normal interrupts
- Ability to mask interrupts at and below a defined priority level
- Ability to select between autovectored or vectored interrupt requests
- Vectored interrupts generated based on priority level
- Ability to generate a separate vector number for normal and fast interrupts
- Ability for software to self-schedule interrupts
- Software visibility of pending interrupts and interrupt signals to core
- Asynchronous operation to support wakeup from low-power modes

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7.4 Low-Power Mode Operation

The interrupt controller is not affected by any low-power modes. All logic between the input sources and generating the raw interrupt to the M•CORE processor is combinational. This allows the M•CORE processor to wake up during low-power stop mode when all system clocks are stopped.

7.5 Block Diagram

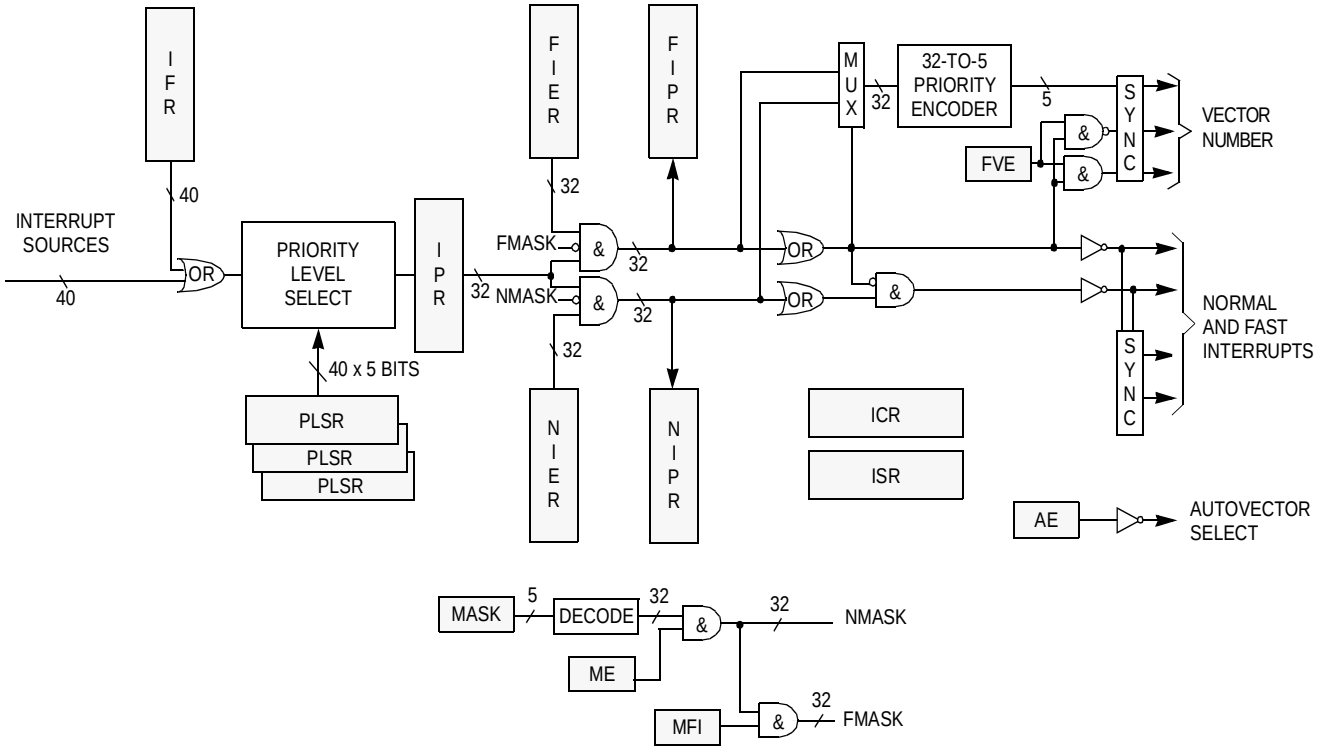

Figure 7-1. Interrupt Controller Block Diagram

7.6 External Signals

No interrupt controller signals connect off-chip.

7.7 Memory Map and Registers

This subsection describes the memory map (see **Table 7-1**) and registers.

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7.7.1 Memory Map

Table 7-1. Interrupt Controller Module Memory Map

Address	Bits 31–24	Bits 23–16	Bits 15–8	Bits 7–0	Access[1]
0x00c5_0000	Interrupt control register (ICR)		Interrupt status register (ISR)		S/U
0x00c5_0004	Interrupt force register high (IFRH)				S/U
0x00c5_0008	IInterrupt force register low (IFRL)				S/U
0x00c5_000c	Interrupt pending register (IPR)				S/U
0x00c5_0010	Normal interrupt enable register (NIER)				S/U
0x00c5_0014	Normal interrupt pending register (NIPR)				S/U
0x00c5_0018	Fast interrupt enable register (FIER)				S/U
0x00c5_001c	Fast interrupt pending register (FIPR)				S/U
0x00c5_0020 through 0x00c5_003c	Unimplemented[2]				—
Priority level select registers (PLSR0–PLSR39)					
0x00c5_0040	PLSR0	PLSR1	PLSR2	PLSR3	S
0x00c5_0044	PLSR4	PLSR5	PLSR6	PLSR7	S
0x00c5_0048	PLSR8	PLSR9	PLSR10	PLSR11	S
0x00c5_004c	PLSR12	PLSR13	PLSR14	PLSR15	S
0x00c5_0050	PLSR16	PLSR17	PLSR18	PLSR19	S
0x00c5_0054	PLSR20	PLSR21	PLSR22	PLSR23	S
0x00c5_0058	PLSR24	PLSR25	PLSR26	PLSR27	S
0x00c5_005c	PLSR28	PLSR29	PLSR30	PLSR31	S
0x00c5_0060	PLSR32	PLSR33	PLSR34	PLSR35	S
0x00c5_0064	PLSR36	PLSR37	PLSR38	PLSR39	S
0x00c5_0068 through 0x00c5_007c	Unimplemented[2]				—

1. S = CPU supervisor mode access only. S/U = CPU supervisor or user mode access. User mode accesses to supervisor only addresses have no effect and result in a cycle termination transfer error.
2. Accesses to unimplemented address locations have no effect and result in a cycle termination transfer error.

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7.7.2 Registers

This subsection contains a description of the interrupt controller module registers.

7.7.2.1 Interrupt Control Register

The 16-bit interrupt control register (ICR) selects whether interrupt requests are autovectored or vectored, and if vectored, whether fast interrupts generate a different vector number than normal interrupts. This register also controls the masking functions.

Address: 0x00c5_0000 and 0x00c5_0001

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	AE	FVE	ME	MFI	0	0	0	0
Write:								
Reset:	1	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	MASK4	MASK3	MASK2	MASK1	MASK0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 7-2. Interrupt Control Register (ICR)

AE — Autovector Enable Bit

The read/write AE bit enables autovectored interrupt requests. Reset sets AE.

1 = Autovectored interrupt requests
0 = Vectored interrupt requests

FVE — Fast Vector Enable Bit

The read/write FVE bit enables fast vectored interrupt requests to have vector numbers separate from normal vectored interrupt requests. Reset clears FVE.

1 = Unique vector numbers for fast vectored interrupt requests
0 = Same vector number for fast and normal vectored interrupt requests

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ME — Mask Enable Bit

The read/write ME bit enables interrupt masking. Reset clears ME.

1 = Interrupt masking enabled
0 = Interrupt masking disabled

MFI — Mask Fast Interrupts Bit

The read/write MFI bit enables masking of fast interrupt requests. Reset clears MFI.

1 = Fast interrupt requests masked by MASK value. All normal interrupt requests are masked.
0 = Fast interrupt requests are not masked regardless of the MASK value. The MASK only applies to normal interrupts. Reset clears MFI.

MASK[4:0] — Interrupt Mask Field

The read/write MASK[4:0] field determines which interrupt priority levels are masked. When the ME bit is set, all pending interrupt requests at priority levels at and below the current MASK value are masked. To mask all normal interrupts without masking any fast interrupts, set the MASK value to 31 with the MFI bit cleared. See **Table 7-2**. Reset clears MASK[4:0].

Table 7-2. MASK Encoding

MASK[4:0]		Masked Priority Levels
Decimal	Binary	
0	00000	0
1	00001	1–0
2	00010	2–0
3	00011	3–0
• • •	• • •	• • •
31	11111	31–0

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7.7.2.2 Interrupt Status Register

The 16-bit, read-only interrupt status register (ISR) reflects the state of the interrupt controller outputs to the M•CORE processor. Writes to this register have no effect and are terminated normally.

Address: 0x00c5_0002 and 0x00c5_0003

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	0	0	0	0	INT	FINT
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	VEC6	VEC5	VEC4	VEC3	VEC2	VEC1	VEC0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 7-3. Interrupt Status Register (ISR)

INT — Normal Interrupt Request Flag

The read-only INT flag indicates whether the normal interrupt request signal to the M•CORE processor is asserted or negated. Reset clears INT.

1 = Normal interrupt request asserted
0 = Normal interrupt request negated

FINT — Fast Interrupt Request Flag

The read-only FINT flag indicates whether the fast interrupt request signal to the M•CORE processor is asserted or negated. Reset clears FINT.

1 = Fast interrupt request asserted
0 = Fast interrupt request negated

VEC[6:0] — Interrupt Vector Number Field

The read-only VEC[6:0] field reflects the state of the 7-bit interrupt vector number. Reset clears VEC[6:0].

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7.7.2.3 Interrupt Force Registers

The two 32-bit read/write interrupt force registers (IFRH and IFRL) individually force interrupt source requests.

Address: 0x00c5_0004 through 0x00c5_0007

	Bit 31	30	29	28	27	26	25	Bit 24
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 23	22	21	20	19	18	17	Bit 16
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IF39	IF38	IF37	IF36	IF35	IF34	IF33	IF32
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 7-4. Interrupt Force Register High (IFRH)

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Address: 0x00c5_0008 through 0x00c5_000b

	Bit 31	30	29	28	27	26	25	Bit 24
Read: Write:	IF31	IF30	IF29	IF28	IF27	IF26	IF25	IF24
Reset:	0	0	0	0	0	0	0	0

	Bit 23	22	21	20	19	18	17	Bit 16
Read: Write:	IF23	IF22	IF21	IF20	IF19	IF18	IF17	IF16
Reset:	0	0	0	0	0	0	0	0

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	IF15	IF14	IF13	IF12	IF11	IF10	IF9	IF8
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IF7	IF6	IF5	IF4	IF3	IF2	IF1	IF0
Reset:	0	0	0	0	0	0	0	0

Figure 7-5. Interrupt Force Register Low (IFRL)

IF[39:0] — Interrupt Force Field

This read/write field forces interrupt requests at the corresponding source numbers. IFRH and IFRL allow software generation of interrupt requests for functional or debug purposes. Writing 0 to an IF bit negates the interrupt request. Reset clears the IF[39:0] field.

1 = Force interrupt request
0 = Interrupt source not forced

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7.7.2.4 Interrupt Pending Register

The 32-bit, read-only interrupt pending register (IPR) reflects any currently pending interrupts which are assigned to each priority level. Writes to this register have no effect and are terminated normally.

Address: 0x00c5_000c through 0x00c5_000f

	Bit 31	30	29	28	27	26	25	Bit 24
Read:	IP31	IP30	IP29	IP28	IP27	IP26	IP25	IP24
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 23	22	21	20	19	18	17	Bit 16
Read:	IP23	IP22	IP21	IP20	IP19	IP18	IP17	IP16
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	IP15	IP14	IP13	IP12	IP11	IP10	IP9	IP8
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 7-6. Interrupt Pending Register (IPR)

IP[31:0] — Interrupt Pending Field

A read-only IPx bit is set when at least one interrupt request is asserted at priority level x. Reset clears IP[31:0].

1 = At least one interrupt request asserted at priority level x
0 = All interrupt requests at level x negated

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7.7.2.5 Normal Interrupt Enable Register

The read/write, 32-bit normal interrupt enable register (NIER) individually enables any current pending interrupts which are assigned to each priority level as a normal interrupt source. Enabling an interrupt source which has an asserted request causes that request to become pending, and a request to the M•CORE processor is asserted if not already outstanding.

Address: 0x00c5_0010 through 0x00c5_0013

	Bit 31	30	29	28	27	26	25	Bit 24
Read: Write:	NIE31	NIE30	NIE29	NIE28	NIE27	NIE26	NIE25	NIE24
Reset:	0	0	0	0	0	0	0	0

	Bit 23	22	21	20	19	18	17	Bit 16
Read: Write:	NIE23	NIE22	NIE21	NIE20	NIE19	NIE18	NIE17	NIE16
Reset:	0	0	0	0	0	0	0	0

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	NIE15	NIE14	NIE13	NIE12	NIE11	NIE10	NIE9	NIE8
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	NIE7	NIE6	NIE5	NIE4	NIE3	NIE2	NIE1	NIE0
Reset:	0	0	0	0	0	0	0	0

Figure 7-7. Normal Interrupt Enable Register (NIER)

NIE[31:0] — Normal Interrupt Enable Field

The read/write NIE[31:0] field enables interrupt requests from sources at the corresponding priority level as normal interrupt requests. Reset clears NIE[31:0].

1 = Normal interrupt request enabled
0 = Normal interrupt request disabled

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7.7.2.6 Normal Interrupt Pending Register

The read-only, 32-bit normal interrupt pending register (NIPR) reflects any currently pending normal interrupts which are assigned to each priority level. Writes to this register have no effect and are terminated normally.

Address: 0x00c5_0014 through 0x00c5_0017

	Bit 31	30	29	28	27	26	25	Bit 24
Read:	NIP31	NIP30	NIP29	NIP28	NIP27	NIP26	NIP25	NIP24
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 23	22	21	20	19	18	17	Bit 16
Read:	NIP23	NIP22	NIP21	NIP20	NIP19	NIP18	NIP17	NIP16
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	NIP15	NIP14	NIP13	NIP12	NIP11	NIP10	NIP9	NIP8
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	NIP7	NIP6	NIP5	NIP4	NIP3	NIP2	NIP1	NIP0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 7-8. Normal Interrupt Pending Register (NIPR)

NIP[31:0] — Normal Interrupt Pending Field

A read-only NIPx bit is set when at least one normal interrupt request is asserted at priority level x. Reset clears NIP[31:0].

1 = At least one normal interrupt request asserted at priority level x
0 = All normal interrupt requests at priority level x negated

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7.7.2.7 Fast Interrupt Enable Register

The read/write, 32-bit fast interrupt enable register (FIER) enables any current pending interrupts which are assigned at each priority level as a fast interrupt source. Enabling an interrupt source which has an asserted request causes that interrupt to become pending, and a request to the M•CORE processor is asserted if not already outstanding.

Address: 0x00c5_0018 through 0x00c5_001b

	Bit 31	30	29	28	27	26	25	Bit 24
Read: Write:	FIE31	FIE30	FIE29	FIE28	FIE27	FIE26	FIE25	FIE24
Reset:	0	0	0	0	0	0	0	0
	Bit 23	22	21	20	19	18	17	Bit 16
Read: Write:	FIE23	FIE22	FIE21	FIE20	FIE19	FIE18	FIE17	FIE16
Reset:	0	0	0	0	0	0	0	0
	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	FIE15	FIE14	FIE13	FIE12	FIE11	FIE10	FIE9	FIE8
Reset:	0	0	0	0	0	0	0	0
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	FIE7	FIE6	FIE5	FIE4	FIE3	FIE2	FIE1	FIE0
Reset:	0	0	0	0	0	0	0	0

Figure 7-9. Fast Interrupt Enable Register (FIER)

FIE[31:0] — Fast Interrupt Enable Field

The read/write FIE[31:0] field enables interrupt requests from sources at the corresponding priority level as fast interrupts. Reset clears FIE[31:0].

1 = Fast interrupt enabled
0 = Fast interrupt disabled

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7.7.2.8 Fast Interrupt Pending Register

The read-only, 32-bit fast interrupt pending register (FIPR) reflects any currently pending fast interrupts which are assigned to each priority level. Writes to this register have no effect and are terminated normally.

Address: 0x00c5_001c through 0x00c5_001f

	Bit 31	30	29	28	27	26	25	Bit 24
Read:	FIP31	FIP30	FIP29	FIP28	FIP27	FIP26	FIP25	FIP24
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 23	22	21	20	19	18	17	Bit 16
Read:	FIP23	FIP22	FIP21	FIP20	FIP19	FIP18	FIP17	FIP16
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	FIP15	FIP14	FIP13	FIP12	FIP11	FIP10	FIP9	FIP8
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	FIP7	FIP6	FIP5	FIP4	FIP3	FIP2	FIP1	FIP0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 7-10. Fast Interrupt Pending Register (FIPR)

FIP[31:0] — Fast Interrupt Pending Field

A read-only FIP[x] bit is set when at least one interrupt request at priority level x is pending and enabled as a fast interrupt. Reset clears FIP[31:0].

1 = At least one fast interrupt request asserted at priority level x
0 = Any fast interrupt requests at priority level x negated

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7.7.2.9 Priority Level Select Registers

There are 40 read/write, 8-bit priority level select registers PLSR0–PLSR39, one for every interrupt source. The PLSRx register assigns a priority level to interrupt source x.

Address: 0x00c5_0040 through 0x00c5_0067

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	PLS4	PLS3	PLS2	PLS1	PLS0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 7-11. Priority Level Select Registers (PLSR0–PLSR39)

PLS[4:0] — Priority Level Select Field

The PLS[4:0] field assigns a priority level from 0 to 31 to the corresponding interrupt source. Reset clears PLS[4:0].

Table 7-3. Priority Select Encoding

PLS[4:0]	Priority Level	Vector Number
00000	0 (lowest)	00000
00001–11110	1–30	00001–11110
11111	31 (highest)	11111

7.8 Functional Description

The interrupt controller collects interrupt requests from multiple interrupt sources and provides an interface to the processor core interrupt logic. Interrupt controller functions include:

- Interrupt source prioritization
- Fast and normal interrupt requests
- Autovectored and vectored interrupt requests
- Interrupt configuration

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7.8.1 Interrupt Sources and Prioritization

Each interrupt source in the system sends a unique signal to the interrupt controller. Up to 40 interrupt sources are supported. Each interrupt source can be programmed to one of 32 priority levels using PLSR in the interrupt controller. The highest priority level is 31 and lowest priority level is 0. By default, each interrupt source is assigned to the priority level 0. Each interrupt source is associated with a 5-bit priority level select value that selects one of 32 priority levels. The interrupt controller uses the priority levels as the basis for the generation of all interrupt signals to the M•CORE processor.

Interrupt requests may be forced by software by writing to IFRH and IFRL. Each bit of IFRH and IFRL is logically ORed with the corresponding interrupt source signal before the priority level select logic. To negate the forced interrupt request, the interrupt handler can clear the appropriate IFR bit. IPR reflects the state of each priority level.

7.8.2 Fast and Normal Interrupt Requests

FIER allows individual enabling or masking of pending fast interrupt requests. FIER is logically ANDed with IPR, and the result is stored in FIPR. FIPR bits are bit-wise ORed together and inverted to form the fast interrupt signal routed to the M•CORE processor. The FIPR allows software to quickly determine the highest priority pending fast interrupt. The output of FIPR also feeds into a 32-to-5 priority encoder to generate the vector number to present to the M•CORE processor if vectored interrupts are required.

NIER allows individual enabling or masking of pending normal interrupt requests. NIER is logically ANDed with IPR, and the result is stored in NIPR. NIPR bits are bit-wise ORed together and inverted to form the normal interrupt signal routed to the M•CORE processor. The normal interrupt signal is only asserted if the fast interrupt signal is negated. The NIPR allows software to quickly determine the highest priority pending normal interrupt. The output of NIPR also feeds into a 32-to-5 priority encoder to generate the vector number to present to the M•CORE processor if vectored interrupts are required. If the fast interrupt signal is asserted, then the vector number is determined by the highest priority fast interrupt.

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If an interrupt is pending at a given priority level and both the corresponding FIER and NIER bits are set, then both the corresponding FIPR and NIPR bits are set, assuming these bits are not masked.

Fast interrupt requests always have priority over normal interrupt requests, even if the normal interrupt request is at a higher priority level than the highest fast interrupt request.

If the fast interrupt signal is asserted when the normal interrupt signal is already asserted, then the normal interrupt signal is negated.

IPR, NIPR, and FIPR are read-only. To clear a pending interrupt, the interrupt must be cleared at the source using a special clearing sequence defined by each source. All interrupt sources to the interrupt controller are to be held until recognized and cleared by the interrupt service routine. The interrupt controller does not have any edge-detect logic. Edge-triggered interrupt sources are handled at the source module.

In ICR, the MASK[4:0] bits can mask interrupt sources at and below a selected priority level. The MFI bit determines whether the mask applies only to normal interrupts or to fast interrupts with all normal interrupts being masked. The ME bit enables interrupt masking.

ISR reflects the current vector number and the states of the signals to the M•CORE processor.

The vector number and fast/normal interrupt sources are synchronized before being sent to the M•CORE processor. Thus, the interrupt controller adds one clock of latency to the interrupt sequence. The fast and normal interrupt raw sources are not synchronized to allow these signals to be used to wake up the M•CORE processor during stop mode when all system clocks are stopped.

7.8.3 Autovectored and Vectored Interrupt Requests

The AE bit in ICR enables autovectored interrupt requests to the M•CORE processor. AE is set by default, and all interrupt requests are autovectored. An interrupt handler may read FIPR or NIPR to determine the priority of the interrupt source. If multiple interrupt sources share the same priority level, then it is up to the interrupt service routine to determine the correct source of the interrupt.

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If the AE bit is 0, then each interrupt request is presented with a vector number. The low five bits of the vector number (4–0) are determined based on the highest pending priority, with active fast interrupts having priority over active normal interrupts. The remaining two bits (vector bits 5 and 6) are determined based on whether the interrupt request is a fast interrupt and the setting of the FVE bit. If FVE is set, then a fast interrupt request has a vector number different from that of a normal interrupt request as shown in **Table 7-4**.

Table 7-4. Fast Interrupt Vector Number

Fast Interrupt	FVE	Interrupt Vector Bits 6:5
No	X	01
X	0	01
Yes	1	10

If FVE is 0, both normal and fast interrupts requests assigned to priority levels 0–31 are mapped to vector numbers 32–63 in the vector table. If FVE is 1, normal interrupt requests assigned to priority levels 0–31 are mapped to vector numbers 32–63 in the vector table.

If FVE is 1, then fast interrupt requests assigned to priority levels 0–31 are mapped to vector numbers 64–95 in the vector table. See **Table 7-5**.

Table 7-5. Vector Table Mapping

Vector Number	Usage	Interrupt Vector Bits 6:5
0–31	Fixed exceptions (including autovectors)	00
32–63	Vectored interrupts 32 = lowest priority 63 = highest priority	01
64–95	Vectored interrupts 64 = lowest priority 95 = highest priority	10
96–127	Vectored interrupts (not used)	11

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7.8.4 Interrupt Configuration

After reset, all interrupts are disabled by default. To properly configure the system to handle interrupt requests, configuration must be performed at three levels:

- M•CORE processor
- Interrupt controller
- Local interrupt sources

Configure the M•CORE first, the interrupt controller second, and the local interrupt sources last.

7.8.4.1 M•CORE Processor Configuration

For fast interrupts, set the FIE[x] bit in FIER in the M•CORE processor. For normal interrupts, set the NIE[x] bit. Both FIE and NIE are cleared at reset. To allow long latency, multicycle instructions to be interrupted before completion, set the IC bit.

VBR in the M•CORE processor defines the base address of the exception vector table. If autovectors are to be used, then initialize the INT and FINT autovectors (vector numbers 10 and 11, respectively). If vectored interrupts are to be used, then initialize the vectored interrupts (vector numbers 32–63 and/or 64–95). Whether 32 or 64 vectors are required depends on whether the fast interrupts share vectors with the normal interrupt sources based on the FVE bit in the interrupt controller ICR.

For each vector number, create an interrupt service routine to service the interrupt, clear the local interrupt flag, and return from the interrupt routine.

7.8.4.2 Interrupt Controller Configuration

By default, each interrupt source to the interrupt controller is assigned a priority level of 0 and disabled. Each interrupt source can be programmed to one of 32 priority levels and enabled as either a fast or normal interrupt source. Also, the FVE and AE bits in ICR can be programmed to select autovectored/vectored interrupts and also determine if the fast interrupt vector number is to be separate from the normal interrupt vector.

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7.8.4.3 Interrupt Source Configuration

Each module that is capable of generating an interrupt request has an interrupt request enable/disable bit. To allow the interrupt source to be asserted, set the local interrupt enable bit.

Once an interrupt request is asserted, the module keeps the source asserted until the interrupt service routine performs a special sequence to clear the interrupt flag. Clearing the flag negates the interrupt request.

7.8.5 Interrupts

The interrupt controller assigns a number to each interrupt source, as **Table 7-6** shows.

Table 7-6. Interrupt Source Assignment

Source	Module	Flag	Source Description	Flag Clearing Mechanism
0	ADC	PF1	Queue 1 conversion pause	Write PF1 = 0 after reading PF1 = 1
1		CF1	Queue 1 conversion complete	Write CF1 = 0 after reading CF1 = 1
2		PF2	Queue 2 conversion pause	Write PF2 = 0 after reading PF2 = 1
3		CF2	Queue 2 conversion complete	Write CF2 = 0 after reading CF2 = 1
4	SPI	MODF	Mode fault	Write to SPICR1 after reading MODF = 1
5		SPIF	Transfer complete	Access SPIDR after reading SPIF = 1
6	SCI1	TDRE	Transmit data register empty	Write SCIDRL after reading TDRE = 1
7		TC	Transmit complete	Write SCIDRL after reading TC = 1
8		RDRF	Receive data register full	Read SCIDRL after reading RDRF = 1
9		OR	Receiver overrun	Read SCIDRL after reading OR = 1
10		IDLE	Receiver line idle	Read SCIDRL after reading IDLE = 1
11	SCI2	TDRE	Transmit data register empty	Write SCIDRL after reading TDRE = 1
12		TC	Transmit complete	Write SCIDRL after reading TC = 1
13		RDRF	Receive data register full	Read SCIDRL after reading RDRF = 1
14		OR	Receiver overrun	Read SCIDRL after reading OR = 1
15		IDLE	Receiver line idle	Read SCIDRL after reading IDLE = 1

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Table 7-6. Interrupt Source Assignment (Continued)

Source	Module	Flag	Source Description	Flag Clearing Mechanism
16	TIM1	C0F	Timer channel 0	Write C0F = 1 or access IC/OC if TFFCA = 1
17		C1F	Timer channel 1	Write 1 to C1F or access IC/OC if TFFCA = 1
18		C2F	Timer channel 2	Write 1 to C2F or access IC/OC if TFFCA = 1
19		C3F	Timer channel 3	Write 1 to C3F or access IC/OC if TFFCA = 1
20		TOF	Timer overflow	Write TOF = 1 or access TIMCNTH/L if TFFCA = 1
21		PAIF	Pulse accumulator input	Write PAIF = 1 or access PAC if TFFCA = 1
22		PAOVF	Pulse accumulator overflow	Write PAOVF = 1 or access PAC if TFFCA = 1
23	TIM2	C0F	Timer channel 0	Write C0F = 1 or access IC/OC if TFFCA = 1
24		C1F	Timer channel 1	Write C1F = 1 or access IC/OC if TFFCA = 1
25		C2F	Timer channel 2	Write C2F = 1 or access IC/OC if TFFCA = 1
26		C3F	Timer channel 3	Write C3F = 1 or access IC/OC if TFFCA = 1
27		TOF	Timer overflow	Write TOF = 1 or access TIMCNTH/L if TFFCA = 1
28		PAIF	Pulse accumulator input	Write PAIF = 1 or access PAC if TFFCA = 1
29		PAOVF	Pulse accumulator overflow	Write PAOVF = 1 or access PAC if TFFCA = 1
30	PIT1	PIF	PIT interrupt flag	Write PIF = 1 or write PMR
31	PIT2	PIF	PIT interrupt flag	Write PIF = 1 or write PMR
32	EPORT	EPF0	Edge port flag 0	Write EPF0 = 1
33		EPF1	Edge port flag 1	Write EPF1 = 1
34		EPF2	Edge port flag 2	Write EPF2 = 1
35		EPF3	Edge port flag 3	Write EPF3 = 1
36		EPF4	Edge port flag 4	Write EPF4 = 1
37		EPF5	Edge port flag 5	Write EPF5 = 1
38		EPF6	Edge port flag 6	Write EPF6 = 1
39		EPF7	Edge port flag 7	Write EPF7 = 1

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Interrupt Controller Module

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Section 8. Static Random-Access Memory (SRAM)

8.1 Contents

8.2 Introduction 175
8.3 Modes of Operation 175
8.4 Low-Power Modes 176
8.5 Standby Power Supply Pin (V_{STBY}) 176
8.6 Standby Operation 176
8.7 Reset Operation 177
8.8 Interrupts. 177

8.2 Introduction

Features of the static random-access memory (SRAM) include:

- On-chip, 8-Kbyte static random-access memory (SRAM)
- Fixed address space
- Byte, half-word (16-bit), or word (32-bit) read/write accesses
- One clock per access (including bytes, half-words, and words)
- Supervisor or user mode access
- Standby power supply switch to support an external power supply

8.3 Modes of Operation

Access to the SRAM is not restricted in any way. The array can be accessed in all supervisor and user modes.

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8.4 Low-Power Modes

In wait, doze, and stop modes, clocks to the SRAM are disabled. No recovery time is required when exiting any low-power mode.

8.5 Standby Power Supply Pin (V_{STBY})

The standby power supply pin (V_{STBY}) provides standby voltage to the RAM array if V_{DD} is lost. V_{STBY} is isolated from all other V_{DD} nodes.

8.6 Standby Operation

When the chip is powered down, the contents of the SRAM array are maintained by the standby power supply, V_{STBY}. If the standby voltage falls below the minimum required voltage, the SRAM contents may be corrupted. The SRAM automatically switches to standby operation with no loss of data when the voltage on V_{DD} is below the voltage on V_{STBY}. In standby mode, the SRAM does not respond to any bus cycles. Unexpected operation may occur if the central processor unit (CPU) requests data from the SRAM in standby mode. If standby operation is not needed, then the V_{STBY} pin should be connected to V_{DD}.

The current on V_{STBY} may exceed its specified maximum value at some time during the transition time during which V_{DD} is at or below the voltage switch threshold to a threshold above V_{SS}. If the standby power supply cannot provide enough current to maintain V_{STBY} above the required minimum value, then a capacitor must be provided from V_{STBY} to V_{SS}. The value of the capacitor, C, can be calculated as:

$$C = I \times \frac{t}{V}$$

where:

I is the difference between the transition current requirement and the maximum power supply current,

t is the duration of the V_{DD} transition near the voltage switch threshold, and

V is the difference between the minimum available supply voltage and the required minimum V_{STBY} voltage.

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8.7 Reset Operation

The SRAM contents are undefined immediately following a power-on reset. SRAM contents are unaffected by system reset.

If a synchronous reset occurs during a read or write access, then the access completes normally and any pipelined access in progress is stopped without corruption of the SRAM contents.

8.8 Interrupts

The SRAM module does not generate interrupt requests.

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Static Random-Access Memory (SRAM)

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Section 9. Non-Volatile Memory FLASH (CMFR)

9.1 Contents

9.2 Introduction 180
9.3 Features 181
9.4 Modes of Operation 182
9.4.1 Stop Mode 182
9.4.2 Disabled Mode 182
9.5 Block Diagram 183
9.6 Glossary of Terms 185
9.7 Registers and Memory Map 186
9.7.1 Control Registers 187
9.7.1.1 CMFR Module Configuration Register 188
9.7.1.2 CMFR Module Test Register 193
9.7.1.3 CMFR High-Voltage Control Register 196
9.7.2 Array Addressing 203
9.7.2.1 Read Page Buffers 203
9.7.2.2 Program Page Buffers 204
9.8 Functional Description 205
9.8.1 Master Reset 205
9.8.2 Register Read and Write Operation 205
9.8.3 Array Read Operation 205
9.8.4 Programming 206
9.8.4.1 Program Sequence 207
9.8.4.2 Program Margin Reads 211
9.8.4.3 Programming Shadow Information 212
9.8.4.4 Program Pulse-Width and Amplitude Modulation 213
9.8.4.5 Overprogramming 213

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9.8.5 Erasing 214
9.8.5.1 Erase Sequence 215
9.8.5.2 Erase Margin Reads 218
9.8.5.3 Erasing Shadow Information Words. 219
9.8.6 Erase Pulse Amplitude and Width Modulation 219
9.8.7 Emulation Operation. 220
9.9 Master Reset 220
9.10 Interrupts. 220

9.2 Introduction

This section describes the operation of the embedded FLASH memory. The FLASH memory can be read, programmed, and erased from a single external programming voltage supply, V_{PP}. The program and erase operations are enabled through the use of an internal charge pump.

The CDR MoneT FLASH uses the Motorola one-transistor bitcell (MoneT). The 128-Kbyte CMFR array is divided into 16-Kbyte (16,384 bytes) array blocks. The CMFR array size is created by using eight array blocks.

The primary function of the CMFR is to serve as electrically programmable and erasable NVM to store program instructions and/or data. It is a class of nonvolatile solid state silicon memory device consisting of an array of isolated elements, a means for selectively adding and removing charge to the elements electrically and a means of selectively sensing the stored charge in the elements. When power is removed from the device, the stored charge of the isolated elements are retained.

The CMFR is arranged into two major sections as shown in **Figure 9-1**. The first section is the MoneT array used to store system program and data. The second section is the bus interface unit (BIU) that controls access and operation of the CMFR array.

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9.3 Features

Features of the CMFR module include:

- MoneT FLASH bitcell
- 128-Kbyte array size using 16-Kbyte blocks
- Array block restriction control:
  - Array block erasing
  - Array protection for program and erase operations
  - Supervisor space and supervisor/unrestricted space selection
  - Data space and instruction/data spaces selection.
- 32-bit word length
- Page mode read:
  - Retains two separate pages
  - Read page size of 32 bytes (8 words)
  - Off-page read access time of two clocks
  - On-page read access time of one clock
- Programming:
  - Program up to 512 bytes at a time
  - Simultaneously program up to eight 64-byte pages located at the same block offset address
- External V_{PP} program and erase power supply

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9.4 Modes of Operation

This subsection describes the two modes of operation:

1. Stop mode
2. Disabled mode

9.4.1 Stop Mode

When the FSTOP bit in the CMFR module configuration register (CMFRMCR) register is set, the CMFR enters a low-power operation mode. Write to FSTOP bit is allowed only when SES = 0 in the CMFR high-voltage control register (no high-voltage operations). When the FSTOP bit is set, only CMFRMCR can be accessed, accesses to the array are ignored, and accesses to other registers are terminated with bus errors. To prevent unpredictable behavior it is recommended to change this bit separately. The CMFR requires a recovery time of 16 clocks after exiting stop mode. This means that if a read access to the array is done immediately after writing FSTOP = 0, the access is completed after 16 clocks.

9.4.2 Disabled Mode

When the DIS bit in CMFRMCR is set, the array is disabled and the BIU does not respond to array accesses. Write to DIS bit is allowed only when SES = 0 (no high-voltage operations). Disabling the CMFR does not place the module in the lowest power consumption mode like stop mode, but does place the CMFR in a safe state and prevents the CMFR from conflicting on the internal bus during an external boot. There is no recovery time required when re-enabling the CMFR.

For details of the CMFR module configuration register (CMFRMCR) see **9.7.1.1 CMFR Module Configuration Register** and **9.7.1.3 CMFR High-Voltage Control Register**.

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9.5 Block Diagram

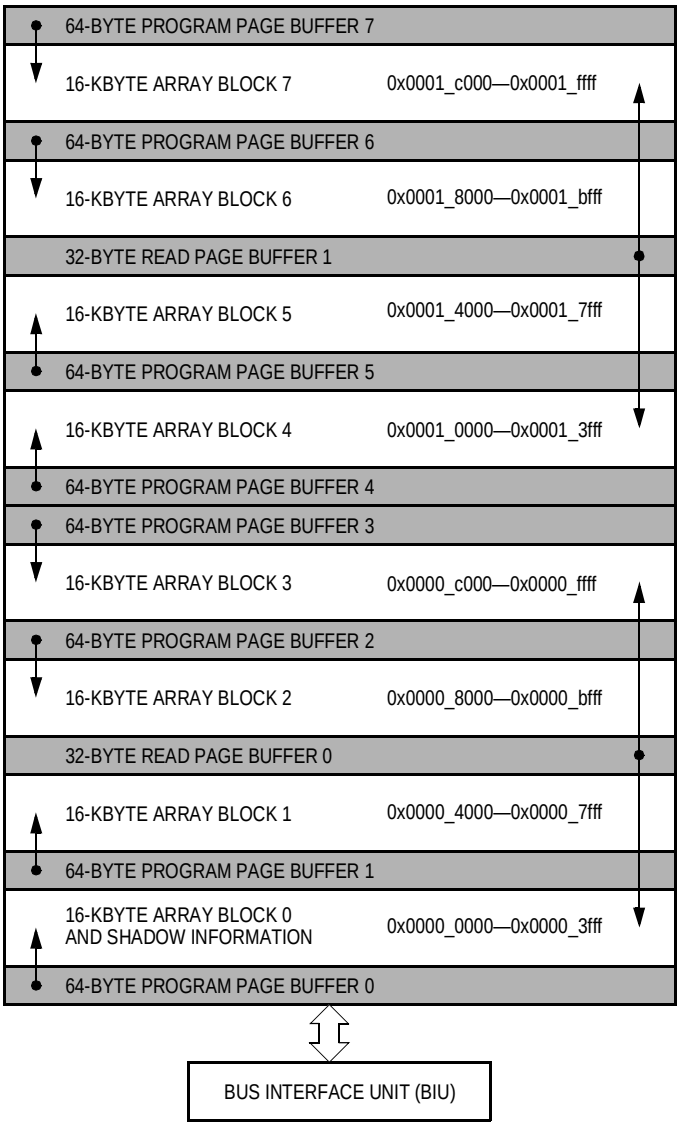

Figure 9-1. CMFR 128-Kbyte Block Diagram

The CMFR is divided into array blocks to allow for independent erase, address attributes restriction, and protection from program and erase for each array block. The size of an array block in the CMFR module is fixed at 16 Kbytes. The total CMFR array is distributed into eight blocks. For a detailed description of the read page buffer operation see **9.7.2.1 Read Page Buffers** and **9.8.3 Array Read Operation**.

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To improve system performance, the BIU accesses information in the array at 32 bytes per access. These 32 bytes are copied in a read page buffer aligned to the low-order addresses. A CMFR array contains two non-overlapping read page buffers. The first read page buffer is associated to the lower array blocks. The second read page buffer is associated to the higher array blocks. Read access time of the data in the current read page buffers is one system clock, while the time to read a new page into a page buffer and access the required information is two system clocks. These accesses are known as an on-page read and an off-page read, respectively. To prevent the BIU from accessing an unnecessary page from the array, the CMFR monitors the address to determine if the required information is in one of the two current read page buffers and the access is valid for the module. This strategy allows the CMFR to have a two-clock read for an off-page access and one-clock for an on-page access. In normal operation write accesses to the CMFR array are not allowed, a write access causes a bus error.

The CMFR requires an external program or erase voltage, V_{PP}, to program or erase the array. Special control logic is included to require a specific series of read and write accesses.

To improve program performance, the CMFR programs up to eight unique 64-byte pages simultaneously in eight separate array blocks. These 64 bytes are aligned to the low-order addresses to form a program page buffer.

Each of the pages being programmed simultaneously are located at the same block offset address. Erasing is performed on one or more of the selected array blocks simultaneously.

An extra row (256 bytes) of the CMFR array is used to provide reset configuration information and is called shadow information. This row may be accessed by setting the SIE bit in the CMFR module configuration register and accessing the CMFR array. The shadow information is in the lowest array block 0 of the CMFR array. Note that the shadow row is erased with block 0.

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9.6 Glossary of Terms

Array block – CMFR array subdivision is a 16-Kbyte contiguous block of information. Each array block can be erased independently.

BIU – Bus interface unit that controls access and operation of the CMFR

CMFR – **C**DR **M**oneT **F**LASH A**R**ray

Erase interlock write – A write to any CMFR array address after initializing the erase sequence

Erase margin read – Special off-page read of the CMFR array in which the CMFR hardware adjusts the reference of the sense amplifier to check for correct erase operation. All CMFR off-page reads between the erase interlock write and clearing the SES bit are erase margin reads.

Initialize program/erase sequence – The write to the high-voltage control register that changes the SES bit from a 0 to a 1

MoneT – The Motorola one-transistor bitcell

Off-page read – Array read operation that requires two clocks and updates a page buffer

On-page read – Array read operation that accesses information in one of the read page buffers and requires one clock.

Overprogrammed – By exceeding the specified programming time and/or voltage, a CMFR bit can be overprogrammed. This causes erased bits in the same column in the same array block to read as programmed.

Programming write – A write to a CMFR array address to transfer information into a program page buffer. The CMFR accepts programming writes after initializing the program sequence until the EHV bit is changed from a 0 to a 1.

Program margin read – Special off-page read of the CMFR array in which the CMFR hardware adjusts the reference of the sense amplifier to check for correct program operation. All CMFR array off-page reads between the first programming write and clearing the SES bit are program margin reads.

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Program page buffer – 64 bytes of information used to program the CMFR. This information is aligned to a 64-byte boundary within the CMFR. The CMFR module has eight program page buffers, one per array block.

Read page buffer – 32-byte block of information that is read from the CMFR array. This information is aligned to a 32-byte boundary within the CMFR. The CMFR module has two read page buffers.

Shadow information – An extra row (256 bytes) of the CMFR array used to provide Motorola internal use data and also possibly user defined information. This row may be accessed by setting the SIE bit in the CMFR module configuration register and accessing the CMFR array. The shadow information is the lowest array block 0 of the CMFR array.

9.7 Registers and Memory Map

The CMFR module consists of two addressed sections. The first is the 32-byte control registers used to configure, program, erase, and test the array while, the second is the array. See **Figure 9-2**.

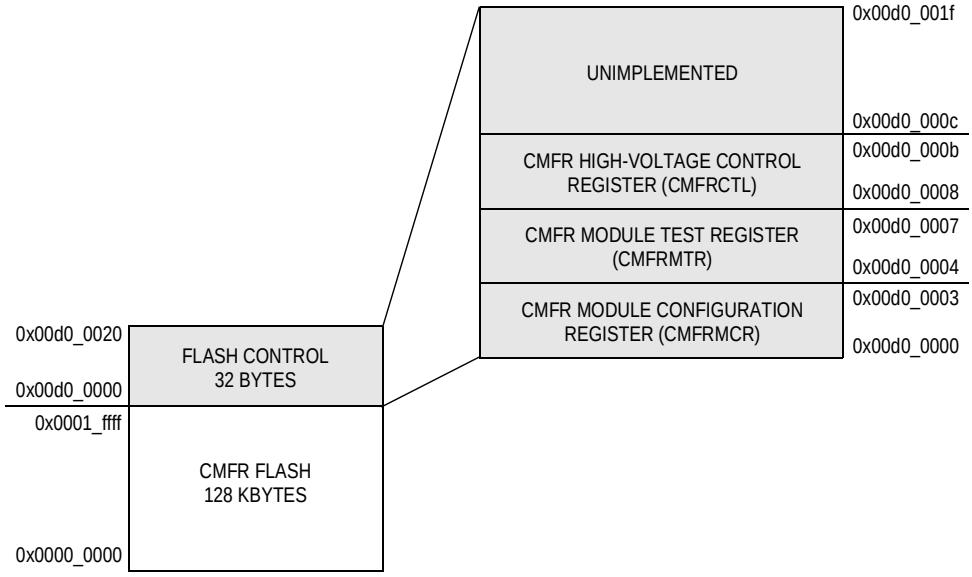

Figure 9-2. CMFR Array and Control Register Addressing

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9.7.1 Control Registers

The control registers control CMFR operation. On reset, the registers are loaded with default reset information.

Table 9-1. Non-Volatile Memory FLASH Memory Map

Address	Control Register Located in Supervisor Data Space
0x00d0_0000	Module configuration register (CMFRMCR)
0x00d0_0004	Module test register (CMFRMTR)
0x00d0_0008	High-voltage control register (CMFRCTL)
0x00d0_000c through 0x00d0_001f	Unimplemented

The access time of a CMFR register is one system clock for both read and write accesses. Accesses to unimplemented registers cause the BIU to generate a transfer error exception.

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9.7.1.1 CMFR Module Configuration Register

The CMFR module configuration register (CMFRMCR) controls operation of the CMFR array and BIU.

Address: 0x00d0_0000 through 0x00d0_0003

	Bit 31	30	29	28	27	26	25	Bit 24
Read:	FSTOP	FDBG	0	EME	SIE	LOCKCTL	DIS	RSVD24
Write:								
Reset:	0	0	0	Note 1	0	0	Note 1	0

	Bit 23	22	21	20	19	18	17	Bit 16
Read:	SUPV7	SUPV6	SUPV5	SUPV4	SUPV3	SUPV2	SUPV1	SUPV0
Write:								
Reset:	1	1	1	1	1	1	1	1

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PROTECT7	PROTECT6	PROTECT5	PROTECT4	PROTECT3	PROTECT2	PROTECT1	PROTECT0
Write:								
Reset:	1	1	1	1	1	1	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Notes:
1. Reset state is determined during reset configuration.

Figure 9-3. CMFR Module Configuration Register (CMFRMCR)

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FSTOP — FLASH Stop Enable Bit

The read-always FSTOP bit causes the CMFR to enter a low-power stop mode. Writing has no effect if SES = 1. When FSTOP is set, the BIU continues to operate to allow accesses to CMFRMCR. Accesses to other registers are terminated with bus error. Accesses to the array are ignored. To prevent unpredictable behavior, change the FSTOP bit in a separate write operation.

1 = CMFR in low-power stop mode
0 = CMFR in normal mode

FDBG — FLASH Debug Enable Bit

The read/write FDBG bit determines whether the set-once LOCKCTL bit is writable when the chip is in debug mode. Writing to the FDBG bit must occur before the LOCKCTL bit is writable.

1 = Debug mode enabled
0 = Debug mode disabled

EME — Emulation Enable Bit

The read-always EME bit enables the CMFR to enter emulation mode. EME is writable when the LOCKCTL and DIS bits are set. During emulation mode the CMFR terminates array access cycles, but does not drive data. Array data can be emulated by reading an external memory, and on-page/off-page timing is the same as in non-emulation mode. Note that write accesses to the array space are the same as normal mode.

1 = Emulation mode enabled
0 = Emulation mode disabled

For more information about emulation operation see **9.8.7 Emulation Operation**.

SIE — Shadow Information Enable Bit

The read-always SIE bit selects the shadow information row. SIE is write-protected when the ERASE bit is clear and the SES bit is set. When SIE is set and an array location is read using supervisor data, the shadow information is read from a location determined by the column, 32 byte read page select, and word addresses of the access. Accessing the control block registers accesses the registers and not the shadow information.

1 = Shadow information enabled; normal array access disabled
0 = Shadow information disabled; normal array access enabled

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The address range of the shadow information is the entire address range of the array, but the high order array addresses, are not used to encode the location.

NOTE: *When SIE = 1, only the program page buffer associated with the lowest block can be programmed. The other program page buffers cannot be accessed and do not apply any programming voltages to their array blocks while programming the shadow information. The shadow information is in block 0.*

LOCKCTL — Lock Control Bit

The read-always, set-once LOCKCTL bit controls the write-lock function. Once the LOCKCTL bit is set in normal operation, the write-lock can only be disabled again by a master reset. The LOCKCTL bit is writable if the device is in debug mode.

1 = Write-locked registers protected
0 = Write-lock disabled

Setting the LOCKCTL bit locks the SUPV[7:0], DATA[7:0] and PROTECT[7:0] bits. Writing to these bits has no effect; the cycle ends normally and the bits do not change.

NOTE: *If LOCKCTL is set before PROTECT[7:0] is cleared, the device must use debug mode to program or erase the CMFR.*

The default reset state of LOCKCTL is 0. It can be set once after master reset to allow protection of the write-locked register bits after initialization.

If the LOCKCTL bit and write-locked register bits are written simultaneously, the new value does not affect the current cycle.

DIS — Disable Bit

The read-always DIS bit disables array information. Writing to DIS has no effect if the SES bit is set. When DIS is set, the array is disabled and the CMFR BIU does not respond to array accesses.

The reset value is defined during reset configuration by the external D28 pin.

1 = Array information disabled
0 = Array information enabled

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RSVD24 — Reserved

Writing to this read/write bit updates the value but has no effect on functionality.

SUPV[7:0] — Supervisor Space Field

The read-always SUPV[7:0] field controls supervisor/unrestricted address space assignment of array blocks. The field is writable when the LOCKCTL bit is clear.

Array blocks that correspond to 1s in SUPV[7:0] are selected for data address space.

Each array block can be mapped into supervisor or unrestricted address space. When an array block is mapped into supervisor address space (SUPV[M] = 1) only supervisor accesses are allowed. A user access to a location in supervisor address space causes a data error exception. When an array block is mapped into unrestricted address space (SUPV[M] = 0) both supervisor and user accesses are allowed.

The default reset state of SUPV[7:0] bits are supervisor address space (SUPV[M] = 1).

1 = Array block in supervisor address space
0 = Array block in unrestricted address space

DATA[7:0] — Data Space Field

The read-always DATA[7:0] field controls data/program address space assignment of array blocks. When LOCKCTL = 1, the DATA[7:0] field is write-protected, and writing to it has no effect.

Array blocks that correspond to 1s in DATA[7:0] are selected for data address space.

Each array block can be mapped into data address space or both data and program address space. When an array block is mapped into data address space (DATA[M] = 1) only data accesses are allowed. A program access to a location in data address space causes a data error exception. When an array block is mapped into both data and program address space (DATA[M] = 0) both data and program accesses are allowed.

The default reset state of DATA[7:0] bits are data and program address space (DATA[M] = 0).

1 = Array block in data address space
0 = Array block is both data and program address space

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PROTECT[7:0] — Block Protect Field

The read-always PROTECT[7:0] field protects array blocks from program and erase operations. If LOCKCTL = 1 or SES = 1, writing to PROTECT[7:0] has no effect.

Array blocks that correspond to 1s in PROTECT[7:0] are selected for data address space.

Each array block can be protected from program and erase operation by setting its PROTECT bit. The CMFR BIU performs all programming and erase interlocks except that the program and erase voltages are not applied to locations within the protected array block(s).

The default reset state of PROTECT[7:0] bits are protected (PROTECT[M] = 1).

1 = Array block protected
0 = Array block not protected

CAUTION: *If the LOCKCTL bit is set before PROTECT[7:0] is cleared, the device must use debug mode to program or erase the CMFR.*

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9.7.1.2 CMFR Module Test Register

The CMFR module test register (CMFRMTR) controls the CMFR array and BIU.

Address: 0x00d0_0004 through 0x00d0_0007

	Bit 31	30	29	28	27	26	25	Bit 24
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:								

	Bit 23	22	21	20	19	18	17	Bit 16
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:								

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	0	0	NVR	PAWS2	PAWS1	PAWS0
Write:								
Reset:					0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	RSVD6	GDB	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 9-4. CMFR Module Test Register (CMFRMTR)

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NVR — Negative Voltage Range Select Bit

The read-always NVR bit modulates the negative pump output to select the negative voltage range in program and erase modes as shown in **Table 9-2**. NVR is writable when the HVS bit is clear but has no effect when the GDB bit is clear.

1 = Negative voltage low range
0 = Negative voltage high range

Table 9-2. Negative Voltage Modulation

PAWS[2:0]	NVR = 0	NVR = 1
100	–6 V	–2 V
101	–7 V	–3 V
110	–8 V	–4 V
111	–9 V	–5 V
0XX	Reserved(1)	

1. When PAWS[2] = 0 and PAWS[1:0] have no effect.

PAWS[2:0] — Pulse Amplitude/Width Select Field

The read-always PAWS[2:0] field selects the pulse drain amplitude and width for program or erase operations. PAWS[2:0] is writable when the HVS bit is clear. PAWS[2] must be set for all program and erase operations. If GDB = 1, the gate/source voltage applied during program/erase is determined by PAWS[1:0] and NVR and shown in **Table 9-2**.

NOTE: *The program pulse time is equal to the value selected by the pulse width timing control. When SES = 1, write to SCLKR[2:0], CLKPE[1:0], and CLKPM[6:0] only when PAWS[2] = 1. Do not write to PAWS[2:0] during high-voltage operations.*

RSVD6 — Reserved

Reserved for factory test and must remain clear at all times

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GDB — Gate or Drain/Source Select Bit

The read-always GDB bit selects gate, source, or drain for voltage modulation. GDB is writable when the SES bit is clear.

GDB selects the gate, source, or drain. In programming, GDB selects gate (GDB = 1) or drain (GDB = 0) voltage for amplitude modulation. When PAWS[2] = 0, mask plugs control amplitude modulation. When PAWS[2] = 1, the PAWS[1:0] bits control amplitude modulation.

1 = Gate selected
0 = Drain/source selected

Table 9-3. Drain Amplitude Modulation (GDB = 0)

PAWS[2:0]	Drain Voltage
100	60% V_{PP}
101	70% V_{PP}
110	80% V_{PP}
111	V_{PP}

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9.7.1.3 CMFR High-Voltage Control Register

The CMFR high-voltage control register (CMFRCTL) controls the program and erase operations of the CMFR.

Address: 0x00d0_0008 through 0x00d0_000b

	Bit 31	30	29	28	27	26	25	Bit 24
Read:	HVS	0	SCLKR2	SCLKR1	SCLKR0	0	CLKPE1	CLKPE0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 23	22	21	20	19	18	17	Bit 16
Read:	0	CLKPM6	CLKPM5	CLKPM4	CLKPM3	CLKPM2	CLKPM1	CLKPM0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	BLOCK7	BLOCK6	BLOCK5	BLOCK4	BLOCK3	BLOCK2	BLOCK1	BLOCK0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	RSVD6	1	0	0	ERASE	SES	EHV
Write:								
Reset:	0	0	1	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 9-5. CMFR High-Voltage Control Register (CMFRCTL)

HVS — High Voltage Status Bit

The read-only HVS bit reflects the status of the program/erase pulse. Writing to HVS has no effect. HVS is set when a pulse is active and during recovery. While HVS = 1, accesses to the array cause a bus error, and SES cannot be changed. The pulse becomes active when the EHV bit is set and is terminated by clearing EHV or by the pulse width timing control. See **Figure 9-6**.

1 = Pulse applied to array or CMFR in recovery
0 = Pulse not applied to array

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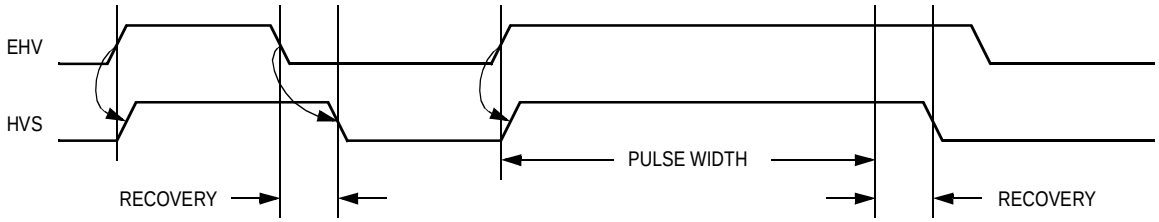

Recovery = 48 scaled clocks or 128 clocks

Figure 9-6. Pulse Status Timing

The recovery time is the time that the CMFR requires to remove the program or erase voltage from the array before switching to another mode of operation. The recovery time is determined by the SCLKR[2:0] field and the ERASE bit. If SCLKR is not 000, the recovery time is 48 of the scaled clock periods. If SCLKR = 000 the recovery time is 128 clocks.

Once reset is completed HVS indicates no program or erase pulse (HVS = 0).

SCLKR[2:0] — System Clock Range Field

The read/write SCLKR[2:0] field selects the system clock range for program/erase pulse timing.

NOTE: *The SCLKR[2:0] bits are not write protected by the SES bit. Unless the PAWS[2] bit is set, writes to SCLKR[2:0] in software should not be changed if SES = 1.*

To control the pulse widths for program and erase operations, the CMFR uses the system clock and the timing control in CMFRCTL. The total pulse time is defined by:

$$\text{pulse width} = \text{system clock period} \times R \times 2^N \times M$$

Where:

R = clock scaling (see **Table 9-4**)
N = 5 + CLKPE[1:0] + ((ERASE) × 10)
M = 1 + CLKPM[6:0]

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Table 9-4. System Clock Range

SCLKR[2:0]	System Clock Frequency (MHz)		Clock Scaling (R)
	Minimum	Maximum(1)	
000	Reserved		
001	8	12	1
010	12	18	3/2
011	18	24	2
100	24	36	3
101	36	40	4
110 and 111	Reserved by Motorola for future use		

1. The maximum system clock frequency is 33 MHz.

The control of the program/erase pulse timing is divided into three functions.

The first term of the timing control is the clock scaling, R. The value of R is determined by the system clock range (SCLKR[2:0]). SCLKR[2:0] defines the base clock of the pulse timer. Use **Table 9-4** to set SCLKR[2:0] based on the system clock frequency.

CAUTION: *If the correct value for SCLKR[2:0] is not selected from the table, the pulse timer may run too fast and cause damage to the device.*

The system clock period is multiplied by the clock scaling value to generate a 83.3-ns to 125-ns scaled clock. This scaled clock is used to run the charge pump submodule and the next functional block of the timing control.

NOTE: *The minimum specified system clock frequency for program and erase operations is 8.0 MHz. The CMFR does not have any means to monitor the system clock frequency and cannot prevent program or erase operation at frequencies below 8.0 MHz. Attempting to program or erase the CMFR at system clock frequencies lower than 8.0 MHz does not damage the device if the maximum pulse times and total times are not exceeded. While some bits in the CMFR array may change state if programmed or erased at system clock frequencies below 8.0 MHz, the full program or erase transition is not assured.*

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CAUTION: *Never stop or alter the system clock frequency during a program or erase operation. Changing the clock frequency during program or erase results in inaccurate pulse widths and variations in the charge pump output.*

The default reset state of SCLKR[2:0] is 000, giving a clock scaling of 1, and the program or erase pulse is not terminated until EHV is cleared by a software write.

CLKPE[1:0] — Clock Period Exponent Field

The read/write CLKPE[1:0] field selects the clock period exponent for program/erase pulse timing. The second term of the timing control is the clock multiplier, 2^N. The program pulse number (pulse), clock period exponent bits (CLKPE[1:0]), and ERASE define the exponent in the 2^N multiply of the clock period. The exponent, N, is defined by the equation:

$$N = 5 + CLKPE[1:0] + [(ERASE) \times 10]$$

All of the exponents are shown in **Table 9-5**.

NOTE: *The CLKPE[1:0] bits are not write protected by the SES bit. Unless the PAWS[2] bit is set, writes to CLKPE[1:0] in software should not be changed if SES = 1.*

The default reset state of CLKPE[1:0] is 00.

Table 9-5. Clock Period Exponent and Pulse Width Range

ERASE	CLKPE[1:0]	Exponent (N)	Pulse Width Range for all System Clock Frequencies from 8.0 MHz to 33.0 MHz	
			Minimum $2^N \times 1.25E-7$	Maximum[1] $2^N \times 128 \times 8.33E-8$
0	00	5	4.00 µs	0.34 ms
	01	6	8.00 µs	0.68 ms
	10	7	16.00 µs	1.36 ms
	11	8	32.0 µs	2.73 ms
1	00	15	4.096 ms	349.5 ms
	01	16	8.192 ms	699.0 ms
	10	17	16.39 ms	1.398 s
	11	18	32.77 ms	2.796 s

1. The maximum system clock frequency is 33 MHz.

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CLKPM[6:0] — Clock Period Multiplier Field

The third term of the timing control is the linear clock multiplier, M. The clock period multiplier, CLKPM[6:0], defines a linear multiplier for the program or erase pulse. M is defined by:

$$M = 1 + (CLKPM[6:0])$$

This allows the program/erase pulse to be from 1 to 128 times the pulse set by the system clock period, SCLKR[2:0] and CLKPE[1:0].

The default reset state of CLKPM[6:0] is binary 000 0000, which gives a multiplier of 1.

NOTE: *The CLKPM[6:0] bits are not write protected by the SES bit. Unless the PAWS[2] bit is set, writes to CLKPM[6:0] in software should not be changed if SES = 1.*

Table 9-6 shows an example of calculating the values of SCLKR[2:0], CLKPE[1:0] and CLKPM[6:0] for a 1-ms program pulse, ERASE = 0, in a system with a 33.0-MHz system clock having a period of 30.3 ns.

Table 9-6. Determining SCLKR[2:0], CLKPE[1:0], and CLKPM[6:0]

No.	Example Calculation
1	Determine SCLKR[2:0] — **Table 9-4** shows that a SCLKR[2:0] value of 100 and an R value of 3 gives a system clock frequency from 24 MHz to 36 MHz.
2	Determine CLKPE[1:0] — **9.7.1 Control Registers** shows that when ERASE = 0, a 1-ms program pulse can be generated by an N value of 7 (CLKPE[1:0] = 10) or 8 (CLKPE[1:0] = 11). An N value of 8 is used in this example.
3	Determine CLKPM[6:0] — Using the selected values of N and R in the pulse width equation, pulse width = system clock period $\times$ R $\times$ 2^N $\times$ M and solving for M yields 42.97. Rounding M to 43 and using the M equation, M = 1 + (CLKPM[6:0]) and solving for CLKPM[6:0] yields 42.
4	Check the results — pulse width = 30.3 ns $\times$ 3 $\times$ 2^8 $\times$ 43 = 1.00 ms where SCLKR[2:0] = 100, CLKPE[1:0] = 11, CLKPM[6:0] = 0101010, ERASE = 0, system clock frequency = 33.0 MHz

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BLOCK[7:0] — Block Program and Erase Field

The read/write BLOCK[7:0] field selects array blocks for program or erase operation. BLOCK[7:0] is writable when the SES bit is clear. If SES is written in the same cycle with BLOCK[7:0] bits, the write permission to BLOCK[7:0] bits depends on the previous value of SES. Up to eight blocks at once can be selected for program operation. Array blocks that correspond to 1s in BLOCK[7:0] are selected for program or erase operation. The BLOCK[7:0] default state is $00, not selected for program or erase.

1 = Array block selected for program or erase
0 = Array block not selected for program or erase

RSVD6 — Reserved

Reserved for test purposes. Writing to this read/write bit updates the values and could affect functionality if set to 1.

ERASE — Program or Erase Select Bit

The read-always ERASE bit selects program or erase operations. ERASE is writable when the SES bit is clear. If SES and ERASE are written in the same cycle, the write permission to ERASE bit depends on the previous value of SES.

When ERASE = 0, the array is configured for programming, and if SES = 1 the SIE bit is write locked. When ERASE = 1, the array is configured for erasing, and SES does not write lock the SIE bit.

1 = Erase operation
0 = Program operation

SES — Start/End Sequence Bit

The read-always SES bit signals the start and end of a program or erase sequence. SES is writable when the HVS and EHV bits are clear. If SES and EHV are written in the same cycle, the write permission to SES depends on the previous value of EHV. At the start of a program or erase sequence, SES is set, locking PROTECT[7:0], BLOCK[7:0], and ERASE.

1 = CMFR configured for program or erase operation
0 = CMFR not configured for program or erase operation

NOTE: *SES does not lock the SCLKR[2:0], CLKPE[1:0], and CLKPM[6:0] bits. Do not change these bits in software when SES = 1 unless PAWS[2] = 1.*

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At this point the CMFR is ready to receive the programming writes, the erase interlock write, or a write to CMFRMCR for programming the reset values of the DIS bit, or a write to CMFRRC.

NOTE: *The erase interlock write is a write to any CMFR array location after SES is set and ERASE = 1.*

If the ERASE bit is a 0, the CMFR BIU accepts programming writes to the CMFR array address for programming. The first programming write selects the program page offset address to be programmed along with the data for the programming buffers at the location written. All programming writes after the first write update the program buffers using the lower address and the block address to select the program page buffers to receive the data. See **9.7.2.2 Program Page Buffers** for further information. After the data has been written to the program buffers the EHV bit is set (written to a 1) to start the programming pulse and lock out further programming writes.

If the ERASE bit is a 1, the CMFR BIU accepts writes to the CMFR array address for erase. An erase interlock write is required before the EHV bit can be set.

At the end of the program or erase operation, the SES bit must be cleared (written to a 0) to return to normal operation and release the program buffers and the locked bits. The CMFR requires a recovery time of 16 clocks after negating SES. This means that if a read access to the CMFR array is done immediately after writing SES = 0, the access is completed after 16 clocks. Also, the FSTOP bit should not be asserted during this recovery time.

The default reset state of SES is not configured for program or erase operation (SES = 0).

EHV — Enable High-Voltage Bit

The read-always EHV bit controls the application of the program or erase voltage to the CMFR. High-voltage operations to the array, special shadow locations or NVM registers can occur only if EHV = 1.

EHV can be asserted only after the SES bit has been asserted and a valid programming write(s) or erase hardware interlock write has occurred. Attempts to assert EHV when SES is negated (including the cycle which writes 0 to SES), or when a valid programming write or erase hardware interlock write has not occurred since SES was asserted have no effect.

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Once EHV is set, SES cannot be changed; attempts to read or write the array or CMFRRC cause bus errors.

The default reset state of EHV disables program or erase pulses (EHV = 0). A master reset while EHV = 1 terminates the high-voltage operation and the CMFR generates the required sequence to disable the high voltage without damage to the high-voltage circuits.

1 = Program/erase pulse enabled
0 = Program/erase pulse disabled

9.7.2 Array Addressing

Information in the array is accessed in 32-byte pages. Two read page buffers are aligned to the low order addresses. The first page buffer is for the lower array blocks. The second page buffer is for the higher array blocks. Access time of information in the read page buffers is one system clock. Access time for an off-page read is two system clocks. To prevent the BIU from accessing an unnecessary page from the array, the CMFR monitors the address to determine if the required information is within one of the two read page buffers and the access is valid for the module. This strategy allows the CMFR to have a 2-clock read for an off-page access and a 1-clock read for an on-page access.

Writing to the array while not in a program/erase sequence causes a bus error.

9.7.2.1 Read Page Buffers

The two 32-byte read page buffers are fully independent and are located in two separate read sections of the array. The BIU monitors the status and address of each page buffer. The status of the read page buffers are usually valid, but are made invalid by these operations:

- Reset
- Programming write
- Erase interlock write
- Setting the EHV bit
- Clearing the SES bit
- Setting or clearing the SIE bit
- Exiting stop mode
- Exiting disable mode
- Exiting boot mode

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Each access to the array determines if the requested location is within the current pages. If the requested location is not within the read page buffers, the appropriate read page buffer is made invalid and a new page of information is fetched from the array. The page buffer address is updated and status is made valid. If the requested location is within one of the current page buffers or has been fetched from the array, the selected bytes are transferred to the CPU, completing the access. Array accesses that make the page buffer(s) invalid are off-page reads that require two system clocks. Array accesses that do not make the page buffer(s) invalid are on-page reads that require one system clock.

9.7.2.2 Program Page Buffers

The CMFR can program up to eight 64-byte pages at one time. Each program page buffer is associated with one array block. All program page buffers share the same block offset address, stored in the BIU. The block offset address is extracted from the address of the first programming write. To select the array block to be programmed, the program page buffers use BLOCK[7:0]. The data programmed in each array block is determined by the programming writes to the program buffer for each block. All program buffer data is unique whereas the program page offset address is shared by all blocks.

An array block is selected for programming if the corresponding BLOCK bit is a 1. If BLOCK[M] = 1, then array block[M] is programmed. If BLOCK[M] = 0, then array block[M] is not programmed. The program page buffers are written regardless of the state of the BLOCK bits, but high-voltage is not applied to blocks for which BLOCK[M] = 0.

Bits in the program page buffers select the non-programmed state if SES = 0. During a program margin read, the program buffers update bits to the non-programmed state for bits that correspond to array bits that the program margin read has determined are programmed.

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9.8 Functional Description

The CMFR is an electrically erasable and programmable non-volatile memory. This subsection describes the functioning of the CMFR during various operational modes.

9.8.1 Master Reset

The device signals a master reset to the CMFR when a full reset is required. A master reset is the highest priority operation for the CMFR and terminates all other operations. The CMFR uses master reset to initialize all register bits to their default reset value. If the CMFR is in program or erase operation (EHV = 1) and a master reset is generated, the module performs the needed interlocks to disable the high voltage without damage to the high voltage circuits. Master reset terminates any other mode of operation and forces the CMFR BIU to a state ready to receive accesses.

9.8.2 Register Read and Write Operation

The CMFR control registers are accessible for read or write operation at all times while the device is powered up except during master reset.

The access time of a CMFR register is one system clock for both read and write accesses. Accesses to unimplemented registers causes the BIU to generate a data error exception.

9.8.3 Array Read Operation

The CMFR array is available for read operation under most conditions while the device is powered up. Reads of the array are ignored (no response) during master reset or while the CMFR is disabled or in stop mode. During programming and erase operation while the high voltage is applied to the array (EHV = 1 or HVS = 1) the BIU generates data errors for all array accesses. At certain points, as defined in the program or erase sequence, reading the array results in a margin read. These margin reads return the status of the program or erase operation and not the data in the array.

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The type of array read is determined by comparing the address of the requested information with the address of the read page buffers. If the requested address is not in one of the read page buffers or if the read page buffer has been made invalid, an off-page read results. This read updates the selected array block's read page buffer address, copies the information from the array into the read page buffer, and drives a word/half-word onto the data bus. The off-page read requires a minimum of two clocks; margin off-page reads require additional clocks (see **9.8.4.2 Program Margin Reads** and **9.8.5.2 Erase Margin Reads**). If the address of the requested information is within the address ranges of either of the read page buffers, the second type of read is performed. This read is an on-page read and requires one clock to transfer information from the read page buffer onto the data bus.

NOTE: *After reset, programming writes, erase interlock write, setting EHV, clearing SES, setting/clearing SIE and exiting stop mode or disable mode, the page buffers do not contain valid information and the CMFR must do an off-page read before an on-page read can be done.*

9.8.4 Programming

To modify the charge stored in the isolated element of the CMFR bit from a logic 1 state to a logic 0 state, a programming operation is required. A programmed bit reads as logic 0. This programming operation applies the required voltages to change the charge state of the selected bits without changing the logic state of any other bits in the array. The program operation cannot change the logic 0 state to a logic 1 state; this transition must be done by the erase operation. An erased bit reads as logic 1. Programming uses a set of eight program buffers of 64 bytes to store the required data, an address offset buffer to store the starting address of the block(s) to be programmed, and a block select buffer that stores information on which block(s) are to be programmed. From one to eight of the program page buffers may be programmed at one time.

CAUTION: *Do not program any page more than once after a successful erase operation. While this does not physically damage the array it causes an increased partial disturb time for the unselected bits on the row and columns that are not programmed. A full erase of all blocks being programmed must be done before the CMFR can be used reliably.*

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Blocks of the CMFR that are protected (PROTECT[block] = 1) are not programmed.

The program sequence is outlined in **9.8.4.1 Program Sequence** and depicted in the flowchart form in **Figure 9-7**.

9.8.4.1 Program Sequence

Use this sequence to enable the high voltage to the array or shadow information for program operation:

1. Make sure the CMFRMTR and CMFRCTL are in their reset states.
2. Set PAWS[2] = 1 and GDB = 1 in CMFRMTR.
3. In CMFRMCR, write PROTECT[7:0] to disable protection of blocks to be programmed.
4. Use the procedure in **Table 9-6** to write the pulse width timing control fields for a program pulse.
5. In CMFRCTL, clear the ERASE bit, and write BLOCK[7:0] to select the array blocks to be programmed.
6. In CMFRCTL, set the SES bit.
7. Programming write — A successful write to the array locations to be programmed. This updates the programming page buffer(s) with the information to be programmed. All accesses to the array after the first write are to the same block offset address regardless of the address provided. Thus the locations accessed after the first programming write are limited to the page locations to be programmed. Off-page read accesses of the array after the first programming write are program margin reads.

NOTE: *All program page buffers share the same block offset address stored in the BIU. The block offset address is extracted from the address of the first programming write. To select the array block(s) to be programmed, the program page buffers use BLOCK[7:0]. Subsequent writes fill in the programming page buffers using the block address to select the program page buffer and the page word address to select the word in the page buffer.*

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8. In CMFRCTL, set the EHV bit.

NOTE: *If a program page buffer word has not received a programming write, no programming voltages are applied to the drain of the corresponding word in the array. At this point, writing to the program page buffers is disabled and causes a bus error until SES has been cleared and set.*

9. Read CMFRCTL until HVS = 0.
10. In CMFRCTL, clear the EHV bit.
11. Verify the program by reading the words of the pages that are being programmed. These are program margin reads. A bit that was successfully programmed returns a 0 during a margin read. It returns a 1 if it has been unsuccessfully programmed. If any bit intended to be programmed does not return a 0 after reading all the locations, the margin read has failed. If the margin read is successful continue to step **12**, otherwise do the following:
    a. Write new pulse width parameters (if required, see **Table 9-9** for the required programming algorithm) CLKPE and CLKPM.
    b. Write new values for PAWS and NVR (if required, see **Table 9-9**)
    c. Go back to step **8** to apply additional pulses.

    To reduce the time for verification, read two locations in each array block that is being programmed after reading a non-programmed bit. After a location has been verified (all bits are programmed), it is not necessary to reverify the location, as no further programming voltages are applied to the drain of the corresponding bits.

CAUTION: *After a program pulse, read at least one location with address bit 5 = 0 and one location with address bit 5 = 1 on each programmed page. Failure to do so may result in the loss of information in the CMFR array, and a full erase of all blocks being programmed must be done before the* CMFR *can be used reliably.*

12. In CMFRCTL, clear the SES bit.
13. If more information needs to be programmed, go to step **3**.

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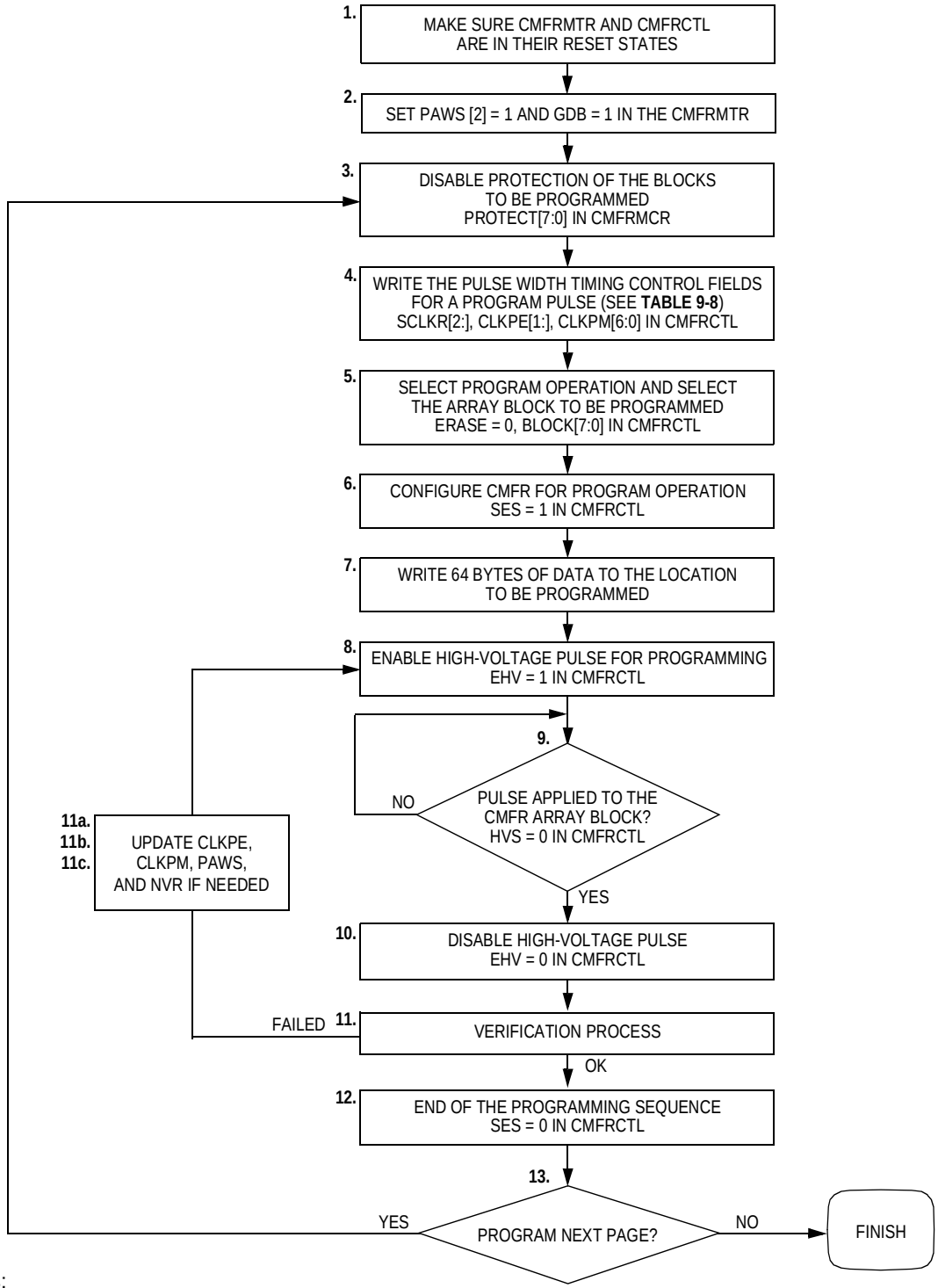

Notes:
1. This page program algorithm assumes the blocks to be programmed are initially erased.
2. Make sure that CMFRMTR is in its reset state at the beginning of the programming process and afterwards.

Figure 9-7. FLASH Programming Flowchart

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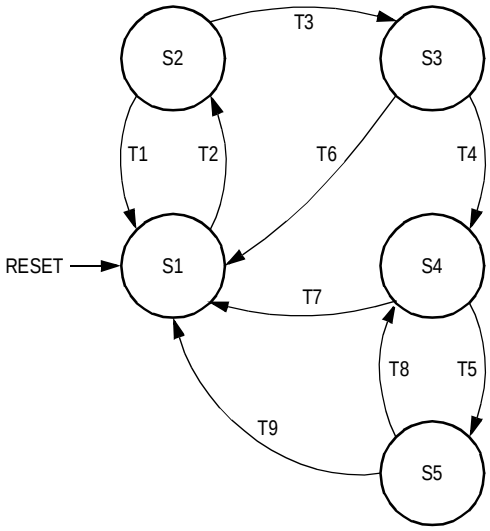

Figure 9-8. Program State Diagram

Table 9-7. Program Interlock State Descriptions

State	Mode	Next State	Transition Requirement	
S1	**Normal operation:** Normal array reads and register accesses. Block protect information and pulse width timing control can be modified.	S2	T2	Write ERASE = 0 and SES = 1
S2	**First program hardware interlock write**: Normal read operation. Array accepts programming writes. Normal register accesses. CMFRCTL write cannot change EHV. If write is to a register other than CMFRMCR, no data is stored in program page buffers; CMFR remains in S2.	S1	T1	Write SES = 0 or master reset
		S3	T3	**Hardware interlock**: Successful programming write to any array location. Latches selected data word into programming page buffer; address latched to select location to program. Bit that has been written remains in program buffer until another write to it, or SES is cleared, or a program margin read determines bit needs no modification by program operation. If write is to a register (except CMFRMCR), no data is stored in program page buffers, and CMFR remains in S2. Writing to CMFRMCR does not allow array to be programmed.

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Table 9-7. Program Interlock State Descriptions (Continued)

State	Mode	Next State	Transition Requirement	
S3	**Expanded program hardware interlock operation:** Program margin reads. Programming writes accepted; all eight program pages can be programmed. Writes can be to any array location. Program page buffers updated using only data, lower address, and block address. Normal register accesses. CMFRCTL write can change EHV. If write is to a register, no data is stored in program page buffer.	S1	T6	Write SES = 0 or master reset
		S4	T4	Write EHV = 1
S4	**Program operation**: High voltage applied to array or shadow information to program CMFR bitcells. Pulse width timer active if SCLKR[2:0] ≠ 0; HVS can be polled to time program pulse. Programming writes not accepted. During programming, array cannot be accessed (bus error). Normal register accesses. CMFRCTL write can change only EHV.	S1	T7	Master reset
		S5	T5	EHV = 0 and HVS = 0
S5	**Program margin read operation**: Reads determine if bits on selected page need modification by program operation. Once bit is fully programmed, data stored in program page is updated; no further programming occurs for that bit and value read is 0. While it is not necessary to read all words on a page to determine if another program pulse is needed, all pages being programmed must be read once after each program pulse.	S4	T8	Write EHV = 1
		S1	T9	Write SES = 0 or a master reset

9.8.4.2 Program Margin Reads

The CMFR provides a program margin read with electrical margin for the program state. Program margin reads provide sufficient margin to assure specified data retention. The program margin read is enabled when SE = 1 and a programming write has occurred. To increase the access time of the program margin read the off-page access time is 17 clocks instead of the usual 2-clock off-page read access time. The program margin read and subsequent on-page program verify reads

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return a 1 for any bit that has not completely programmed. Bits left in the non-programmed state after the programming write read as a 0s. Bits that have completed programming read as 0s and update the data in the programming page buffer so that no further programming of those bits occurs.

Table 9-8. Results of Programming Margin Read

Current Data in Program Page Buffer	Current Bit State	Read Output	New Data for the Program Page Buffer
0	Programmed — 0	0	1
0	Erased — 1	1	0
1	Programmed — 0	0	1
1	Erased — 1	0	1

The program margin read occurs while doing the off-page read. A program margin read must be done for all pages that are being programmed after each program pulse.

CAUTION: *Failure to read each page that is being programmed after each program pulse may result in the loss of information in the array. While this does not physically damage the array a full erase of all blocks being programmed must be done before the CMFR can be used reliably.*

9.8.4.3 Programming Shadow Information

Programming the shadow information uses the same procedure as programming the array except that only program page 0 is used to program the shadow information. Before starting the program sequence SIE must be a 1. BLOCK and PROTECT bits do not affect programming of the shadow locations.

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9.8.4.4 Program Pulse-Width and Amplitude Modulation

To prevent bits from possibly becoming depleted (over programmed), the first programming pulses should be of reduced duration and with reduced drain voltage. Refer to **Table 9-9** for the required programming steps to insure FLASH reliability.

NOTE: *The values of PAWS[2:0] and NVR should be updated on the appropriate pulse to change the programming voltage and CLKPM should be updated to adjust the pulse width.*

Table 9-9. Required Programming Algorithm

Voltage Step	PAWS[2:0]	NVR	Pulse Width	Number of Pulses
–2 V	1 0 0	1	250 µs	4
–3 V	1 0 1	1	250 µs	4
–4 V	1 1 0	1	250 µs	4
–5 V	1 1 1	1	250 µs	4
–6 V	1 0 0	0	50 µs	20
–7 V	1 0 1	0	50 µs	20
–8 V	1 1 0	0	50 µs	20
–9 V	1 1 1	0	50 µs	20
–9 V	1 1 1	0	100 µs	Any additional

GDB = 1 for all programming operations.
Margin reads are required after every pulse.

9.8.4.5 Overprogramming

Programming a bit without a program margin read after each program pulse or exceeding the specified program times or voltages results in an overprogrammed state. Once a bit is overprogrammed, data in the array block that is located in the same column is lost as the overprogrammed bit causes the entire column to appear programmed. To restore an array block with an overprogrammed bit, the block must be erased and reprogrammed.

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9.8.5 Erasing

To modify the charge stored in the isolated element of a bit from a logic 0 state to a logic 1 state, an erase operation is required. The erase operation cannot change the logic 1 state to a logic 0 state; this transition must be done by the program operation. Erase is a bulk operation that affects the stored charge of all the isolated elements in an array block. To make the block erasable, the array is divided into blocks that are physically isolated from each other. Each of the array blocks may be erased in isolation or in any combination. The array block size is fixed for all blocks at 16 Kbytes and the module is comprised of eight blocks. Array blocks that are protected (PROTECT[M] = 1) are not erased.

The array blocks selected for erase operation are determined by BLOCK[7:0].

NOTE: *Erasing BLOCK 0 also erases the shadow information.*

The erase sequence is outlined in **9.8.5.1 Erase Sequence** and depicted in the flowchart form in **Figure 9-9**.

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9.8.5.1 Erase Sequence

Use this sequence to enable the high voltage to the array or shadow information for erase operation:

1. Make sure that CMFRMTR is in its reset state, and write PAWS[2:0] = 111 to override firmware amplitude modulation.
2. In CMFRMCR, write PROTECT[7:0] to disable protection of the blocks to be erased.
3. Use the procedure in **Table 9-6** to write the pulse-width timing control fields for an erase pulse with BLOCK[7:0] selecting the blocks to be erased and ERASE = SES = 1 in CMFRCTL.
4. Execute an erase interlock write to any array location.
5. In CMFRCTL, write EHV = 1.
6. Read CMFRCTL until HVS = 0.
7. In CMFRCTL, write EHV = 0.
8. Verify the erase by reading all locations that are being erased, including the shadow information if the block that contains it is erased. Off-page reads are erase margin reads that update the read page buffer. If all the locations read as erased, continue to the next step otherwise, update PAWS and NVR (if required, see **Table 9-9**). Then go back to step **5**.

   To reduce the time for verification, upon the first read of a 0, go to step **5**. After a location has been verified (all bits are erased), it is not necessary to reverify locations after subsequent erase pulses.
9. In CMFRCTL, write SES = 0.
10. Make sure that CMFRMTR is in its reset state.

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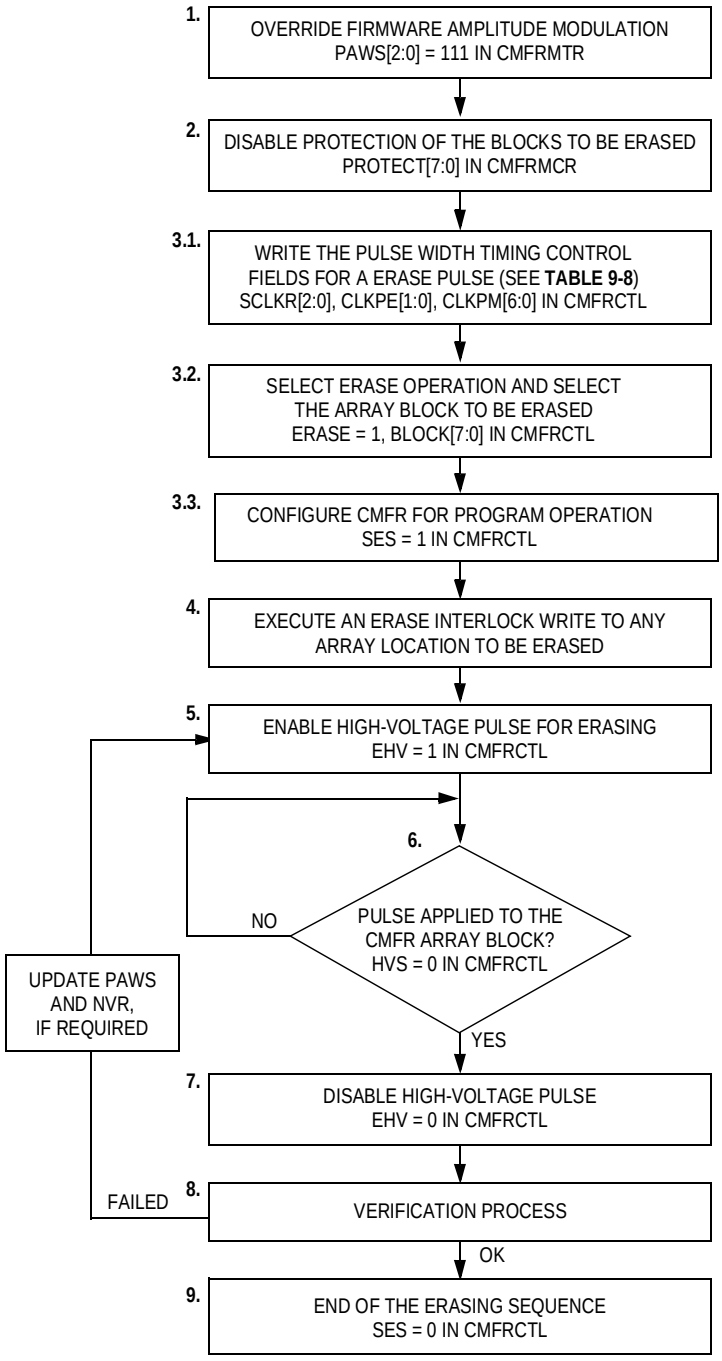

Note: Make sure that CMFRMTR is i its reset state at the beginning of the erasing process and afterwards.

Figure 9-9. FLASH Erasing Flowchart

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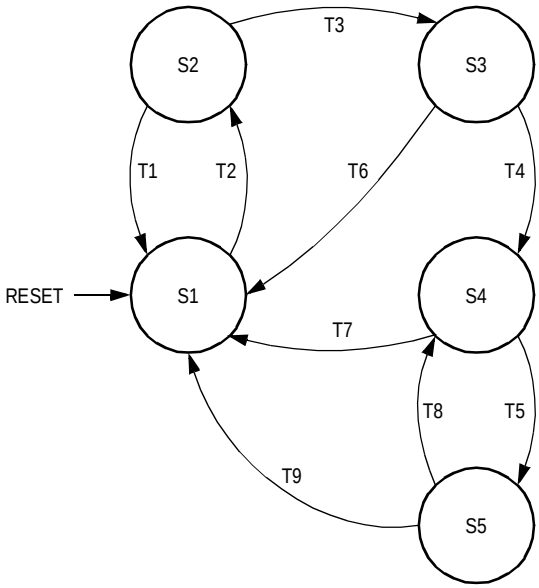

Figure 9-10. Erase State Diagram

Table 9-10 Erase Interlock State Descriptions

State	Mode	Next State	Transition Requirement	
S1	**Normal operation**: Normal array reads and register accesses. Block protect information and pulse-width timing control can be modified.	S2	T2	Write ERASE = 1 and SES = 1
S2	**Erase hardware interlock write**: Normal read operation. CMFR accepts erase hardware interlock write to any array location. Normal register access (except CMFRMCR). CMFRCTL write cannot set EHV. Register write (except CMFRMCR) is not erase hardware interlock write; CMFR remains in S2. CMFRMCR write causes transition to S3.	S1	T1	Write SES = 0 or a master reset
		S3	T3	**Hardware interlock**: Write to any array location is erase interlock write. Register write other than CMFRMCR is not erase hardware interlock write; CMFR remains in S2. CMFRMCR write causes transition to S3; NVM fuses cleared during high-voltage pulse

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Table 9-10 Erase Interlock State Descriptions (Continued)

State	Mode	Next State	Transition Requirement	
S3	**High voltage write enable**: Erase margin reads occur. CMFR accepts erase hardware interlock write. Normal register accesses (except CMFRMCR). CMFRMCR write causes NVM fuses to be cleared during the high-voltage pulse. If CMFRMCR was written, a CMFRMCR read returns the NVM fuses value. CMFRCTL write can change EHV. When HVS goes high, NVR and PAWS are locked.	S1	T6	Write SES = 0 or a master reset
		S4	T4	Write EHV = 1
S4	**Erase operation**: High voltage applied to array blocks to erase bitcells. Pulse-width timer active if SCLKR[2:0] ≠ 0; HVS can be polled to time the erase pulse. During erase, array cannot be accessed (bus error). Normal register accesses. CMFRCTL write can change only EHV.	S1	T7	Master reset
		S5	T5	EHV = 0 and HVS = 0
S5	**Erase margin read operation**: Reads determine if bits in selected blocks need modification by the erase operation. Erased bit reads as 1. All words in erased blocks must be read to determine if erase is complete.	S4	T8	Write EHV = 1
		S1	T9	Write SES = 0 or a master reset

9.8.5.2 Erase Margin Reads

The CMFR provides an erase margin read with electrical margin for the erase state. Erase margin reads provide sufficient margin to assure specified data retention. The erase margin read is enabled when SES = 1 and the erase write has occurred. The erase margin read and subsequent on-page erase verify reads return a 0 for any bit that has not completely erased. Bits that have completed erasing read as a 1s. To increase the access time of the erase margin read, the off-page access time is 17 clocks instead of the usual 2-clock off-page read access time. The erase margin read occurs while doing an off-page read. All locations within the block(s) that are being erased must read as a 1 to determine that no more erase pulses are required.

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9.8.5.3 Erasing Shadow Information Words

The shadow information words are erased with either array block 0 depending upon the array configuration. To verify that the shadow information words are erased with block 0, erase margin reads should be performed with the SIE bit set in CMFRMCR while the shadow information is read. For the erase operation to be completed, block 0 must also be fully verified.

NOTE: *Setting SIE = 1 disables normal array access and should be cleared after verifying the shadow information.*

9.8.6 Erase Pulse Amplitude and Width Modulation

Refer to **Table 9-11** for the required erase algorithm to insure reliability of the FLASH.

NOTE: *The values of PAWS[2:0] and NVR should be updated on the appropriate pulse to change the erase voltage.*

Table 9-11. Required Erase Algorithm

Voltage Step	PAWS[2:0]	NVR	Pulse Width	Number of Pulses
–2 V	1 0 0	1	100 ms	1
–3 V	1 0 1	1	100 ms	1
–4 V	1 1 0	1	100 ms	1
–5 V	1 1 1	1	100 ms	1
–6 V	1 0 0	0	100 ms	1
–7 V	1 0 1	0	100 ms	1
–8 V	1 1 0	0	100 ms	1
–9 V	1 1 1	0	100 ms	20

GDB = 0 for all erase operations.
Margin reads are required after the first –9-V pulse.

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9.8.7 Emulation Operation

In emulation mode, to support emulation of the internal FLASH memory with external memory devices, the CMFR responds to an array access only by terminating the access. During emulation, the CMFR does not drive any data and the data should be provided by an external device. This synchronizes the timing of 1-clock on-page accesses and 2-clock off-page accesses during emulation from external memory.

9.9 Master Reset

The device signals a master reset to the CMFR when a full reset is required. A master reset is the highest priority operation for the CMFR and terminates all other operations. The CMFR uses master reset to initialize all register bits to their default reset value. If the CMFR is in program or erase operation (EHV = 1) and a master reset is generated, the module performs the needed interlocks to disable the high voltage without damage to the high voltage circuits. Master reset terminates any other mode of operation and forces the CMFR BIU to a state ready to receive accesses.

9.10 Interrupts

The CMFR does not generate interrupt requests.

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Section 10. Clock Module

10.1 Contents

10.2 Introduction 222
10.3 Features 222
10.4 Modes of Operation 223
10.4.1 Normal PLL Mode 223
10.4.2 1:1 PLL Mode 223
10.4.3 External Clock Mode 223
10.4.4 Low-Power Options 223
10.4.4.1 Wait and Doze Modes 223
10.4.4.2 Stop Mode 224
10.5 Block Diagram 224
10.6 Signal Descriptions 225
10.6.1 EXTAL 225
10.6.2 XTAL 225
10.6.3 CLKOUT 225
10.6.4 V_{DDSYN} and V_{SSSYN} 225
10.6.5 RSTOUT 226
10.7 Memory Map and Registers 226
10.7.1 Module Memory Map 226
10.7.2 Register Descriptions 227
10.7.2.1 Synthesizer Control Register 227
10.7.2.2 Synthesizer Status Register 230
10.7.2.3 Synthesizer Test Register 233
10.7.2.4 Synthesizer Test Register 2 234
10.8 Functional Description 235
10.8.1 System Clock Modes 235
10.8.2 System Clocks Generation 236

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10.8.3 PLL Lock Detection 236
10.8.3.1 PLL Loss of Lock Conditions 238
10.8.3.2 PLL Loss of Lock Reset 238
10.8.4 Loss of Clock Detection 238
10.8.4.1 Alternate Clock Selection 239
10.8.4.2 Loss-of-Clock Reset 242
10.8.5 Clock Operation During Reset 243
10.8.6 PLL Operation 243
10.8.6.1 Phase and Frequency Detector (PFD) 245
10.8.6.2 Charge Pump/Loop Filter 245
10.8.6.3 Voltage Control Output (VCO) 246
10.8.6.4 Multiplication Factor Divider (MFD) 246
10.9 Reset 246
10.10 Interrupts 246

10.2 Introduction

The clock module contains:

- Crystal oscillator (OSC)
- Phase-locked loop (PLL)
- Reduced frequency divider (RFD)
- Status and control registers
- Control logic

To improve noise immunity, the PLL and OSC have their own power supply pins, V_{DDSYN} and V_{SSSYN}. All other circuits are powered by the normal internal supply pins, V_{DD} and V_{SS}.

10.3 Features

Features of the clock module include:

- 2- to 10-MHz reference crystal
- Support for low-power modes
- Separate clock out signal

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10.4 Modes of Operation

The clock module can be operated in normal PLL mode, 1:1 PLL mode, or external clock mode.

10.4.1 Normal PLL Mode

In normal PLL mode, the PLL is fully programmable. It can synthesize frequencies ranging from 2x to 9x the reference frequency and has a post divider capable of reducing this synthesized frequency without disturbing the PLL. The PLL reference can be either a crystal oscillator or an external clock.

10.4.2 1:1 PLL Mode

In 1:1 PLL mode, the PLL synthesizes a frequency equal to the external clock input reference frequency. The post divider is not active.

10.4.3 External Clock Mode

In external clock mode, the PLL is bypassed, and the external clock is applied to EXTAL.

10.4.4 Low-Power Options

During wakeup from a low-power mode, the FLASH clock always clocks through at least 16 cycles before the core clocks are enabled. This allows the FLASH module time to recover from the low-power mode, and software can immediately resume fetching instructions from the memory.

10.4.4.1 Wait and Doze Modes

In wait and doze modes, the system clocks to the peripherals are enabled, and the clocks to the CPU, FLASH, and random-access memory (RAM) are stopped. Each module can disable the module clocks locally at the module level.

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10.4.4.2 Stop Mode

In stop mode, all system clocks are disabled. There are several options for enabling/disabling the PLL and/or crystal oscillator in stop mode at the price of increased wakeup recovery time. The PLL can be disabled in stop mode, but then it requires a wakeup period before it can relock. The OSC can also be disabled during stop mode, but then it requires a wakeup period to restart.

When the PLL is enabled in stop mode (STPMD[1:0]), the external CLKOUT signal can support systems using CLKOUT as the clock source.

There is also a fast wakeup option for quickly enabling the system clocks during stop recovery. This eliminates the wakeup recovery time but at a price of sending a potentially unstable clock to the system. To prevent a non-locked PLL frequency overshoot when using the fast wakeup option, change the RFD divisor to the current RFD value plus one before entering stop mode.

In external clock mode, there are no wakeup periods for oscillator startup or PLL lock.

10.5 Block Diagram

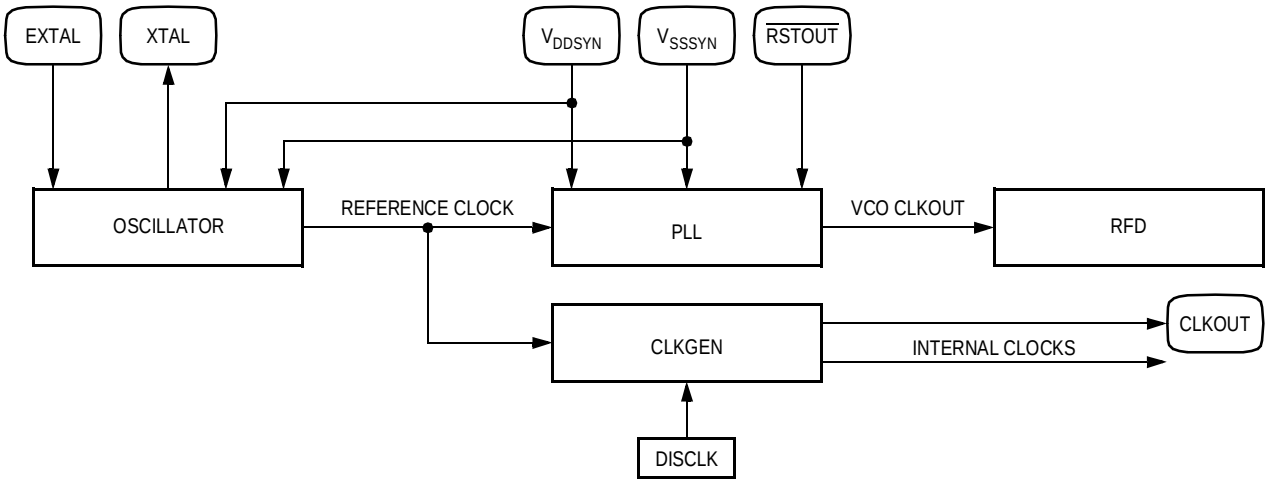

Figure 10-1. Clock Module Block Diagram

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10.6 Signal Descriptions

The clock module signals are summarized in **Table 10-1** and a brief description follows. For more detailed information, refer to **Section 4. Signal Description**.

Table 10-1. Signal Properties

Name	Function
EXTAL	Oscillator or clock input
XTAL	Oscillator output
CLKOUT	System clock output
V_{DDSYN}	Clock module power supply inputs
V_{SSSYN}	
$\overline{RSTOUT}$	Reset signal from reset controller

10.6.1 EXTAL

This input is driven by an external clock except when used as a connection to the external crystal when using the internal oscillator.

10.6.2 XTAL

This output is an internal oscillator connection to the external crystal.

10.6.3 CLKOUT

This output reflects the internal system clock.

10.6.4 V_{DDSYN} and V_{SSSYN}

These are dedicated power and ground inputs for the frequency synthesizer.

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10.6.5 $\overline{\text{RSTOUT}}$

The $\overline{\text{RSTOUT}}$ pin is asserted by:

- Internal system reset signal, or
- FRCRSTOUT bit in the reset control status register (RCR); see **5.6.1 Reset Control Register**

10.7 Memory Map and Registers

The clock programming model consists of these registers:

- Synthesizer control register (SYNCR) — Defines clock operation
- Synthesizer status register (SYNSR) — Reflects clock status
- Synthesizer test register (SYNTR) — Used for factory test
- Synthesizer test register 2 (SYNTR2) — Used only for factory test

10.7.1 Module Memory Map

Table 10-2. Clock Module Memory Map

Address	Register Name	Access(1)
0x00c3_0000	Synthesizer control register (SYNCR)	S
0x00c3_0002	Synthesizer status register (SYNSR)	S
0x00c3_0003	Synthesizer test register (SYNTR)	S
0x00c3_0004	Synthesizer test register 2 (SYNTR2)	S

1. S = CPU supervisor mode access only.

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10.7.2 Register Descriptions

This subsection provides a description of the clock module registers.

10.7.2.1 Synthesizer Control Register

The synthesizer control register (SYNCR) is read/write always.

Address: 0x00c3_0000 and 0x00c3_0001

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	LOLRE	MFD2	MFD1	MFD0	LOCRE	RFD2	RFD1	RFD0
Reset:	0	0	1	0	0	0	0	1
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LOCEN	DISCLK	FWKUP	RSVD4	STMPD1	STMPD0	RSVD1	RSVD0
Reset:	0	0	0	0	0	0	0	0

Figure 10-2. Synthesizer Control Register (SYNCR)

LOLRE — Loss of Lock Reset Enable Bit

The LOLRE bit determines how the system handles a loss of lock indication. When operating in normal mode or 1:1 PLL mode, the PLL must be locked before setting the LOLRE bit. Otherwise reset is immediately asserted. To prevent an immediate reset, the LOLRE bit must be cleared before writing the MFD[2:0] bits or entering stop mode with the PLL disabled.

1 = Reset on loss of lock
0 = No reset on loss of lock

NOTE: *In external clock mode, the LOLRE bit has no effect.*

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MFD[2:0] — Multiplication Factor Divider Field

MFD[2:0] contain the binary value of the divider in the PLL feedback loop. See **Table 10-3**. The MFD[2:0] value is the multiplication factor applied to the reference frequency. When MFD[2:0] are changed or the PLL is disabled in stop mode, the PLL loses lock. In 1:1 PLL mode, MFD[2:0] are ignored, and the multiplication factor is one.

NOTE: *In external clock mode, the MFD[2:0] bits have no effect. See **Table 10-6**.*

Table 10-3. System Frequency Multiplier of the Reference Frequency(1) in Normal PLL Mode

		MFD[2:0]							
		000 (2x)	**001 (3x)**	**010 (4x)**	**011 (5x)**	**100 (6x)**	**101 (7x)**	**110 (8x)**	**111 (9x)**
RFD[2:0]	**000 (÷ 1)**	2	3	4	5	6	7	8	9
	001 (÷ 2)(2)	1	3/2	2	5/2	3	7/2	4	9/2
	010 (÷ 4)	1/2	3/4	1	5/4	3/2	7/4	2	9/4
	011 (÷ 8)	1/4	3/8	1/2	5/8	3/4	7/8	1	9/8
	100 (÷ 16)	1/8	3/16	1/4	5/16	3/8	7/16	1/2	9/16
	101 (÷ 32)	1/16	3/32	1/8	5/32	3/16	7/32	1/4	9/32
	110 (÷ 64)	1/32	3/64	1/16	5/64	3/32	7/64	1/8	9/64
	111 (÷ 128)	1/64	3/128	1/32	5/128	3/64	7/128	1/16	9/128

1. $f_{sys} = f_{ref}$ x (MFD + 2)/2^{RFD}
2. Default value out of reset

LOCRE — Loss of Clock Reset Enable Bit

The LOCRE bit determines how the system handles a loss of clock condition. When the LOCEN bit is clear, LOCRE has no effect. If the LOCS flag in SYNSR indicates a loss of clock condition, setting the LOCRE bit causes an immediate reset. To prevent an immediate reset, the LOCRE bit must be cleared before entering stop mode with the PLL disabled.

1 = Reset on loss of clock
0 = No reset on loss of clock

NOTE: *In external clock mode, the LOCRE bit has no effect.*

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RFD[2:0] — Reduced Frequency Divider Field

The binary value written to RFD[2:0] is the PLL frequency divisor. See **Table 10-3**. Changing RFD[2:0] does not affect the PLL or cause a relock delay. Changes in clock frequency are synchronized to the next falling edge of the current system clock. To avoid surpassing the allowable system operating frequency, write to RFD[2:0] only when the LOCK bit is set.

NOTE: *In external clock mode, the RFD[2:0] bits have no effect. See **Table 10-6**.*

LOCEN — Loss of Clock Enable Bit

The LOCEN bit enables the loss of clock function. LOCEN does not affect the loss of lock function.

1 = Loss of clock function enabled
0 = Loss of clock function disabled

NOTE: *In external clock mode, the LOCEN bit has no effect.*

DISCLK — Disable CLKOUT Bit

The DISCLK bit determines whether CLKOUT is driven. Setting the DISCLK bit holds CLKOUT low.

1 = CLKOUT disabled
0 = CLKOUT enabled

FWKUP — Fast Wakeup Bit

The FWKUP bit determines when the system clocks are enabled during wakeup from stop mode.

1 = System clocks enabled on wakeup regardless of PLL lock status
0 = System clocks enabled only when PLL is locked or operating normally

NOTE: *When FWKUP = 0, if the PLL or OSC is enabled and unintentionally lost in stop mode, the PLL wakes up in self-clocked mode or reference clock mode depending on the clock that was lost.*

In external clock mode, the FWKUP bit has no effect on the wakeup sequence.

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STPMD[1:0] — Stop Mode Bits

STPMD[1:0] control PLL and CLKOUT operation in stop mode as shown in **Table 10-4**.

Table 10-4. STPMD[1:0] Operation in Stop Mode

STPMD[1:0]	Operation During Stop Mode			
	System Clocks	PLL	OSC	CLKOUT
00	Disabled	Enabled	Enabled	Enabled
01	Disabled	Enabled	Enabled	Disabled
10	Disabled	Disabled	Enabled	Disabled
11	Disabled	Disabled	Disabled	Disabled

RSVD4, RSVD1, and RSVD0 — Reserved

Writing to these read/write bits updates their values but has no effect on functionality.

10.7.2.2 Synthesizer Status Register

The synthesizer status register (SYNSR) is a read-only register that can be read at any time. Writing to the SYNSR has no effect and terminates the cycle normally.

Address: 0x00c3_0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PLLMODE	PLLSEL	PLLREF	LOCKS	LOCK	LOCS	0	0
Write:								
Reset:	Note 1	Note 1	Note 1	Note 2	Note 2	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Notes:
1. Reset state determined during reset configuration.
2. See the LOCKS and LOCK bit descriptions.

Figure 10-3. Synthesizer Status Register (SYNSR)

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PLLMODE — Clock Mode Bit

The MODE bit is configured at reset and reflects the clock mode as shown in **Table 10-5**.

1 = PLL clock mode
0 = External clock mode

Table 10-5. System Clock Modes

MODE:PLLSEL:PLLREF	Clock Mode
000	External clock mode
100	1:1 PLL mode
110	Normal PLL mode with external clock reference
111	Normal PLL mode with crystal oscillator reference

PLLSEL — PLL Select Bit

The PLLSEL bit is configured at reset and reflects the PLL mode as shown in **Table 10-5**.

1 = Normal PLL mode
0 = 1:1 PLL mode

PLLREF — PLL Reference Bit

The PLLREF bit is configured at reset and reflects the PLL reference source in normal PLL mode as shown in **Table 10-5**.

1 = Crystal clock reference
0 = External clock reference

LOCKS — Sticky PLL Lock Bit

The LOCKS flag is a sticky indication of PLL lock status.

1 = No unintentional PLL loss of lock since last system reset or MFD change
0 = PLL loss of lock since last system reset or MFD change or currently not locked due to exit from STOP with FWKUP set

The lock detect function sets the LOCKS bit when the PLL achieves lock after:

– A system reset, or
– A write to SYNCR that changes the MFD[2:0] bits

When the PLL loses lock, LOCKS is cleared. When the PLL relocks, LOCKS remains cleared until one of the two listed events occurs.

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In stop mode, if the PLL is intentionally disabled, then the LOCKS bit reflects the value prior to entering stop mode. However, if FWKUP is set, then LOCKS is cleared until the PLL regains lock. Once lock is regained, the LOCKS bit reflects the value prior to entering stop mode. Furthermore, reading the LOCKS bit at the same time that the PLL loses lock does not return the current loss of lock condition.

In external clock mode, LOCKS remains cleared after reset. In normal PLL mode and 1:1 PLL mode, LOCKS is set after reset.

LOCK — PLL Lock Flag

1 = PLL locked
0 = PLL not locked

The LOCK flag is set when the PLL is locked. PLL lock occurs when the synthesized frequency is within approximately 0.75 percent of the programmed frequency. The PLL loses lock when a frequency deviation of greater than approximately 1.5 percent occurs. Reading the LOCK flag at the same time that the PLL loses lock or acquires lock does not return the current condition of the PLL. The power-on reset circuit uses the LOCK bit as a condition for releasing reset.

If operating in external clock mode, LOCK remains cleared after reset.

LOCS — Sticky Loss Of Clock Flag

1 = Loss of clock detected since exiting reset or oscillator not yet recovered from exit from stop mode with FWKUP = 1
0 = Loss of clock not detected since exiting reset

The LOCS flag is a sticky indication of whether a loss of clock condition has occurred at any time since exiting reset in normal PLL and 1:1 PLL modes. LOCS = 0 when the system clocks are operating normally. LOCS = 1 when system clocks have failed due to a reference failure or PLL failure.

After entering stop mode with FWKUP set and the PLL and oscillator intentionally disabled (STPMD[1:0] = 11), the PLL exits stop mode in SCM while the oscillator starts up. During this time, LOCS is temporarily set regardless of LOCEN. It is cleared once the oscillator comes up and the PLL is attempting to lock.

If a read of the LOCS flag and a loss of clock condition occur simultaneously, the flag does not reflect the current loss of clock condition.

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A loss of clock condition can be detected only if LOCEN = 1 or the oscillator has not yet returned from exit from stop mode with FWKUP = 1.

NOTE: *The LOCS flag is always 0 in external clock mode.*

10.7.2.3 Synthesizer Test Register

The synthesizer test register (SYNTR) is only for factory testing. When not in test mode, SYNTR is read-only.

Address: 0x00c3_0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 10-4. Synthesizer Test Register (SYNTR)

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10.7.2.4 Synthesizer Test Register 2

The synthesizer test register 2 (SYNTR2) is only for factory testing.

Address: 0x00c3_0004 through 0x00c3_0007

	Bit 31	30	29	28	27	26	25	Bit 24
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 23	22	21	20	19	18	17	Bit 16
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	0	0	0	0	RSVD9	RSVD8
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RSVD7	RSVD6	RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 10-5. Synthesizer Test Register 2 (SYNTR2)

Bits 31–10

Bits 31–10 are read-only. Writing to bits 31–10 has no effect.

RSVD9–RSVD0 — Reserved

The RSVD bits can be read at any time. Writes to these bits update the register values but have no effect on functionality.

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10.8 Functional Description

This subsection provides a functional description of the clock module.

10.8.1 System Clock Modes

The system clock source is determined during reset. The value of V_{DDSYN} is latched during reset and is expected to remain at that state after reset is negated. If V_{DDSYN} is changed during a reset other than power-on reset, the internal clocks may glitch as the clock source is changed between external clock mode and PLL clock mode. Whenever V_{DDSYN} is changed in reset, an immediate loss of lock condition occurs.

Table 10-6 shows the clock-out frequency to clock-in frequency relationships for the possible clock modes.

Table 10-6. Clock-Out and Clock-In Relationships

Clock Mode	PLL Options[1]
Normal PLL clock mode	$f_{sys} = f_{ref} \times (MFD + 2)/2^{RFD}$
1:1 PLL clock mode	$f_{sys} = f_{ref}$
External clock mode	$f_{sys} = f_{ref}/2$

1. f_{ref} = input reference frequency
   f_{sys} = CLKOUT frequency
   MFD ranges from 0 to 7.
   RFD ranges from 0 to 7.

CAUTION: *XTAL must be tied low in external clock mode when reset is asserted. If it is not, clocks could be suspended indefinitely.*

The external clock is divided by two internally to produce the system clocks.

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10.8.2 System Clocks Generation

In normal PLL clock mode, the default system frequency is two times the reference frequency after reset. The RFD[2:0] and MFD[2:0] bits in SYNCR select the frequency multiplier.

When programming the PLL, do not exceed the maximum system clock frequency listed in the electrical specifications. Use this procedure to accommodate the frequency overshoot that occurs when the MFD bits are changed:

1. Determine the appropriate value for the MFD and RFD fields in SYNCR. The amount of jitter in the system clocks can be minimized by selecting the maximum MFD factor that can be paired with an RFD factor to provide the required frequency.
2. Write a value of RFD (from step **1**) + 1 to the RFD field of SYNCR.
3. Write the MFD value from step **1** to SYNCR.
4. Monitor the LOCK flag in SYNSR. When the PLL achieves lock, write the RFD value from step **1** to the RFD field of SYNCR. This changes the system clocks frequency to the required frequency.

NOTE: *Keep the maximum system clock frequency below the limit given in* ***Section 22. Electrical Specifications****.*

10.8.3 PLL Lock Detection

The lock detect logic monitors the reference frequency and the PLL feedback frequency to determine when frequency lock is achieved. Phase lock is inferred by the frequency relationship, but is not guaranteed. The LOCK flag in SYNSR reflects the PLL lock status. A sticky lock flag, LOCKS, is also provided.

The lock detect function uses two counters. One is clocked by the reference and the other is clocked by the PLL feedback. When the reference counter has counted N cycles, its count is compared to that of the feedback counter. If the feedback counter has also counted N cycles, the process is repeated for N + K counts. Then, if the two counters still match, the lock criteria is relaxed by 1/2 and the system is notified that the PLL has achieved frequency lock.

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After lock is detected, the lock circuit continues to monitor the reference and feedback frequencies using the alternate count and compare process. If the counters do not match at any comparison time, then the LOCK flag is cleared to indicate that the PLL has lost lock. At this point, the lock criteria is tightened and the lock detect process is repeated.

The alternate count sequences prevent false lock detects due to frequency aliasing while the PLL tries to lock. Alternating between tight and relaxed lock criteria prevents the lock detect function from randomly toggling between locked and non-locked status due to phase sensitivities. **Figure 10-6** shows the sequence for detecting locked and non-locked conditions.

In external clock mode, the PLL is disabled and cannot lock.

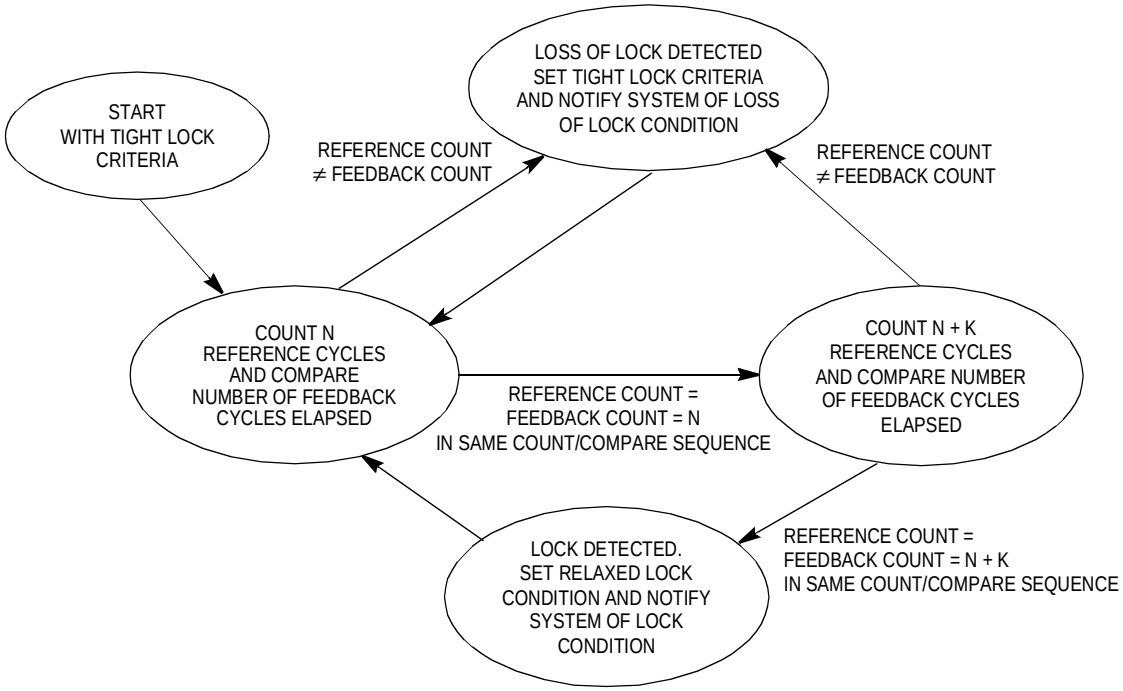

Figure 10-6. Lock Detect Sequence

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10.8.3.1 PLL Loss of Lock Conditions

Once the PLL acquires lock after reset, the LOCK and LOCKS flags are set. If the MFD is changed, or if an unexpected loss of lock condition occurs, the LOCK and LOCKS flags are negated. While the PLL is in the non-locked condition, the system clocks continue to be sourced from the PLL as the PLL attempts to relock. Consequently, during the relocking process, the system clocks frequency is not well defined and may exceed the maximum system frequency, violating the system clock timing specifications.

However, once the PLL has relocked, the LOCK flag is set. The LOCKS flag remains cleared if the loss of lock is unexpected. The LOCKS flag is set when the loss of lock is caused by changing MFD. If the PLL is intentionally disabled during stop mode, then after exit from stop mode, the LOCKS flag reflects the value prior to entering stop mode once lock is regained.

10.8.3.2 PLL Loss of Lock Reset

If the LOLRE bit in SYNCR is set, a loss of lock condition asserts reset. Reset reinitializes the LOCK and LOCKS flags. Therefore, software must read the LOL bit in reset status register (RSR) to determine if a loss of lock caused the reset. See **5.6.2 Reset Status Register**.

To exit reset in PLL mode, the reference must be present, and the PLL must achieve lock.

In external clock mode, the PLL cannot lock. Therefore, a loss of lock condition cannot occur, and the LOLRE bit has no effect.

10.8.4 Loss of Clock Detection

The LOCEN bit in SYNCR enables the loss of clock detection circuit to monitor the input clocks to the phase and frequency detector (PFD). When either the reference or feedback clock frequency falls below the minimum frequency, the loss of clock circuit sets the sticky LOCS flag in SYNSR.

NOTE: *In external clock mode, the loss of clock circuit is disabled.*

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10.8.4.1 Alternate Clock Selection

Depending on which clock source fails, the loss-of-clock circuit switches the system clocks source to the remaining operational clock. The alternate clock source generates the system clocks until reset is asserted. As **Table 10-7** shows, if the reference fails, the PLL goes out of lock and into self-clocked mode (SCM). The PLL remains in SCM until the next reset. When the PLL is operating in SCM, the system frequency depends on the value in the RFD field. The SCM system frequency stated in electrical specifications assumes that the RFD has been programmed to binary 000. If the loss-of-clock condition is due to PLL failure, the PLL reference becomes the system clocks source until the next reset, even if the PLL regains and relocks.

Table 10-7. Loss of Clock Summary

Clock Mode	System Clock Source Before Failure	Reference Failure Alternate Clock Selected by LOC Circuit(1) Until Reset	PLL Failure Alternate Clock Selected by LOC Circuit Until Reset
PLL	PLL	PLL self-clocked mode	PLL reference
External	External clock	None	NA

1. The LOC circuit monitors the reference and feedback inputs to the PFD. See **Figure 10-8**.

A special loss-of-clock condition occurs when both the reference and the PLL fail. The failures may be simultaneous, or the PLL may fail first. In either case, the reference clock failure takes priority and the PLL attempts to operate in SCM. If successful, the PLL remains in SCM until the next reset. If the PLL cannot operate in SCM, the system remains static until the next reset. Both the reference and the PLL must be functioning properly to exit reset.

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Table 10-8. Stop Mode Operation (Sheet 1 of 3)

MODE In	LOCEN	LOCRE	LOLRE	PLL	OSC	FWKUP	Expected PLL Action at Stop	PLL Action During Stop	MODE Out	LOCKS	LOCK	LOCS	Comments
EXT	X	X	X	X	X	X	—	—	EXT	0	0	0	
								Lose reference clock	Stuck	—	—	—	
NRM	0	0	0	Off	Off	0	Lose lock, f.b. clock, reference clock	Regain	NRM	‘LK	1	‘LC	
								No regain	Stuck	—	—	—	
NRM	X	0	0	Off	Off	1	Lose lock, f.b. clock, reference clock	Regain clocks, but don’t regain lock	SCM–> unstable NRM	0–>‘LK	0–>1	1–>‘LC	Block LOCS and LOCKS until clock and lock respectively regain; enter SCM regardless of LOCEN bit until reference regained
								No reference clock regain	SCM–>	0–>	0–>	1–>	Block LOCS and LOCKS until clock and lock respectively regain; enter SCM regardless of LOCEN bit
								No f.b. clock regain	Stuck	—	—	—	
NRM	0	0	0	Off	On	0	Lose lock	Regain	NRM	‘LK	1	‘LC	Block LOCKS from being cleared
								Lose reference clock or no lock regain	Stuck	—	—	—	
								Lose reference clock, regain	NRM	‘LK	1	‘LC	Block LOCKS from being cleared
NRM	0	0	0	Off	On	1	Lose lock	No lock regain	Unstable NRM	0–>‘LK	0–>1	‘LC	Block LOCKS until lock regained
								Lose reference clock or no f.b. clock regain	Stuck	—	—	—	
								Lose reference clock, regain	Unstable NRM	0–>‘LK	0–>1	‘LC	LOCS not set because LOCEN = 0
NRM	0	0	0	On	On	0	—	—	NRM	‘LK	1	‘LC	
								Lose lock or clock	Stuck	—	—	—	
								Lose lock, regain	NRM	0	1	‘LC	
								Lose clock and lock, regain	NRM	0	1	‘LC	LOCS not set because LOCEN = 0
NRM	0	0	0	On	On	1	—	—	NRM	‘LK	1	‘LC	
								Lose lock	Unstable NRM	0	0–>1	‘LC	
								Lose lock, regain	NRM	0	1	‘LC	
								Lose clock	Stuck	—	—	—	
								Lose clock, regain without lock	Unstable NRM	0	0–>1	‘LC	
								Lose clock, regain with lock	NRM	0	1	‘LC	

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Table 10-8. Stop Mode Operation (Sheet 2 of 3)

MODE In	LOCEN	LOCRE	LOLRE	PLL	OSC	FWKUP	Expected PLL Action at Stop	PLL Action During Stop	MODE Out	LOCKS	LOCK	LOCS	Comments
NRM	X	X	1	Off	X	X	Lose lock, f.b. clock, reference clock	RESET	RESET	—	—	—	Reset immediately
NRM	0	0	1	On	On	X	—	—	NRM	‘LK	1	‘LC	
								Lose lock or clock	RESET	—	—	—	Reset immediately
NRM	1	0	0	Off	Off	0	Lose lock, f.b. clock, reference clock	Regain	NRM	‘LK	1	‘LC	REF not entered during stop; SCM entered during stop only during OSC startup
								No regain	Stuck	—	—	—	
NRM	1	0	0	Off	On	0	Lose lock, f.b. clock	Regain	NRM	‘LK	1	‘LC	REF mode not entered during stop
								No f.b. clock or lock regain	Stuck	—	—	—	
								Lose reference clock	SCM	0	0	1	Wakeup without lock
NRM	1	0	0	Off	On	1	Lose lock, f.b. clock	Regain f.b. clock	Unstable NRM	0–>‘LK	0–>1	‘LC	REF mode not entered during stop
								No f.b. clock regain	Stuck	—	—	—	
								Lose reference clock	SCM	0	0	1	Wakeup without lock
NRM	1	0	0	On	On	0	—	—	NRM	‘LK	1	‘LC	
								Lose reference clock	SCM	0	0	1	Wakeup without lock
								Lose f.b. clock	REF	0	X	1	Wakeup without lock
								Lose lock	Stuck	—	—	—	
								Lose lock, regain	NRM	0	1	‘LC	
NRM	1	0	0	On	On	1	—	—	NRM	‘LK	1	‘LC	
								Lose reference clock	SCM	0	0	1	Wakeup without lock
								Lose f.b. clock	REF	0	X	1	Wakeup without lock
								Lose lock	Unstable NRM	0	0–>1	‘LC	
NRM	1	0	1	On	On	X	—	—	NRM	‘LK	1	‘LC	
								Lose lock or clock	RESET	—	—	—	Reset immediately
NRM	1	1	X	Off	X	X	Lose lock, f.b. clock, reference clock	RESET	RESET	—	—	—	Reset immediately
NRM	1	1	0	On	On	0	—	—	NRM	‘LK	1	‘LC	
								Lose clock	RESET	—	—	—	Reset immediately
								Lose lock	Stuck	—	—	—	
								Lose lock, regain	NRM	0	1	‘LC	

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Table 10-8. Stop Mode Operation (Sheet 3 of 3)

MODE In	LOCEN	LOCRE	LOLRE	PLL	OSC	FWKUP	Expected PLL Action at Stop	PLL Action During Stop	MODE Out	LOCKS	LOCK	LOCS	Comments
NRM	1	1	0	On	On	1	—	—	NRM	‘LK	1	‘LC	
								Lose clock	RESET	—	—	—	Reset immediately
								Lose lock	Unstable NRM	0	0–>1	‘LC	
								Lose lock, regain	NRM	0	1	‘LC	
NRM	1	1	1	On	On	X	—	—	NRM	‘LK	1	‘LC	
								Lose clock or lock	RESET	—	—	—	Reset immediately
REF	1	0	0	X	X	X	—	—	REF	0	X	1	
								Lose reference clock	Stuck	—	—	—	
SCM	1	0	0	Off	X	0	PLL disabled	Regain SCM	SCM	0	0	1	Wakeup without lock
SCM	1	0	0	Off	X	1	PLL disabled	Regain SCM	SCM	0	0	1	
SCM	1	0	0	On	On	0	—	—	SCM	0	0	1	Wakeup without lock
								Lose reference clock	SCM				
SCM	1	0	0	On	On	1	—	—	SCM	0	0	1	
								Lose reference clock	SCM				

PLL = PLL enabled during STOP mode. PLL = On when STPMD[1:0] = 00 or 01
OSC = OSC enabled during STOP mode. OSC = On when STPMD[1:0] = 00, 01, or 10
MODES
NRM = normal PLL crystal clock reference or normal PLL external reference or PLL 1:1 mode. During PLL 1:1 or normal external reference mode, the oscillator is never enabled. Therefore, during these modes, refer to the OSC = On case regardless of STPMD values.
EXT = external clock mode
REF = PLL reference mode due to losing PLL clock or lock from NRM mode
SCM = PLL self-clocked mode due to losing reference clock from NRM mode
RESET = immediate reset
LOCKS
‘LK = expecting previous value of LOCKS before entering stop
0–>‘LK = current value is 0 until lock is regained which then will be the previous value before entering stop
0–> = current value is 0 until lock is regained but lock is never expected to regain
LOCS
‘LC = expecting previous value of LOCS before entering stop
1–>‘LC = current value is 1 until clock is regained which then will be the previous value before entering stop
1–> = current value is 1 until clock is regained but CLK is never expected to regain

10.8.4.2 Loss-of-Clock Reset

When a loss-of-clock condition is recognized, reset is asserted if the LOCRE bit in SYNCR is set. The LOCS bit in SYNSR is cleared after reset. Therefore, the LOC bit must be read in RSR to determine that a loss of clock condition occurred. LOCRE has no effect in external clock mode.

To exit reset in PLL mode, the reference must be present, and the PLL must acquire lock.

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10.8.5 Clock Operation During Reset

In external clock mode, the system is static and does not recognize reset until a clock is applied to EXTAL.

In PLL mode, the PLL operates in self-clocked mode (SCM) during reset until the input reference clock to the PLL begins operating within the limits given in the electrical specifications.

If a PLL failure causes a reset, the system enters reset using the reference clock. Then the clock source changes to the PLL operating in SCM. If SCM is not functional, the system becomes static. Alternately, if the LOCEN bit in SYNCR is clear when the PLL fails, the system becomes static. If external reset is asserted, the system cannot enter reset unless the PLL is capable of operating in SCM.

10.8.6 PLL Operation

In PLL mode, the PLL synthesizes the system clocks. The PLL can multiply the reference clock frequency by 2x to 9x, provided that the system clock (CLKOUT) frequency remains within the range listed in electrical specifications. For example, if the reference frequency is 2 MHz, the PLL can synthesize frequencies of 4 MHz to 18 MHz. In addition, the RFD can reduce the system frequency by dividing the output of the PLL. The RFD is not in the feedback loop of the PLL, so changing the RFD divisor does not affect PLL operation.

Figure 10-8 shows the external support circuitry for the crystal oscillator with example component values. Actual component values depend on crystal specifications.

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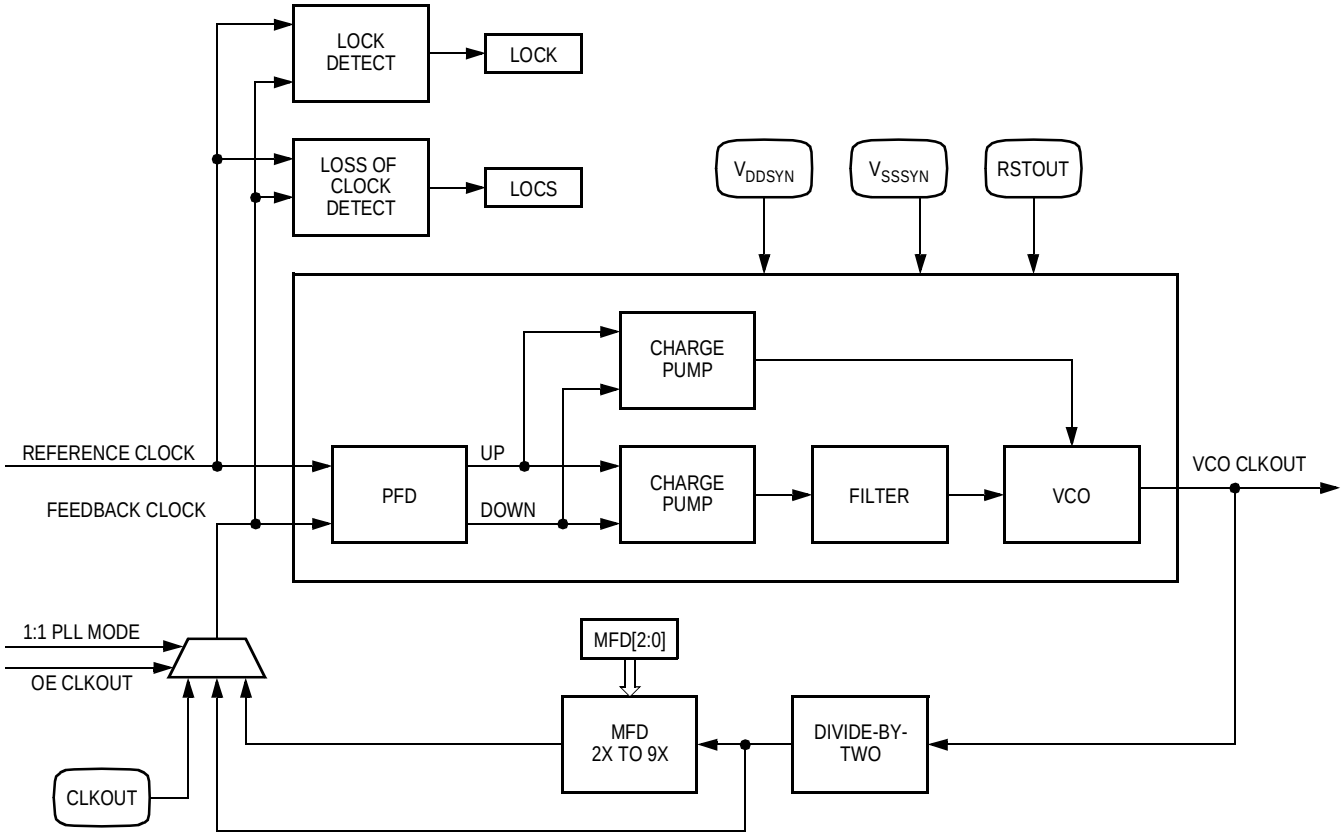

Figure 10-7. PLL Block Diagram

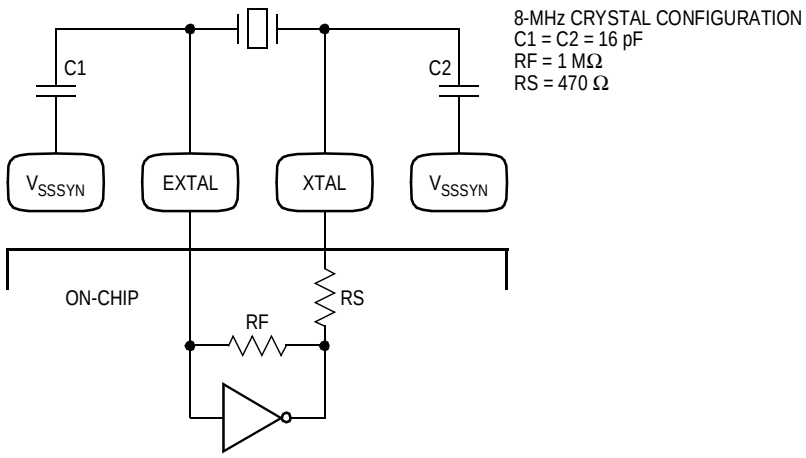

Figure 10-8. Crystal Oscillator Example

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10.8.6.1 Phase and Frequency Detector (PFD)

The PFD is a dual-latch phase-frequency detector. It compares both the phase and frequency of the reference and feedback clocks. The reference clock comes from either the crystal oscillator or an external clock source. The feedback clock comes from:

- CLKOUT in 1:1 PLL mode, or
- VCO output divided by two if CLKOUT is disabled in 1:1 PLL mode, or
- VCO output divided by the MFD in normal PLL mode

When the frequency of the feedback clock equals the frequency of the reference clock, the PLL is frequency-locked. If the falling edge of the feedback clock lags the falling edge of the reference clock, the PFD pulses the UP signal. If the falling edge of the feedback clock leads the falling edge of the reference clock, the PFD pulses the DOWN signal. The width of these pulses relative to the reference clock depends on how much the two clocks lead or lag each other. Once phase lock is achieved, the PFD continues to pulse the UP and DOWN signals for very short durations during each reference clock cycle. These short pulses continually update the PLL and prevent the frequency drift phenomenon known as dead-banding.

10.8.6.2 Charge Pump/Loop Filter

In 1:1 PLL mode, the charge pump uses a fixed current. In normal mode the current magnitude of the charge pump varies with the MFD as shown in **Table 10-9**.

Table 10-9. Charge Pump Current and MFD in Normal Mode Operation

Charge Pump Current	MFD
1X	0 ≤ MFD < 2
2X	2 ≤ MFD < 6
4X	6 ≤ MFD

The UP and DOWN signals from the PFD control whether the charge pump applies or removes charge, respectively, from the loop filter. The filter is integrated on the chip.

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10.8.6.3 Voltage Control Output (VCO)

The voltage across the loop filter controls the frequency of the VCO output. The frequency-to-voltage relationship (VCO gain) is positive, and the output frequency is four times the target system frequency.

10.8.6.4 Multiplication Factor Divider (MFD)

When the PLL is not in 1:1 PLL mode, the MFD divides the output of the VCO and feeds it back to the PFD. The PFD controls the VCO frequency via the charge pump and loop filter such that the reference and feedback clocks have the same frequency and phase. Thus, the frequency of the input to the MFD, which is also the output of the VCO, is the reference frequency multiplied by the same amount that the MFD divides by. For example, if the MFD divides the VCO frequency by six, the PLL is frequency locked when the VCO frequency is six times the reference frequency. The presence of the MFD in the loop allows the PLL to perform frequency multiplication, or synthesis.

In 1:1 PLL mode, the MFD is bypassed, and the effective multiplication factor is one.

10.9 Reset

The clock module can assert a reset when a loss of clock or loss of lock occurs as described in **10.8 Functional Description**.

Reset initializes the clock module registers to a known startup state as described in **10.7 Memory Map and Registers**.

10.10 Interrupts

The clock module does not generate interrupt requests.

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Section 11. Ports Module

11.1 Contents

11.2 Introduction 248
11.3 Signals 249
11.4 Memory Map and Registers 249
11.4.1 Memory Map 250
11.4.2 Register Descriptions 251
11.4.2.1 Port Output Data Registers 251
11.4.2.2 Port Data Direction Registers. 252
11.4.2.3 Port Pin Data/Set Data Registers 253
11.4.2.4 Port Clear Output Data Registers 254
11.4.2.5 Port C/D Pin Assignment Register. 255
11.4.2.6 Port E Pin Assignment Register. 256
11.5 Functional Description 257
11.5.1 Pin Functions 258
11.5.2 Port Digital I/O Timing 259
11.6 Interrupts. 259

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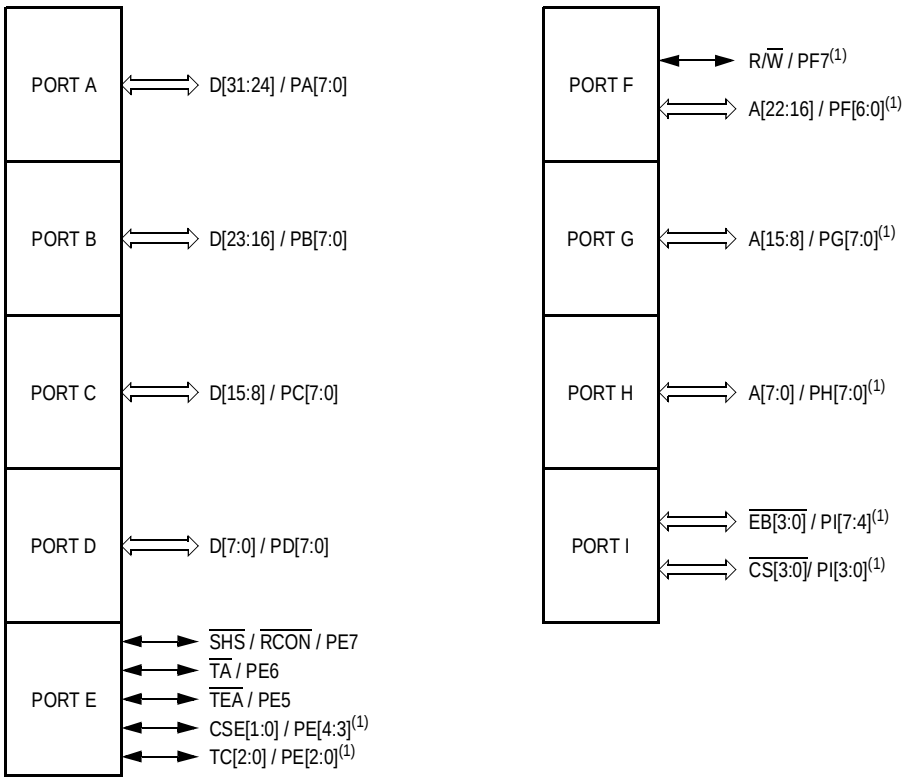
11.2 Introduction

Many of the pins associated with the external interface may be used for several different functions. Their primary function is to provide an external interface to access off-chip resources. When not used for their primary functions, many of the pins may be used as digital input/output (I/O) pins. In some cases, the pin function is set by the operating mode, and the alternate pin functions are not supported.

To facilitate the digital I/O function, these pins are grouped into 8-bit ports. Each port has registers that configure the pins for the desired function, monitor the pins, and control the pins within the ports.



Note 1. These pins are found only on the 144-pin package.

Figure 11-1. Ports Module Block Diagram

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11.3 Signals

See **Table 11-3** in **11.5 Functional Description** for signal location and naming convention.

11.4 Memory Map and Registers

The ports programming model consists of these registers:

- The port output data registers (PORTx) store the data to be driven on the corresponding port pins when the pins are configured for digital output.
- The port data direction registers (DDRx) control the direction of the port pin drivers when the pins are configured for digital I/O.
- Port pin data/set data registers (PORTxP/SETx):
  - Reflect the current state of the port pins
  - Allow for setting individual bits in PORTx
- The port clear output data registers (CLRx) allow for clearing individual bits in PORTx.
- The port pin assignment registers (PCDPAR and PEPAR) control the function of each pin of the C, D, E, I7, and I6 ports.

In emulation mode, accesses to the port registers are ignored and the port access goes external so that emulation hardware can satisfy the port access request. The cycle termination is always provided by the port logic, even in emulation mode.

All port registers are word-, half-word, and byte-accessible and are grouped to allow coherent access to port data register groups. Writing to reserved bits in the port registers has no effect and reading returns 0s.

The I/O ports have a base address of 0x00c0_0000.

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11.4.1 Memory Map

Table 11-1. I/O Port Module Memory Map

Address	Bits 31–24	Bits 23–16	Bits 15–8	Bits 7–0	Access[1]
0x00c0_0000	PORTA	PORTB	PORTC	PORTD	S/U
0x00c0_0004	PORTE	PORTF	PORTG	PORTH	S/U
0x00c0_0008	PORTI	Reserved[2]			S/U
0x00c0_000c	DDRA	DDRB	DDRC	DDRD	S/U
0x00c0_0010	DDRE	DDRF	DDRG	DDRH	S/U
0x00c0_0014	DDRI	Reserved[2]			S/U
0x00c0_0018	PORTAP/SETA	PORTBP/SETB	PORTCP/SETC	PORTDP/SETD	S/U
0x00c0_001c	PORTEP/SETE	PORTFP/SETF	PORTGP/SETG	PORTHP/SETH	S/U
0x00c0_0020	PORTIP/SETI	Reserved[2]			S/U
0x00c0_0024	CLRA	CLRB	CLRC	CLRD	S/U
0x00c0_0028	CLRE	CLRF	CLRG	CLRH	S/U
0x00c0_002c	CLRI	Reserved[2]			S/U
0x00c0_0030	PCDPAR	PEPAR	Reserved[2]		S/U
0x00c0_0034–0x00c0_003c	Reserved[2]				S/U

1. S/U = CPU supervisor or user mode access. User mode accesses to supervisor only addresses have no effect and result in a cycle termination transfer error.
2. Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.

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11.4.2 Register Descriptions

This subsection provides a description of the I/O port registers.

11.4.2.1 Port Output Data Registers

The port output data registers (PORTx) store the data to be driven on the corresponding port x pins when the pins are configured for digital output. Reading PORTx returns the current value in the register, not the port x pin values.

The SETx and CLRx registers also affect the PORTx register bits. To set bits in PORTx, write 1s to the corresponding bits in PORTxP/SETx. To clear bits in PORTx, write 0s to the corresponding bits in CLRx.

PORTx are read/write registers when not in emulation mode. Reset sets PORTx.

Address: 0x00c0_0000 — PORTA
0x00c0_0001 — PORTB
0x00c0_0002 — PORTC
0x00c0_0003 — PORTD
0x00c0_0004 — PORTE
0x00c0_0005 — PORTF
0x00c0_0006 — PORTG
0x00c0_0007 — PORTH
0x00c0_0008 — PORTI

	7	6	5	4	3	2	1	Bit 0
Read: Write:	PORTx7	PORTx6	PORTx5	PORTx4	PORTx3	PORTx2	PORTx1	PORTx0
Reset:	1	1	1	1	1	1	1	1

Figure 11-2. Port Output Data Registers (PORTx)

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11.4.2.2 Port Data Direction Registers

A port data direction register (DDRx) controls the direction of the port x pin drivers when the pins are configured for digital I/O. Setting any bit in DDRx configures the corresponding port x pin as an output. Clearing any bit in DDRx configures the corresponding pin as an input. When a pin is not configured for digital I/O, its corresponding data direction bit has no effect.

DDRx are read/write registers when not in emulation mode. Reset clears DDRx.

Address: 0x00c0_000c — DDRA
0x00c0_000d — DDRB
0x00c0_000e — DDRC
0x00c0_000f — DDRD
0x00c0_0010 — DDRE
0x00c0_0011 — DDRF
0x00c0_0012 — DDRG
0x00c0_0013 — DDRH
0x00c0_0014 — DDRI

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRx7	DDRx6	DDRx5	DDRx4	DDRx3	DDRx2	DDRx1	DDRx0
Reset:	0	0	0	0	0	0	0	0

Figure 11-3. Port Data Direction Registers (DDRx)

DDRx[7:0] — Port x Data Direction Bits
1 = Pin configured as output
0 = Pin configured as input

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11.4.2.3 Port Pin Data/Set Data Registers

Reading a port pin data/set data register (PORTxP/SETx) returns the current state of the port x pins.

Writing 1s to PORTxP/SETx sets the corresponding bits in PORTx. Writing 0s has no effect.

PORTxP/SETx are read/write registers when not in emulation mode.

Address: 0x00c0_0018 — PORTAP/SETA
0x00c0_0019 — PORTBP/SETB
0x00c0_001a — PORTCP/SETC
0x00c0_001b — PORTDP/SETD
0x00c0_001c — PORTEP/SETE
0x00c0_001d — PORTFP/SETF
0x00c0_001e — PORTGP/SETG
0x00c0_001f — PORTHP/SETH
0x00c0_0020 — PORTIP/SETI

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PORTxP7	PORTxP6	PORTxP5	PORTxP4	PORTxP3	PORTxP2	PORTxP1	PORTxP0
Write:	SETx7	SETx6	SETx5	SETx4	SETx3	SETx2	SETx1	SETx0
Reset:	P	P	P	P	P	P	P	P

P = Current pin state

Figure 11-4. Port Pin Data/Set Data Registers (PORTxP/SETx)

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11.4.2.4 Port Clear Output Data Registers

Writing 0s to a port clear output data register (CLRx) clears the corresponding bits in PORTx. Writing 1s has no effect. Reading CLRx returns 0s.

CLRx are read/write registers when not in emulation mode.

Address: 0x00c0_0024 — CLRA
0x00c0_0025 — CLRB
0x00c0_0026 — CLRC
0x00c0_0027 — CLRD
0x00c0_0028 — CLRE
0x00c0_0029 — CLRF
0x00c0_002a — CLRG
0x00c0_002b — CLRH
0x00c0_002c — CLRI

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:	CLRx7	CLRx6	CLRx5	CLRx4	CLRx3	CLRx2	CLRx1	CLRx0
Reset:	0	0	0	0	0	0	0	0

Figure 11-5. Port Clear Output Data Registers (CLRx)

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11.4.2.5 Port C/D Pin Assignment Register

The port C/D pin assignment register (PCDPAR) controls the pin function of ports C, D, I7, and I6.

PCDPAR is a read/write register when not in emulation mode.

Address: 0x00c0_0030

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PCDPA	0	0	0	0	0	0	0
Write:								
Reset:	See note	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Note: Reset state determined during reset configuration. PCDPA = 1 except in single-chip mode or when an external boot device is selected with a 16-bit port size in master mode.

Figure 11-6. Port C, D, I7, and I6 Pin Assignment Register (PCDPAR)

PCDPA — Port C, D, I7, and I6 Pin Assignment Bit
1 = Port C, D, I7, and I6 pins configured for primary function
0 = Port C, D, I7, and I6 pins configured for digital I/O

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11.4.2.6 Port E Pin Assignment Register

The port E pin assignment register (PEPAR) controls the pin function of port E.

PEPAR is a read/write register when not in emulation mode.

Address: 0x00c0_0031

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PEPA7	PEPA6	PEPA5	PEPA4	PEPA3	PEPA2	PEPA1	PEPA0
Reset:	See note							

Note: Reset state determined during reset configuration as shown in **Table 11-2**.

Figure 11-7. Port E Pin Assignment Register (PEPAR)

PEPA[7:0] — Port E Pin Assignment Bits
1 = Port E pins configured for primary function
0 = Port E pins configured for digital I/O

Table 11-2. PEPAR Reset Values

PEPAR	Pin	Master Mode	Single-Chip Mode	Emulation Mode
PEPA7	$\overline{\text{SHS}}$	1	0	1
PEPA6	$\overline{\text{TA}}$	1	0	1
PEPA5	$\overline{\text{TEA}}$	1	0	1
PEPA[4:3]	CSE[1:0]	0	0	1
PEPA[2:0]	TC[2:0]	0	0	1

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11.5 Functional Description

The initial pin function is determined during reset configuration. The pin assignment registers (PCDPAR and PEPAR) allow the user to select between digital I/O or another pin function after reset.

In single-chip mode, all pins are configured as digital I/O by default.

Every digital I/O pin is individually configurable as an input or an output via a data direction register (DDRx).

Every port has an output data register (PORTx) and a pin data register (PORTxP/SETx) to monitor and control the state of its pins. Data written to PORTx is stored and then driven to the corresponding PORTx pins configured as outputs.

Reading PORTx returns the current state of the register regardless of the state of the corresponding pins.

Reading PORTxP returns the current state of the corresponding pins, regardless of whether the pins are input or output.

Every port has a set register (PORTxP/SETx) and a clear register (CLRx) for setting or clearing individual bits in PORTx.

In master mode and emulation mode, ports A and B function as the upper external data bus, D[31:16]. When the PCDPA bit is set, ports C and D function as the lower external data bus, D[15:0]. Ports E–I are configured to support external memory and emulation functions.

In master mode, the function of $\overline{\text{EB}}$[3:2] is determined by the PCDPA bit. The function of $\overline{\text{CS}}$[3:0] is determined by the individual chip select enable (CSENx) bits.

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11.5.1 Pin Functions

Table 11-3. Ports A–I Supported Pin Functions

Pin	Port	Master Mode	Single-Chip Mode	Emulation Mode(1)
D[31:24]	A	D[31:24] (I/O)	PA[7:0] (I/O)	D[31:24] (I/O)
D[23:16]	B	D[23:16] (I/O)	PB[7:0](I/O)	D[23:16](I/O)
D[15:8]	C	D[15:8] (I/O) (PCDPA = 1) or PC[7:0] (I/O) (PCDPA = 0)	PC[7:0] (I/O) (PCDPA = 0)(2)	D[15:8] (I/O) (PCDPA = 1)
D[7:0]	D	D[7:0] (I/O) (PCDPA = 1) or PD[7:0] (I/O) (PCDPA = 0)	PD[7:0] (I/O) (PCDPA = 0)(2)	D[7:0] (I/O) (PCDPA = 1)
$\overline{SHS}$(3)	E	$\overline{SHS}$ (O) (PEPAR7 = 1) or PE7 (I/O) (PEPAR7 = 0)	PE7 (I/O) (PEPAR7 = 0)(4)	$\overline{SHS}$ (O) (PEPAR7 = 1)
$\overline{TA}$		$\overline{TA}$ (I) (PEPAR6 = 1) or PE6 (I/O) (PEPAR6 = 0)	PE6 (I/O) (PEPAR6 = 0)(4)	$\overline{TA}$ (I) (PEPAR6 = 1)
$\overline{TEA}$		$\overline{TEA}$ (I) (PEPAR5 = 1) or PE5 (I/O) (PEPAR5 = 0)	PE5 (I/O) (PEPAR5 = 0)(4)	$\overline{TEA}$ (I) (PEPAR5 = 1)
CSE[1:0]		CSE[1:0] (O) (PEPAR[4:3] = 1) or PE[4:3] (I/O) (PEPAR[4:3] = 0)	PE[4:3] (I/O) (PEPAR[4:3] = 0)(4)	CSE[1:0] (O) (PEPAR[4:3] = 1)
TC[2:0]		TC[2:0] (O) (PEPAR[2:0] = 1) or PE[2:0] (I/O) (PEPAR[2:0] = 0)	PE[2:0] (I/O) (PEPAR[2:0] = 0)(4)	TC[2:0] (O) (PEPAR[2:0] = 1)
R/$\overline{W}$	F	R/$\overline{W}$ (O)	PF7 (I/O)	R/$\overline{W}$ (O)
A[22:16]		A[22:16] (O)	PF[6:0] (I/O)	A[22:16] (O)
A[15:8]	G	A[15:8] (O)	PG[7:0] (I/O)	A[15:8] (O)
A[7:0]	H	A[7:0] (O)	PH[7:0] (I/O)	A[7:0] (O)
$\overline{EB[3:2]}$	I	$\overline{EB[3:2]}$ (O) (PCDPA = 1) or PI[7:6] (I/O) (PCDPA = 0)	PI[7:6] (I/O) (PCDPA = 0)(2)	$\overline{EB[3:2]}$ (O) (PCDPA = 1)
$\overline{EB[1:0]}$		$\overline{EB[1:0]}$ (O)	PI[5:4] (I/O)	$\overline{EB[1:0]}$ (O)
$\overline{CS[3:0]}$		$\overline{CS[3:0]}$ (O) (CSENx = 1) or PI[3:0] (I/O) (CSENx = 0)	PI[3:0] (I/O)(5)	$\overline{CS[3:0]}$ (O)(5)

1. Digital I/O pin function provided by port replacement unit.
2. Writing PCDPA = 1 has an undefined pin operation for D[31:16] and $\overline{EB[3:2]}$ in single-chip mode.
3. This pin functions as the reset configuration override enable (RCON) during reset.
4. Writing PEPAx = 1 has an undefined pin operation for port E pins in single-chip mode.
5. CSENx has no effect on selecting $\overline{CS}$[3:0] pin function in single-chip or emulation modes.

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11.5.2 Port Digital I/O Timing

Input data on all pins configured as digital I/O is synchronized to the rising edge of CLKOUT. See **Figure 11-8**.

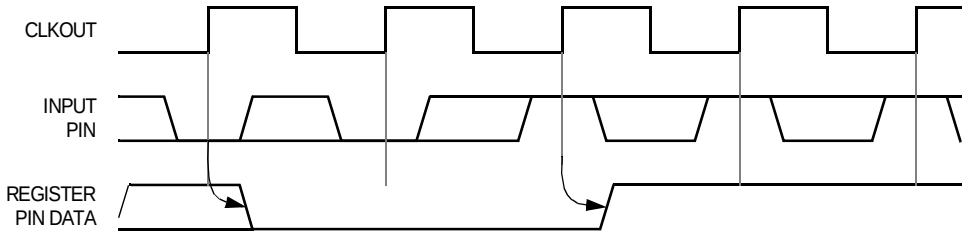

Figure 11-8. Digital Input Timing

Data written to PORTx of any pin configured as a digital output is immediately driven to its respective pin. See **Figure 11-9**.

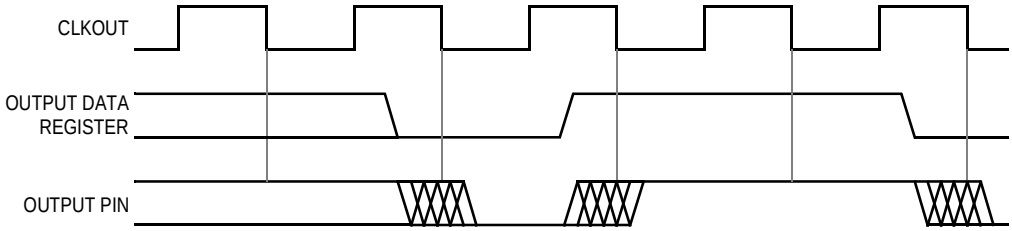

Figure 11-9. Digital Output Timing

11.6 Interrupts

The ports module does not generate interrupt requests.

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Ports Module

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Section 12. Edge Port Module (EPORT)

12.1 Contents

12.2 Introduction 261
12.3 Low-Power Mode Operation 262
12.3.1 Wait and Doze Modes 262
12.3.2 Stop Mode 263
12.4 Interrupt/General-Purpose I/O Pin Descriptions 263
12.5 Memory Map and Registers 263
12.5.1 Memory Map 263
12.5.2 Registers 264
12.5.2.1 EPORT Pin Assignment Register 264
12.5.2.2 EPORT Data Direction Register. 266
12.5.2.3 Edge Port Interrupt Enable Register 267
12.5.2.4 Edge Port Data Register 268
12.5.2.5 Edge Port Pin Data Register 268
12.5.2.6 Edge Port Flag Register. 269

12.2 Introduction

The edge port module (EPORT) has eight external interrupt pins. Each pin can be configured individually as a low level-sensitive interrupt pin, an edge-detecting interrupt pin (rising edge, falling edge, or both), or a general-purpose input/output (I/O) pin. See **Figure 12-1**.

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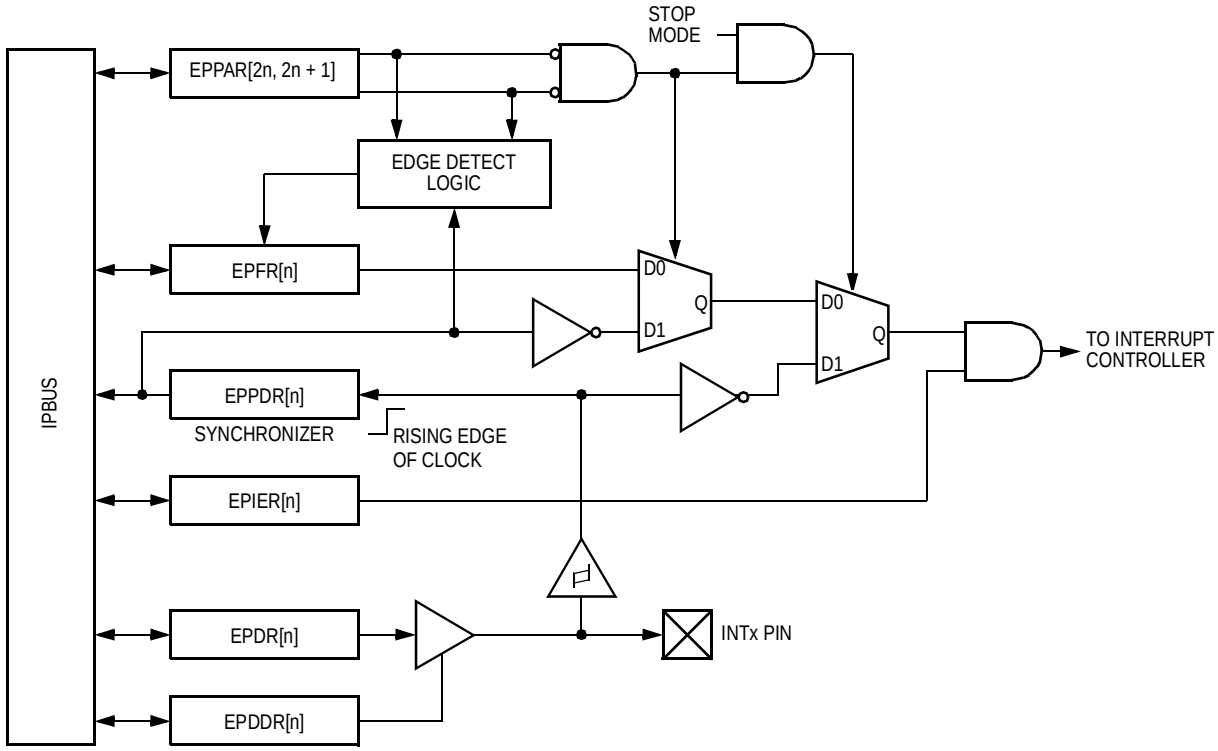

Figure 12-1. EPORT Block Diagram

12.3 Low-Power Mode Operation

This subsection describes the operation of the EPORT module in low-power modes.

12.3.1 Wait and Doze Modes

In wait and doze modes, the EPORT module continues to operate normally and may be configured to exit the low-power modes by generating an interrupt request on either a selected edge or a low level on an external pin.

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12.3.2 Stop Mode

In stop mode, there are no clocks available to perform the edge-detect function. Only the level-detect logic is active (if configured) to allow any low level on the external interrupt pin to generate an interrupt (if enabled) to exit stop mode.

NOTE: *The input pin synchronizer is bypassed for the level-detect logic since no clocks are available.*

12.4 Interrupt/General-Purpose I/O Pin Descriptions

All pins default to general-purpose input pins at reset. The pin value is synchronized to the rising edge of CLKOUT when read from the EPORT pin data register (EPPDR). The values used in the edge/level detect logic are also synchronized to the rising edge of CLKOUT. These pins use Schmitt triggered input buffers which have built in hysteresis designed to decrease the probability of generating false edge-triggered interrupts for slow rising and falling input signals.

12.5 Memory Map and Registers

This subsection describes the memory map and register structure.

12.5.1 Memory Map

Refer to **Table 12-1** for a description of the EPORT memory map. The EPORT has a base address of 0x00c6_0000.

Table 12-1. Edge Port Module Memory Map

Address	Bits 15–8	Bits 7–0	Access(1)
0x00c6_0000	EPORT pin assignment register (EPPAR)		S
0x00c6_0002	EPORT data direction register (EPDDR)	EPORT interrupt enable register (EPIER)	S
0x00c6_0004	EPORT data register (EPDR)	EPORT pin data register (EPPDR)	S/U
0x00c6_0006	EPORT flag register (EPFR)	Reserved(2)	S/U

1. S = CPU supervisor mode access only. S/U = CPU supervisor or user mode access. User mode accesses to supervisor only addresses have no effect and result in a cycle termination transfer error.
2. Writing to reserved address locations has no effect, and reading returns 0s.

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12.5.2 Registers

The EPORT programming model consists of these registers:

- The EPORT pin assignment register (EPPAR) controls the function of each pin individually.
- The EPORT data direction register (EPDDR) controls the direction of each one of the pins individually.
- The EPORT interrupt enable register (EPIER) enables interrupt requests for each pin individually.
- The EPORT data register (EPDR) holds the data to be driven to the pins.
- The EPORT pin data register (EPPDR) reflects the current state of the pins.
- The EPORT flag register (EPFR) individually latches EPORT edge events.

12.5.2.1 EPORT Pin Assignment Register

Address: 0x00c6_0000 and 0x00c6_0001

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	EPPA7		EPPA6		EPPA5		EPPA4	
Reset:	0	0	0	0	0	0	0	0
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EPPA3		EPPA2		EPPA1		EPPA0	
Reset:	0	0	0	0	0	0	0	0

Figure 12-2. EPORT Pin Assignment Register (EPPAR)

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EPPA[7:0] — EPORT Pin Assignment Select Fields

The read/write EPPAx fields configure EPORT pins for level detection and rising and/or falling edge detection as **Table 12-2** shows.

Pins configured as level-sensitive are inverted so that a logic 0 on the external pin represents a valid interrupt request. Level-sensitive interrupt inputs are not latched. To guarantee that a level-sensitive interrupt request is acknowledged, the interrupt source must keep the signal asserted until acknowledged by software.

Pins configured as edge-triggered are latched and need not remain asserted for interrupt generation. A pin configured for edge detection is monitored regardless of its configuration as input or output.

Table 12-2. EPPAx Field Settings

EPPAx	Pin Configuration
00	Pin INTx level-sensitive
01	Pin INTx rising edge triggered
10	Pin INTx falling edge triggered
11	Pin INTx both falling edge and rising edge triggered

Interrupt requests generated in the EPORT module can be masked by the interrupt controller module. EPPAR functionality is independent of the selected pin direction.

Reset clears the EPPAx fields.

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12.5.2.2 EPORT Data Direction Register

Address: 0x00c6_0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EPDD7	EPDD6	EPDD5	EPDD4	EPDD3	EPDD2	EPDD1	EPDD0
Reset:	0	0	0	0	0	0	0	0

Figure 12-3. EPORT Data Direction Register (EPDDR)

EPDD[7:0] — Edge Port Data Direction Bits

Setting any bit in the EPDDR configures the corresponding pin as an output. Clearing any bit in EPDDR configures the corresponding pin as an input. Pin direction is independent of the level/edge detection configuration. Reset clears EPDD[7:0].

To use an EPORT pin as an external interrupt request source, its corresponding bit in EPDDR must be clear. Software can generate interrupt requests by programming the EPORT data register when the EPDDR selects output.

1 = Corresponding EPORT pin configured as output
0 = Corresponding EPORT pin configured as input

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12.5.2.3 Edge Port Interrupt Enable Register

Address: 0x00c6_0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EPIE7	EPIE6	EPIE5	EPIE4	EPIE3	EPIE2	EPIE1	EPIE0
Reset:	0	0	0	0	0	0	0	0

Figure 12-4. EPORT Port Interrupt Enable Register (EPIER)

EPIE[7:0] — Edge Port Interrupt Enable Bits

The read/write EPIE[7:0] bits enable EPORT interrupt requests. If a bit in EPIER is set, EPORT generates an interrupt request when:

- The corresponding bit in the EPORT flag register (EPFR) is set or later becomes set, or
- The corresponding pin level is low and the pin is configured for level-sensitive operation

Clearing a bit in EPIER negates any interrupt request from the corresponding EPORT pin. Reset clears EPIE[7:0].

1 = Interrupt requests from corresponding EPORT pin enabled
0 = Interrupt requests from corresponding EPORT pin disabled

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12.5.2.4 Edge Port Data Register

Address: 0x00c6_0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EPD7	EPD6	EPD5	EPD4	EPD3	EPD2	EPD1	EPD0
Reset:	1	1	1	1	1	1	1	1

Figure 12-5. EPORT Port Data Register (EPDR)

EPD[7:0] — Edge Port Data Bits

Data written to EPDR is stored in an internal register; if any pin of the port is configured as an output, the bit stored for that pin is driven onto the pin. Reading EDPR returns the data stored in the register. Reset sets EPD[7:0].

12.5.2.5 Edge Port Pin Data Register

Address: 0x00c6_0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	EPPD7	EPPD6	EPPD5	EPPD4	EPPD3	EPPD2	EPPD1	EPPD0
Write:								
Reset:	P	P	P	P	P	P	P	P

= Writes have no effect and the access terminates without a transfer error exception.

P = Current pin state

Figure 12-6. EPORT Port Pin Data Register (EPPDR)

EPPD[7:0] — Edge Port Pin Data Bits

The read-only EPPDR reflects the current state of the EPORT pins. Writing to EPPDR has no effect, and the write cycle terminates normally. Reset does not affect EPPDR.

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12.5.2.6 Edge Port Flag Register

Address: 0x00c6_0006

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EPF7	EPF6	EPF5	EPF4	EPF3	EPF2	EPF1	EPF0
Reset:	0	0	0	0	0	0	0	0

Figure 12-7. EPORT Port Flag Register (EPFR)

EPF[7:0] — Edge Port Flag Bits

When an EPORT pin is configured for edge triggering, its corresponding read/write bit in EPFR indicates that the selected edge has been detected. Reset clears EPF[7:0].

1 = Selected edge for INTx pin has been detected.
0 = Selected edge for INTx pin has not been detected.

Bits in this register are set when the selected edge is detected on the corresponding pin. A bit remains set until cleared by writing a 1 to it. Writing 0 has no effect. If a pin is configured as level-sensitive (EPPARx = 00), pin transitions do not affect this register.

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Edge Port Module (EPORT)

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Section 13. Watchdog Timer Module

13.1 Contents

13.2 Introduction 271
13.3 Modes of Operation 272
13.3.1 Wait Mode 272
13.3.2 Doze Mode 272
13.3.3 Stop Mode 272
13.3.4 Debug Mode 272
13.4 Block Diagram 273
13.5 Signals 273
13.6 Memory Map and Registers 274
13.6.1 Memory Map 274
13.6.2 Registers 274
13.6.2.1 Watchdog Control Register 275
13.6.2.2 Watchdog Modulus Register 277
13.6.2.3 Watchdog Count Register 278
13.6.2.4 Watchdog Service Register 279

13.2 Introduction

The watchdog timer is a 16-bit timer used to help software recover from runaway code. The watchdog timer has a free-running down-counter (watchdog counter) that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

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13.3 Modes of Operation

This subsection describes the operation of the watchdog timer in low-power modes and debug mode of operation.

13.3.1 Wait Mode

In wait mode with the WAIT bit set in the watchdog control register (WCR), watchdog timer operation stops. In wait mode with the WAIT bit clear, the watchdog timer continues to operate normally.

13.3.2 Doze Mode

In doze mode with the DOZE bit set in WCR, watchdog timer module operation stops. In doze mode with the DOZE bit clear, the watchdog timer continues to operate normally.

13.3.3 Stop Mode

The watchdog operation stops in stop mode. When stop mode is exited, the watchdog operation continues operation from the state it was in prior to entering stop mode.

13.3.4 Debug Mode

In debug mode with the DBG bit set in WCR, watchdog timer module operation stops. In debug mode with the DBG bit clear, the watchdog timer continues to operate normally. When debug mode is exited, watchdog timer operation continues from the state it was in before entering debug mode, but any updates made in debug mode remain.

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13.4 Block Diagram

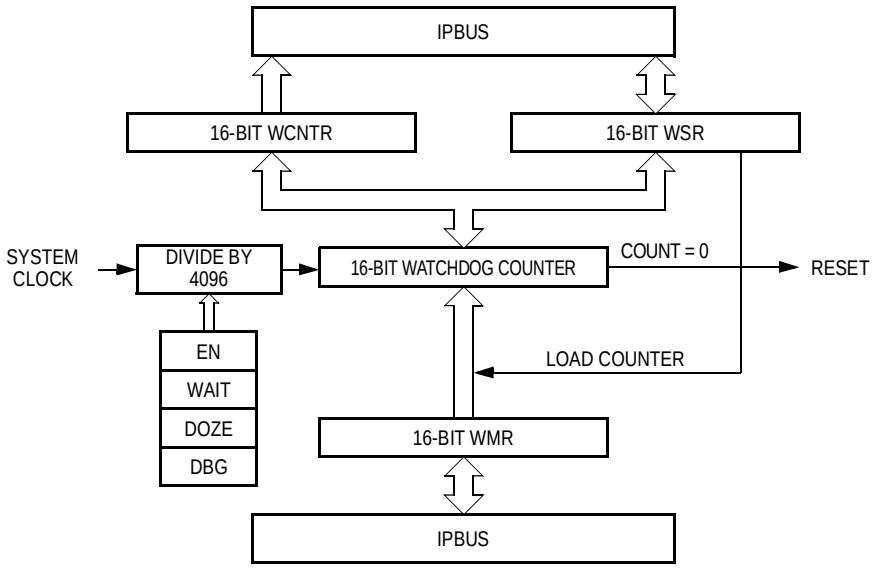

Figure 13-1. Watchdog Timer Block Diagram

13.5 Signals

The watchdog timer module has no off-chip signals.

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13.6 Memory Map and Registers

This subsection describes the memory map and registers for the watchdog timer. The watchdog timer has a base address of 0x00c7_0000.

13.6.1 Memory Map

Refer to **Table 13-1** for an overview of the watchdog memory map.

Table 13-1. Watchdog Timer Module Memory Map

Address	Bits 15–8	Bits 7–0	Access[1]
0x00c7_0000	Watchdog control register (WCR)		S
0x00c7_0002	Watchdog modulus register (WMR)		S
0x00c7_0004	Watchdog count register (WCNTR)		S/U
0x00c7_0006	Watchdog service register (WSR)		S/U

1. S = CPU supervisor mode access only. S/U = CPU supervisor or user mode access. User mode accesses to supervisor only addresses have no effect and result in a cycle termination transfer error.

13.6.2 Registers

The watchdog timer programming model consists of these registers:

- The watchdog control register (WCR) configures watchdog timer operation.
- The watchdog modulus register (WMR) determines the timer modulus reload value.
- The watchdog count register (WCNTR) provides visibility to the watchdog counter value.
- The watchdog service register (WSR) requires a service sequence to prevent reset.

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13.6.2.1 Watchdog Control Register

The 16-bit read/write watchdog control register (WCR) configures watchdog timer operation.

Address: 0x00c7_0000 and 0x00c7_0001

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	WAIT	DOZE	DBG	EN
Write:								
Reset:	0	0	0	0	1	1	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 13-2. Watchdog Control Register (WCR)

WAIT — Wait Mode Bit

The read-always, write-once WAIT bit controls the function of the watchdog timer in wait mode. Once written, the WAIT bit is not affected by further writes except in debug mode. Reset sets WAIT.

1 = Watchdog timer stopped in wait mode
0 = Watchdog timer not affected in wait mode

DOZE — Doze Mode Bit

The read-always, write-once DOZE bit controls the function of the watchdog timer in doze mode. Once written, the DOZE bit is not affected by further writes except in debug mode. Reset sets DOZE.

1 = Watchdog timer stopped in doze mode
0 = Watchdog timer not affected in doze mode

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DBG — Debug Mode Bit

The read-always, write-once DBG bit controls the function of the watchdog timer in debug mode. Once written, the DBG bit is not affected by further writes except in debug mode.

During debug mode, watchdog timer registers can be written and read normally. When debug mode is exited, timer operation continues from the state it was in before entering debug mode, but any updates made in debug mode remain. If a write-once register is written for the first time in debug mode, the register is still writable when debug mode is exited.

1 = Watchdog timer stopped in debug mode
0 = Watchdog timer not affected in debug mode

NOTE: *Changing the DBG bit from 1 to 0 during debug mode starts the watchdog timer. Changing the DBG bit from 0 to 1 during debug mode stops the watchdog timer.*

EN — Watchdog Enable Bit

The read-always, write-once EN bit enables the watchdog timer. Once written, the EN bit is not affected by further writes except in debug mode. When the watchdog timer is disabled, the watchdog counter and prescaler counter are held in a stopped state.

1 = Watchdog timer enabled
0 = Watchdog timer disabled

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13.6.2.2 Watchdog Modulus Register

Address: 0x00c7_0002 and 0x00c7_0003

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8
Reset:	1	1	1	1	1	1	1	1

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0
Reset:	1	1	1	1	1	1	1	1

Figure 13-3. Watchdog Modulus Register (WMR)

WM[15:0] — Watchdog Modulus Field

The read-always, write-once WM[15:0] field contains the modulus that is reloaded into the watchdog counter by a service sequence. Once written, the WM[15:0] field is not affected by further writes except in debug mode. Writing to WMR immediately loads the new modulus value into the watchdog counter. The new value is also used at the next and all subsequent reloads. Reading WMR returns the value in the modulus register.

Reset initializes the WM[15:0] field to 0xFFFF.

NOTE: *The prescaler counter is reset anytime a new value is loaded into the watchdog counter and also during reset.*

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13.6.2.3 Watchdog Count Register

Address: 0x00c7_0004 and 0x00c7_0005

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	WC15	WC14	WC13	WC12	WC11	WC10	WC9	WC8
Write:								
Reset:	1	1	1	1	1	1	1	1

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0
Write:								
Reset:	1	1	1	1	1	1	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 13-4. Watchdog Count Register (WCNTR)

WC[15:0] — Watchdog Count Field

The read-only WC[15:0] field reflects the current value in the watchdog counter. Reading the 16-bit WCNTR with two 8-bit reads is not guaranteed to return a coherent value. Writing to WCNTR has no effect, and write cycles are terminated normally.

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13.6.2.4 Watchdog Service Register

When the watchdog timer is enabled, writing 0x5555 and then 0xAAAA to the watchdog service register (WSR) before the watchdog counter times out prevents a reset. If WSR is not serviced before the timeout, the watchdog timer sends a signal to the reset controller module which sets the WDR bit and asserts a system reset.

Both writes must occur in the order listed before the timeout, but any number of instructions can be executed between the two writes. However, writing any value other than 0x5555 or 0xAAAA to WSR resets the servicing sequence, requiring both values to be written to keep the watchdog timer from causing a reset.

Address: 0x00c7_0006 and 0x00c7_0007

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	WS15	WS14	WS13	WS12	WS11	WS10	WS9	WS8
Reset:	0	0	0	0	0	0	0	0
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WS7	WS6	WS5	WS4	WS3	WS2	WS1	WS0
Reset:	0	0	0	0	0	0	0	0

Figure 13-5. Watchdog Service Register (WSR)

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Watchdog Timer Module

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Section 14. Programmable Interrupt Timer Modules (PIT1 and PIT2)

14.1 Contents

14.2 Introduction 282
14.3 Block Diagram 282
14.4 Modes of Operation 283
14.4.1 Wait Mode 283
14.4.2 Doze Mode 283
14.4.3 Stop Mode 283
14.4.4 Debug Mode 283
14.5 Signals 283
14.6 Memory Map and Registers 284
14.6.1 Memory Map 284
14.6.2 Registers 284
14.6.2.1 PIT Control and Status Register 285
14.6.2.2 PIT Modulus Register 288
14.6.2.3 PIT Count Register 289
14.7 Functional Description 290
14.7.1 Set-and-Forget Timer Operation 290
14.7.2 Free-Running Timer Operation 291
14.7.3 Timeout Specifications 291
14.8 Interrupt Operation 292

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14.2 Introduction

The programmable interrupt timer (PIT) is a 16-bit timer that provides precise interrupts at regular intervals with minimal processor intervention. The timer can either count down from the value written in the modulus latch, or it can be a free-running down-counter.

This device has two programmable interrupt timers. PIT1 has a base address located at 0x00c8_0000. PIT2 base address is 0x00c9_0000.

14.3 Block Diagram

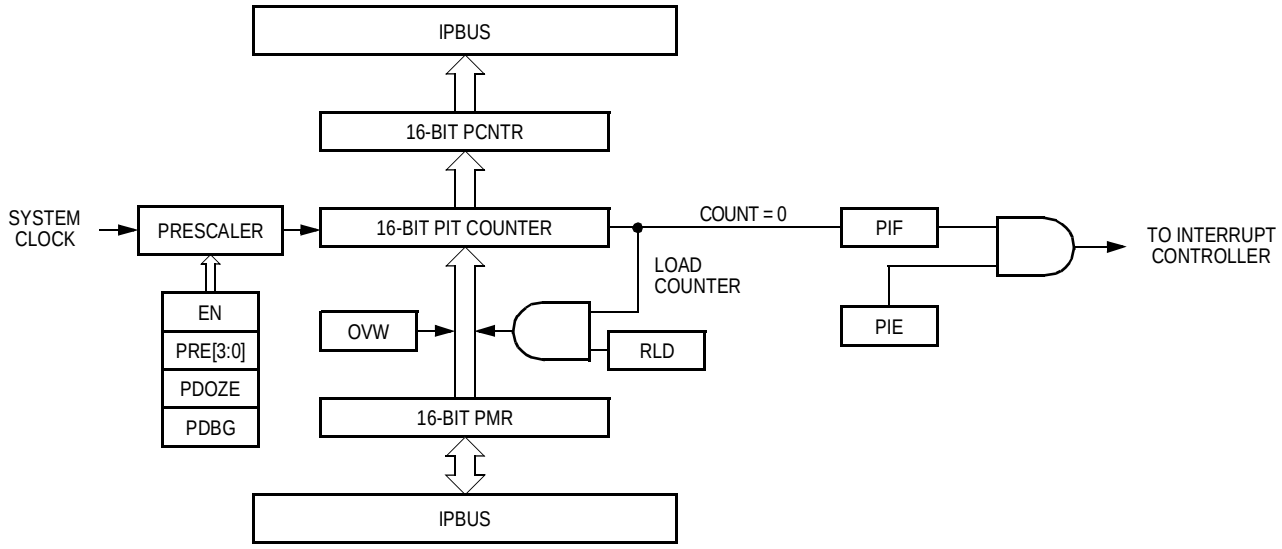

Figure 14-1. PIT Block Diagram

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14.4 Modes of Operation

This subsection describes the three low-power modes and the debug mode.

14.4.1 Wait Mode

In wait mode, the PIT module continues to operate normally and can be configured to exit the low-power mode by generating an interrupt request.

14.4.2 Doze Mode

In doze mode with the PDOZE bit set in the PIT control and status register (PCSR), PIT module operation stops. In doze mode with the PDOZE bit clear, doze mode does not affect PIT operation. When doze mode is exited, PIT operation continues from the state it was in before entering doze mode.

14.4.3 Stop Mode

In stop mode, the system clock is absent, and PIT module operation stops.

14.4.4 Debug Mode

In debug mode with the PDBG bit set in PCSR, PIT module operation stops. In debug mode with the PDBG bit clear, debug mode does not affect PIT operation. When debug mode is exited, PIT operation continues from the state it was in before entering debug mode, but any updates made in debug mode remain.

14.5 Signals

The PIT module has no off-chip signals.

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14.6 Memory Map and Registers

This subsection describes the memory map and register structure for PIT1 and PIT2.

14.6.1 Memory Map

Refer to **Table 14-1** for a description of the memory map.

This device has two programmable interrupt timers. PIT1 has a base address located at 0x00c8_0000. PIT2 base address is 0x00c9_0000.

Table 14-1. Programmable Interrupt Timer Modules Memory Map

PIT1 Address	PIT2 Address	Bits 15–8	Bits 7–0	Access(1)
0x00c8_0000	0x00c9_0000	PIT control and status register (PCSR)		S
0x00c8_0002	0x00c9_0002	PIT modulus register (PMR)		S
0x00c8_0004	0x00c9_0004	PIT count register (PCNTR)		S/U
0x00c8_0006	0x00c9_0006	Unimplemented(2)		—

1. S = CPU supervisor mode access only. S/U = CPU supervisor or user mode access. User mode accesses to supervisor only addresses have no effect and result in a cycle termination transfer error.
2. Accesses to unimplemented address locations have no effect and result in a cycle termination transfer error.

14.6.2 Registers

The PIT programming model consists of these registers:

- The PIT control and status register (PCSR) configures the timer's operation.
- The PIT modulus register (PMR) determines the timer modulus reload value.
- The PIT count register (PCNTR) provides visibility to the counter value.

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14.6.2.1 PIT Control and Status Register

Address: PIT1 — 0x00c8_0000 and 0x00c8_0001
PIT2 — 0x00c9_0000 and 0x00c9_0001

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	0	0	PRE3	PRE2	PRE1	PRE0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	PDOZE	PDBG	OVW	PIE	PIF	RLD	EN
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 14-2. PIT Control and Status Register (PCSR)

PRE[3:0] — Prescaler Bits

The read/write PRE[3:0] bits select the system clock divisor to generate the PIT clock as **Table 14-2** shows.

To accurately predict the timing of the next count, change the PRE[3:0] bits only when the enable bit (EN) is clear. Changing the PRE[3:0] resets the prescaler counter. System reset and the loading of a new value into the counter also reset the prescaler counter. Setting the EN bit and writing to PRE[3:0] can be done in this same write cycle. Clearing the EN bit stops the prescaler counter.

PDOZE — Doze Mode Bit

The read/write PDOZE bit controls the function of the PIT in doze mode. Reset clears PDOZE.

1 = PIT function stopped in doze mode
0 = PIT function not affected in doze mode

When doze mode is exited, timer operation continues from the state it was in before entering doze mode.

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Table 14-2. Prescaler Select Encoding

PRE[3:0]	System Clock Divisor
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1,024
1011	2,048
1100	4,096
1101	8,192
1110	16,384
1111	32,768

PDBG — Debug Mode Bit

The read/write PDBG bit controls the function of the PIT in debug mode. Reset clears PDBG.

1 = PIT function stopped in debug mode
0 = PIT function not affected in debug mode

During debug mode, register read and write accesses function normally. When debug mode is exited, timer operation continues from the state it was in before entering debug mode, but any updates made in debug mode remain.

NOTE: *Changing the PDBG bit from 1 to 0 during debug mode starts the PIT timer. Likewise, changing the PDBG bit from 0 to 1 during debug mode stops the PIT timer.*

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OVW — Overwrite Bit

The read/write OVW bit enables writing to PMR to immediately overwrite the value in the PIT counter.

1 = Writing PMR immediately replaces value in PIT counter.
0 = Value in PMR replaces value in PIT counter when count reaches 0x0000.

PIE — PIT Interrupt Enable Bit

The read/write PIE bit enables the PIF flag to generate interrupt requests.

1 = PIF interrupt requests enabled
0 = PIF interrupt requests disabled

PIF — PIT Interrupt Flag

The read/write PIF flag is set when the PIT counter reaches 0x0000. Clear PIF by writing a 1 to it or by writing to PMR. Writing 0 has no effect. Reset clears PIF.

1 = PIT count has reached 0x0000.
0 = PIT count has not reached 0x0000.

RLD — Reload Bit

The read/write RLD bit enables loading the value of PMR into the PIT counter when the count reaches 0x0000.

1 = Counter reloaded from PMR on count of 0x0000
0 = Counter rolls over to 0xFFFF on count of 0x0000

EN — PIT Enable Bit

The read/write EN bit enables PIT operation. When the PIT is disabled, the counter and prescaler are held in a stopped state.

1 = PIT enabled
0 = PIT disabled

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14.6.2.2 PIT Modulus Register

The 16-bit read/write PIT modulus register (PMR) contains the timer modulus value for loading into the PIT counter when the count reaches 0x0000 and the RLD bit is set.

When the OVW bit is set, PMR is transparent, and the value written to PMR is immediately loaded into the PIT counter. The prescaler counter is reset anytime a new value is loaded into the PIT counter and also during reset. Reading the PMR returns the value written in the modulus latch. Reset initializes PMR to 0xFFFF.

Address: PIT1 — 0x00c8_0002 and 0x00c8_0003
PIT2 — 0x00c9_0002 and 0x00c9_0003

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	PM15	PM14	PM13	PM12	PM11	PM10	PM9	PM8
Reset:	1	1	1	1	1	1	1	1

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0
Reset:	1	1	1	1	1	1	1	1

Figure 14-3. PIT Modulus Register (PMR)

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14.6.2.3 PIT Count Register

The 16-bit, read-only PIT control register (PCNTR) contains the counter value. Reading the 16-bit counter with two 8-bit reads is not guaranteed to be coherent. Writing to PCNTR has no effect, and write cycles are terminated normally.

Address: PIT1 — 0x00c8_0004 and 0x00c8_0005
PIT2 — 0x00c9_0004 and 0x00c9_0005

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
Write:								
Reset:	1	1	1	1	1	1	1	1

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Write:								
Reset:	1	1	1	1	1	1	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 14-4. PIT Count Register (PCNTR)

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14.7 Functional Description

This subsection describes the PIT functional operation.

14.7.1 Set-and-Forget Timer Operation

This mode of operation is selected when the RLD bit in the PCSR register is set.

When the PIT counter reaches a count of 0x0000, the PIF flag is set in PCSR. The value in the modulus latch is loaded into the counter, and the counter begins decrementing toward 0x0000. If the PIE bit is set in PCSR, the PIF flag issues an interrupt request to the CPU.

When the OVW bit is set in PCSR, the counter can be directly initialized by writing to PMR without having to wait for the count to reach 0x0000.

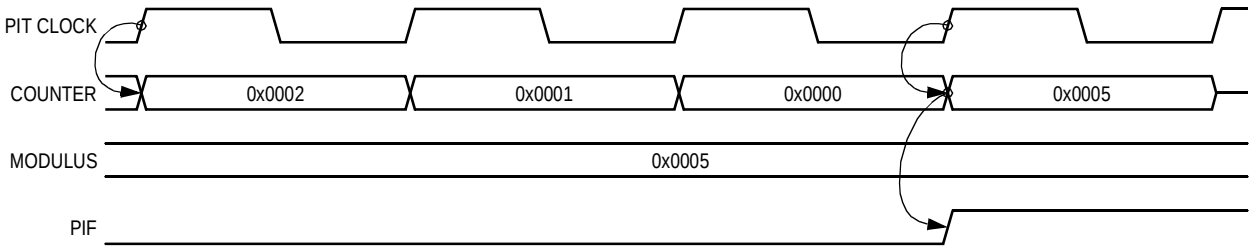

Figure 14-5. Counter Reloading from the Modulus Latch

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14.7.2 Free-Running Timer Operation

This mode of operation is selected when the RLD bit in PCSR is clear. In this mode, the counter rolls over from 0x0000 to 0xFFFF without reloading from the modulus latch and continues to decrement.

When the counter reaches a count of 0x0000, the PIF flag is set in PCSR. If the PIE bit is set in PCSR, the PIF flag issues an interrupt request to the CPU.

When the OVW bit is set in PCSR, the counter can be directly initialized by writing to PMR without having to wait for the count to reach 0x0000.

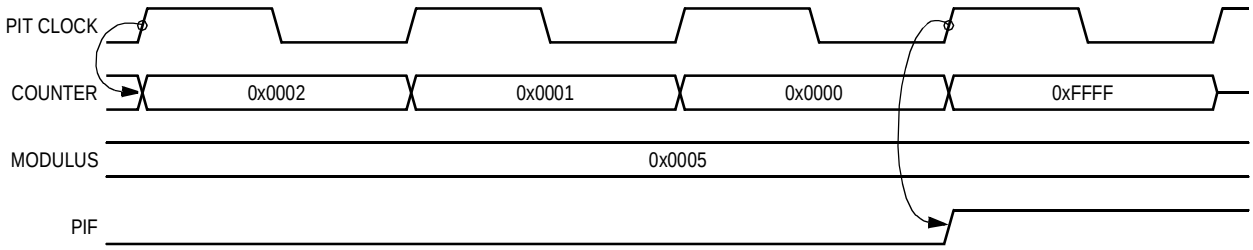

Figure 14-6. Counter in Free-Running Mode

14.7.3 Timeout Specifications

The 16-bit PIT counter and prescaler supports different timeout periods. The prescaler divides the system clock as selected by the PRE[3:0] bits in PCSR. The PM[15:0] bits in PMR select the timeout period.

$$\text{timeout period} = \text{PRE}[3:0] \times (\text{PM}[15:0] + 1) \text{ clocks}$$

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14.8 Interrupt Operation

Table 14-3 lists the interrupt requests generated by the PIT.

Table 14-3. PIT Interrupt Requests

Interrupt Request	Flag	Enable Bit
Timeout	PIF	PIE

The PIF flag is set when the PIT counter reaches 0x0000. The PIE bit enables the PIF flag to generate interrupt requests. Clear PIF by writing a 1 to it or by writing to the PMR.

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Section 15. Timer Modules (TIM1 and TIM2)

15.1 Contents

15.2 Introduction 295
15.3 Features 295
15.4 Block Diagram 296
15.5 Modes of Operation 297
15.5.1 Supervisor and User Modes 297
15.5.2 Run Mode 297
15.5.3 Stop Mode 297
15.5.4 Wait, Doze, and Debug Modes 297
15.5.5 Test Mode 297
15.6 Signal Description 298
15.6.1 ICOC[2:0] 298
15.6.2 ICOC3 298
15.7 Memory Map and Registers 298
15.7.1 Timer Input Capture/Output Compare Select Register 300
15.7.2 Timer Compare Force Register 301
15.7.3 Timer Output Compare 3 Mask Register 302
15.7.4 Timer Output Compare 3 Data Register 303
15.7.5 Timer Counter Registers 304
15.7.6 Timer System Control Register 1 305
15.7.7 Timer Toggle-On-Overflow Register 306
15.7.8 Timer Control Register 1 307
15.7.9 Timer Control Register 2 308
15.7.10 Timer Interrupt Enable Register 309
15.7.11 Timer System Control Register 2 310
15.7.12 Timer Flag Register 1 312
15.7.13 Timer Flag Register 2 313
15.7.14 Timer Channel Registers 314

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15.7.15 Pulse Accumulator Control Register 315
15.7.16 Pulse Accumulator Flag Register 317
15.7.17 Pulse Accumulator Counter Registers 318
15.7.18 Timer Port Data Register 319
15.7.19 Timer Port Data Direction Register 320
15.7.20 Timer Test Register 321
15.8 Functional Description 321
15.8.1 Prescaler 321
15.8.2 Input Capture 321
15.8.3 Output Compare 322
15.8.4 Pulse Accumulator 323
15.8.4.1 Event Counter Mode 323
15.8.4.2 Gated Time Accumulation Mode 324
15.8.5 General-Purpose I/O Ports 325
15.9 Reset 326
15.10 Interrupts 326
15.10.1 Timer Channel Interrupts (CxF) 326
15.10.2 Pulse Accumulator Overflow (PAOVF) 327
15.10.3 Pulse Accumulator Input (PAIF) 327
15.10.4 Timer Overflow (TOF) 327

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15.2 Introduction

The MMC2107 has two 4-channel timer modules (TIM1 and TIM2). Each consists of a 16-bit programmable counter driven by a 7-stage programmable prescaler. Each of the four timer channels can be configured for input capture or output. Additionally, one of the channels, channel 3, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator. The pulse accumulator shares timer channel 3 when in event mode.

15.3 Features

Features of the timer include:

- Four 16-bit input capture/output compare channels
- 16-bit architecture
- Programmable prescaler
- Pulse widths variable from microseconds to seconds
- Single 16-bit pulse accumulator
- Toggle-on-overflow feature for pulse-width modulator (PWM) generation
- Option for enabling timer port pullups on reset

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15.4 Block Diagram

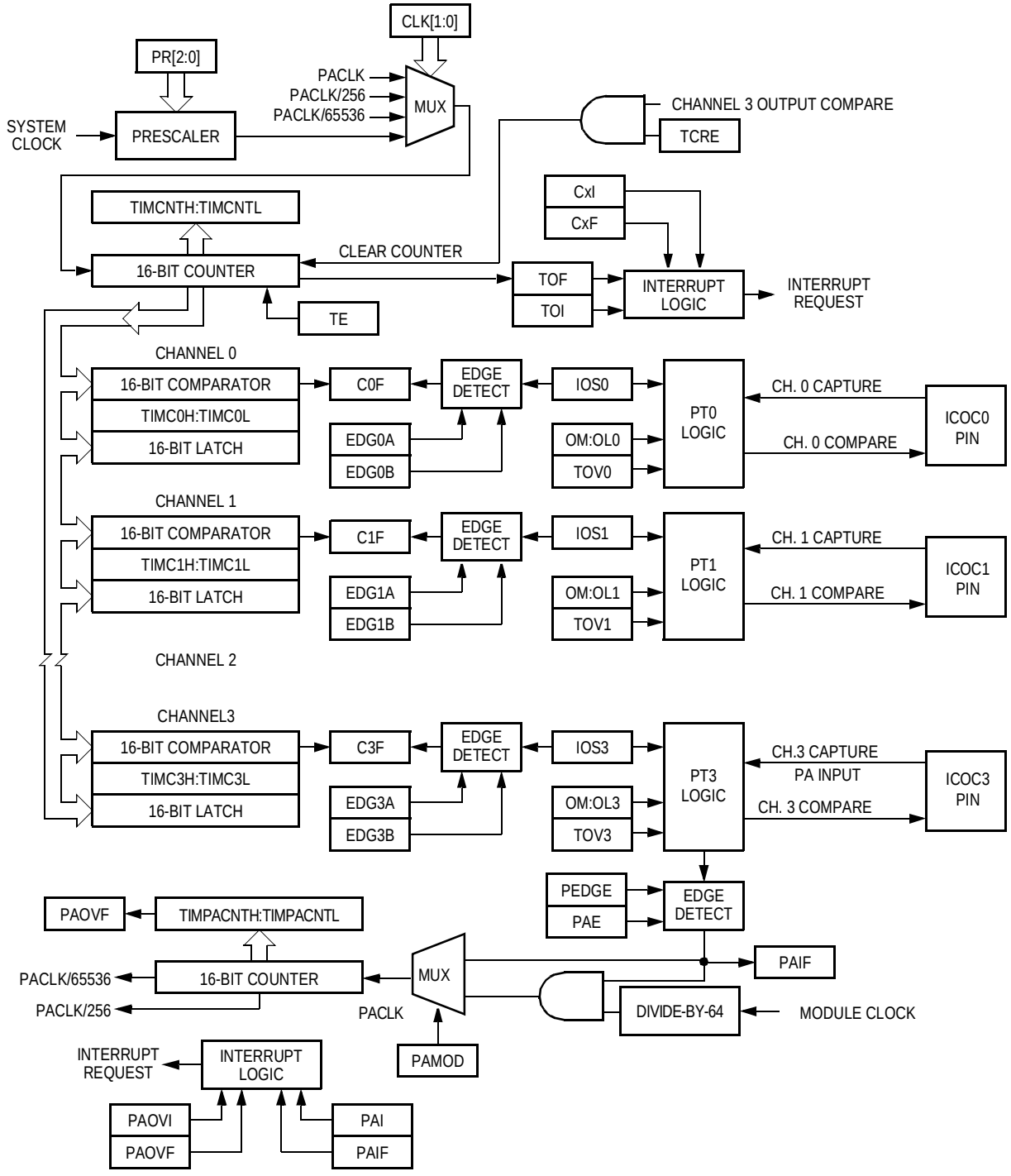

Figure 15-1. Timer Block Diagram

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15.5 Modes of Operation

This subsection describes the supervisor and user modes, the five low-power options, and test mode.

15.5.1 Supervisor and User Modes

The SO bit in the chip-select control register determines whether the processor is operating in user mode or supervisor mode. Accessing supervisor address locations while not in supervisor mode causes the timer to assert a transfer error.

15.5.2 Run Mode

Clearing the TIMEN bit in the timer system control register 1 (TIMSCR1) or the PAE bit in the pulse accumulator control register (TIMPACTL) reduces power consumption in run mode. Timer registers are still accessible, but all timer functions are disabled.

15.5.3 Stop Mode

If the central processor unit (CPU) enters stop mode, timer operation stops. Upon exiting stop mode, the timer resumes operation unless stop mode was exited by reset.

15.5.4 Wait, Doze, and Debug Modes

The timer is unaffected by these low-power modes.

15.5.5 Test Mode

A high signal on the TEST pin puts the processor in test mode or special mode. The timer behaves as in user mode, except that timer test registers are accessible.

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15.6 Signal Description

Table 15-1 provides an overview of the signal properties.

Table 15-1. Signal Properties

Name[1]	Port	Function	Reset State	Pullup
ICOC0	TIMPORT0	Channel 0 IC/OC pin	Pin state	Active
ICOC1	TIMPORT1	Timer channel 1 IC/OC pin	Pin state	Active
ICOC2	TIMPORT2	Timer channel 2 IC/OC pin	Pin state	Active
ICOC3	TIMPORT3	Timer channel 3 IC/OC or PA pin	Pin state	Active

1. Pin signal names may change according to user requirements.

15.6.1 ICOC[2:0]

The ICOC[2:0] pins are for channel 2–0 input capture and output compare functions. These pins are available for general-purpose input/output (I/O) when not configured for timer functions.

15.6.2 ICOC3

The ICOC3 pin is for channel 3 input capture and output compare functions or for the pulse accumulator input. This pin is available for general-purpose I/O when not configured for timer functions.

15.7 Memory Map and Registers

See Table 15-2 for a memory map of the two timer modules. Timer 1 has a base address of 0x00ce_0000. Timer 2 has a base address of 0x00cf_0000.

NOTE: *Reading reserved or unimplemented locations returns 0s. Writing to reserved or unimplemented locations has no effect.*

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Table 15-2. Timer Modules Memory Map

Address		Bits 7–0	Access[1]
TIM1	TIM2		
0x00ce_0000	0x00cf_0000	Timer IC/OC select register (TIMIOS)	S
0x00ce_0001	0x00cf_0001	Timer compare force register (TIMCFORC)	S
0x00ce_0002	0x00cf_0002	Timer output compare 3 mask register (TIMOC3M)	S
0x00ce_0003	0x00cf_0003	Timer output compare 3 data register (TIMOC3D)	S
0x00ce_0004	0x00cf_0004	Timer counter register high (TIMCNTH)	S
0x00ce_0005	0x00cf_0005	Timer counter register low (TIMCNTL)	S
0x00ce_0006	0x00cf_0006	Timer system control register 1 (TIMSCR1)	S
0x00ce_0007	0x00cf_0007	Reserved[2]	—
0x00ce_0008	0x00cf_0008	Timer toggle-on-overflow register (TMTOV)	S
0x00ce_0009	0x00cf_0009	Timer control register 1 (TIMCTL1)	S
0x00ce_000a	0x00cf_000a	Reserved[2]	—
0x00ce_000b	0x00cf_000b	Timer control register 2 (TIMCTL2)	S
0x00ce_000c	0x00cf_000c	Timer interrupt enable register (TIMIE)	S
0x00ce_000d	0x00cf_000d	Timer system control register 2 (TIMSCR2)	S
0x00ce_000e	0x00cf_000e	Timer flag register 1 (TIMFLG1)	S
0x00ce_000f	0x00cf_000f	Timer flag register 2 (TIMFLG2)	S
0x00ce_0010	0x00cf_0010	Timer channel 0 register high (TIMC0H)	S
0x00ce_0011	0x00cf_0011	Timer channel 0 register low (TIMC0L)	S
0x00ce_0012	0x00cf_0012	Timer channel 1 register high (TIMC1H)	S
0x00ce_0013	0x00cf_0013	Timer channel 1 register low (TIMC1L)	S
0x00ce_0014	0x00cf_0014	Timer channel 2 register high (TIMC2H)	S
0x00ce_0015	0x00cf_0015	Timer channel 2 register low (TIMC2L)	S
0x00ce_0016	0x00cf_0016	Timer channel 3 register high (TIMC3H)	S
0x00ce_0017	0x00cf_0017	Timer channel 3 register low (TIMC3L)	S
0x00ce_0018	0x00cf_0018	Pulse accumulator control register (TIMPACTL)	S
0x00ce_0019	0x00cf_0019	Pulse accumulator flag register (TIMPAFLG)	S
0x00ce_001a	0x00cf_001a	Pulse accumulator counter register high (TIMPACNTH)	S
0x00ce_001b	0x00cf_001b	Pulse accumulator counter register low (TIMPACNTL)	S
0x00ce_001c	0x00cf_001c	Reserved[2]	—
0x00ce_001d	0x00cf_001d	Timer port data register (TIMPORT)	S
0x00ce_001e	0x00cf_001e	Timer port data direction register (TIMDDR)	S
0x00ce_001f	0x00cf_001f	Timer test register (TIMTST)	S

1. S = CPU supervisor mode access only.
2. Writes have no effect, reads return 0s, and the access terminates without a transfer error exception.

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15.7.1 Timer Input Capture/Output Compare Select Register

Address: TIM1 — 0x00ce_0000
TIM2 — 0x00cf_0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	IOS3	IOS2	IOS1	IOS0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-2. Timer Input Capture/Output Compare Select Register (TIMIOS)

Read: Anytime; always read $00

Write: Anytime

IOS[3:0] — I/O Select Bits

The IOS[3:0] bits enable input capture or output compare operation for the corresponding timer channels.

1 = Output compare enabled
0 = Input capture enabled

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15.7.2 Timer Compare Force Register

Address: TIM1 — 0x00ce_0001
TIM2 — 0x00cf_0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:					FOC3	FOC2	FOC1	FOC0
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-3. Timer Compare Force Register (TIMCFORC)

Read: Anytime

Write: Anytime

FOC[3:0] — Force Output Compare Bits

Setting an FOC bit causes an immediate output compare on the corresponding channel. Forcing an output compare does not set the output compare flag.

1 = Force output compare
0 = No effect

NOTE: *A successful channel 3 output compare overrides any channel 2:0 compares. For each OC3M bit that is set, the output compare action reflects the corresponding OC3D bit.*

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15.7.3 Timer Output Compare 3 Mask Register

Address: TIM1 — 0x00ce_0002
TIM2 — 0x00cf_0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	OC3M3	OC3M2	OC3M1	OC3M0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-4. Timer Output Compare 3 Mask Register (TIMOC3M)

Read: Anytime

Write: Anytime

OC3M[3:0] — Output Compare 3 Mask Bits

Setting an OC3M bit configures the corresponding TIMPORT pin to be an output. OC3Mx makes the timer port pin an output regardless of the data direction bit when the pin is configured for output compare (IOSx = 1). The OC3Mx bits do not change the state of the TIMDDR bits.

1 = Corresponding TIMPORT pin configured as output
0 = No effect

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15.7.4 Timer Output Compare 3 Data Register

Address: TIM1 — 0x00ce_0003
TIM2 — 0x00cf_0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	OC3D3	OC3D2	OC3D1	OC3D0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-5. Timer Output Compare 3 Data Register (TIMOC3D)

Read: Anytime

Write: Anytime

OC3D[3:0] — Output Compare 3 Data Bits

When a successful channel 3 output compare occurs, these bits transfer to the timer port data register if the corresponding OC3Mx bits are set.

NOTE: *A successful channel 3 output compare overrides any channel 2:0 compares. For each OC3M bit that is set, the output compare action reflects the corresponding OC3D bit.*

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15.7.5 Timer Counter Registers

Address: TIM1 — 0x00ce_0004
TIM2 — 0x00cf_0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	14	13	12	11	10	9	Bit 8
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-6. Timer Counter Register High (TIMCNTH)

Address: TIM1 — 0x00ce_0005
TIM2 — 0x00cf_0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-7. Timer Counter Register Low (TIMCNTL)

Read: Anytime

Write: Only in test (special) mode; has no effect in normal modes

To ensure coherent reading of the timer counter, such that a timer rollover does not occur between two back-to-back 8-bit reads, it is recommended that only half-word (16-bit) accesses be used.

A write to TIMCNT may have an extra cycle on the first count because the write is not synchronized with the prescaler clock. The write occurs at least one cycle before the synchronization of the prescaler clock.

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15.7.6 Timer System Control Register 1

Address: TIM1 — 0x00ce_0006
TIM2 — 0x00cf_0006

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TIMEN	0	0	TFFCA	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-8. Timer System Control Register (TIMSCR1)

Read: Anytime

Write: Anytime

TIMEN — Timer Enable Bit

TIMEN enables the timer. When the timer is disabled, only the registers are accessible. Clearing TIMEN reduces power consumption.

1 = Timer enabled
0 = Timer and timer counter disabled

TFFCA — Timer Fast Flag Clear All Bit

TFFCA enables fast clearing of the main timer interrupt flag registers (TIMFLG1 and TIMFLG2) and the PA flag register (TIMPAFLG). TFFCA eliminates the software overhead of a separate clear sequence.

When TFFCA is set:

- An input capture read or a write to an output compare channel clears the corresponding channel flag, CxF.
- Any access of the timer count registers (TIMCNTH/L) clears the TOF flag.
- Any access of the PA counter registers (TIMPACNT) clears both the PAOVF and PAIF flags in TIMPAFLG.

Writing logic 1s to the flags clears them only when TFFCA is clear.

1 = Fast flag clearing
0 = Normal flag clearing

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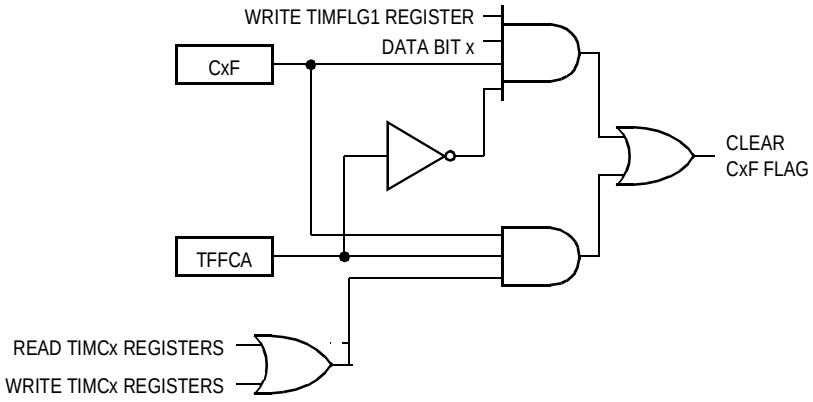

Figure 15-9. Fast Clear Flag Logic

15.7.7 Timer Toggle-On-Overflow Register

Address: TIM1 — 0x00ce_0008
TIM2 — 0x00cf_0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	TOV3	TOV2	TOV1	TOV0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-10. Timer Toggle-On-Overflow Register (TIMTOV)

Read: Anytime

Write: Anytime

TOV[3:0]— Toggle-On-Overflow Bits

TOV[3:0] toggles the output compare pin on overflow. This feature only takes effect when in output compare mode. When set, it takes precedence over forced output compare but not channel 3 override events.

1 = Toggle output compare pin on overflow feature enabled
0 = Toggle output compare pin on overflow feature disabled

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15.7.8 Timer Control Register 1

Address: TIM1 — 0x00ce_0009
TIM2 — 0x00cf_0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-11. Timer Control Register 1 (TIMCTL1)

Read: Anytime

Write: Anytime

OMx/OLx — Output Mode/Output Level Bits

These bit pairs select the output action to be taken as a result of a successful output compare. When either OMx or OLx is set and the IOSx bit is set, the pin is an output regardless of the state of the corresponding DDR bit.

Table 15-3. Output Compare Action Selection

OMx:OLx	Action on Output Compare
00	Timer disconnected from output pin logic
01	Toggle OCx output line
10	Clear OCx output line
11	Set OCx line

Channel 3 shares a pin with the pulse accumulator input pin. To use the PAI input, clear both the OM3 and OL3 bits and clear the OC3M3 bit in the output compare 3 mask register.

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15.7.9 Timer Control Register 2

Address: TIM1 — 0x00ce_000b
TIM2 — 0x00cf_000b

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG10
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-12. Timer Control Register 2 (TIMCTL2)

Read: Anytime

Write: Anytime

EDGx[B:A] — Input Capture Edge Control Bits

These eight bit pairs configure the input capture edge detector circuits.

Table 15-4. Input Capture Edge Selection

EDGx[B:A]	Edge Selection
00	Input capture disabled
01	Input capture on rising edges only
10	Input capture on falling edges only
11	Input capture on any edge (rising or falling)

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15.7.10 Timer Interrupt Enable Register

Address: TIM1 — 0x00ce_000c
TIM2 — 0x00cf_000c

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	C3I	C2I	C1I	C0I
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-13. Timer Interrupt Enable Register (TIMIE)

Read: Anytime

Write: Anytime

C[3:0]I — Channel Interrupt Enable Bits

C[3:0]I enable the C[3:0]F flags in timer flag register 1 to generate interrupt requests.

1 = Corresponding channel interrupt requests enabled
0 = Corresponding channel interrupt requests disabled

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15.7.11 Timer System Control Register 2

Address: TIM1 — 0x00ce_000d
TIM2 — 0x00cf_000d

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOI	0	PUPT	RDPT	TCRE	PR2	PR1	PR0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-14. Timer System Control Register 2 (TIMSCR2)

Read: Anytime

Write: Anytime

TOI — Timer Overflow Interrupt Enable Bit

TOI enables timer overflow interrupt requests.
1 = Overflow interrupt requests enabled
0 = Overflow interrupt requests disabled

PUPT — Timer Pullup Enable Bit

PUPT enables pullup resistors on the timer ports when the ports are configured as inputs.
1 = Pullup resistors enabled
0 = Pullup resistors disabled

RDPT — Timer Drive Reduction Bit

RDPT reduces the output driver size.
1 = Output drive reduction enabled
0 = Output drive reduction disabled

TCRE — Timer Counter Reset Enable Bit

TCRE enables a counter reset after a channel 3 compare.
1 = Counter reset enabled
0 = Counter reset disabled

NOTE: *When the timer channel 3 registers contain $0000 and TCRE is set, the timer counter registers remain at $0000 all the time.*

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When the timer channel 3 registers contain $FFFF and TCRE is set, TOF never gets set even though the timer counter registers go from $FFFF to $0000.

PR[2:0] — Prescaler Bits

These bits select the prescaler divisor for the timer counter.

Table 15-5. Prescaler Selection

PR[2:0]	Prescaler Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

NOTE: *The newly selected prescaled clock does not take effect until the next synchronized edge of the prescaled clock when the clock count transitions to $0000.)*

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15.7.12 Timer Flag Register 1

Address: TIM1 — 0x00ce_000e
TIM2 — 0x00cf_000e

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	C3F	C2F	C1F	C0F
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-15. Timer Flag Register 1 (TIMFLG1)

Read: Anytime

Write: Anytime; writing 1 clears flag; writing 0 has no effect

C[3:0]F — Channel Flags

A channel flag is set when an input capture or output compare event occurs. Clear a channel flag by writing a 1 to it.

NOTE: *When the fast flag clear all bit, TFFCA, is set, an input capture read or an output compare write clears the corresponding channel flag. TFFCA is in timer system control register 1 (TIMSCR1).*

When a channel flag is set, it does not inhibit subsequent output compares or input captures.

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15.7.13 Timer Flag Register 2

Address: TIM1 — 0x00ce_000f
TIM2 — 0x00cf_000f

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-16. Timer Flag Register 2 (TIMFLG2)

Read: Anytime

Write: Anytime; writing 1 clears flag; writing 0 has no effect

TOF — Timer Overflow Flag

TOF is set when the timer counter rolls over from $FFFF to $0000. If the TOI bit in TIMSCR2 is also set, TOF generates an interrupt request. Clear TOF by writing a 1 to it.

1 = Timer overflow
0 = No timer overflow

NOTE: *When the timer channel 3 registers contain $FFFF and TCRE is set, TOF never gets set even though the timer counter registers go from $FFFF to $0000.*

When the fast flag clear all bit, TFFCA, is set, any access to the timer counter registers clears timer flag register 2. The TFFCA bit is in timer system control register 1 (TIMSCR1).

When TOF is set, it does not inhibit subsequent overflow events.

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15.7.14 Timer Channel Registers

Address: TIMC0H — 0x00ce_0010/0x00cf_0010
TIMC1H — 0x00ce_0012/0x00cf_0012
TIMC2H — 0x00ce_0014/0x00cf_0014
TIMC3H — 0x00ce_0016/0x00cf_0016

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	0	0	0	0	0	0	0	0

Figure 15-17. Timer Channel [0:3] Register High (TIMCxH)

Address: TIMC0L — 0x00ce_0011/0x00cf_0011
TIMC1L — 0x00ce_0013/0x00cf_0013
TIMC2L — 0x00ce_0015/0x00cf_0015
TIMC3L — 0x00ce_0017/0x00cf_0017

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	0	0	0	0	0	0	0	0

Figure 15-18. Timer Channel [0:3] Register Low (TIMCxL)

Read: Anytime

Write: Output compare channel, anytime; input capture channel, no effect

When a channel is configured for input capture (IOSx = 0), the timer channel registers latch the value of the free-running counter when a defined transition occurs on the corresponding input capture pin.

When a channel is configured for output compare (IOSx = 1), the timer channel registers contain the output compare value.

To ensure coherent reading of the timer counter, such that a timer rollover does not occur between back-to-back 8-bit reads, it is recommended that only half-word (16-bit) accesses be used.

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15.7.15 Pulse Accumulator Control Register

Address: TIM1 — 0x00ce_0018
TIM2 — 0x00cf_0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	PAE	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-19. Pulse Accumulator Control Register (TIMPACTL)

Read: Anytime

Write: Anytime

PAE — Pulse Accumulator Enable Bit

PAE enables the pulse accumulator.
1 = Pulse accumulator enabled
0 = Pulse accumulator disabled

NOTE: *The pulse accumulator can operate in event mode even when the timer enable bit, TIMEN, is clear.*

PAMOD — Pulse Accumulator Mode Bit

PAMOD selects event counter mode or gated time accumulation mode.
1 = Gated time accumulation mode
0 = Event counter mode

PEDGE — Pulse Accumulator Edge Bit

PEDGE selects falling or rising edges on the PAI pin to increment the counter.

In event counter mode (PAMOD = 0):
1 = Rising PAI edge increments counter
0 = Falling PAI edge increments counter

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In gated time accumulation mode (PAMOD = 1):
1 = Low PAI input enables divided-by-64 clock to pulse accumulator and trailing rising edge on PAI sets PAIF flag.
0 = High PAI input enables divided-by-64 clock to pulse accumulator and trailing falling edge on PAI sets PAIF flag.

NOTE: *The timer prescaler generates the divided-by-64 clock. If the timer is not active, there is no divided-by-64 clock.*

To operate in gated time accumulation mode:

1. Apply logic 0 to $\overline{\text{RESET}}$ pin.
2. Initialize registers for pulse accumulator mode test.
3. Apply appropriate level to PAI pin.
4. Enable timer.

CLK[1:0] — Clock Select Bits

CLK[1:0] select the timer counter input clock as shown in **Table 15-6**.

Table 15-6. Clock Selection

CLK[1:0]	Timer Counter Clock(1)
00	Timer prescaler clock(2)
01	PACLK
10	PACLK/256
11	PACLK/65536

1. Changing the CLKx bits causes an immediate change in the timer counter clock input.
2. When PAE = 0, the timer prescaler clock is always the timer counter clock.

PAOVI — Pulse Accumulator Overflow Interrupt Enable Bit

PAOVI enables the PAOVF flag to generate interrupt requests.
1 = PAOVF interrupt requests enabled
0 = PAOVF interrupt requests disabled

PAI — Pulse Accumulator Input Interrupt Enable Bit

PAI enables the PAIF flag to generate interrupt requests.
1 = PAIF interrupt requests enabled
0 = PAIF interrupt requests disabled

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15.7.16 Pulse Accumulator Flag Register

Address: TIM1 — 0x00ce_0019
TIM2 — 0x00cf_0019

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	PAOVF	PAIF
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-20. Pulse Accumulator Flag Register (TIMPAFLG)

Read: Anytime

Write: Anytime; writing 1 clears the flag; writing 0 has no effect

PAOVF — Pulse Accumulator Overflow Flag

PAOVF is set when the 16-bit pulse accumulator rolls over from $FFFF to $0000. If the PAOVI bit in TIMPACTL is also set, PAOVF generates an interrupt request. Clear PAOVF by writing a 1 to it.

1 = Pulse accumulator overflow
0 = No pulse accumulator overflow

PAIF — Pulse Accumulator Input Flag

PAIF is set when the selected edge is detected at the PAI pin. In event counter mode, the event edge sets PAIF. In gated time accumulation mode, the trailing edge of the gate signal at the PAI pin sets PAIF. If the PAI bit in TIMPACTL is also set, PAIF generates an interrupt request. Clear PAIF by writing a 1 to it.

1 = Active PAI input
0 = No active PAI input

NOTE: *When the fast flag clear all enable bit, TFFCA, is set, any access to the pulse accumulator counter registers clears all the flags in TIMPAFLG.*

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15.7.17 Pulse Accumulator Counter Registers

Address: TIM1 — 0x00ce_001a
TIM2 — 0x00cf_001a

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	0	0	0	0	0	0	0	0

Figure 15-21. Pulse Accumulator Counter Register High (TIMPACNTH)

Address: TIM1 — 0x00ce_001b
TIM2 — 0x00cf_001b

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	0	0	0	0	0	0	0	0

Figure 15-22. Pulse Accumulator Counter Register Low (TIMPACNTL)

Read: Anytime

Write: Anytime

These registers contain the number of active input edges on the PAI pin since the last reset.

NOTE: *Reading the pulse accumulator counter registers immediately after an active edge on the PAI pin may miss the last count since the input first has to be synchronized with the bus clock.*

To ensure coherent reading of the PA counter, such that the counter does not increment between back-to-back 8-bit reads, it is recommended that only half-word (16-bit) accesses be used.

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15.7.18 Timer Port Data Register

Address: TIM1 — 0x00ce_001d
TIM2 — 0x00cf_001d

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PORTT3	PORTT2	PORTT1	PORTT0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-23. Timer Port Data Register (TIMPORT)

Read: Anytime; read pin state when corresponding TIMDDR bit is 0; read pin driver state when corresponding TIMDDR bit is 1

Write: Anytime

PORTT[3:0] — Timer Port Input Capture/Output Compare Data Bits

Data written to TIMPORT is buffered and drives the pins only when they are configured as general-purpose outputs.

Reading an input (DDR bit = 0) reads the pin state; reading an output (DDR bit = 1) reads the latch.

Writing to a pin configured as a timer output does not change the pin state.

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15.7.19 Timer Port Data Direction Register

Address: TIM1 — 0x00ce_001e
TIM2 — 0x00cf_001e

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	DDRT3	DDRT2	DDRT1	DDRT0
Write:								
Reset:	0	0	0	0	0	0	0	0
Timer function:					IC/OC3	IC/OC2	IC/OC1	IC/OC0
Pulse accumulator function:					PAI			

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-24. Timer Port Data Direction Register (TIMDDR)

Read: Anytime

Write: Anytime

DDRT[3:0] — TIMPORT Data Direction Bits

These bits control the port logic of TIMPORT. Reset clears the timer port data direction register, configuring all timer port pins as inputs.

1 = Corresponding pin configured as output
0 = Corresponding pin configured as input

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15.7.20 Timer Test Register

The timer test register (TIMTST) is only for factory testing. When not in test mode, TIMTST is read-only.

Address: TIM1 — 0x00ce_001f
TIM2 — 0x00cf_001f

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-25. Timer Test Register (TIMTST)

15.8 Functional Description

The timer module is a 16-bit, 4-channel timer with input capture and output compare functions and a pulse accumulator.

15.8.1 Prescaler

The prescaler divides the module clock by 1, 2, 4, 8, 16, 32, 64, or 128. The PR[2:0] bits in TIMSCR2 select the prescaler divisor.

15.8.2 Input Capture

Clearing an I/O select bit, IOSx, configures channel x as an input capture channel. The input capture function captures the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the timer transfers the value in the timer counter into the timer channel registers, TIMCxH and TIMCxL.

The minimum pulse width for the input capture input is greater than two module clocks.

The input capture function does not force data direction. The timer port data direction register controls the data direction of an input capture pin.

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Pin conditions such as rising or falling edges can trigger an input capture only on a pin configured as an input.

An input capture on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests.

15.8.3 Output Compare

Setting an I/O select bit, IOSx, configures channel x as an output compare channel. The output compare function can generate a periodic pulse with a programmable polarity, duration, and frequency. When the timer counter reaches the value in the channel registers of an output compare channel, the timer can set, clear, or toggle the channel pin. An output compare on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests.

The output mode and level bits, OMx and OLx, select, set, clear, or toggle on output compare. Clearing both OMx and OLx disconnects the pin from the output logic.

Setting a force output compare bit, FOCx, causes an output compare on channel x. A forced output compare does not set the channel flag.

A successful output compare on channel 3 overrides output compares on all other output compare channels. A channel 3 output compare can cause bits in the output compare 3 data register to transfer to the timer port data register, depending on the output compare 3 mask register. The output compare 3 mask register masks the bits in the output compare 3 data register. The timer counter reset enable bit, TCRE, enables channel 3 output compares to reset the timer counter. A channel 3 output compare can reset the timer counter even if the OC3/PAI pin is being used as the pulse accumulator input.

An output compare overrides the data direction bit of the output compare pin but does not change the state of the data direction bit.

Writing to the timer port bit of an output compare pin does not affect the pin state. The value written is stored in an internal latch. When the pin becomes available for general-purpose output, the last value written to the bit appears at the pin.

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15.8.4 Pulse Accumulator

The pulse accumulator (PA) is a 16-bit counter that can operate in two modes:

1. Event counter mode — Counts edges of selected polarity on the pulse accumulator input pin, PAI
2. Gated time accumulation mode — Counts pulses from a divide-by-64 clock

The PA mode bit, PAMOD, selects the mode of operation.

The minimum pulse width for the PAI input is greater than two module clocks.

15.8.4.1 Event Counter Mode

Clearing the PAMOD bit configures the PA for event counter operation. An active edge on the PAI pin increments the PA. The PA edge bit, PEDGE, selects falling edges or rising edges to increment the PA.

An active edge on the PAI pin sets the PA input flag, PAIF. The PA input interrupt enable bit, PAI, enables the PAIF flag to generate interrupt requests.

NOTE: *The PAI input and timer channel 3 use the same pin. To use the PAI input, disconnect it from the output logic by clearing the channel 3 output mode and output level bits, OM3 and OL3. Also clear the channel 3 output compare 3 mask bit, OC3M3.*

The PA counter registers, TIMPACNTH/L, reflect the number of active input edges on the PAI pin since the last reset.

The PA overflow flag, PAOVF, is set when the PA rolls over from $FFFF to $0000. The PA overflow interrupt enable bit, PAOVI, enables the PAOVF flag to generate interrupt requests.

NOTE: *The PA can operate in event counter mode even when the timer enable bit, TIMEN, is clear.*

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15.8.4.2 Gated Time Accumulation Mode

Setting the PAMOD bit configures the PA for gated time accumulation operation. An active level on the PAI pin enables a divide-by-64 clock to drive the PA. The PA edge bit, PEDGE, selects low levels or high levels to enable the divided-by-64 clock.

The trailing edge of the active level at the PAI pin sets the PA input flag, PAIF. The PA input interrupt enable bit, PAI, enables the PAIF flag to generate interrupt requests.

NOTE: *The PAI input and timer channel 3 use the same pin. To use the PAI input, disconnect it from the output logic by clearing the channel 3 output mode and output level bits, OM3 and OL3. Also clear the channel 3 output compare mask bit, OC3M3.*

The PA counter registers, TIMPACNTH/L reflect the number of pulses from the divide-by-64 clock since the last reset.

NOTE: *The timer prescaler generates the divide-by-64 clock. If the timer is not active, there is no divide-by-64 clock.*

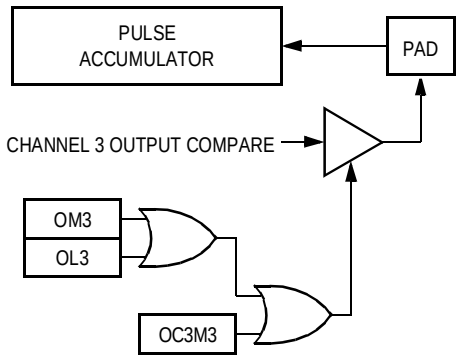

Figure 15-26. Channel 3 Output Compare/Pulse Accumulator Logic

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15.8.5 General-Purpose I/O Ports

An I/O pin used by the timer defaults to general-purpose I/O unless an internal function which uses that pin is enabled.

The timer pins can be configured for either an input capture function or an output compare function. The IOSx bits in the timer IC/OC select register configure the timer port pins as either input capture or output compare pins.

The timer port data direction register controls the data direction of an input capture pin. External pin conditions trigger input captures on input capture pins configured as inputs.

To configure a pin for input capture:

1. Clear the pin's IOS bit in TIMIOS.
2. Clear the pin's DDR bit in TIMDDR.
3. Write to TIMCTL2 to select the input edge to detect.

TIMDDR does not affect the data direction of an output compare pin. The output compare function overrides the data direction register but does not affect the state of the data direction register.

To configure a pin for output compare:

1. Set the pin's IOS bit in TIMIOS.
2. Write the output compare value to TIMCxH/L.
3. Clear the pin's DDR bit in TIMDDR.
4. Write to the OMx/OLx bits in TIMCTL1 to select the output action.

Table 15-7. TIMPORT I/O Function

In		Out	
Data Direction Register	**Output Compare Action**	**Reading at Data Bus**	**Reading at Pin**
0	0	Pin	Pin
0	1	Pin	Output compare action
1	1	Port data register	Output compare action
1	0	Port data register	Port data register

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15.9 Reset

Reset initializes the timer registers to a known startup state as described in the **15.7 Memory Map and Registers**.

15.10 Interrupts

Table 15-8 lists the interrupt requests generated by the timer.

Table 15-8. Timer Interrupt Requests

Interrupt Request	Flag	Enable Bit
Channel 3 IC/OC	C3F	C3I
Channel 2 IC/OC	C2F	C2I
Channel 1 IC/OC	C1F	C1I
Channel 0 IC/OC	C0F	C0I
PA overflow	PAOVF	PAOVI
PA input	PAIF	PAI
Timer overflow	TOF	TOI

15.10.1 Timer Channel Interrupts (CxF)

A channel flag is set when an input capture or output compare event occurs. Clear a channel flag by writing a 1 to it.

NOTE: *When the fast flag clear all bit, TFFCA, is set, an input capture read or an output compare write clears the corresponding channel flag. TFFCA is in timer system control register 1 (TIMSCR1).*

When a channel flag is set, it does not inhibit subsequent output compares or input captures

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15.10.2 Pulse Accumulator Overflow (PAOVF)

PAOVF is set when the 16-bit pulse accumulator rolls over from $FFFF to $0000. If the PAOVI bit in TIMPACTL is also set, PAOVF generates an interrupt request. Clear PAOVF by writing a 1 to it.

NOTE: *When the fast flag clear all enable bit, TFFCA, is set, any access to the pulse accumulator counter registers clears all the flags in TIMPAFLG.*

15.10.3 Pulse Accumulator Input (PAIF)

PAIF is set when the selected edge is detected at the PAI pin. In event counter mode, the event edge sets PAIF. In gated time accumulation mode, the trailing edge of the gate signal at the PAI pin sets PAIF. If the PAI bit in TIMPACTL is also set, PAIF generates an interrupt request. Clear PAIF by writing a 1 to it.

NOTE: *When the fast flag clear all enable bit, TFFCA, is set, any access to the pulse accumulator counter registers clears all the flags in TIMPAFLG.*

15.10.4 Timer Overflow (TOF)

TOF is set when the timer counter rolls over from $FFFF to $0000. If the TOI bit in TIMSCR2 is also set, TOF generates an interrupt request. Clear TOF by writing a 1 to it.

NOTE: *When the timer channel 3 registers contain $FFFF and TCRE is set, TOF never gets set even though the timer counter registers go from $FFFF to $0000.*

When the fast flag clear all bit, TFFCA, is set, any access to the timer counter registers clears timer flag register 2. The TFFCA bit is in timer system control register 1 (TIMSCR1).

When TOF is set, it does not inhibit future overflow events.

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Section 16. Serial Communications Interface Modules (SCI1 and SCI2)

16.1 Contents

16.2 Introduction 330
16.3 Features 331
16.4 Block Diagram 332
16.5 Modes of Operation 333
16.5.1 Doze Mode 333
16.5.2 Stop Mode 333
16.6 Signal Description 334
16.6.1 RXD 334
16.6.2 TXD 334
16.7 Memory Map and Registers 334
16.7.1 SCI Baud Rate Registers 336
16.7.2 SCI Control Register 1 337
16.7.3 SCI Control Register 2 340
16.7.4 SCI Status Register 1 342
16.7.5 SCI Status Register 2 344
16.7.6 SCI Data Registers 345
16.7.7 SCI Pullup and Reduced Drive Register 346
16.7.8 SCI Port Data Register 347
16.7.9 SCI Data Direction Register 348
16.8 Functional Description 349
16.9 Data Format 349
16.10 Baud Rate Generation 350
16.11 Transmitter 351
16.11.1 Frame Length 352
16.11.2 Transmitting a Frame 353
16.11.3 Break Frames 355
16.11.4 Idle Frames 355

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16.12 Receiver 356
16.12.1 Frame Length 356
16.12.2 Receiving a Frame 356
16.12.3 Data Sampling 357
16.12.4 Framing Errors 362
16.12.5 Baud Rate Tolerance 362
16.12.5.1 Slow Data Tolerance 363
16.12.5.2 Fast Data Tolerance 364
16.12.6 Receiver Wakeup 365
16.12.6.1 Idle Input Line Wakeup (WAKE = 0) 365
16.12.6.2 Address Mark Wakeup (WAKE = 1) 365
16.13 Single-Wire Operation 366
16.14 Loop Operation 367
16.15 I/O Ports 368
16.16 Reset 369
16.17 Interrupts 369
16.17.1 Transmit Data Register Empty 369
16.17.2 Transmission Complete 369
16.17.3 Receive Data Register Full 370
16.17.4 Idle Receiver Input 370
16.17.5 Overrun 370

16.2 Introduction

The serial communications interface (SCI) allows asynchronous serial communications with peripheral devices and other microcontroller units (MCU).

The MMC2107 has two identical SCI modules, each with its own control registers and input/output (I/O) pins.

In the text that follows, SCI register names are denoted generically. Thus, SCIPORT refers interchangeably to SCI1PORT and SCI2PORT, the port data registers for SCI1 and SCI2, respectively.

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16.3 Features

Features of each SCI module include:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Separate receiver and transmitter central processor unit (CPU) interrupt requests
- Programmable transmitter output polarity
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- General-purpose, I/O capability

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16.4 Block Diagram

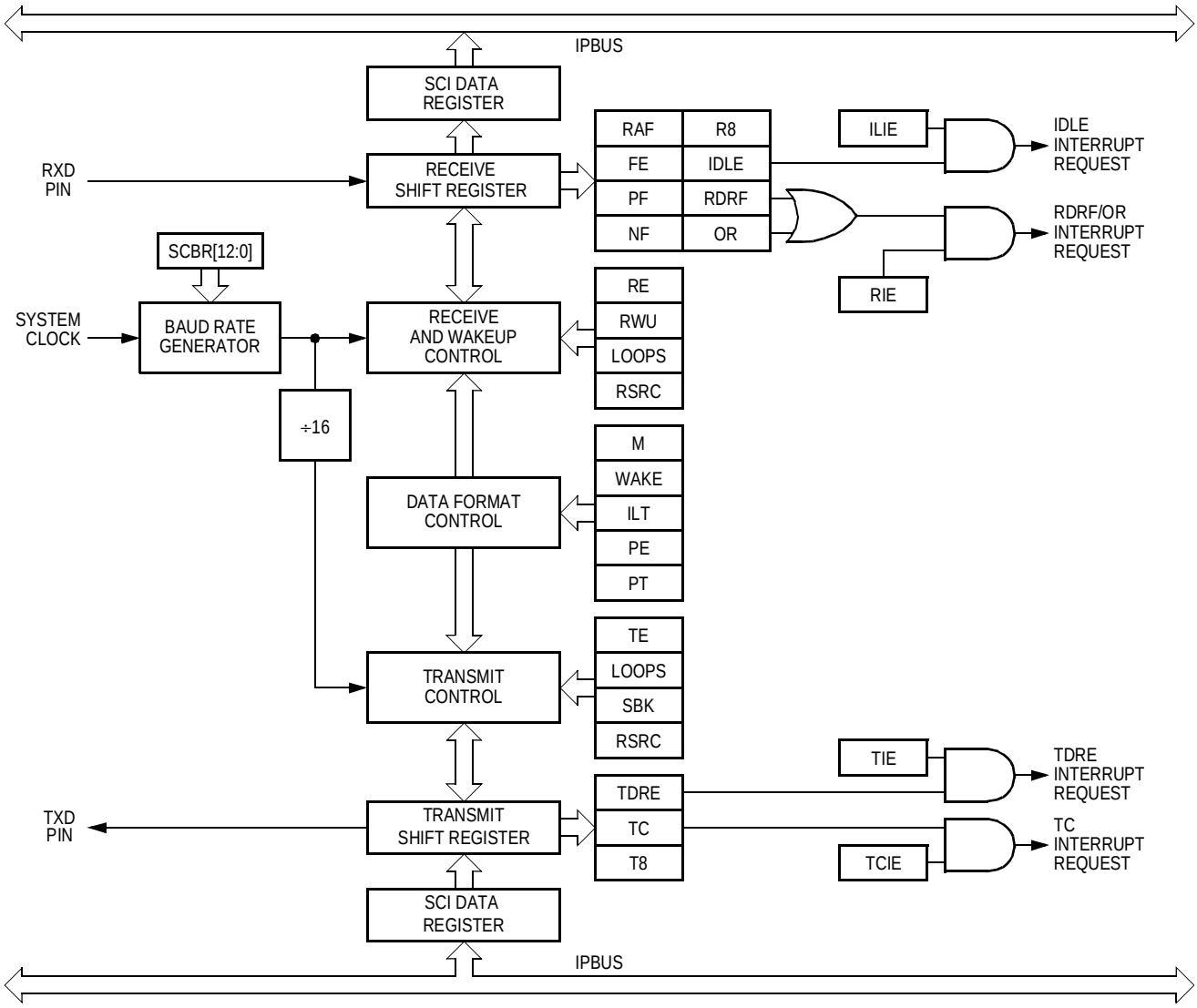

Figure 16-1. SCI Block Diagram

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16.5 Modes of Operation

SCI operation is identical in run, special, and emulation modes. The SCI has two low-power modes, doze and stop.

NOTE: *Run mode is the normal mode of operation and the WAIT instruction does not affect SCI operation.*

16.5.1 Doze Mode

When the SCIDOZ bit in the SCI pullup and reduced drive (SCIPURD) register is set, the DOZE instruction stops the SCI clock and puts the SCI in a low-power state. The DOZE instruction does not affect SCI register states. Any transmission or reception in progress stops at doze mode entry and resumes when an internal or external interrupt request brings the CPU out of doze mode. Exiting doze mode by reset aborts any transmission or reception in progress and resets the SCI.

When the SCIDOZ bit is clear, execution of the DOZE instruction has no effect on the SCI. Normal module operation continues, allowing any SCI interrupt to bring the CPU out of doze mode.

16.5.2 Stop Mode

The STOP instruction stops the SCI clock and puts the SCI in a low-power state. The STOP instruction does not affect SCI register states. Any transmission or reception in progress halts at stop mode entry and resumes when an external interrupt request brings the CPU out of stop mode. Exiting stop mode by reset aborts any transmission or reception in progress and resets the SCI.

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16.6 Signal Description

Table 16-1 gives an overview of the signals which are described here.

Table 16-1. Signal Properties

Name	Function	Port	Reset State	Pullup
RXD	Receive data pin	SCIPORT0	0	Disabled
TXD	Transmit data pin	SCIPORT1	0	Disabled

16.6.1 RXD

RXD is the SCI receiver pin. RXD is available for general-purpose I/O when it is not configured for receiver operation.

16.6.2 TXD

TXD is the SCI transmitter pin. TXD is available for general-purpose I/O when it is not configured for transmitter operation.

16.7 Memory Map and Registers

Table 16-1 shows the SCI memory map.

NOTE: *Reading unimplemented addresses (0x00cc_000b through 0x00cc_000f) returns 0s. Writing to unimplemented addresses has no effect. Accessing unimplemented addresses does not generate an error response.*

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Table 16-2. Serial Communications Interface Module Memory Map(1)

Address		Bits 7–0	Access(2)
SCI1	SCI2		
0x00cc_0000	0x00cd_0000	SCI baud register high (SCIBDH)	S/U
0x00cc_0001	0x00cd_0001	SCI baud register low (SCIBDL)	S/U
0x00cc_0002	0x00cd_0002	SCI control register1 (SCICR1)	S/U
0x00cc_0003	0x00cd_0003	SCI control register 2 (SCICR2)	S/U
0x00cc_0004	0x00cd_0004	SCI status register 1 (SCISR1)	S/U
0x00cc_0005	0x00cd_0005	SCI status register 2 (SCISR2)	S/U
0x00cc_0006	0x00cd_0006	SCI data register high (SCIDRH)	S/U
0x00cc_0007	0x00cd_0007	SCI data register low (SCIDRL)	S/U
0x00cc_0008	0x00cd_0008	SCI pullup and reduced drive register (SCIPURD)	S/U
0x00cc_0009	0x00cd_0009	SCI port data register (SCIPORT)	S/U
0x00cc_000a	0x00cd_000a	SCI data direction register (SCIDDR)	S/U
0x00cc_000b to 0x00cc_000f	0x00cd_000b to 0x00cd_000f	Reserved(3)	S/U

1. Each module is assigned 64 Kbytes of address space, all of which may not be decoded. Accesses outside of the specified module memory map generate a bus error exception.
2. S/U = CPU supervisor or user mode access. User mode accesses to supervisor only addresses have no effect and result in a cycle termination transfer error.
3. Within the specified module memory map, accessing reserved addresses does not generate a bus error exception. Reads of reserved addresses return 0s and writes have no effect.

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16.7.1 SCI Baud Rate Registers

Address: SCI1 — 0x00cc_0000
SCI2 — 0x00cd_0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 16-2. SCI Baud Rate Register High (SCIBDH)

Address: SCI1 — 0x00cc_0001
SCI2 — 0x00cd_0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
Write:								
Reset:	0	0	0	0	0	1	0	0

Figure 16-3. SCI Baud Rate Register Low (SCIBDL)

Read: Anytime

Write: Anytime

SBR[12:8], SBR[7:0] — SCI Baud Rate Bits

These read/write bits control the SCI baud rate:

$$\text{SCI baud rate} = \frac{f_{sys}}{16 \times \text{SBR}[12:0]}$$

where:

$1 \leq \text{SBR}[12:0] \leq 8191$

NOTE: *The baud rate generator is disabled until the TE bit or the RE bit in SCICR2 is set for the first time after reset. The baud rate generator is disabled when SBR[12:0] = 0.*

Writing to SCIBDH has no effect without also writing to SCIBDL. Writing to SCIBDH puts the data in a temporary location until data is written to SCIBDL.

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16.7.2 SCI Control Register 1

Address: SCI1 — 0x00cc_0002
SCI2 — 0x00cd_0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LOOPS	WOMS	RSRC	M	WAKE	ILT	PE	PT
Reset:	0	0	0	0	0	0	0	0

Figure 16-4. SCI Control Register 1 (SCICR1)

Read: Anytime

Write: Anytime

LOOPS — Loop Select Bit

This read/write control bit switches the SCI between normal mode and loop mode. Reset clears LOOPS.

1 = Loop mode SCI operation
0 = Normal mode SCI operation

The SCI operates normally (LOOPS = 0, RSRC = X) when the output of its transmitter is connected to the TXD pin, and the input of its receiver is connected to the RXD pin.

In loop mode (LOOPS =1, RSRC = 0), the input to the SCI receiver is internally disconnected from the RXD pin logic and instead connected to the output of the SCI transmitter. The behavior of TXD is governed by the DDRSC1 bit in SCIDDR. If DDRSC1 = 1, the TXD pin is driven with the output of the SCI transmitter. If DDRSC1 = 0, the TXD pin idles high. See **16.14 Loop Operation** for additional information.

For either loop mode or single-wire mode to function, both the SCI receiver and transmitter must be enabled by setting the RE and TE bits in SCIxCR2.

NOTE: *The RXD pin becomes general-purpose I/O when LOOPS = 1, regardless of the state of the RSRC bit. DDRSC0 in SCIDDR is the data direction bit for the RXD pin.*

Table 16-3 shows how the LOOPS, RSRC, and DDRSC0 bits affect SCI operation and the configuration of the RXD and TXD pins.

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Table 16-3. SCI Normal, Loop, and Single-Wire Mode Pin Configurations

LOOPS	RSRC	SCI Mode	Receiver Input	RXD Pin Function	DDRSC0	Transmitter Output	TXD Pin Function
0	X	Normal	Tied to RXD input buffer	Receive pin	X	Tied to TXD output driver	Transmit pin
1	0	Loop	Tied to transmitter output	General-purpose I/O	0	Tied to receiver input only	None (idles high)
					1	Tied to receiver input and TXD output driver	Transmit pin
	1	Single-wire	Tied to TXD		0	No connection	Receive pin
					1	Tied to TXD output driver	Transmit pin

WOMS — Wired-OR Mode Select Bit

This read/write bit configures the TXD and RXD pins for open-drain operation. This allows all of the TXD pins to be tied together in a multiple-transmitter system. WOMS also affects the TXD and RXD pins when they are general-purpose outputs. External pullup resistors are necessary on open-drain outputs. Reset clears WOMS.

1 = TXD and RXD pins open-drain when outputs
0 = TXD and RXD pins CMOS drive when outputs

RSRC — Receiver Source Bit

This read/write bit selects the internal feedback path to the receiver input when LOOPS = 1. Reset clears RSRC.

1 = Receiver input tied to TXD pin when LOOPS = 1
0 = Receiver input tied to transmitter output when LOOPS = 1

M — Data Format Mode Bit

This read/write bit selects 11-bit or 10-bit frames. Reset clears M.

1 = Frames have 1 start bit, 9 data bits, and 1 stop bit.
0 = Frames have 1 start bit, 8 data bits, and 1 stop bit.

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WAKE — Wakeup Bit

This read/write bit selects the condition that wakes up the SCI receiver when it has been placed in a standby state by setting the RWU bit in SCICR2. When WAKE is set, a logic 1 (address mark) in the most significant bit position of a received data character wakes the receiver. An idle condition on the RXD pin does so when WAKE = 0. Reset clears WAKE.

1 = Address mark receiver wakeup
0 = Idle line receiver wakeup

ILT — Idle Line Type Bit

This read/write bit determines when the receiver starts counting logic 1s as idle character bits. The counting begins either after the start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit may cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. Reset clears ILT.

1 = Idle frame bit count begins after stop bit.
0 = Idle frame bit count begins after start bit.

PE — Parity Enable Bit

This read/write bit enables the parity function. When enabled, the parity function inserts a parity bit in the most significant bit position of an SCI data word. Reset clears PE.

1 = Parity function enabled
0 = Parity function disabled

PT — Parity Type Bit

This read/write bit selects even parity or odd parity. With even parity, an even number of 1s clears the parity bit and an odd number of 1s sets the parity bit. With odd parity, an odd number of 1s clears the parity bit and an even number of 1s sets the parity bit. Reset clears PT.

1 = Odd parity when PE = 1
0 = Even parity when PE = 1

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16.7.3 SCI Control Register 2

Address: SCI1 — 0x00cc_0003
SCI2 — 0x00cd_0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset:	0	0	0	0	0	0	0	0

Figure 16-5. SCI Control Register 2 (SCICR2)

Read: Anytime

Write: Anytime

TIE — Transmitter Interrupt Enable Bit

This read/write bit allows the TDRE flag to generate interrupt requests. Reset clears TIE.

1 = TDRE interrupt requests enabled
0 = TDRE interrupt requests disabled

TCIE — Transmission Complete Interrupt Enable Bit

This read/write bit allows the TC flag to generate interrupt requests. Reset clears TCIE.

1 = TC interrupt requests enabled
0 = TC interrupt requests disabled

RIE — Receiver Interrupt Enable Bit

This read/write bit allows the RDRF and OR flags to generate interrupt requests. Reset clears RIE.

1 = RDRF and OR interrupt requests enabled
0 = RDRF and OR interrupt requests disabled

ILIE — Idle Line Interrupt Enable Bit

This read/write bit allows the IDLE flag to generate interrupt requests. Reset clears ILIE.

1 = IDLE interrupt requests enabled
0 = IDLE interrupt requests disabled

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TE — Transmitter Enable Bit

This read/write bit enables the transmitter and configures the TXD pin as the transmitter output. Toggling TE queues an idle frame. Reset clears TE.

1 = Transmitter enabled
0 = Transmitter disabled

RE — Receiver Enable Bit

This read/write bit enables the receiver. Reset clears RE.

1 = Receiver enabled
0 = Receiver disabled

NOTE: *When LOOPS = 0 and TE = RE = 1, the RXD pin is an input and the TXD pin is an output regardless of the state of the DDRSC1 (TXD) and DDRSC0 (RXD) bits.*

RWU — Receiver Wakeup Bit

This read/write bit puts the receiver in a standby state that inhibits receiver interrupt requests. The WAKE bit determines whether an idle input or an address mark wakes up the receiver and clears RWU. Reset clears RWU.

1 = Receiver asleep when RE = 1
0 = Receiver awake when RE = 1

SBK — Send Break Bit

Setting this read/write bit causes the SCI to send break frames of 10 (M = 0) or 11 (M =1) logic 0s. To send one break frame, set SBK and then clear it before the break frame is finished transmitting. As long as SBK is set, the transmitter continues to send break frames.

1 = Transmitter sends break frames.
0 = Transmitter does not send break frames.

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16.7.4 SCI Status Register 1

Address: SCI1 — 0x00cc_0004
SCI2 — 0x00cd_0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
Write:								
Reset:	1	1	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 16-6. SCI Status Register 1 (SCISR1)

Read: Anytime

Write: Has no meaning or effect

TDRE — Transmit Data Register Empty Flag

The TDRE flag is set when the transmit shift register receives a word from the SCI data register. It signals that the SCIDRH and SCIDRL are empty and can receive new data to transmit. If the TIE bit in the SCICR2 is also set, TDRE generates an interrupt request. Clear TDRE by reading SCISR1 and then writing to SCIDRL. Reset sets TDRE.

1 = Transmit data register empty
0 = Transmit data register not empty

TC — Transmit Complete Flag

The TC flag is set when TDRE = 1 and no data, preamble, or break frame is being transmitted. It signals that no transmission is in progress. If the TCIE bit is set in SCICR2, TC generates an interrupt request. When TC is set, the TXD pin is idle (logic 1). TC is cleared automatically when a data, preamble, or break frame is queued. Clear TC by reading SCISR1 with TC set and then writing to SCIDRL. TC cannot be cleared while a transmission is in progress. Reset sets TC.

1 = No transmission in progress
0 = Transmission in progress

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RDRF — Receive Data Register Full Flag

The RDRF flag is set when the data in the receive shift register is transferred to SCIDRH and SCIDRL. It signals that the received data is available to the MCU. If the RIE bit is set in SCICR2, RDRF generates an interrupt request. Clear RDRF by reading the SCISR1 and then reading SCIDRL. Reset clears RDRF.

1 = Received data available in SCIDRH and SCIDRL
0 = Received data not available in SCIDRH and SCIDRL

IDLE — Idle Line Flag

The IDLE flag is set when 10 (if M = 0) or 11 (if M = 1) consecutive logic 1s appear on the receiver input. If the ILIE bit in SCICR2 is set, IDLE generates an interrupt request. Once IDLE is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag. Clear IDLE by reading SCISR1 and then reading SCIDRL. Reset clears IDLE.

1 = Receiver idle
0 = Receiver active or idle since reset or idle since IDLE flag last cleared

NOTE: *When RWU =1, an idle line condition does not set the IDLE flag.*

OR — Overrun Flag

The OR flag is set if data is not read from SCIDRL before the receive shift register receives the stop bit of the next frame. This is a receiver overrun condition. If the RIE bit in SCICR2 is set, OR generates an interrupt request. The data in the shift register is lost, but the data already in the SCIDRH and SCIDRL is not affected. Clear OR by reading SCISR1 and then reading SCIDRL. Reset clears OR.

1 = Overrun
0 = No overrun

NF — Noise Flag

The NF flag is set when the SCI detects noise on the receiver input. NF is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear NF by reading SCISR1 and then reading SCIDRL. Reset clears NF.

1 = Noise
0 = No noise

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FE — Framing Error Flag

The FE flag is set when a logic 0 is accepted as the stop bit. FE is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. FE inhibits further data reception until it is cleared. Clear FE by reading SCISR1 and then reading SCIDRL. Reset clears FE.

1 = Framing error
0 = No framing error

PF — Parity Error Flag

The PF flag is set when PE = 1 and the parity of the received data does not match its parity bit. Clear PF by reading SCISR1 and then reading SCIDRL. Reset clears PF.

1 = Parity error
0 = No parity error

16.7.5 SCI Status Register 2

Address: SCI1 — 0x00cc_0005
SCI2 — 0x00cd_0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	RAF
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 16-7. SCI Status Register 2 (SCISR2)

Read: Anytime

Write: Has no meaning or effect

RAF — Receiver Active Flag

The RAF flag is set when the receiver detects a logic 0 during the RT1 time period of the start bit search. When the receiver detects an idle character, it clears RAF. Reset clears RAF.

1 = Reception in progress
0 = No reception in progress

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16.7.6 SCI Data Registers

Address: SCI1 — 0x00cc_0006
SCI2 — 0x00cd_0006

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R8	T8	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 16-8. SCI Data Register High (SCIDRH)

Address: SCI1 — 0x00cc_0007
SCI2 — 0x00cd_0007

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 16-9. SCI Data Register Low (SCIDRL)

Read: Anytime

Write: Anytime; writing to R8 has no effect

R8 — Receive Bit 8

The R8 bit is the ninth received data bit when using the 9-bit data format (M = 1). Reset clears R8.

T8 — Transmit Bit 8

The T8 bit is the ninth transmitted data bit when using the 9-bit data format (M = 1). Reset clears T8.

R[7:0] — Receive Bits [7:0]

The R[7:0] bits are receive bits [7:0] when using the 9-bit or 8-bit data format. Reset clears R[7:0].

T[7:0] — Transmit Bits [7:0]

The T[7:0] bits are transmit bits [7:0] when using the 9-bit or 8-bit data format. Reset clears T[7:0].

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NOTE: *If the value of T8 is the same as in the previous transmission, T8 does not have to be rewritten. The same value is transmitted until T8 is rewritten.*

When using the 8-bit data format, only SCIDRL needs to be accessed.

When using 8-bit write instructions to transmit 9-bit data, write first to SCIDRH, then to SCIDRL.

16.7.7 SCI Pullup and Reduced Drive Register

Address: SCI1 — 0x00cc_0008
SCI2 — 0x00cd_0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SCISDOZ	0	RSVD5	RDPSCI	0	0	RSVD1	PUPSCI
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 16-10. SCI Pullup and Reduced Drive Register (SCIPURD)

Write: Anytime

SCISDOZ — SCI Stop in Doze Mode Bit

The SCISDOZ bit disables the SCI in doze mode.
1 = SCI disabled in doze mode
0 = SCI enabled in doze mode

RSVD[5:1] — Reserved

Writing to these read/write bits updates their values but has no effect on functionality.

RDPSCI — Reduced Drive Bit

This read/write bit controls the drive capability of TXD and RXD.
1 = Reduced TXD and RXD pin drive
0 = Full TXD and RXD pin drive

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PUPSCI — Pullup Enable Bit

This read/write bit enables the pullups on pins TXD and RXD. If a pin is programmed as an output, the pullup is disabled.

1 = TXD and RXD pullups enabled
0 = TXD and RXD pullups disabled

16.7.8 SCI Port Data Register

Address: SCI1 — 0x00cc_0009
SCI2 — 0x00cd_0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RSVD7	RSVD6	RSVD5	RSVD4	RSVD3	RSVD2	PORTSC1	PORTSC0
Reset:	0	0	0	0	0	0	0	0
Pin function:							TXD	RXD

Figure 16-11. SCI Port Data Register (SCIPORT)

Read: Anytime; when DDRSCx = 0, its pin is configured as an input, and reading PORTSCx returns the pin level; when DDRSCx = 1, its pin is configured as an output, and reading PORTSCx returns the pin driver input level.

Write: Anytime; data stored in internal latch drives pin only if DDRSC bit = 1

RSVD[7:2] — Reserved

Writing to these read/write bits updates their values but has no effect on functionality.

PORTSC[1:0] — SCIPORT Data Bits

These are the read/write data bits of the SCI port.

NOTE: *Writes to SCIPORT do not change the pin state when the pin is configured for SCI input.*

To ensure correct reading of the SCI pin values from SCIPORT, always wait at least one cycle after writing to SCIDDR before reading SCIPORT.

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16.7.9 SCI Data Direction Register

Address: SCI1 — 0x00cc_000a
SCI2 — 0x00cd_000a

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RSVD7	RSVD6	RSVD5	RSVD4	RSVD3	RSVD2	DDRSC1	DDRSC0
Reset:	0	0	0	0	0	0	0	0

Figure 16-12. SCI Data Direction Register (SCIDDR)

Read: Anytime

Write: Anytime

RSVD[7:2] — Reserved

Writing to these read/write bits updates their values but has no effect on functionality.

DDRSC[1:0] — SCIPORT Data Direction Bits

These bits control the data direction of the SCIPORT pins. Reset clears DDRSC[1:0].

1 = Corresponding pin configured as output
0 = Corresponding pin configured as input

NOTE: *When LOOPS = 0 and TE = RE = 1, the RXD pin is an input and the TXD pin is an output regardless of the state of the DDRSC1 (TXD) and DDRSC0 (RXD) bits.*

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16.8 Functional Description

The SCI allows full-duplex, asynchronous, non-return-to-zero (NRZ) serial communication between the MCU and remote devices, including other MCUs. The SCI transmitter and receiver operate independently, although they use the same baud rate generator. The CPU monitors the status of the SCI, writes the data to be transmitted, and processes received data.

16.9 Data Format

The SCI uses the standard NRZ mark/space data format shown in **Figure 16-13**.

Each frame has a start bit, eight or nine data bits, and one or two stop bits. Clearing the M bit in SCCR1 configures the SCI for 10-bit frames. Setting the M bit configures the SCI for 11-bit frames.

When the SCI is configured for 9-bit data, the ninth data bit is the T8 bit in SCI data register high (SCIDRH). It remains unchanged after transmission and can be used repeatedly without rewriting it. A frame with nine data bits has a total of 11 bits.

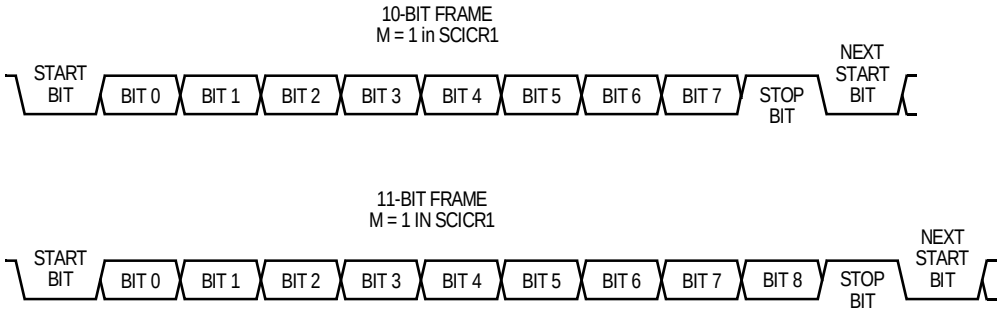

Figure 16-13. SCI Data Formats

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16.10 Baud Rate Generation

A 13-bit modulus counter in the baud rate generator derives the baud rate for both the receiver and the transmitter. The value from 0 to 8191 written to SCIBDH and SCIBDL determines the system clock divisor. The baud rate clock is synchronized with the bus clock and drives the receiver. The baud rate clock divided by 16 drives the transmitter. The receiver acquisition rate is 16 samples per bit time.

Baud rate generation is subject to two sources of error:

1. Integer division of the module clock may not give the exact target frequency.
2. Synchronization with the bus clock can cause phase shift.

Table 16-4. Example Baud Rates (System Clock = 33 MHz)

SBR[12:0]	Receiver Clock (Hz)	Transmitter Clock (Hz)	Target Baud Rate	Percent Error
0x0012	1,833,333.3	114,583.3	115,200	0.54
0x0024	916,666.7	57,291.7	57,600	0.54
0x0036	611,111.1	38,194.4	38,400	0.54
0x003d	540,983.6	33,811.4	33,600	0.63
0x0048	458,333.3	28,645.8	28,800	0.54
0x006b	308,411.2	19,275.7	19,200	0.39
0x0008f	230,769.2	14,423.1	14,400	0.16
0x00d7	153,488.4	95,93.0	9,600	0.07
0x01ae	76,744.2	4,796.5	4,800	0.07
0x035b	38,416.8	2,401.0	2,400	0.04
0x06b7	19,197.2	1,199.8	1,200	0.01
0x0d6d	9,601.4	600.1	600	0.01
0x1adb	4,800.0	300.0	300	0

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16.11 Transmitter

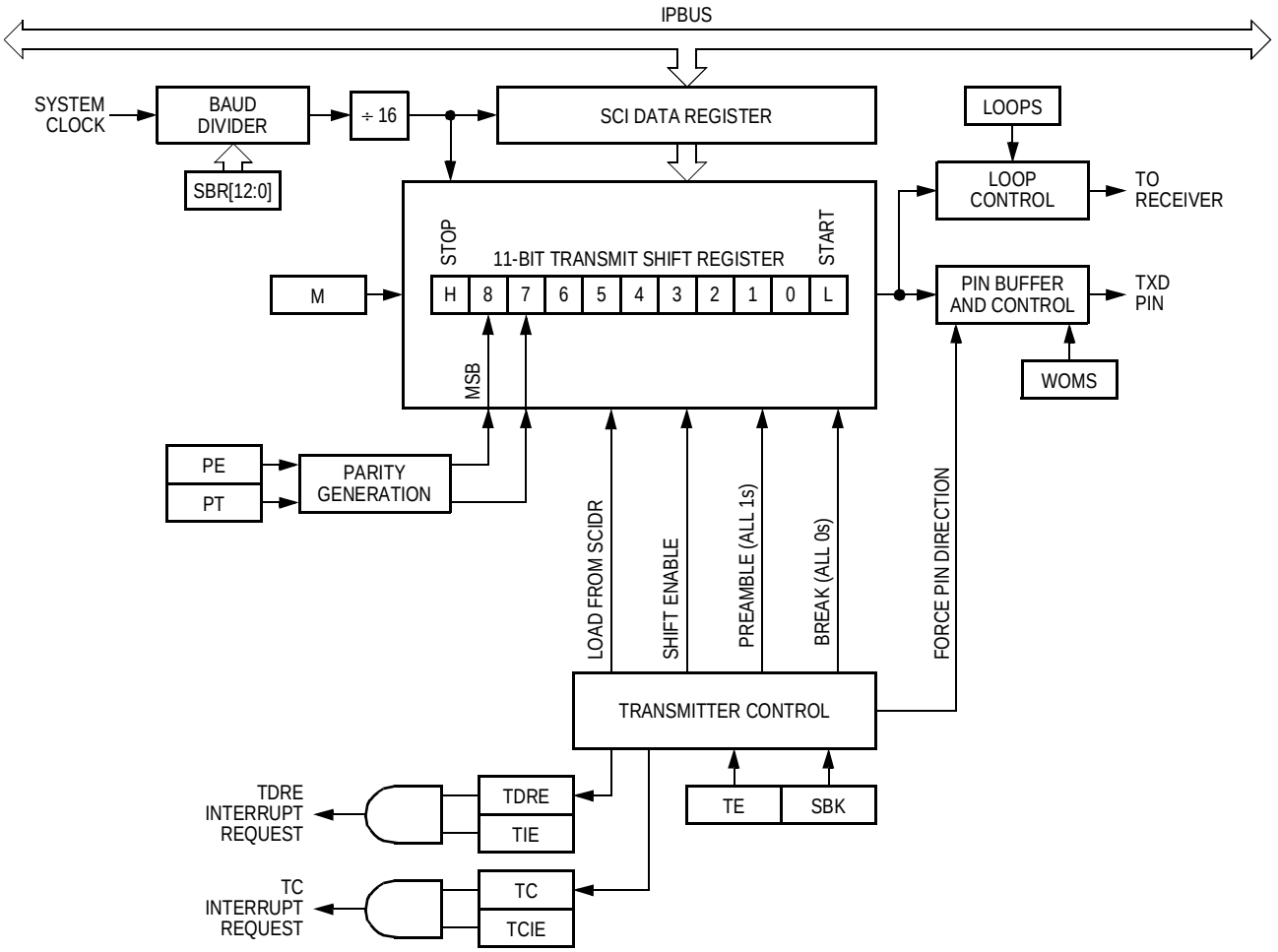

Figure 16-14. Transmitter Block Diagram

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16.11.1 Frame Length

The transmitter can generate either 10-bit or 11-bit frames. In SCICR1, the M bit selects frame length, and the PE bit enables the parity function. One data bit may be an address mark or an extra stop bit. All frames begin with a start bit and end with one or two stop bits. When transmitting 9-bit data, bit T8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

Table 16-5. Example 10-Bit and 11-Bit Frames

M Bit	Frame Length	Start Bit	Data Bits	Parity Bit	Address Mark[(1)]	Stop Bit(s)
0	10 bits	1	8	No	No	1
		1	7	No	No	2
		1	7	No	Yes	1
		1	7	Yes	No	1
1	11 bits	1	9	No	No	1
		1	8	No	No	2
		1	8	No	Yes	1
		1	8	Yes	No	1
		1	7	No	Yes	2
		1	7	Yes	No	2

1. When implementing a multidrop network using the SCI, the address mark bit is used to designate subsequent data frames as a network address and not device data.

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16.11.2 Transmitting a Frame

To begin an SCI transmission:

1. Configure the SCI:
   a. Write a baud rate value to SCIBDH and SCIBDL.
   b. Write to SCICR1 to:
      i. Enable or disable loop mode and select the receiver feedback path
      ii. Select open-drain or wired-OR SCI outputs
      iii. Select 10-bit or 11-bit frames
      iv. Select the receiver wakeup condition: address mark or idle line
      v. Select idle line type
      vi. Enable or disable the parity function and select odd or even parity
   c. Write to SCICR2 to:
      i. Enable or disable TDRE, TC, RDRF, and IDLE interrupt requests
      ii. Enable the transmitter and queue a break frame
      iii. Enable or disable the receiver
      iv. Put the receiver in standby if required
2. Transmit a byte:
   a. Clear the TDRE flag by reading SCISR1 and, if sending 9-bit data, write the ninth data bit to SCDRH.
   b. Write the byte to be transmitted (or low-order 8 bits if sending 9-bit data) to SCIDRL.
3. Repeat step **2** for each subsequent transmission.

Writing the TE bit from 0 to 1 loads the transmit shift register with a preamble of 10 (if M = 0) or 11 (if M = 1) logic 1s. When the preamble shifts out, the SCI transfers the data from SCIDRH and SCIDRL to the transmit shift register. The transmit shift register prefaces the data with a 0 start bit and appends the data with a 1 stop bit and begins shifting out the frame.

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The SCI sets the TDRE flag every time it transfers data from SCIDRH and SCIDRL to the transmit shift register. TDRE indicates that SCIDRH and SCIDRL can accept new data. If the TIE bit is set, TDRE generates an interrupt request.

NOTE: *SCIDRH and SCIDRL transfer data to the transmit shift register and sets TDRE 9/16ths of a bit time after the previous frame's stop bit starts to shift out.*

Hardware supports odd or even parity. When parity is enabled, the most significant data bit is the parity bit.

When the transmit shift register is not transmitting a frame, the TXD pin goes to the idle condition, logic 1. Clearing the TE bit while the transmitter is idle will return control of the TXD pin to the SCI data direction (SCIDDR) and SCI port (SCIPORT) registers.

If the TE bit is cleared while a transmission is in progress (while TC = 0), the frame in the transmit shift register continues to shift out. Then the TXD pin reverts to being a general-purpose I/O pin even if there is data pending in the SCI data register. To avoid accidentally cutting off a message, always wait until TDRE is set after the last frame before clearing TE.

To separate messages with preambles with minimum idle line time, use this sequence between messages:

1. Write the last byte of the first message to SCIDRH and SCIDRL.
2. Wait until the TDRE flag is set, indicating the transfer of the last frame to the transmit shift register.
3. Queue a preamble by clearing and then setting the TE bit.
4. Write the first byte of the second message to SCIDRH and SCIDRL.

When the SCI relinquishes the TXD pin, the SCIPORT and SCIDDR registers control the TXD pin.

To force TXD high when turning off the transmitter, set bit 1 of the SCI port register (SCIPORT) and bit 1 of the SCI data direction register (SCIDDR). The TXD pin goes high as soon as the SCI relinquishes control of it.

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16.11.3 Break Frames

Setting the SBK bit in SCICR2 loads the transmit shift register with a break frame. A break frame contains all logic 0s and has no start, stop, or parity bit. Break frame length depends on the M bit in the SCICR1 register. As long as SBK is set, the SCI continuously loads break frames into the transmit shift register. After SBK is clear, the transmit shift register finishes transmitting the last break frame and then transmits at least one logic 1. The automatic logic 1 at the end of a break frame guarantees the recognition of the next start bit.

The SCI recognizes a break frame when a start bit is followed by eight or nine 0 data bits and a 0 where the stop bit should be. Receiving a break frame has these effects on SCI registers:

- Sets the FE flag
- Sets the RDRF flag
- Clears the SCIDRH and SCIDRL
- May set the OR flag, NF flag, PE flag, or the RAF flag

16.11.4 Idle Frames

An idle frame contains all logic 1s and has no start, stop, or parity bit. Idle frame length depends on the M bit in the SCICR1 register. The preamble is a synchronizing idle frame that begins the first transmission after writing the TE bit from 0 to 1.

If the TE bit is cleared during a transmission, the TXD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle frame to be sent after the frame currently being transmitted.

NOTE: *When queueing an idle frame, return the TE bit to logic 1 before the stop bit of the current frame shifts out to the TXD pin. Setting TE after the stop bit appears on TXD causes data previously written to SCIDRH and SCIDRL to be lost toggle TE for a queued idle frame while the TDRE flag is set and immediately before writing new data to SCIDRH and SCIDRL.*

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16.12 Receiver

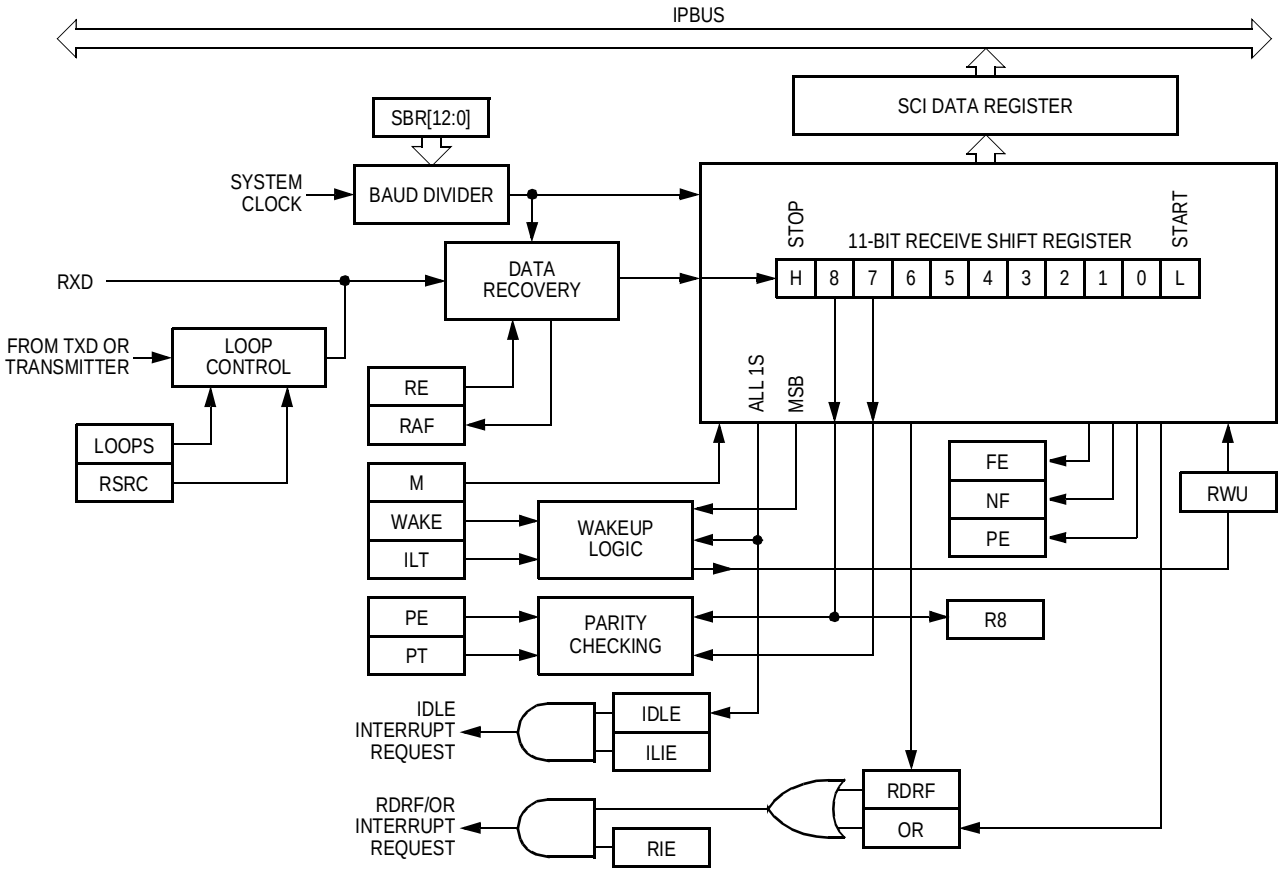

Figure 16-15. SCI Receiver Block Diagram

16.12.1 Frame Length

The receiver can handle either 8-bit or 9-bit data. The state of the M bit in SCICR1 selects frame length. When receiving 9-bit data, bit R8 in SCIDRH is the ninth bit (bit 8).

16.12.2 Receiving a Frame

When the SCI receives a frame, the receive shift register shifts the frame in from the RXD pin.

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After an entire frame shifts into the receive shift register, the data portion of the frame transfers to SCIDRH and SCIDRL. The RDRF flag is set, indicating that the received data can be read. If the RIE bit is also set, RDRF generates an interrupt request.

16.12.3 Data Sampling

The receiver samples the RXD pin at the RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock resynchronizes:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a 0 preceded by three 1s. When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

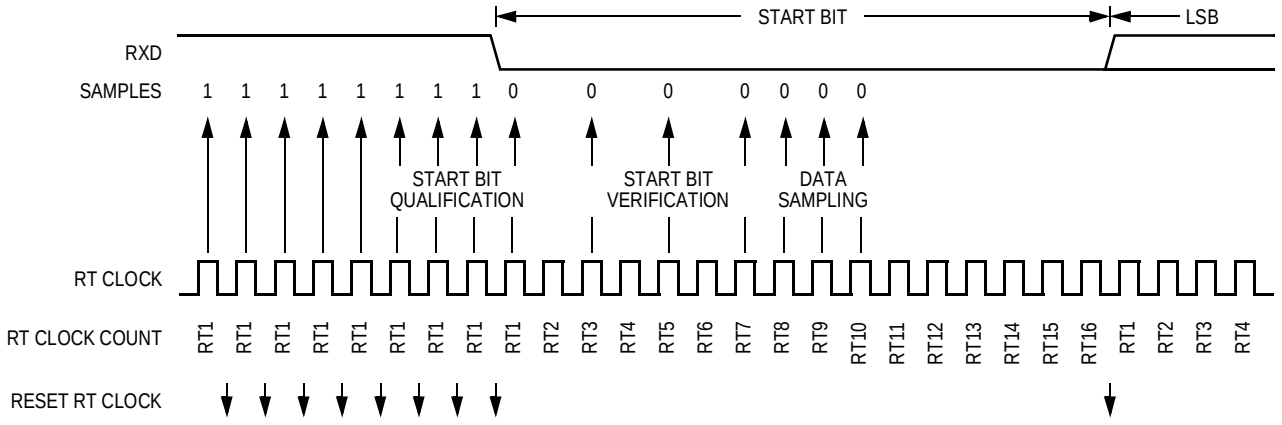

Figure 16-16. Receiver Data Sampling

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To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7.

Table 16-6. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

To determine the value of a data bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10.

Table 16-7. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE: *The RT8, RT9, and RT10 data samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 samples are logic 1s following a successful start bit verification, the NF flag is set and the receiver interprets the bit as a start bit (logic 0).*

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The RT8, RT9, and RT10 samples also verify stop bits.

Table 16-8. Stop Bit Recovery

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
000	1	0
001	1	1
010	1	1
011	0	1
100	1	1
101	0	1
110	0	1
111	0	0

In **Figure 16-17**, the verification samples RT3 and RT5 determine that the first low detected was noise and not the beginning of a start bit. The RT clock is reset and the start bit search begins again. The NF flag is not set because the noise occurred before the start bit was verified.

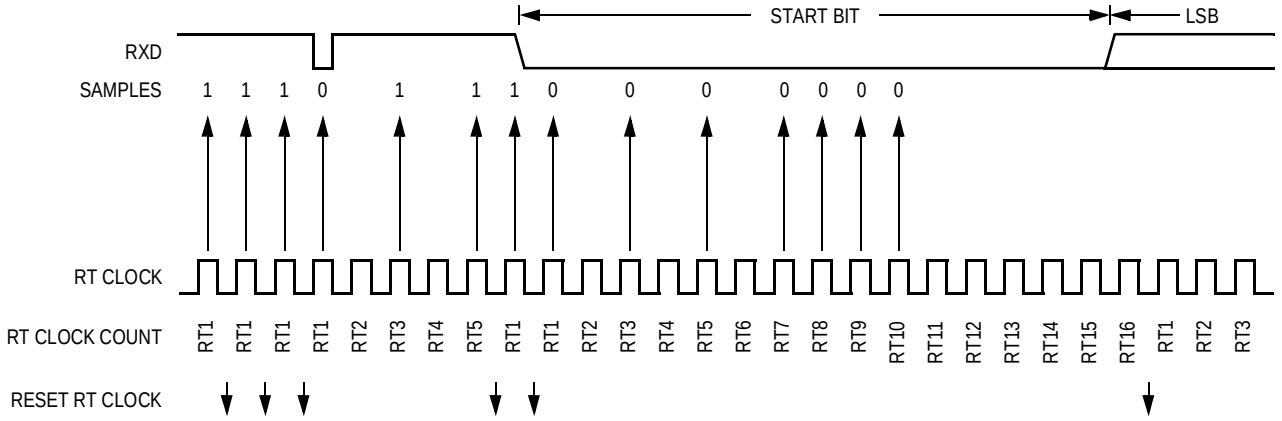

Figure 16-17. Start Bit Search Example 1

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In **Figure 16-18**, noise is perceived as the beginning of a start bit although the RT3 sample is high. The RT3 sample sets the noise flag. Although the perceived bit time is misaligned, the RT8, RT9, and RT10 data samples are within the bit time, and data recovery is successful.

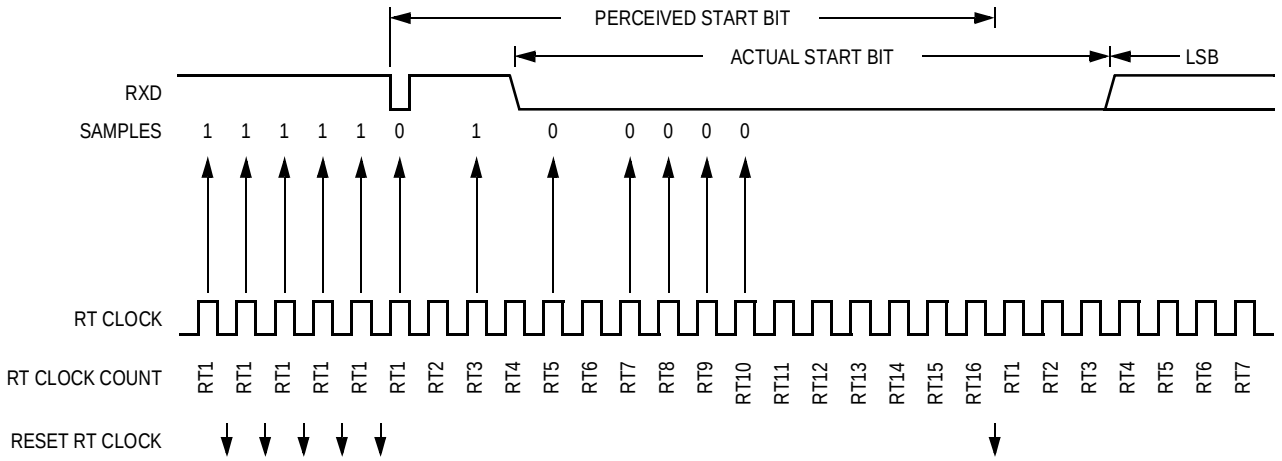

Figure 16-18. Start Bit Search Example 2

In **Figure 16-19** a large burst of noise is perceived as the beginning of a start bit, although the RT5 sample is high. The RT5 sample sets the noise flag. Although this is a worst-case misalignment of perceived bit time, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

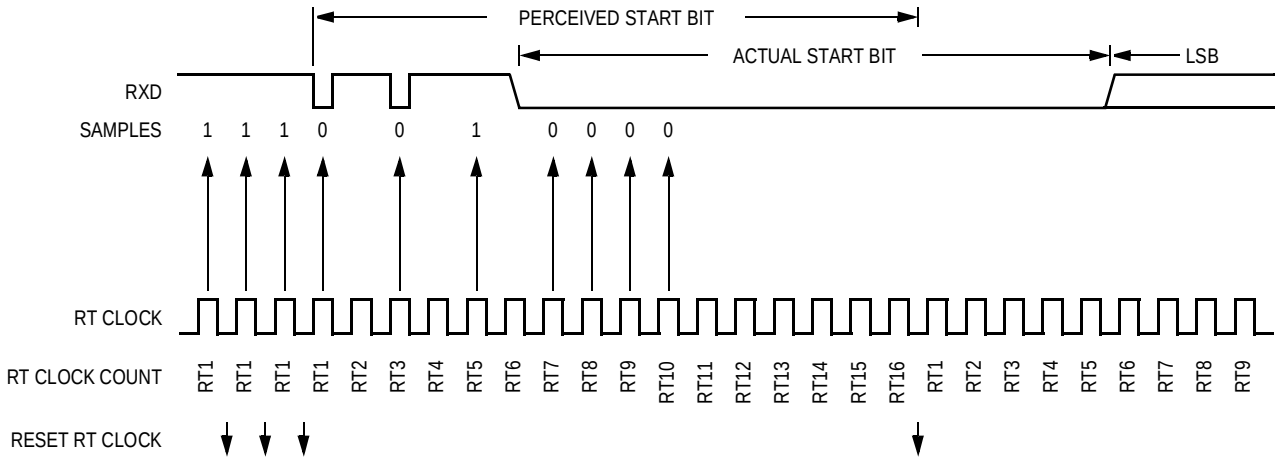

Figure 16-19. Start Bit Search Example 3

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Figure 16-20 shows the effect of noise early in the start bit time. Although this noise does not affect proper synchronization with the start bit time, it does set the noise flag.

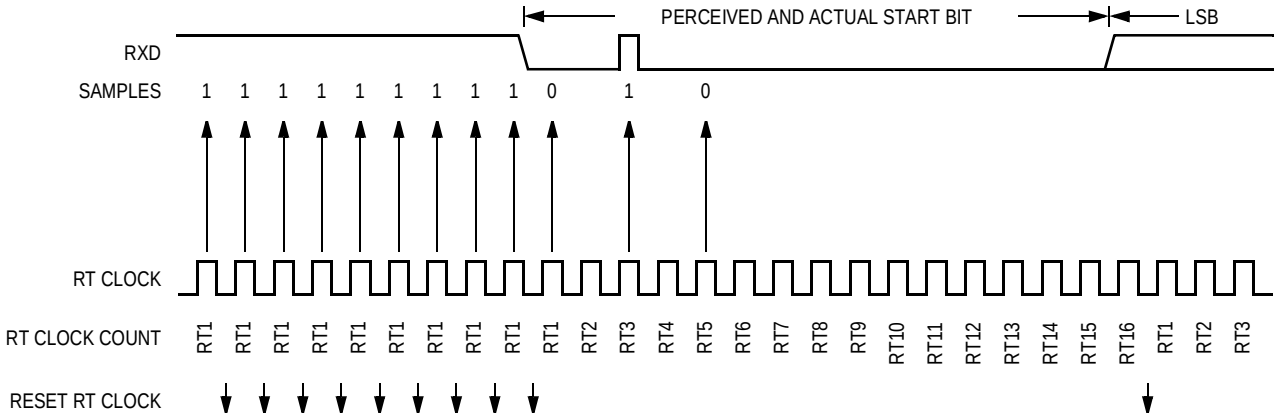

Figure 16-20. Start Bit Search Example 4

Figure 16-21 shows a burst of noise near the beginning of the start bit that resets the RT clock. The sample after the reset is low but is not preceded by three high samples that would qualify as a falling edge. Depending on the timing of the start bit search and on the data, the frame may be missed entirely or it may set the framing error flag.

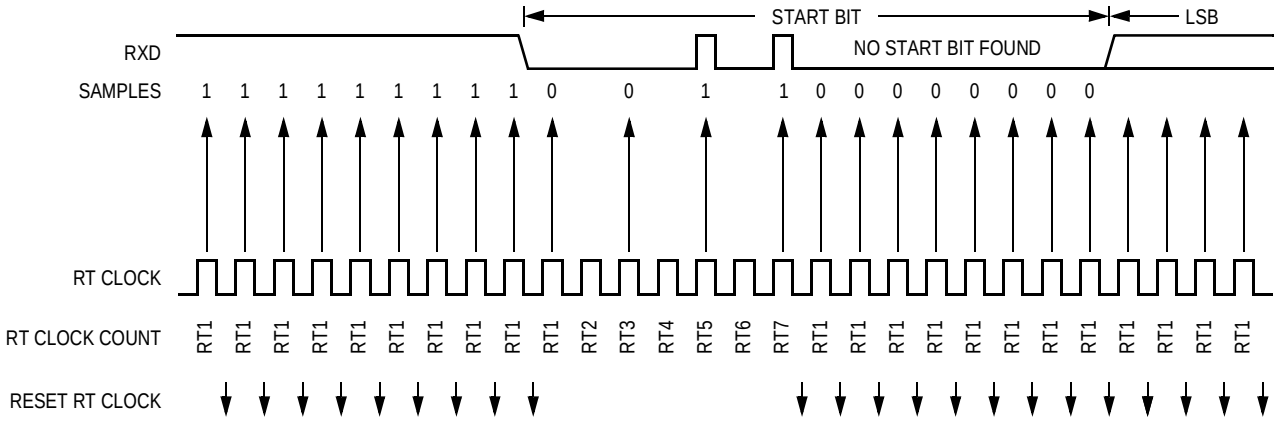

Figure 16-21. Start Bit Search Example 5

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In **Figure 16-22** a noise burst makes the majority of data samples RT8, RT9, and RT10 high. This sets the noise flag but does not reset the RT clock. In start bits only, the RT8, RT9, and RT10 data samples are ignored.

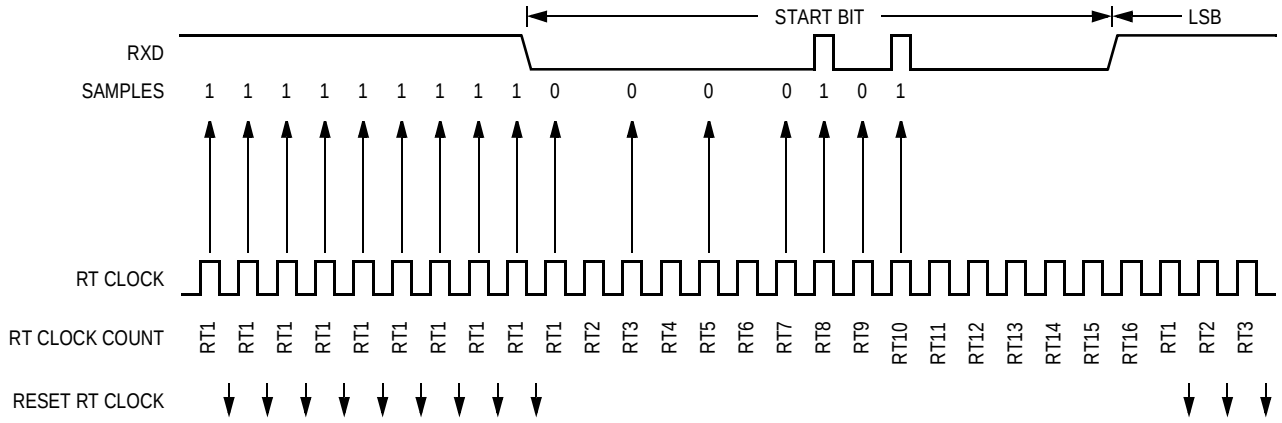

Figure 16-22. Start Bit Search Example 6

16.12.4 Framing Errors

If the data recovery logic does not detect a 1 where the stop bit should be in an incoming frame, it sets the FE flag in SCISR1. A break frame also sets the FE flag because a break frame has no stop bit. The FE flag is set at the same time that the RDRF flag is set.

16.12.5 Baud Rate Tolerance

A transmitting device may be operating at a baud rate below or above the receiver baud rate. Accumulated bit time misalignment can cause one of the RT8, RT9, and RT10 stop bit data samples to fall outside the stop bit. A noise error occurs if the samples are not all the same value. If more than one of the samples is outside the stop bit, a framing error occurs. In most applications, the baud rate tolerance is much more than the degree of misalignment that is likely to occur.

As the receiver samples an incoming frame, it resynchronizes the RT clock on any valid falling edge within the frame. Resynchronization within frames corrects misalignments between transmitter bit times and receiver bit times.

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16.12.5.1 Slow Data Tolerance

Figure 16-23 shows how much a slow received frame can be misaligned without causing a noise error or a framing error. The slow stop bit begins at RT8 instead of RT1 but arrives in time for the stop bit data samples at RT8, RT9, and RT10.

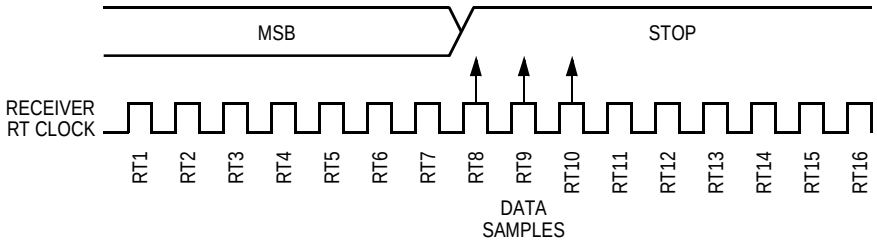

Figure 16-23. Slow Data

For 8-bit data, sampling of the stop bit takes the receiver:

9 bit times × 16 RT cycles + 10 RT cycles = 154 RT cycles.

With the misaligned data shown in **Figure 16-23**, the receiver counts 154 RT cycles at the point when the count of the transmitting device is:

9 bit times × 16 RT cycles + 3 RT cycles = 147 RT cycles.

The maximum percent difference between the receiver count and the transmitter count for slow 8-bit data with no errors is:

$$\left|\frac{154-147}{154}\right| \times 100 = 4.54\%$$

For 9-bit data, sampling of the stop bit takes the receiver:

10 bit times × 16 RT cycles + 10 RT cycles = 170 RT cycles.

With the misaligned data shown in **Figure 16-23**, the receiver counts 170 RT cycles at the point when the count of the transmitting device is:

10 bit times × 16 RT cycles + 3 RT cycles = 163 RT cycles.

The maximum percent difference between the receiver count and the transmitter count for slow 9-bit data with no errors is:

$$\left|\frac{170-163}{170}\right| \times 100 = 4.12\%$$

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16.12.5.2 Fast Data Tolerance

Figure 16-24 shows how much a fast received frame can be misaligned without causing a noise error or a framing error. The fast stop bit ends at RT10 instead of RT16 but is still sampled at RT8, RT9, and RT10.

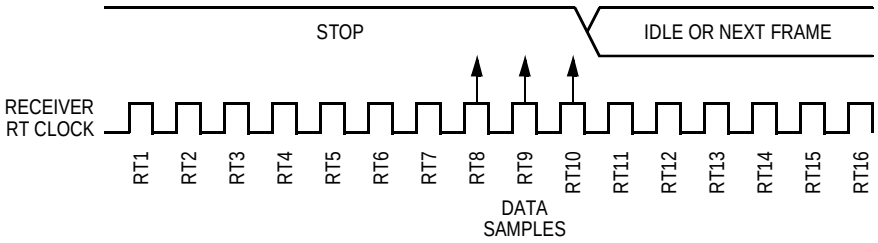

Figure 16-24. Fast Data

For 8-bit data, sampling of the stop bit takes the receiver:

$$9 \text{ bit times} \times 16 \text{ RT cycles} + 10 \text{ RT cycles} = 154 \text{ RT cycles.}$$

With the misaligned data shown in **Figure 16-24**, the receiver counts 154 RT cycles at the point when the count of the transmitting device is:

$$10 \text{ bit times} \times 16 \text{ RT cycles} = 160 \text{ RT cycles.}$$

The maximum percent difference between the receiver count and the transmitter count for fast 8-bit data with no errors is:

$$\left|\frac{154 - 160}{154}\right| \times 100 = 3.90\%$$

For 9-bit data, sampling of the stop bit takes the receiver:

$$10 \text{ bit times} \times 16 \text{ RT cycles} + 10 \text{ RT cycles} = 170 \text{ RT cycles.}$$

With the misaligned data shown in **Figure 16-24**, the receiver counts 170 RT cycles at the point when the count of the transmitting device is:

$$11 \text{ bit times} \times 16 \text{ RT cycles} = 176 \text{ RT cycles.}$$

The maximum percent difference between the receiver count and the transmitter count for fast 9-bit data with no errors is:

$$\left|\frac{170 - 176}{170}\right| \times 100 = 3.53\%$$

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16.12.6 Receiver Wakeup

So that the SCI can ignore transmissions intended only for other devices in multiple-receiver systems, the receiver can be put into a standby state. Setting the RWU bit in SCICR2 puts the receiver into a standby state during which receiver interrupts are disabled.

The transmitting device can address messages to selected receivers by including addressing information in the initial frame or frames of each message.

The WAKE bit in SCICR1 determines how the SCI is brought out of the standby state to process an incoming message. The WAKE bit enables either idle line wakeup or address mark wakeup.

16.12.6.1 Idle Input Line Wakeup (WAKE = 0)

When WAKE = 0, an idle condition on the RXD pin clears the RWU bit and wakes up the receiver. The initial frame or frames of every message contain addressing information. All receivers evaluate the addressing information, and receivers for which the message is addressed process the frames that follow. Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another idle frame appears on the RXD pin.

Idle line wakeup requires that messages be separated by at least one idle frame and that no message contains idle frames.

The idle frame that wakes up the receiver does not set the IDLE flag or the RDRF flag.

The ILT bit in SCICR1 determines whether the receiver begins counting logic 1s as idle frame bits after the start bit or after the stop bit.

16.12.6.2 Address Mark Wakeup (WAKE = 1)

When WAKE = 1, an address mark clears the RWU bit and wakes up the receiver. An address mark is a 1 in the most significant data bit position. The receiver interprets the data as address data. When using address mark wakeup, the MSB of all non-address data must be 0. User code must compare the address data to the receiver’s address and, if the

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addresses match, the receiver processes the frames that follow. If the addresses do not match, user code must put the receiver back to sleep by setting the RWU bit. The RWU bit remains set and the receiver remains on standby until another address frame appears on the RXD pin.

The address mark clears the RWU bit before the stop bit is received and sets the RDRF flag.

Address mark wakeup allows messages to contain idle frames but requires that the most significant byte (MSB) be reserved for address data.

NOTE: *With the WAKE bit clear, setting the RWU bit after the RXD pin has been idle can cause the receiver to wake up immediately.*

16.13 Single-Wire Operation

Normally, the SCI uses the TXD pin for transmitting and the RXD pin for receiving (LOOPS = 0, RSRC = X). In single-wire mode, the RXD pin is disconnected from the SCI and is available as a general-purpose I/O pin. The SCI uses the TXD pin for both receiving and transmitting.

In single-wire mode (LOOPS = 1, RXRC = 1), setting the data direction bit for the TXD pin configures TXD as the output for transmitted data. Clearing the data direction bit configures TXD as the input for received data.

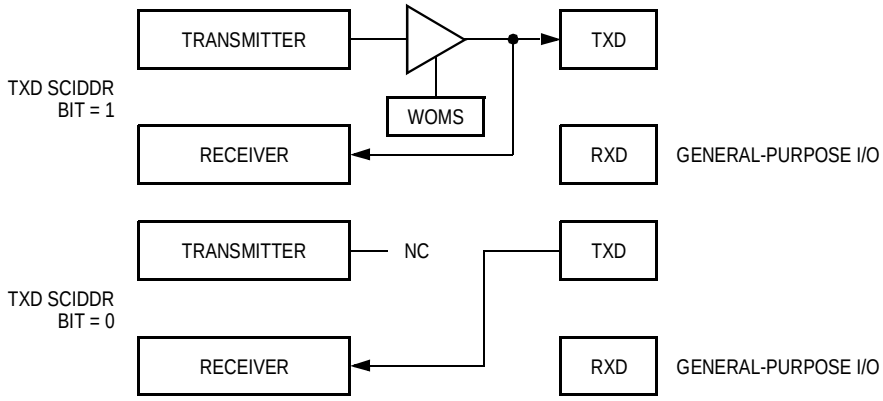

Figure 16-25. Single-Wire Operation (LOOPS = 1, RSRC = 1)

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Enable single-wire operation by setting the LOOPS bit and the RSRC bit in SCICR1. Setting the LOOPS bit disables the path from the RXD pin to the receiver. Setting the RSRC bit connects the receiver input to the output of the TXD pin driver. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

The WOMS bit in the SCICR1 register configures the TXD pin for full CMOS drive or for open-drain drive. WOMS controls the TXD pin in both normal operation and in single-wire operation. When WOMS is set, the DDR bit for the TXD pin does not have to be cleared for transmitter to receive data.

16.14 Loop Operation

In loop mode (LOOPS = 1, RSRC = 0), the transmitter output goes to the receiver input. The RXD pin is disconnected from the SCI and is available as a general-purpose I/O pin.

Setting the DDR bit for the TXD pin connects the transmitter output to the TXD pin. Clearing the data direction bit disconnects the transmitter output from the TXD pin.

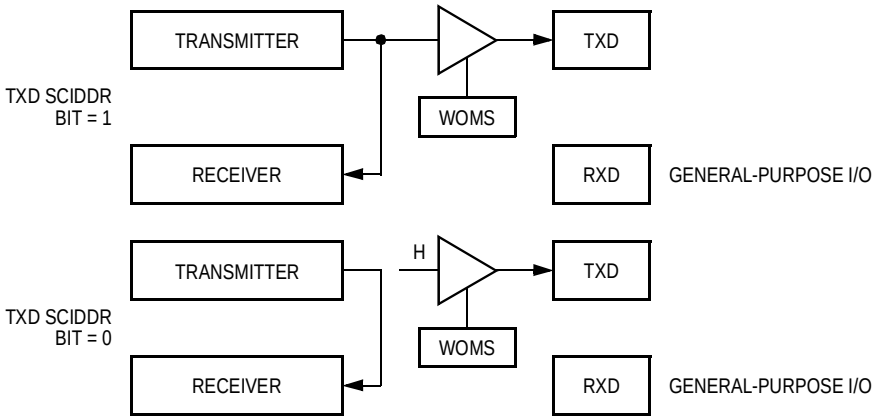

Figure 16-26. Loop Operation (LOOPS = 1, RSRC = 0)

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Enable loop operation by setting the LOOPS bit and clearing the RSRC bit in SCICR1. Setting the LOOPS bit disables the path from the RXD pin to the receiver. Clearing the RSRC bit connects the transmitter output to the receiver input. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

The WOMS bit in SCICR1 configures the TXD pin for full CMOS drive or for open-drain drive. WOMS controls the TXD pin during both normal operation and loop operation.

16.15 I/O Ports

The SCIPORT register is associated with two pins:

- The TXD pin is connected to SCIPORT1.
- The RXD pin is connected to SCIPORT0.

The SCI data direction register (SCIDDR) configures the pins as inputs or outputs. The SCI pullup and reduced drive register (SCIPURD) controls pin drive capability and enables or disables pullups. The WOMS bit in SCICR1 configures output ports as full CMOS drive outputs or as open-drain outputs.

Table 16-9. SCI Port Control Summary

Pullup Enable Control			Reduced Drive Control			Wired-OR Mode Control		
Register	**Bit**	**Reset State**	**Register**	**Bit**	**Reset State**	**Register**	**Bit**	**Reset State**
SCIPURD	PUPSCI	0	SCIPURD	RDPSCI	0	SCICR1	WOMS	CMOS drive

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16.16 Reset

Reset initializes the SCI registers to a known startup state as described in **16.7 Memory Map and Registers**.

16.17 Interrupts

Table 16-10 lists the five interrupt requests associated with each SCI module.

Table 16-10. SCI Interrupt Request Sources

Source	Flag	Enable Bit
Transmitter	TDRE	TIE
	TC	TCIE
Receiver	RDRF	RIE
	OR	RIE
	IDLE	ILIE

16.17.1 Transmit Data Register Empty

The TDRE flag is set when the transmit shift register receives a byte from the SCI data register. It signals that SCIDRH and SCIDRL are empty and can receive new data to transmit. If the TIE bit in SCICR2 is also set, TDRE generates an interrupt request. Clear TDRE by reading SCISR1 and then writing to SCIDRL. Reset sets TDRE.

16.17.2 Transmission Complete

The TC flag is set when TDRE = 1 and no data, preamble, or break frame is being transmitted. It signals that no transmission is in progress. If the TCIE bit is set in SCICR2, TC generates an interrupt request. When TC is set, the TXD pin is idle (logic 1). TC is cleared automatically when a data, preamble, or break frame is queued. Clear TC by reading SCISR1 with TC set and then writing to the SCIDRL register. TC cannot be cleared while a transmission is in progress.

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16.17.3 Receive Data Register Full

The RDRF flag is set when the data in the receive shift register transfers to SCIDRH and SCIDRL. It signals that the received data is available to be read. If the RIE bit is set in SCICR2, RDRF generates an interrupt request. Clear RDRF by reading SCISR1 and then reading SCIDRL.

16.17.4 Idle Receiver Input

The IDLE flag is set when 10 (if M = 0) or 11 (if M = 1) consecutive logic 1s appear on the receiver input. This signals an idle condition on the receiver input. If the ILIE bit in SCICR2 is set, IDLE generates an interrupt request. Once IDLE is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag. Clear IDLE by reading SCISR1 with IDLE set and then reading SCIDRL.

16.17.5 Overrun

The OR flag is set if data is not read from SCIDRL before the receive shift register receives the stop bit of the next frame. This signals a receiver overrun condition. If the RIE bit in SCICR2 is set, OR generates an interrupt request. The data in the shift register is lost, but the data already in SCIDRH and SCIDRL is not affected. Clear OR by reading SCISR1 and then reading SCIDRL.

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Section 17. Serial Peripheral Interface Module (SPI)

17.1 Contents

17.2 Introduction 372
17.3 Features 372
17.4 Modes of Operation 373
17.5 Block Diagram 373
17.6 Signal Description 374
17.6.1 MISO (Master In/Slave Out) 374
17.6.2 MOSI (Master Out/Slave In) 374
17.6.3 SCK (Serial Clock) 375
17.6.4 SS (Slave Select) 375
17.7 Memory Map and Registers 375
17.7.1 SPI Control Register 1 376
17.7.2 SPI Control Register 2 378
17.7.3 SPI Baud Rate Register 379
17.7.4 SPI Status Register 381
17.7.5 SPI Data Register 382
17.7.6 SPI Pullup and Reduced Drive Register 383
17.7.7 SPI Port Data Register 384
17.7.8 SPI Port Data Direction Register 385
17.8 Functional Description 386
17.8.1 Master Mode 387
17.8.2 Slave Mode 387
17.8.3 Transmission Formats 388
17.8.3.1 Transfer Format When CPHA = 1 388
17.8.3.2 Transfer Format When CPHA = 0 390
17.8.4 SPI Baud Rate Generation 393
17.8.5 Slave-Select Output 393
17.8.6 Bidirectional Mode 394

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17.8.7 Error Conditions 395
17.8.7.1 Write Collision Error 395
17.8.7.2 Mode Fault Error 395
17.8.8 Low-Power Mode Options 396
17.8.8.1 Run Mode 396
17.8.8.2 Doze Mode. 396
17.8.8.3 Stop Mode 396
17.9 Reset 397
17.10 Interrupts. 397
17.10.1 SPI Interrupt Flag (SPIF) 397
17.10.2 Mode Fault (MODF) Flag 397

17.2 Introduction

The serial peripheral interface (SPI) module allows full-duplex, synchronous, serial communication between the microcontroller unit (MCU) and peripheral devices. Software can poll the SPI status flags or SPI operation can be interrupt driven.

17.3 Features

Features include:

- Master mode and slave mode
- Wired-OR mode
- Slave-select output
- Mode fault error flag with central processor unit (CPU) interrupt capability
- Double-buffered operation
- Serial clock with programmable polarity and phase
- Control of SPI operation during doze mode
- Reduced drive control for lower power consumption

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17.4 Modes of Operation

The SPI functions in these three modes:

1. Run mode — Run mode is the normal mode of operation.
2. Doze mode — Doze mode is a configurable low-power mode.
3. Stop mode — The SPI is inactive in stop mode.

17.5 Block Diagram

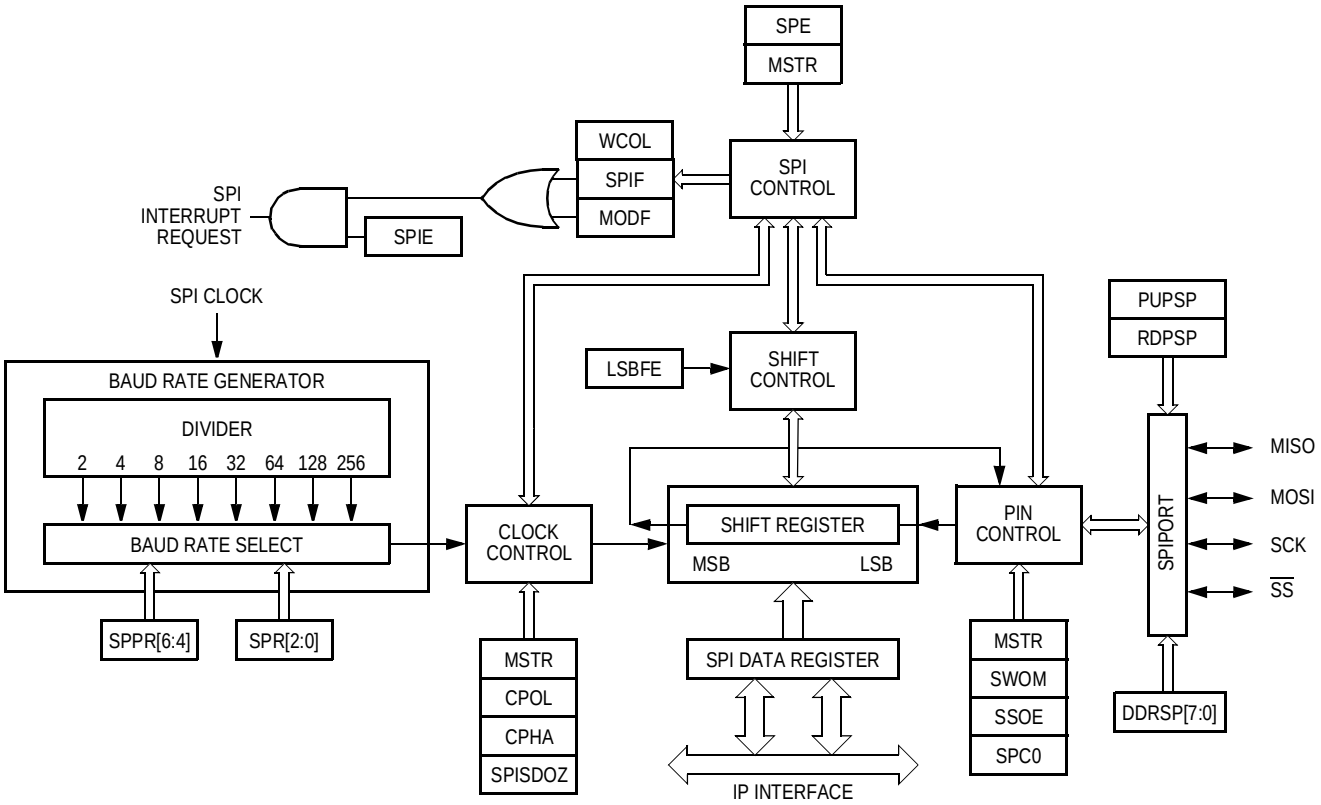

Figure 17-1. SPI Block Diagram

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17.6 Signal Description

An overview of the signals is provided in **Table 17-1**.

Table 17-1. Signal Properties

Name	Port	Function(1)	Reset State
MISO	SPIPORT0	Master data in/slave data out	0
MOSI	SPIPORT1	Master data out/slave data in	0
SCK	SPIPORT2	Serial clock	0
$\overline{SS}$	SPIPORT3	Slave select	0

1. The SPI ports (MISO, MOSI, SCK, and $\overline{SS}$) are general-purpose I/O ports when the SPI is disabled (SPE = 0).

17.6.1 MISO (Master In/Slave Out)

MISO is one of the two SPI data pins.

In master mode, MISO is the data input. In slave mode, MISO is the data output and is three-stated until a master drives the $\overline{SS}$ input pin low.

In bidirectional mode, a slave MISO pin is the SISO pin (slave in/slave out).

In a multiple-master system, all MISO pins are tied together.

17.6.2 MOSI (Master Out/Slave In)

MOSI is one of the two SPI data pins.

In master mode, MOSI is the data output. In slave mode, MOSI is the data input.

In bidirectional mode, a master MOSI pin is the MOMI pin (master out/master in).

In a multiple-master system, all MOSI pins are tied together.

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17.6.3 SCK (Serial Clock)

The SCK pin is the serial clock pin for synchronizing transmissions between master and slave devices. In master mode, SCK is an output. In slave mode, SCK is an input.

In a multiple-master system, all SCK pins are tied together.

17.6.4 $\overline{SS}$ (Slave Select)

In master mode, the $\overline{SS}$ pin can be:

- A mode-fault input
- A general-purpose input
- A general-purpose output
- A slave-select output

In slave mode, the $\overline{SS}$ pin is always a slave-select input.

17.7 Memory Map and Registers

Table 17-2 shows the SPI memory map.

NOTE: *Reading reserved addresses (0x00cb_004 and 0x00cb_0009 through 0x00cb_000b) and unimplemented addresses (0x00cb_000c through 0x00cb_000f) returns 0s. Writing to unimplemented addresses has no effect. Accessing unimplemented addresses does not generate an error response.*

Table 17-2. SPI Memory Map

Address	Bits 7–0	Access(1)
0x00cb_0000	SPI control register 1 (SPICR1)	S/U
0x00cb_0001	SPI control register 2 (SPICR2)	S/U
0x00cb_0002	SPI baud rate register (SPIBR)	S/U
0x00cb_0003	SPI status register (SPISR)	S/U
0x00cb_0005	SPI data register (SPIDR)	S/U
0x00cb_0006	SPI pullup and reduced drive register (SPIPURD)	S/U
0x00cb_0007	SPI port data register (SPIPORT)	S/U
0x00cb_0008	SPI port data direction register (SPIDDR)	S/U

1. S/U = CPU supervisor or user mode access. User mode accesses to supervisor only addresses have no effect and result in a cycle termination transfer error.

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17.7.1 SPI Control Register 1

Address: 0x00cb_0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIE	SPE	SWOM	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset:	0	0	0	0	0	1	0	0

Figure 17-2. SPI Control Register 1 (SPICR1)

Read: Anytime

Write: Anytime

SPIE — SPI Interrupt Enable Bit

The SPIE bit enables the SPIF and MODF flags to generate interrupt requests. Reset clears SPIE.

1 = SPIF and MODF interrupt requests enabled
0 = SPIF and MODF interrupt requests disabled

SPE — SPI System Enable Bit

The SPE bit enables the SPI and dedicates SPI port pins [3:0] to SPI functions. When SPE is clear, the SPI system is initialized but in a low-power disabled state. Reset clears SPE.

1 = SPI enabled
0 = SPI disabled

SWOM — SPI Wired-OR Mode Bit

The SWOM bit configures the output buffers of SPI port pins [3:0] as open-drain outputs. SWOM controls SPI port pins [3:0] whether they are SPI outputs or general-purpose outputs. Reset clears SWOM.

1 = Output buffers of SPI port pins [3:0] open-drain
0 = Output buffers of SPI port pins [3:0] CMOS drive

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MSTR — Master Bit

The MSTR bit selects SPI master mode or SPI slave mode operation. Reset clears MSTR.

1 = Master mode
0 = Slave mode

CPOL — Clock Polarity Bit

The CPOL bit selects an inverted or non-inverted SPI clock. To transmit data between SPI modules, the SPI modules must have identical CPOL values. Reset clears CPOL.

1 = Active-low clock; SCK idles high
0 = Active-high clock; SCK idles low

CPHA — Clock Phase Bit

The CPHA bit delays the first edge of the SCK clock. Reset sets CPHA.

1 = First SCK edge at start of transmission
0 = First SCK edge 1/2 cycle after start of transmission

SSOE — Slave Select Output Enable Bit

The SSOE bit and the DDRSP3 bit configure the $\overline{SS}$ pin as a general-purpose input or a slave-select output. Reset clears SSOE.

Table 17-3. $\overline{SS}$ Pin I/O Configurations

DDRSP3	SSOE	Master Mode	Slave Mode
0	0	Mode-fault input	Slave-select input
0	1	General-purpose input	Slave-select input
1	0	General-purpose output	Slave-select input
1	1	Slave-select output	Slave-select input

NOTE: *Setting the SSOE bit disables the mode fault detect function.*

LSBFE — LSB-First Enable Bit

The LSBFE enables data to be transmitted LSB first. Reset clears LSBFE.

1 = Data transmitted LSB first.
0 = Data transmitted MSB first

NOTE: *In SPIDR, the MSB is always bit 7 regardless of the LSBFE bit.*

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17.7.2 SPI Control Register 2

Address: 0x00cb_0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	SPISDOZ	SPC0
Write:								
Reset:	0	0	0	0	0	1	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 17-3. SPI Control Register 2 (SPICR2)

Read: Anytime

Write: Anytime; writing to unimplemented bits has no effect

SPISDOZ — SPI Stop in Doze Bit

The SPIDOZ bit stops the SPI clocks when the CPU is in doze mode. Reset clears SPISDOZ.

1 = SPI inactive in doze mode
0 = SPI active in doze mode

SPC0 — Serial Pin Control Bit 0

The SPC0 bit enables the bidirectional pin configurations shown in **Table 17-4**. Reset clears SPC0.

Table 17-4. Bidirectional Pin Configurations

	Pin Mode	SPC0	MSTR	MISO Pin[1]	MOSI Pin[2]	SCK Pin[3]	$\overline{SS}$ Pin[4]
A	Normal	0	0	Slave data output	Slave data input	SCK input	Slave-select input
B			1	Master data input	Master data output	SCK output	MODF input (DDRSP3 = 0) or GP output (DDRSP3 = 1)
C	Bidirectional	1	0	Slave data I/O	GP[5] I/O	SCK input	Slave-select input
D			1	GP I/O	Master data I/O	SCK output	MODF input (DDRSP3 = 0) or GP output (DDRSP3 = 1)

1. Slave output is enabled if SPIDDR bit 0 = 1, $\overline{SS}$ = 0, and MSTR = 0 (A, C).
2. Master output is enabled if SPIDDR bit 1 = 1 and MSTR = 1 (B, D).
3. SCK output is enabled if SPIDDR bit 2 = 1 and MSTR = 1 (B, D).
4. $\overline{SS}$ output is enabled if SPIDDR bit 3 = 1, SPICR1 bit 1 (SSOE) = 1, and MSTR = 1 (B, D).
5. GP = General-purpose

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17.7.3 SPI Baud Rate Register

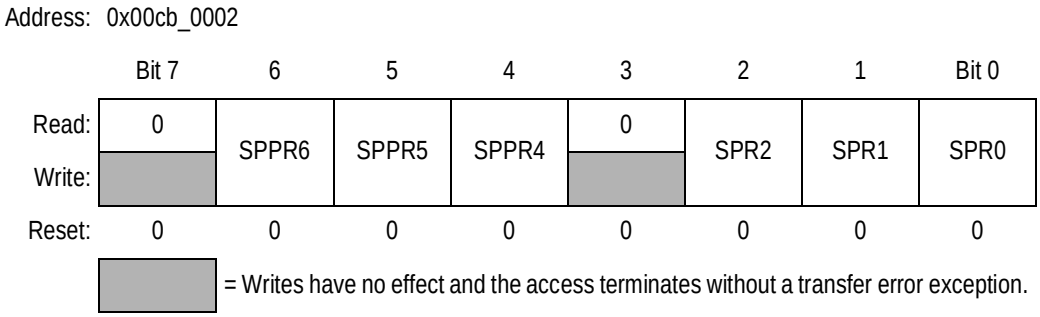

Figure 17-4. SPI Baud Rate Register (SPIBR)

Read: Anytime

Write: Anytime; writing to unimplemented bits has no effect

SPPR[6:4] — SPI Baud Rate Preselection Bits

The SPPR[6:4] and SPR[2:0] bits select the SPI clock divisor as shown in **Table 17-5**. Reset clears SPPR[6:4] and SPR[2:0], selecting an SPI clock divisor of 2.

SPR[2:0] — SPI Baud Rate Bits

The SPPR[6:4] and SPR[2:0] bits select the SPI clock divisor as shown in **Table 17-5**. Reset clears SPPR[6:4] and SPR[2:0], selecting an SPI clock divisor of 2.

NOTE: *Writing to SPIBR during a transmission may cause spurious results.*

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Table 17-5. SPI Baud Rate Selection (33-MHz Module Clock)

SPPR[6:4]	SPR[2:0]	SPI Clock Divisor	Baud Rate	SPPR[6:4]	SPR[2:0]	SPI Clock Divisor	Baud Rate
000	000	2	16.5 MHz	100	000	10	3.3 MHz
000	001	4	8.25 MHz	100	001	20	1.65 MHz
000	010	8	4.125 MHz	100	010	40	825 MHz
000	011	16	2.06 MHz	100	011	80	412.5 kHz
000	100	32	1.03 MHz	100	100	160	206.25 kHz
000	101	64	515.62 kHz	100	101	320	103.13 kHz
000	110	128	257.81 kHz	100	110	640	51.56 kHz
000	111	256	128.9 kHz	100	111	1280	25.78 kHz
001	000	4	8.25 MHz	101	000	12	2.75 MHz
001	001	8	4.12 MHz	101	001	24	1.375 MHz
001	010	16	2.06 MHz	101	010	48	687.5 kHz
001	011	32	1.03 MHz	101	011	96	343.75 kHz
001	100	64	515.62 kHz	101	100	192	171.88 kHz
001	101	128	257.81 kHz	101	101	384	85.94 kHz
001	110	256	128.9 kHz	101	110	768	42.97 kHz
001	111	512	64.45 kHz	101	111	1536	21.48 kHz
010	000	6	5.5 MHz	110	000	14	2.36 MHz
010	001	12	2.75 MHz	110	001	28	1.18 MHz
010	010	24	1.375 MHz	110	010	56	589.29 kHz
010	011	48	687.5 kHz	110	011	112	296.64 kHz
010	100	96	343.75 kHz	110	100	224	147.32 kHz
010	101	192	171.88 kHz	110	101	448	73.66 kHz
010	110	384	85.94 kHz	110	110	896	36.83 kHz
010	111	768	42.97 kHz	110	111	1792	18.42 kHz
011	000	8	4.13 MHz	111	000	16	2.06 MHz
011	001	16	2.06 MHz	111	001	32	1.03 MHz
011	010	32	1.03 MHz	111	010	64	515.63 kHz
011	011	64	515.63 kHz	111	011	128	257.81 kHz
011	100	128	257.81 kHz	111	100	256	128.91 kHz
011	101	256	128.91 kHz	111	101	512	64.45 kHz
011	110	512	64.45 kHz	111	110	1024	32.23 kHz
011	111	1024	32.23 kHz	111	111	2048	16.11 kHz

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17.7.4 SPI Status Register

Address: 0x00cb_0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SPIF	WCOL	0	MODF	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 17-5. SPI Status Register (SPISR)

Read: Anytime

Write: Has no meaning or effect

SPIF — SPI Interrupt Flag

The SPIF flag is set after the eighth SCK cycle in a transmission when received data transfers from the shift register to SPIDR. If the SPIE bit is also set, SPIF generates an interrupt request. Once SPIF is set, no new data can be transferred into SPIDR until SPIF is cleared. Clear SPIF by reading SPISR with SPIF set and then accessing SPIDR. Reset clears SPIF.

1 = New data available in SPIDR
0 = No new data available in SPIDR

WCOL — Write Collision Flag

The WCOL flag is set when software writes to SPIDR during a transmission. Clear WCOL by reading SPISR with WCOL set and then accessing SPIDR. Reset clears WCOL.

1 = Write collision
0 = No write collision

MODF — Mode Fault Flag

The MODF flag is set when the $\overline{SS}$ pin of a master SPI is driven low and the $\overline{SS}$ pin is configured as a mode-fault input. If the SPIE bit is also set, MODF generates an interrupt request. A mode fault clears the SPE, MSTR, and DDRSP[2:0] bits. Clear MODF by reading SPISR with MODF set and then writing to SPICR1. Reset clears MODF.

1 = Mode fault
0 = No mode fault

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17.7.5 SPI Data Register

Address: 0x00cb_0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	6	5	4	3	2	1	BIT 0
Reset:	0	0	0	0	0	0	0	0

Figure 17-6. SPI Data Register (SPIDR)

Read: Anytime; normally read only after SPIF is set

Write: Anytime; see WCOL

SPIDR is both the input and output register for SPI data. Writing to SPIDR while a transmission is in progress sets the WCOL flag and disables the attempted write. Read SPIDR after the SPIF flag is set and before the end of the next transmission. If the SPIF flag is not serviced before a new byte enters the shift register, the new byte and any successive bytes are lost. The byte already in the SPIDR remains there until SPIF is serviced.

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17.7.6 SPI Pullup and Reduced Drive Register

Address: 0x00cb_0006

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	RSVD5	RDPSP	0	0	RSVD1	PUPSP
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 17-7. SPI Pullup and Reduced Drive Register (SPIPURD)

Read: Anytime

Write: Anytime; writing to unimplemented bits has no effect

RSVD5 and RSVD1 — Reserved

Writing to these read/write bits updates their values but has no effect on functionality.

RDPSP — SPI Port Reduced Drive Control Bit

1 = Reduced drive capability on SPIPORT bits [7:4]
0 = Full drive enabled on SPIPORT bits [7:4]

PUPSP — SPI Port Pullup Enable Bit

1 = Pullup devices enabled for SPIPORT bits [3:0]
0 = Pullup devices disabled for SPIPORT bits [3:0]

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17.7.7 SPI Port Data Register

Address: 0x00cb_0007

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RSVD7	RSVD6	RSVD5	RSVD4	PORTSP3	PORTSP2	PORTSP1	PORTSP0
Reset:	0	0	0	0	0	0	0	0
Pin function:					$\overline{SS}$	SCK	MOSI/ MOMI	MISO/ SISO

Figure 17-8. SPI Port Data Register (SPIPORT)

Read: Anytime

Write: Anytime

RSVD[7:4] — Reserved

Writing to these read/write bits updates their values but has no effect on functionality.

PORTSP[3:0] — SPI Port Data Bits

Data written to SPIPORT drives pins only when they are configured as general-purpose outputs.

Reading an input (DDRSP bit clear) returns the pin level; reading an output (DDRSP bit set) returns the pin driver input level.

Writing to any of the PORTSP[3:0] pins does not change the pin state when the pin is configured for SPI output.

SPIPORT I/O function depends upon the state of the SPE bit in SPICR1 and the state the DDRSP bits in SPIDDR.

Table 17-6. SPI Port Summary

Pullup Enable Control			Reduced Drive Control			Wired-OR Mode Control		
Register	**Bit**	**Reset State**	**Register**	**Bit**	**Reset State**	**Register**	**Bit**	**Reset State**
SPIPURD	PUPSP	0	SPIPURD	RDPSP[1:0]	Full drive	SPICR1	SWOM	Normal

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17.7.8 SPI Port Data Direction Register

Address: 0x00cb_0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RSVD7	RSVD6	RSVD5	RSVD4	DDRSP3	DDRSP2	DDRSP1	DDRSP0
Reset:	0	0	0	0	0	0	0	0
Pin function:					$\overline{SS}$	SCK	MOSI/ MOMI	MISO/ SISO

Figure 17-9. SPI Port Data Direction Register (SPIDDR)

Read: Anytime

Write: Anytime

RSVD[7:4] — Reserved

Writing to these read/write bits updates their values but has no effect on functionality.

DDRSP[3:0] — Data Direction Bits

The DDRSP[3:0] bits control the data direction of SPIPORT pins. Reset clears DDRSP[3:0].

1 = Corresponding pin configured as output
0 = Corresponding pin configured as input

In slave mode, DDRSP3 has no meaning or effect. In master mode, DDRSP3 determines whether SPI port pin 3 is a mode-fault input, a general-purpose output, or a slave-select output.

NOTE: *When the SPI is enabled (SPE = 1), the MISO, MOSI, and SCK pins:*

- *Are inputs if their SPI functions are input functions regardless of the state of their DDRSP bits.*
- *Are outputs if their SPI functions are output functions only if their DDRSP bits are set.*

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17.8 Functional Description

The SPI module allows full-duplex, synchronous, serial communication between the MCU and peripheral devices. Software can poll the SPI status flags or SPI operation can be interrupt driven.

Setting the SPE bit in SPICR1 enables the SPI and dedicates four SPI port pins to SPI functions:

- Slave select ($\overline{SS}$)
- Serial clock (SCK)
- Master out/slave in (MOSI)
- Master in/slave out (MISO)

When the SPE bit is clear, the $\overline{SS}$, SCK, MOSI, and MISO pins are general-purpose I/O pins controlled by SPIDDR.

The 8-bit shift register in a master SPI is linked by the MOSI and MISO pins to the 8-bit shift register in the slave. The linked shift registers form a distributed 16-bit register. In an SPI transmission, the SCK clock from the master shifts the data in the 16-bit register eight bit positions, and the master and slave exchange data. Data written to the master SPIDR register is the output data to the slave. After the exchange, data read from the master SPIDR is the input data from the slave.

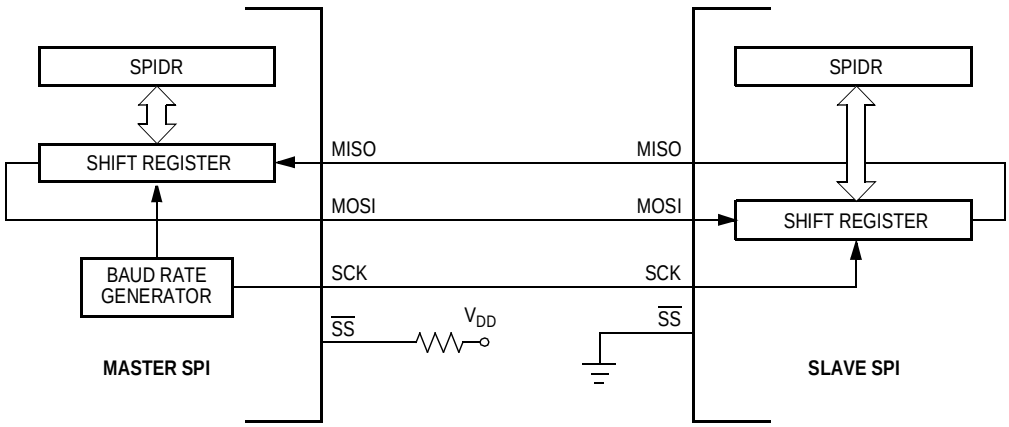

Figure 17-10. Full-Duplex Operation

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17.8.1 Master Mode

Setting the MSTR bit in SPICR1 puts the SPI in master mode. Only a master SPI can initiate a transmission. Writing to the master SPIDR begins a transmission. If the shift register is empty, the byte transfers to the shift register and begins shifting out on the MOSI pin under the control of the master SCK clock. The SCK clock starts one-half SCK cycle after writing to SPIDR.

The SPR[2:0] and SPPR[6:4] bits in SPIBR control the baud rate generator and determine the speed of the shift register. The SCK pin is the SPI clock output. Through the SCK pin, the baud rate generator of the master controls the shift register of the slave.

The MSTR bit in SPICR1 and the SPC0 bit in SPICR2 control the function of the data pins, MOSI and MISO.

The $\overline{SS}$ pin is normally an input that remains in the inactive high state. Setting the DDRSP3 bit in SPIDDR configures $\overline{SS}$ as an output. The DDRSP3 bit and the SSOE bit in SPICR1 can configure $\overline{SS}$ for general-purpose I/O, mode fault detection, or slave selection.
See **Table 17-3**.

The $\overline{SS}$ output goes low during each transmission and is high when the SPI is in the idle state. Driving the master $\overline{SS}$ input low sets the MODF flag in SPISR, indicating a mode fault. More than one master may be trying to drive the MOSI and SCK lines simultaneously. A mode fault clears the data direction bits of the MISO, MOSI (or MOMI), and SCK pins to make them inputs. A mode fault also clears the SPE and MSTR bits in SPICR1. If the SPIE bit is also set, the MODF flag generates an interrupt request.

17.8.2 Slave Mode

Clearing the MSTR bit in SPICR1 puts the SPI in slave mode. The SCK pin is the SPI clock input from the master, and the $\overline{SS}$ pin is the slave-select input. For a transmission to occur, the $\overline{SS}$ pin must be driven low and remain low until the transmission is complete.

The MSTR bit and the SPC0 bit in SPICR2 control the function of the data pins, MOSI and MISO. The $\overline{SS}$ input also controls the MISO pin. If $\overline{SS}$ is low, the MSB in the shift register shifts out on the MISO pin. If $\overline{SS}$

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is high, the MISO pin is in a high impedance state, and the slave ignores the SCK input.

NOTE: *When using peripherals with full-duplex capability, do not simultaneously enable two receivers that drive the same MISO output line.*

As long as only one slave drives the master input line, it is possible for several slaves to receive the same transmission simultaneously.

If the CPHA bit in SPICR1 is clear, odd-numbered edges on the SCK input latch the data on the MOSI pin. Even-numbered edges shift the data into the LSB position of the SPI shift register and shift the MSB out to the MISO pin.

If the CPHA bit is set, even-numbered edges on the SCK input latch the data on the MOSI pin. Odd-numbered edges shift the data into the LSB position of the SPI shift register and shift the MSB out to the MISO pin.

The transmission is complete after the eighth shift. The received data transfers to SPIDR, setting the SPIF flag in SPISR.

17.8.3 Transmission Formats

The CPHA and CPOL bits in SPICR1 select one of four combinations of serial clock phase and polarity. Clock phase and polarity must be identical for the master SPI device and the communicating slave device.

17.8.3.1 Transfer Format When CPHA = 1

Some peripherals require the first SCK edge to occur before the slave MSB becomes available at its MISO pin. When the CPHA bit is set, the master SPI waits for a synchronization delay of one-half SCK clock cycle. Then it issues the first SCK edge at the beginning of the transmission. The first edge causes the slave to transmit its MSB to the MISO pin of the master. The second edge and the following even-numbered edges latch the data. The third edge and the following odd-numbered edges shift the latched slave data into the master shift register and shift master data out on the master MOSI pin.

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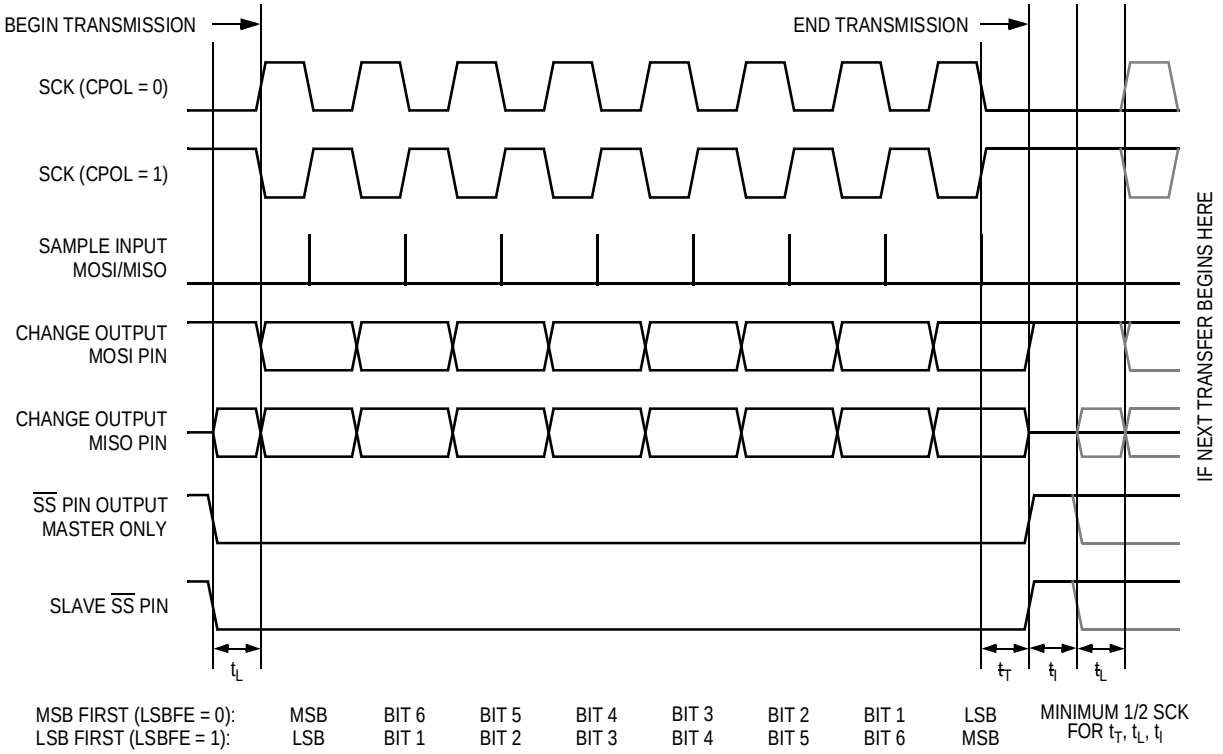
After the 16th and final SCK edge:

- Data that was in the master SPIDR register is in the slave SPIDR. Data that was in the slave SPIDR register is in the master SPIDR.
- The SCK clock stops and the SPIF flag in SPISR is set, indicating that the transmission is complete. If the SPIE bit in SPCR1 is set, SPIF generates an interrupt request.

Figure 17-11 shows the timing of a transmission with the CPHA bit set. The $\overline{SS}$ pin of the master must be either high or configured as a general-purpose output not affecting the SPI.



Legend:
t_L = Minimum leading time before the first SCK edge
t_T = Minimum trailing time after the last SCK edge
t_I = Minimum idling time between transmissions (minimum SS high time)
t_L, t_T, and t_I are guaranteed for master mode and required for slave mode.

Figure 17-11. SPI Clock Format 1 (CPHA = 1)

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When CPHA = 1, the slave $\overline{SS}$ line can remain low between bytes. This format is good for systems with a single master and a single slave driving the MISO data line.

Writing to SPIDR while a transmission is in progress sets the WCOL flag to indicate a write collision and inhibits the write. WCOL does not generate an interrupt request; the SPIF interrupt request comes at the end of the transfer that was in progress at the time of the error.

17.8.3.2 Transfer Format When CPHA = 0

In some peripherals, the slave MSB is available at its MISO pin as soon as the slave is selected. When the CPHA bit is clear, the master SPI delays its first SCK edge for half a SCK cycle after the transmission starts. The first edge and all following odd-numbered edges latch the slave data. Even-numbered SCK edges shift slave data into the master shift register and shift master data out on the master MOSI pin.

After the 16th and final SCK edge:

- Data that was in the master SPIDR is in the slave SPIDR. Data that was in the slave SPIDR is in the master SPIDR.
- The SCK clock stops and the SPIF flag in SPISR is set, indicating that the transmission is complete. If the SPIE bit in SPCR1 is set, SPIF generates an interrupt request.

Figure 17-12 shows the timing of a transmission with the CPHA bit clear. The $\overline{SS}$ pin of the master must be either high or configured as a general-purpose output not affecting the SPI.

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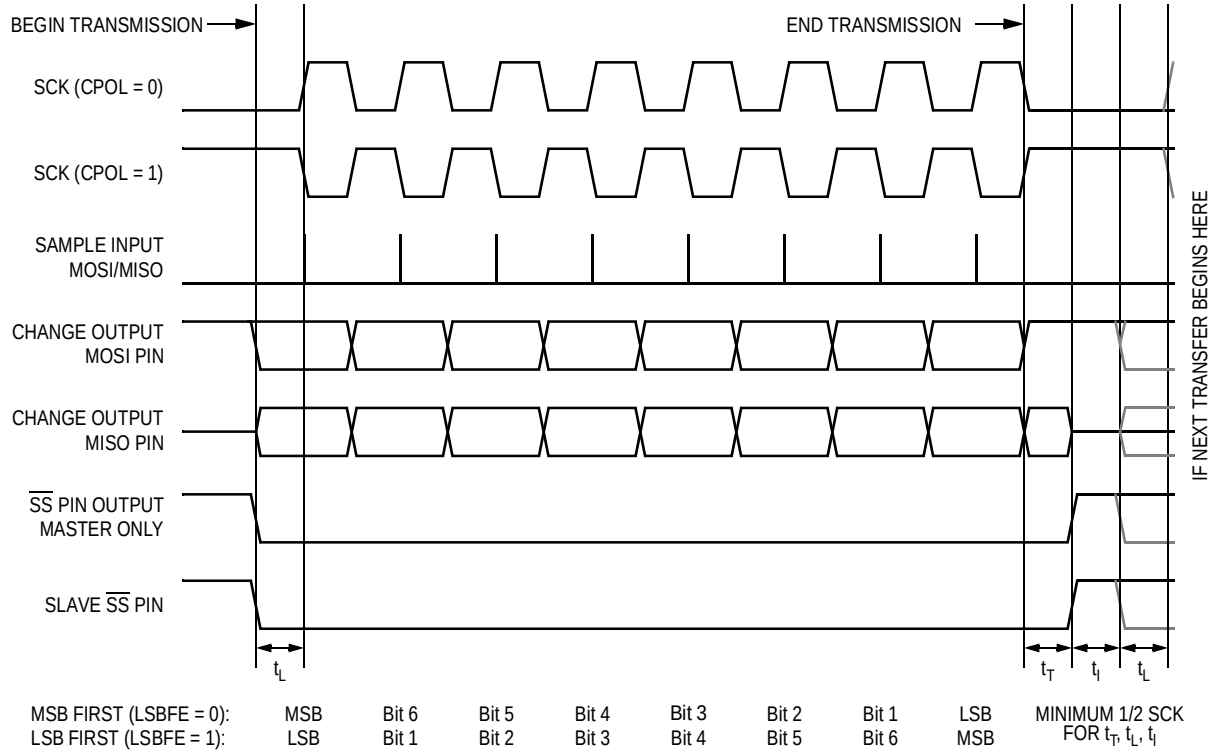

Legend:
t_L = Minimum leading time before the first SCK edge
t_T = Minimum trailing time after the last SCK edge
t_I = Minimum idling time between transmissions (minimum $\overline{SS}$ high time)
t_L, t_T, and t_I are guaranteed for master mode and required for slave mode.

Figure 17-12. SPI Clock Format 0 (CPHA = 0)

When CPHA = 0, the slave $\overline{SS}$ pin must be negated and reasserted between bytes.

NOTE: *Clock skew between the master and slave can cause data to be lost when:*

- *CPHA = 0, and,*
- *The baud rate is the SPI clock divided by two, and*
- *The master SCK frequency is half the slave SPI clock frequency, and*
- *Software writes to the slave SPIDR just before the synchronized $\overline{SS}$ signal goes low.*

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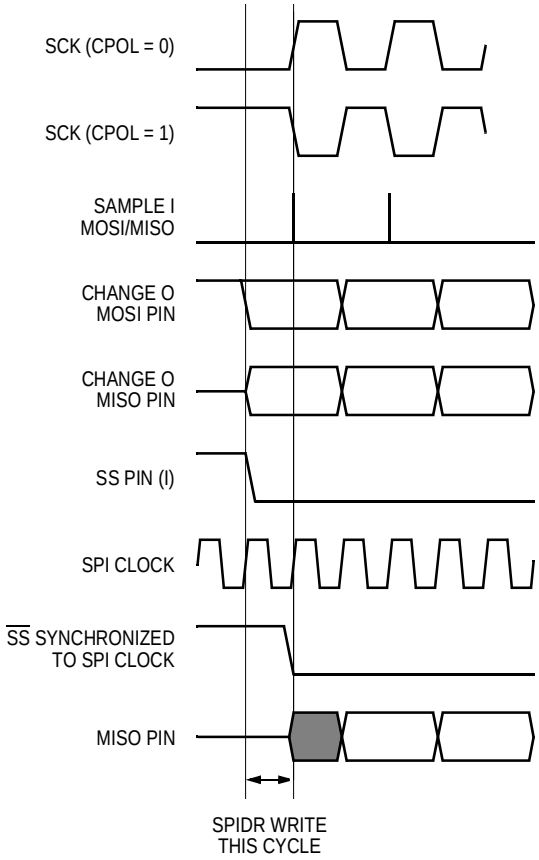

Figure 17-13. Transmission Error Due to Master/Slave Clock Skew

The synchronized $\overline{SS}$ signal is synchronized to the SPI clock. **Figure 17-13** shows an example with the synchronized $\overline{SS}$ signal almost a full SPI clock cycle late. While the synchronized $\overline{SS}$ of the slave is high, writing is allowed even though the $\overline{SS}$ pin is already low. The write can change the MISO pin while the master is sampling the MISO line. The first bit of the transfer may not be stable when the master samples it, so the byte sent to the master may be corrupted.

Also, if the slave generates a late write, its state machine may not have time to reset, causing it to incorrectly receive a byte from the master.

This error is most likely when the SCK frequency is half the slave SPI clock frequency. At other baud rates, the SCK skew is no more than one SPI clock, and there is more time between the synchronized $\overline{SS}$ signal and the first SCK edge. For example, with a SCK frequency one-fourth

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the slave SPI clock frequency, there are two SPI clocks between the fall of $\overline{SS}$ and the SCK edge.

As long as another late SPIDR write does not occur, the following bytes to and from the slave are correctly transmitted.

17.8.4 SPI Baud Rate Generation

The baud rate generator divides the SPI clock to produce the SPI baud clock. The SPPR[6:4] and SPR[2:0] bits in SPIBR select the SPI clock divisor:

$$\text{SPI clock divisor} = (\text{SPPR} + 1) \times 2^{(\text{SPR}+1)}$$

where:

SPPR = the value written to bits SPPR[6:4]
SPR = the value written to bits SPR[2:0]

The baud rate generator is active only when the SPI is in master mode and transmitting. Otherwise, the divider is inactive to reduce I_{DD} current.

17.8.5 Slave-Select Output

The slave-select output feature automatically drives the $\overline{SS}$ pin low during transmission to select external devices and drives it high during idle to deselect external devices. When $\overline{SS}$ output is selected, the $\overline{SS}$ output pin is connected to the $\overline{SS}$ input pin of the external device.

In master mode only, setting the SSOE bit in SPICR1 and the DDRSP[3] bit in SPIDDR configures the $\overline{SS}$ pin as a slave-select output.

Setting the SSOE bit disables the mode fault feature.

NOTE: *Be careful when using the slave-select output feature in a multimaster system. The mode fault feature is not available for detecting system errors between masters.*

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17.8.6 Bidirectional Mode

Setting the SPC0 bit in SPICR1 selects bidirectional mode (see **Table 17-7**). The SPI uses only one data pin for the interface with external device(s). The MSTR bit determines which pin to use. In master mode, the MOSI pin is the master out/master in pin, MOMI. In slave mode, the MISO pin is the slave out/slave in pin, SISO. The MISO pin in master mode and MOSI pin in slave mode are general-purpose I/O pins.

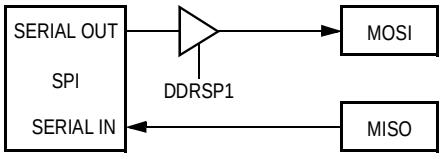
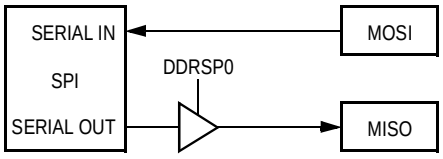
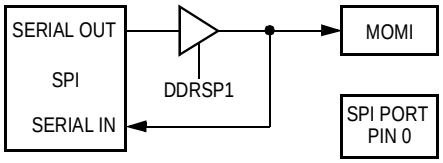
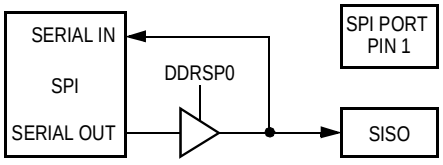
The direction of each data I/O pin depends on its data direction register bit. A pin configured as an output is the output from the shift register. A pin configured as an input is the input to the shift register, and data coming out of the shift register is discarded.

The SCK pin is an output in master mode and an input in slave mode.

The $\overline{SS}$ pin can be an input or an output in master mode, and it is always an input in slave mode.

In bidirectional mode, a mode fault does not clear DDRSP0, the data direction bit for the SISO pin.

Table 17-7. Normal Mode and Bidirectional Mode

SPE = 1	Master Mode, MSTR = 1	Slave Mode, MSTR = 0
Normal Mode SPC0 = 0	 SWOM enables open drain output.	 SWOM enables open drain output.
Bidirectional Mode SPC0 = 1	 SWOM enables open drain output. SPI port pin 0 is general-purpose I/O.	 SWOM enables open drain output. SPI port pin 1 is general-purpose I/O.

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17.8.7 Error Conditions

The SPI has two error conditions:

- Write collision error
- Mode fault error

17.8.7.1 Write Collision Error

The WCOL flag in SPISR indicates that a serial transfer was in progress when the MCU tried to write new data to SPIDR. Valid write times are listed below (see **Figure 17-11** and **Figure 17-12** for definitions of t_T and t_l):

- In master mode, a valid write is within t_l (when $\overline{SS}$ is high).
- In slave phase 0, a valid write within t_l (when $\overline{SS}$ is high).
- In slave phase 1, a valid write is within t_T or t_l (after the last SCK edge and before $\overline{SS}$ goes low), excluding the first two SPI clocks after the last SCK edge (the beginning of t_T is an illegal write).

A write during any other time causes a WCOL error. The write is disabled to avoid writing over the data being transmitted. WCOL does not generate an interrupt request because the WCOL flag can be read upon completion of the transmission that was in progress at the time of the error.

17.8.7.2 Mode Fault Error

If the $\overline{SS}$ input of a master SPI goes low, it indicates a system error in which more than one master may be trying to drive the MOSI and SCK lines simultaneously. This condition is not permitted in normal operation; it sets the MODF flag in SPISR. If the SPIE bit in SPICR1 is also set, MODF generates an interrupt request.

Configuring the $\overline{SS}$ pin as a general-purpose output or a slave-select output disables the mode fault function.

A mode fault clears the SPE and MSTR bits and the DDRSP bits of the SCK, MISO, and MOSI (or MOMI) pins. This forces those pins to be high-impedance inputs to avoid any conflict with another output driver.

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If the mode fault error occurs in bidirectional mode, the DDRSP bit of the SISO pin is not affected, since it is a general-purpose I/O pin.

17.8.8 Low-Power Mode Options

This subsection describes the low-power mode options.

17.8.8.1 Run Mode

Clearing the SPE bit in SPICR1 puts the SPI in a disabled, low-power state. SPI registers are accessible, but SPI clocks are disabled.

17.8.8.2 Doze Mode

SPI operation in doze mode depends on the state of the SPISDOZ bit in SPICR2.

- If SPISDOZ is clear, the SPI operates normally in doze mode.
- If SPISDOZ is set, the SPI clock stops, and the SPI enters a low-power state in doze mode.
  - Any master transmission in progress stops at doze mode entry and resumes at doze mode exit.
  - Any slave transmission in progress continues if a master continues to drive the slave SCK pin. The slave stays synchronized to the master SCK clock.

NOTE: *Although the slave shift register can receive MOSI data, it cannot transfer data to SPIDR or set the SPIF flag in doze or stop mode. If the slave enters doze mode in an idle state and exits doze mode in an idle state, SPIF remains clear and no transfer to SPIDR occurs.*

17.8.8.3 Stop Mode

SPI operation in stop mode is the same as in doze mode with the SPISDOZ bit set.

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17.9 Reset

Reset initializes the SPI registers to a known startup state as described in **17.7 Memory Map and Registers**. A transmission from a slave after reset and before writing to the SPIDR register is either indeterminate or the byte last received from the master before the reset. Reading the SPIDR after reset returns 0s.

17.10 Interrupts

Table 17-8. SPI Interrupt Request Sources

Interrupt Request	Flag	Enable Bit
Mode fault	MODF	SPIE
Transmission complete	SPIF	

17.10.1 SPI Interrupt Flag (SPIF)

SPIF is set after the eighth SCK cycle in a transmission when received data transfers from the shift register to SPIDR. If the SPIE bit is also set, SPIF generates an interrupt request. Once SPIF is set, no new data can be transferred into SPIDR until SPIF is cleared. Clear SPIF by reading SPISR with SPIF set and then accessing SPIDR. Reset clears SPIF.

17.10.2 Mode Fault (MODF) Flag

MODF is set when the $\overline{SS}$ pin of a master SPI is driven low and the $\overline{SS}$ pin is configured as a mode-fault input. If the SPIE bit is also set, MODF generates an interrupt request. A mode fault clears the SPE, MSTR, and DDRSP[2:0] bits. Clear MODF by reading SPISR with MODF set and then writing to SPICR1. Reset clears MODF.

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Section 18. Queued Analog-to-Digital Converter (QADC)

18.1 Contents

18.2 Introduction 401
18.3 Features 402
18.4 Block Diagram 403
18.5 Modes of Operation 404
18.5.1 Debug Mode 404
18.5.2 Stop Mode 405
18.6 Signals 405
18.6.1 Port QA Pin Functions 406
18.6.1.1 Port QA Analog Input Pins 406
18.6.1.2 Port QA Digital Input/Output Pins 407
18.6.2 Port QB Pin Functions 407
18.6.2.1 Port QB Analog Input Pins 407
18.6.2.2 Port QB Digital Input Pins 407
18.6.3 External Trigger Input Pins 408
18.6.4 Multiplexed Address Output Pins 408
18.6.5 Multiplexed Analog Input Pins 409
18.6.6 Voltage Reference Pins 409
18.6.7 Dedicated Analog Supply Pins 409
18.7 Memory Map 409
18.8 Register Descriptions 411
18.8.1 QADC Module Configuration Register 411
18.8.2 QADC Test Register 412
18.8.3 Port Data Registers 412
18.8.4 Port QA Data Direction Register 414
18.8.5 Control Registers 416
18.8.5.1 Control Register 0 416
18.8.5.2 Control Register 1 419
18.8.5.3 QADC Control Register 2 422

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18.8.6 Status Registers 427
18.8.6.1 QADC Status Register 0 427
18.8.6.2 QADC Status Register 1 436
18.8.7 Conversion Command Word Table 437
18.8.8 Result Registers 441
18.8.8.1 Right-Justified Unsigned Result Register. 441
18.8.8.2 Left-Justified Signed Result Register 442
18.8.8.3 Left-Justified Unsigned Result Register 442

18.9 Functional Description 443
18.9.1 QADC Bus Accessing 443
18.9.2 External Multiplexing 443
18.9.2.1 External Multiplexing Operation 443
18.9.2.2 Module Version Options. 444
18.9.2.3 External Multiplexed Address Configuration 446
18.9.3 Analog Subsystem 446
18.9.3.1 Analog-to-Digital Converter Operation 446
18.9.3.2 Conversion Cycle Times 446
18.9.3.3 Channel Decode and Multiplexer 448
18.9.3.4 Sample Buffer 448
18.9.3.5 Digital-to-Analog Converter (DAC) Array 449
18.9.3.6 Comparator 449
18.9.3.7 Bias 449
18.9.3.8 Successive-Approximation Register 449
18.9.3.9 State Machine 450

18.10 Digital Control 450
18.10.1 Queue Priority Timing Examples. 450
18.10.1.1 Queue Priority 451
18.10.1.2 Queue Priority Schemes 453
18.10.2 Boundary Conditions 465
18.10.3 Scan Modes 466
18.10.4 Disabled Mode 467
18.10.5 Reserved Mode 467
18.10.6 Single-Scan Modes 467
18.10.6.1 Software-Initiated Single-Scan Mode. 468
18.10.6.2 External Trigger Single-Scan Mode 469
18.10.6.3 External Gated Single-Scan Mode. 470
18.10.6.4 Interval Timer Single-Scan Mode. 470

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18.10.7 Continuous-Scan Modes 472
18.10.7.1 Software-Initiated Continuous-Scan Mode. 473
18.10.7.2 External Trigger Continuous-Scan Mode 474
18.10.7.3 External Gated Continuous-Scan Mode 474
18.10.7.4 Periodic Timer Continuous-Scan Mode 475
18.10.8 QADC Clock (QCLK) Generation 476
18.10.9 Periodic/Interval Timer 480
18.10.10 Conversion Command Word Table 481
18.10.11 Result Word Table 485
18.11 Pin Connection Considerations 486
18.11.1 Analog Reference Pins. 486
18.11.2 Analog Power Pins 486
18.11.3 Conversion Timing Schemes 488
18.11.4 Analog Supply Filtering and Grounding 490
18.11.5 Accommodating Positive/Negative Stress Conditions 494
18.11.6 Analog Input Considerations 495
18.11.7 Analog Input Pins 497
18.11.7.1 Settling Time for the External Circuit 498
18.11.7.2 Error Resulting from Leakage 499
18.12 Interrupts. 500
18.12.1 Interrupt Operation 500
18.12.2 Interrupt Sources 501

18.2 Introduction

The queued analog-to-digital converter (QADC) is a 10-bit, unipolar, successive approximation converter. A minimum of eight analog input channels can be supported using internal multiplexing. A maximum of 18 input channels can be supported in the expanded, externally multiplexed mode. The actual number of channels depends upon the number of pins available to the QADC module.

The QADC consists of an analog front-end and a digital control subsystem, which includes an IPbus interface block.

The analog section includes input pins, an analog multiplexer, and sample and hold analog circuits. The analog conversion is performed by

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the digital-to-analog converter (DAC) resistor-capacitor (RC) array and a high-gain comparator.

The digital control section contains queue control logic to sequence the conversion process and interrupt generation logic. Also included are the periodic/interval timer, control and status registers, the conversion command word (CCW) table, random-access memory (RAM), and the result table RAM.

The bus interface unit (BIU) allows the QADC to operate with the applications software through the IPbus environment.

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18.3 Features

Features of the QADC module include:

- Internal sample and hold
- Up to eight analog input channels using internal multiplexing
- Directly supports up to four external multiplexers (for example, the MC14051)
- Up to 18 total input channels with internal and external multiplexing
- Programmable input sample time for various source impedances
- Two conversion command queues with a total of 64 entries
- Sub-queues possible using pause mechanism
- Queue complete and pause software interrupts available on both queues
- Queue pointers indicate current location for each queue
- Automated queue modes initiated by:
  - External edge trigger and gated trigger
  - Periodic/interval timer, within QADC module [queues 1 and 2]
  - Software command
- Single-scan or continuous-scan of queues
- 64 result registers

- Output data readable in three formats:
  - Right-justified unsigned
  - Left-justified signed
  - Left-justified unsigned
- Unused analog channels can be used as digital ports

18.4 Block Diagram

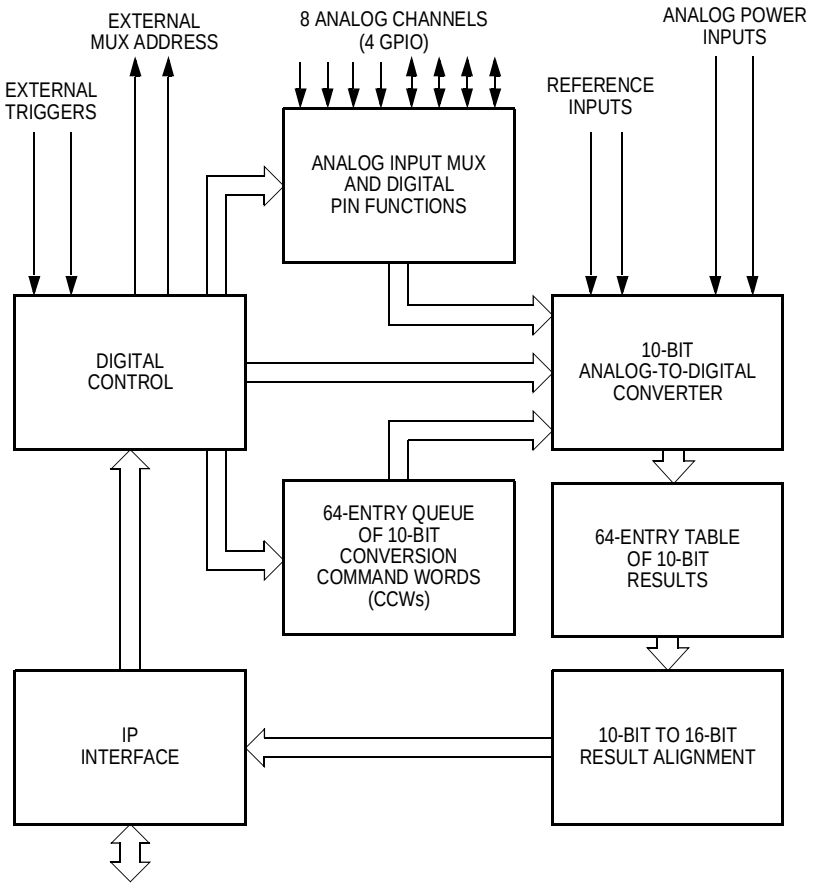

Figure 18-1. QADC Block Diagram

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18.5 Modes of Operation

This subsection describes the two modes of operation:

- Debug mode
- Stop mode

18.5.1 Debug Mode

If the QDBG bit in the module configuration register (QADCMCR) is set, then the QADC enters debug mode when background debug mode is enabled and a breakpoint is processed.

When in debug mode and the QDBG bit is set, the QADC finishes any conversion in progress and then freezes. Depending on when debug mode is asserted, the three possible queue freeze scenarios are:

- When a queue is not executing, the QADC freezes immediately.
- When a queue is executing, the QADC completes the current conversion and then freezes.
- If during the execution of the current conversion, the queue operating mode for the active queue is changed, or a queue 2 abort occurs, the QADC freezes immediately.

When the QADC enters debug mode while a queue is active, the current CCW location of the queue pointer is saved.

Debug mode:

- Stops the analog clock
- Holds the periodic/interval timer in reset
- Prevents external trigger events from being captured
- Keeps all QADC registers and RAM accessible

Although the QADC saves a pointer to the next CCW in the current queue, the software can force the QADC to execute a different CCW by writing new queue operating modes for normal operation. The QADC looks at the queue operating modes, the current queue pointer, and any pending trigger events to decide which CCW to execute.

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18.5.2 Stop Mode

The QADC enters a low-power idle state whenever the QSTOP bit is set or the part is in stop mode.

QADC stop:

- Disables the analog-to-digital converter, effectively turning off the analog circuit.
- Aborts the conversion sequence in progress
- Changes the data direction register (DDRQA), port data registers (PORTQA and PORTQB), control registers (QACR2, QACR1, and QACR0) and the status registers (QASR1 and QASR0) to read-only. Only the module configuration register (QADCMCR) is writable.
- Causes the RAM to not be accessible, can not read valid results from RAM (result word table and CCW) nor write to the RAM (result word table and CCW).
- Resets QACR1, QACR2, QASR0, and QASR1
- Holds the QADC periodic/interval timer in reset

Because the bias currents to the analog circuit are turned off in stop, the QADC requires some recovery time (t_{SR}) to stabilize the analog circuits.

18.6 Signals

The QADC uses the external pins shown in **Figure 18-2**. There are eight channel/port pins that can support up to 18 channels when external multiplexing is used (including internal channels). All of the channel pins can also be used as general-purpose digital port pins. In addition, there are also two analog reference pins and two analog submodule power pins.

The QADC has external trigger inputs and the multiplexer outputs combined onto some of the channel pins.

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18.6.1 Port QA Pin Functions

The four port QA pins can be used as analog inputs or as a bidirectional 4-bit digital input/output port.

18.6.1.1 Port QA Analog Input Pins

When used as analog inputs, the four port QA pins are referred to as AN[56:55, 53:52]. Due to the digital output drivers associated with port QA, the analog characteristics of port QA may be different from those of port QB.

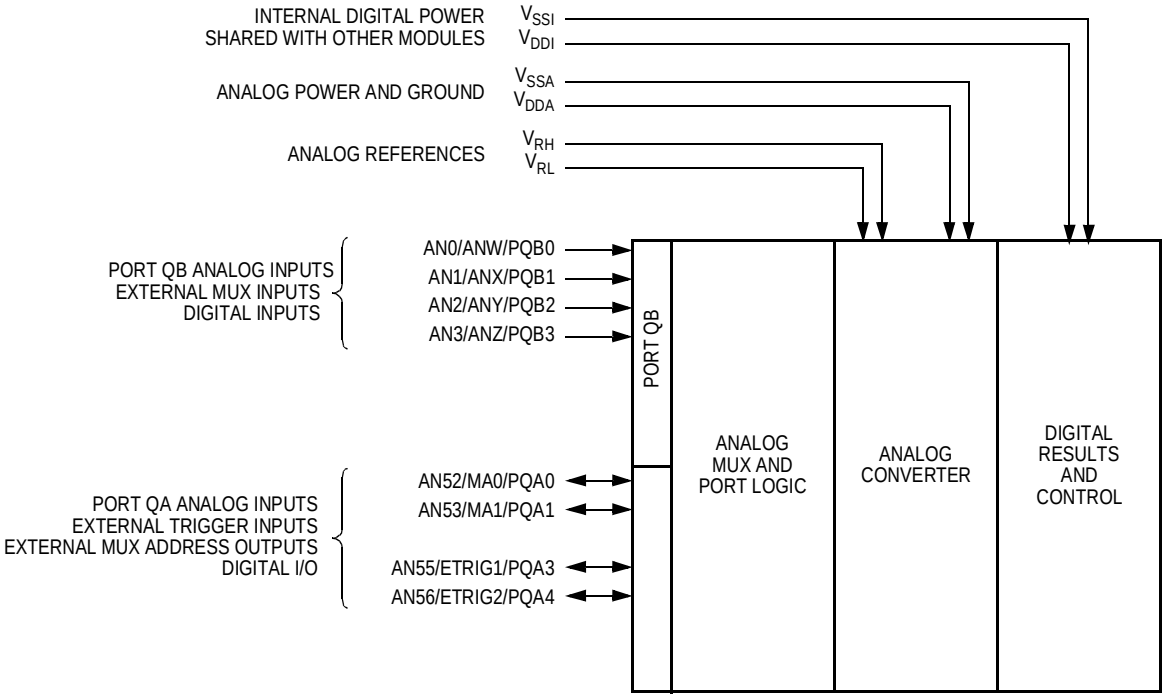

Figure 18-2. QADC Input and Output Signals

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18.6.1.2 Port QA Digital Input/Output Pins

Port QA pins are referred to as PQA[4:3, 1:0] when used as a bidirectional 4-bit digital input/output port. These four pins may be used for general-purpose digital input signals or digital output signals.

Port QA pins are connected to a digital input synchronizer during reads and may be used as general-purpose digital inputs when the applied voltages meet high-voltage input (V_{IH}) and low-voltage input (V_{IL}) requirements.

Each port QA pin is configured as an input or output by programming the upper half of the port data direction register (DDRQA). The digital input signal states are read by the software in the upper half of the port data register when the port data direction register specifies that the pins are inputs. The digital data in the port data register is driven onto the port QA pins when the corresponding bit in the port data direction register specifies output. Since the outputs are configured as output drivers, external pullup provisions are not necessary when the output is used to drive another integrated circuit.

18.6.2 Port QB Pin Functions

The four port QB pins can be used as analog inputs or as an 4-bit digital input-only port.

18.6.2.1 Port QB Analog Input Pins

When used as analog inputs, the four port QB pins are referred to as AN[3:0]. Since port QB functions as analog and digital input only, the analog characteristics may be different from those of port QA.

18.6.2.2 Port QB Digital Input Pins

Port QB pins are referred to as PQB[3:0] when used as an 4-bit digital input only port. In addition to functioning as analog input pins, the port QB pins are also connected to the input of a synchronizer during reads and may be used as general-purpose digital inputs when the applied voltages meet V_{IH} and V_{IL} requirements.

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Since port QB pins are input only, a data direction register is not necessary. The digital input signal states are read by the software in the lower half of the port data register.

18.6.3 External Trigger Input Pins

The QADC uses two external trigger pins (ETRIG[2:1]). Each of the two input external trigger pins is associated with one of the scan queues, queue 1 or queue 2. The assignment of ETRIG[2:1] to a queue is made in QACR0 by the TRG bit. When TRG = 0, ETRIG1 triggers queue 1 and ETRIG2 triggers queue 2. When TRG = 1, ETRIG1 triggers queue 2 and ETRIG2 triggers queue 1.

18.6.4 Multiplexed Address Output Pins

In the non-multiplexed mode, the eight channel pins are connected to an internal multiplexer which routes the analog signals into the internal A/D converter.

In the externally multiplexed mode, the QADC allows automatic channel selection through up to four external 4-to-1 selector chips. The QADC provides a 2-bit multiplexed address output to the external multiplex chips to allow selection of one of four inputs. The multiplexed address output signals (MA[1:0]) can be used as multiplexed address output bits or as general-purpose I/O.

MA[1:0] are used as the address inputs for one to two dual 4-channel multiplexer chips. Since the MA[1:0] pins are digital outputs in the multiplexed mode, the software programmed input/output direction for the multiplexed address pins in the data direction register is superseded.

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18.6.5 Multiplexed Analog Input Pins

In the external multiplexed mode, four of the port QB pins are redefined to each represent four input channels. See **Table 18-1**.

Table 18-1. Multiplexed Analog Input Channels

Multiplexed Analog Input	Channels
ANw	Even numbered channels from 0 to 6
ANx	Odd numbered channels from 1 to 7
ANy	Even channels from 16 to 22
ANz	Odd channels from 17 to 23

18.6.6 Voltage Reference Pins

V_{RH} and V_{RL} are the dedicated input pins for the high and low reference voltages. Separating the reference inputs from the power supply pins allows for additional external filtering, which increases reference voltage precision and stability, and subsequently contributes to a higher degree of conversion accuracy.

18.6.7 Dedicated Analog Supply Pins

V_{DDA} and V_{SSA} pins supply power to the analog subsystems of the QADC module. Dedicated power is required to isolate the sensitive analog circuitry from the normal levels of noise present on the digital power supply.

18.7 Memory Map

The QADC occupies 1 Kbyte, or 512 16-bit entries, of address space. Ten 16-bit registers are control, port, and status registers, 64 16-bit entries are the CCW table, and 64 16-bit entries are the result table which occupies 192 16-bit address locations because the result data is readable in three data alignment formats. **Table 18-2** is the QADC memory map.

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Table 18-2. QADC Memory Map

Address	MSB	LSB	Access[1]
0x00ca_0000	QADC module configuration register (QADCMCR)		S
0x00ca_0002	QADC test register (QADCTEST)[2]		S
0x00ca_0004	Reserved[3]		—
0x00ca_0006	Port QA data register (PORTQA)	Port QB data register (PORTQB)	S/U
0x00ca_0008	Port QA data direction register (DDRQA)		S/U
0x00ca_000a	QADC control register 0 (QACR0)		S/U
0x00ca_000c	QADC control register 1 (QACR1)		S/U
0x00ca_000e	QADC control register 2 (QACR2)		S/U
0x00ca_0010	QADC status register 0 (QASR0)		S/U
0x00ca_0012	QADC status register 1 (QASR1)		S/U
0x00ca_0014– 0x00ca_01fe	Reserved[3]		—
0x00ca_0200– 0x00ca_027e	Conversion command word table (CCW)		S/U
0x00ca_0280– 0x00ca_02fe	Right justified, unsigned result register (RJURR)		S/U
0x00ca_0300– 0x00ca_037e	Left justified, signed result register (LJSRR)		S/U
0x00ca_0380– 0x00ca_03fe	Left justified, unsigned result register (LJURR)		S/U

1. S = CPU supervisor mode access only. S/U = CPU supervisor or user mode access. User mode accesses to supervisor only addresses have no effect and result in a cycle termination transfer error.
2. Access results in the module generating an access termination transfer error if not in test mode.
3. Read/writes have no effect and the access terminates with a transfer error exception.

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18.8 Register Descriptions

This subsection describes the QADC registers.

18.8.1 QADC Module Configuration Register

The QADCMCR contains fields and bits that control freeze and stop modes and determines the privilege level required to access most registers.

Address: 0x00ca_0000 and 0x00ca_0001

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	QSTOP	QDBG	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SUPV	0	0	0	0	0	0	0
Write:								
Reset:	1	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 18-3. QADC Module Configuration Register (QADCMCR)

QSTOP — Stop Enable Bit
- 1 = Forces QADC to idle state
- 0 = QADC is not forced to idle state

QDBG — Debug Enable Bit
- 1 = Finish any conversion in progress, then freezes in debug mode
- 0 = Ignore request to enter debug mode and continue conversions

SUPV — Supervisor/Unrestricted Data Space Bit
- 1 = Only supervisor mode access allowed; user mode accesses have no effect and result in a cycle termination transfer error
- 0 = Supervisor and user mode accesses allowed

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18.8.2 QADC Test Register

QADCTEST is used only during factory testing of the MCU. Attempts to access this register outside of factory test mode will result in access privilege violation.

Address: 0x00ca_0002 and 0x00ca_0003

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	Access results in the module generating an access termination transfer error if not in test mode.							

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Access results in the module generating an access termination transfer error if not in test mode.							

Figure 18-4. QADC Test Register (QADCTEST)

18.8.3 Port Data Registers

QADC ports A and B are accessed through two 8-bit port data registers (PORTQA and PORTQB).

Port QA pins are referred to as PQA[4:3, 1:0] when used as a bidirectional, 4-bit, input/output port that may be used for general-purpose digital input signals or digital output signals. Port QA can also be used for analog inputs (AN[56:55, 53:52]), external trigger inputs (ETRIG[2:1]), and external multiplexer address outputs (MA[1:0]).

Port QB pins are referred to as PQB[3:0] when used as an input-only, 4-bit, digital port that may be used for general-purpose digital input signals. Data for PQB[3:0] is accessed from PORTQB. Port QB can also be used for non-multiplexed (AN[3:0]) and multiplexed (ANz, ANy, ANx, ANw) analog inputs.

PORTQA and PORTQB are not initialized by reset.

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Address: 0x00ca_0006

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	PQA4	PQA3	0	PQA1	PQA0
Write:								
Reset:	0	0	0	P	P	0	P	P

= Writes have no effect and the access terminates without a transfer error exception.

P = Current pin state if DDR is input, otherwise undefined

Analog Channel:			AN56	AN55	AN53	AN52
Muxed Address Outputs:					MA1	MA0
External Trigger Inputs:			ETRIG2	ETRIG1		

Figure 18-5. QADC Port QA Data Register (PORTQA)

Address: 0x00ca_0007

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PQB3	PQB2	PQB1	PQB0
Write:								
Reset:	0	0	0	0	P	P	P	P

= Writes have no effect and the access terminates without a transfer error exception.

P = Current pin state if DDR is input, otherwise undefined

Analog Channel:			AN3	AN2	AN1	AN0
Muxed Analog Inputs:			AN2	ANy	ANx	ANw

Figure 18-6. QADC Port QB Data Register (PORTQB)

Read: Anytime

Write: Anytime except stop mode

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18.8.4 Port QA Data Direction Register

The port data direction register (DDRQA) is associated with the port QA digital I/O pins. The bidirectional pins may have somewhat higher leakage and capacitance specifications. Any bit in this register set to 1 configures the corresponding pin as an output. Any bit in this register cleared to 0 configures the corresponding pin as an input. The software is responsible for ensuring that DDR bits are not set to 1 on pins used for analog inputs. When the DDR bit is set to 1 and the pin is selected for analog conversion, the voltage sampled is that of the output digital driver as influenced by the load.

When the MUX (externally multiplexed) bit is set in QACR0, the data direction register settings are ignored for the bits corresponding to PQA[1:0], the two multiplexed address (MA[1:0]) output pins. The MA[1:0] pins are forced to be digital outputs, regardless of the data direction setting, and the multiplexed address outputs are driven. The data returned during a port data register read is the value of MA[1:0], regardless of the data direction setting.

Similarly, when the external trigger pins are assigned to port pins and external trigger queue operating mode is selected, the data direction setting for the corresponding pins, PQA3 or PQA4, is ignored. The port pins are forced to be digital inputs for ETRIG1 and/or ETRIG2. The data driven during a port data register read is the actual value of the pin, regardless of the data direction setting.

NOTE: *Use caution when mixing digital and analog inputs. They should be isolated as much as possible. Rise and fall times should be as large as possible to minimize ac coupling effects.*

Since port QB is input-only, a data direction register is not needed. Therefore, the lower byte of the port data direction register is not implemented.

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Address: 0x00ca_0008 and 0x00ca_0009

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	0	DDQA4	DDQA3	0	DDQA1	DDQA0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 18-7. QADC Port QA Data Direction Register (DDRQA)

Read: Anytime

Write: Anytime except stop mode

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18.8.5 Control Registers

This subsection describes the QADC control registers.

18.8.5.1 Control Register 0

Control register 0 (QACR0) establishes the QCLK with prescaler parameter fields and defines whether external multiplexing is enabled. They are typically written once when the software initializes the QADC and not changed afterward.

Address: 0x00ca_000a and 0x00ca_000b

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	MUX	0	0	TRG	0	0	0	PSH8
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PSH7	PSH6	PSH5	PSH4	PSA	PSL2	PSL1	PSL0
Write:								
Reset:	0	0	1	1	0	1	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 18-8. QADC Control Register 0 (QACR0)

Read: Anytime

Write: Anytime except stop mode

MUX — Externally Multiplexed Mode Bit

The MUX bit allows the software to select the externally multiplexed mode, which affects the interpretation of the channel numbers and forces the MA[1:0] pins to be outputs.

1 = Externally multiplexed, 18 possible channels
0 = Internally multiplexed, eight possible channels

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TRG — Trigger Assignment Bit

The TRG bit allows the software to assign the ETRIG[2:1] pins to queue 1 and queue 2.

1 = ETRIG1 triggers queue 2, ETRIG2 triggers queue 1
0 = ETRIG1 triggers queue 1, ETRIG2 triggers queue 2

PSH[8:4] — Prescaler Clock High Time Field

The PSH field selects the QCLK high time in the prescaler. **See Section 22. Electrical Specifications** for operating clock frequency (f_{QCLK}) values. To keep the QCLK within the specified range, the PSH field selects the high time of the QCLK, which can range from 1 to 32 system clock cycles. The minimum high time for the QCLK is specified as t_{PSH}. **Table 18-3** displays the bits in PSH field which enable a range of QCLK high times.

Table 18-3. Prescaler Clock High Times

PSH[8:4]	QCLK High Time
00000	1 system clock cycle
00001	2 system clock cycles
00010	3 system clock cycles
00011	4 system clock cycles
00100	5 system clock cycles
00101	6 system clock cycles
00110	7 system clock cycles
00111	8 system clock cycles
01000	9 system clock cycles
01001	10 system clock cycles
01010	11 system clock cycles
01011	12 system clock cycles
01100	13 system clock cycles
01101	14 system clock cycles
01110	15 system clock cycles
01111	16 system clock cycles

PSH[8:4]	QCLK High Time
10000	17 system clock cycles
10001	18 system clock cycles
10010	19 system clock cycles
10011	20 system clock cycles
10100	21 system clock cycles
10101	22 system clock cycles
10110	23 system clock cycles
10111	24 system clock cycles
11000	25 system clock cycles
11001	26 system clock cycles
11010	27 system clock cycles
11011	28 system clock cycles
11100	29 system clock cycles
11101	30 system clock cycles
11110	31 system clock cycles
11111	32 system clock cycles

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PSA — Prescaler Add Clock Tick Bit

PSA is maintained for software compatibility but has no functional benefit to this version of the module.

PSL[2:0] — Prescaler Clock Low Time Field

The PSL field selects the QCLK low time in the prescaler. See **Section 22. Electrical Specifications** for f_{QCLK} values.

To keep the QCLK within the specified range, the PSL field selects the low time of the QCLK, which can range from one to eight system clock cycles. The minimum low time for the clock is specified as t_{PSL}.

Table 18-4 displays the bits in PSL field which enable a range of QCLK low times.

Table 18-4. Prescaler Clock Low Times

PSL[2:0]	QCLK Low Time
000	1 system clock cycle
001	2 system clock cycles
010	3 system clock cycles
011	4 system clock cycles
100	5 system clock cycles
101	6 system clock cycles
110	7 system clock cycles
111	8 system clock cycles

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18.8.5.2 Control Register 1

Control register 1 (QACR1) is the mode control register for the operation of queue 1. The applications software defines the queue operating mode for the queue and may enable a completion and/or pause interrupt. Most of the bits are typically written once when the software initializes the QADC and not changed afterward.

Stop mode resets the register ($0000)

Address: 0x00ca_000c and 0x00ca_000d

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	CIE1	PIE1	0	MQ112	MQ111	MQ110	MQ19	MQ18
Write:			SSE1					
Reset:	0	0	0	0	0	0	0	0
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 18-9. QADC Control Register 1 (QACR1)

Read: Anytime

Write: Anytime except stop mode

CIE1 — Queue 1 Completion Interrupt Enable Bit

CIE1 enables an interrupt upon completion of queue 1. The interrupt request is initiated when the conversion is complete for the CCW in queue 1.

1 = Enable interrupt after the conversion of the sample requested by the last CCW in queue 1

0 = Disable queue 1 completion interrupt

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PIE1 — Queue 1 Pause Interrupt Enable Bit

PIE1 enables an interrupt when queue 1 enters the pause state. The interrupt request is initiated when conversion is complete for a CCW that has the pause bit set.

1 = Enable an interrupt after an end-of-conversion for queue 1 which has the pause bit set.

0 = Disable the pause interrupt associated with queue 1.

SSE1 — Queue 1 Single-Scan Enable Bit

SSE1 enables a single-scan of queue 1 to start after a trigger event occurs. The SSE1 bit may be set to a 1 during the same write cycle when the MQ1 bits are set for one of the single-scan queue operating modes. The single-scan enable bit can be written as a 1 or a 0, but is always read as a 0, unless a test mode is selected. The SSE1 bit enables a trigger event to initiate queue execution for any single-scan operation on queue 1.The QADC clears the SSE1 bit when the single-scan is complete.

1 = Accept a trigger event to start queue 1 in a single-scan mode.

0 = Trigger events are not accepted for single-scan modes.

MQ1[12:8] — Queue 1 Operating Mode Field

The MQ1 field selects the queue operating mode for queue 1.

Table 18-5 shows the bits in the MQ1 field which enable different queue 1 operating modes.

Table 18-5. Queue 1 Operating Modes

MQ1[12:8]	Operating Mode
00000	Disabled mode, conversions do not occur
00001	Software-triggered single-scan mode (started with SSE1)
00010	External-trigger rising-edge single-scan mode
00011	External-trigger falling-edge single-scan mode
00100	Interval timer single-scan mode: time = QCLK period $\times 2^7$
00101	Interval timer single-scan mode: time = QCLK period $\times 2^8$
00110	Interval timer single-scan mode: time = QCLK period $\times 2^9$
00111	Interval timer single-scan mode: time = QCLK period $\times 2^{10}$
01000	Interval timer single-scan mode: time = QCLK period $\times 2^{11}$

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Table 18-5. Queue 1 Operating Modes (Continued)

MQ1[12:8]	Operating Mode
01001	Interval timer single-scan mode: time = QCLK period × 2^{12}
01010	Interval timer single-scan mode: time = QCLK period × 2^{13}
01011	Interval timer single-scan mode: time = QCLK period × 2^{14}
01100	Interval timer single-scan mode: time = QCLK period × 2^{15}
01101	Interval timer single-scan mode: time = QCLK period × 2^{16}
01110	Interval timer single-scan mode: time = QCLK period × 2^{17}
01111	Externally gated single-scan mode (started with SSE1)
10000	Reserved mode
10001	Software-triggered continuous-scan mode
10010	External-trigger rising-edge continuous-scan mode
10011	External-trigger falling-edge continuous-scan mode
10100	Periodic timer continuous-scan mode: time = QCLK period × 2^{7}
10101	Periodic timer continuous-scan mode: time = QCLK period × 2^{8}
10110	Periodic timer continuous-scan mode: time = QCLK period × 2^{9}
10111	Periodic timer continuous-scan mode: time = QCLK period × 2^{10}
11000	Periodic timer continuous-scan mode: time = QCLK period × 2^{11}
11001	Periodic timer continuous-scan mode: time = QCLK period × 2^{12}
11010	Periodic timer continuous-scan mode: time = QCLK period × 2^{13}
11011	Periodic timer continuous-scan mode: time = QCLK period × 2^{14}
11100	Periodic timer continuous-scan mode: time = QCLK period × 2^{15}
11101	Periodic timer continuous-scan mode: time = QCLK period × 2^{16}
11110	Periodic timer continuous-scan mode: time = QCLK period × 2^{17}
11111	Externally gated continuous-scan mode

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18.8.5.3 QADC Control Register 2

Control register 2 (QACR2) is the mode control register for the operation of queue 2. Software specifies the queue operating mode of queue 2 and may enable a completion and/or a pause interrupt. Most of the bits are typically written once when the software initializes the QADC and not changed afterward.

Stop mode resets the register ($007f)

Address: 0x00ca_000e and 0x00ca_000f

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	CIE2	PIE2	0	MQ212	MQ211	MQ210	MQ29	MQ28
Write:			SSE2					
Reset:	0	0	0	0	0	0	0	0
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RESUME	BQ26	BQ25	BQ24	BQ23	BQ22	BQ21	BQ20
Write:								
Reset:	0	1	1	1	1	1	1	1

Figure 18-10. QADC Control Register 2 (QACR2)

Read: Anytime

Write: Anytime except stop mode

CIE2 — Queue 2 Completion Software Interrupt Enable Bit

CIE2 enables an interrupt upon completion of queue 2. The interrupt request is initiated when the conversion is complete for the CCW in queue 2.

1 = Enable an interrupt after an end-of-conversion for queue 2.
0 = Disable the queue completion interrupt associated with queue 2.

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PIE2 — Queue 2 Pause Software Interrupt Enable Bit

PIE2 enables an interrupt when queue 2 enters the pause state. The interrupt request is initiated when conversion is complete for a CCW that has the pause bit set.

1 = Enable an interrupt after an end-of-conversion for queue 2 which has the pause bit set.
0 = Disable the pause interrupt associated with queue 2.

SSE2 — Queue 2 Single-Scan Enable Bit

SSE2 enables a single-scan of queue 2 to start after a trigger event occurs. The SSE2 bit may be set to a 1 during the same write cycle when the MQ2 bits are set for one of the single-scan queue operating modes. The single-scan enable bit can be written as a 1 or a 0, but is always read as a 0, unless a test mode is selected. The SSE2 bit enables a trigger event to initiate queue execution for any single-scan operation on queue 2. The QADC clears the SSE2 bit when the single-scan is complete.

1 = Accept a trigger event to start queue 2 in a single-scan mode.
0 = Trigger events are not accepted for single-scan modes.

MQ2[12:8] — Queue 2 Operating Mode Field

The MQ2 field selects the queue operating mode for queue 2.

Table 18-6 shows the bits in the MQ2 field which enable different queue 2 operating modes.

Table 18-6. Queue 2 Operating Modes

MQ2[12:8]	Operating Modes
00000	Disabled mode, conversions do not occur
00001	Software triggered single-scan mode (started with SSE2)
00010	External trigger rising edge single-scan mode
00011	External trigger falling edge single-scan mode
00100	Interval timer single-scan mode: time = QCLK period x 2^7
00101	Interval timer single-scan mode: time = QCLK period x 2^8
00110	Interval timer single-scan mode: time = QCLK period x 2^9
00111	Interval timer single-scan mode: time = QCLK period x 2^{10}
01000	Interval timer single-scan mode: time = QCLK period x 2^{11}

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Table 18-6. Queue 2 Operating Modes (Continued)

MQ2[12:8]	Operating Modes
01001	Interval timer single-scan mode: time = QCLK period x 2^{12}
01010	Interval timer single-scan mode: time = QCLK period x 2^{13}
01011	Interval timer single-scan mode: time = QCLK period x 2^{14}
01100	Interval timer single-scan mode: time = QCLK period x 2^{15}
01101	Interval timer single-scan mode: time = QCLK period x 2^{16}
01110	Interval timer single-scan mode: time = QCLK period x 2^{17}
01111	Reserved mode
10000	Reserved mode
10001	Software triggered continuous-scan mode
10010	External trigger rising edge continuous-scan mode
10011	External trigger falling edge continuous-scan mode
10100	Periodic timer continuous-scan mode: time = QCLK period x 2^{7}
10101	Periodic timer continuous-scan mode: time = QCLK period x 2^{8}
10110	Periodic timer continuous-scan mode: time = QCLK period x 2^{9}
10111	Periodic timer continuous-scan mode: time = QCLK period x 2^{10}
11000	Periodic timer continuous-scan mode: time = QCLK period x 2^{11}
11001	Periodic timer continuous-scan mode: time = QCLK period x 2^{12}
11010	Periodic timer continuous-scan mode: time = QCLK period x 2^{13}
11011	Periodic timer continuous-scan mode: time = QCLK period x 2^{14}
11100	Periodic timer continuous-scan mode: time = QCLK period x 2^{15}
11101	Periodic timer continuous-scan mode: time = QCLK period x 2^{16}
11110	Periodic timer continuous-scan mode: time = QCLK period x 2^{17}
11111	Reserved mode

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RESUME — Queue 2 Resume Bit

RESUME selects the queue 2 resumption point after suspension due to queue 1. If RESUME is changed during the execution of queue 2, the change is not recognized until an end-of-queue condition is reached or the queue operating mode of queue 2 is changed.

The primary reason for selecting re-execution of the entire queue or subqueue is to guarantee that all samples are taken consecutively in one scan (coherency).

When subqueues are not used, queue 2 execution restarts after suspension with the first CCW in queue 2. When a pause has previously occurred in queue 2 execution, queue execution restarts after suspension with the first CCW in the current subqueue.

A subqueue is considered to be a stand-alone sequence of conversions. Once a pause flag has been set to report subqueue completion, that subqueue is not repeated until all CCWs in queue 2 are executed.

An example of using the RESUME bit is when the frequency of queue 1 trigger events prohibit queue 2 completion. If the rate of queue 1 execution is too high, it is best for queue 2 execution to continue with the CCW that was being converted when queue 2 was suspended. This allows queue 2 to eventually complete execution.

1 = After suspension, begin execution with the aborted CCW in queue 2.
0 = After suspension, begin execution with the first CCW of queue 2 or the current subqueue of queue 2.

BQ2[6:0] — Beginning of Queue 2 Field

BQ2[6:0] indicates the CCW location where queue 2 begins. To allow the length of queue 1 and queue 2 to vary, a programmable pointer identifies the CCW table location where queue 2 begins. The BQ2 field also serves as an end-of-queue condition for queue 1. Setting BQ2[6:0] beyond physical CCW table memory space allows queue 1 all 64 entries.

Software defines the beginning of queue 2 by programming the BQ2 field in QACR2. BQ2 is usually programmed before or at the same time as the queue operating mode for queue 2 is selected. If BQ2 is 64 or greater, queue 2 has no entries, the entire CCW table is dedicated to queue 1 and CCW63 is the end-of-queue 1. If BQ2[6:0] is 0, the entire CCW table is dedicated to queue 2. As a special case,

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when a queue operating mode for queue 1 is selected and a trigger event occurs for queue 1 with BQ2 set to 0, queue 1 execution is terminated after CCW0 is read. Conversions do not occur.

The BQ2[6:0] pointer may be changed dynamically, to alternate between queue 2 scan sequences. A change in BQ2[6:0] after queue 2 has begun or if queue 2 has a trigger pending does not affect queue 2 until queue 2 is started again. For example, two scan sequences could be defined as follows: The first sequence starts at CCW10, with a pause after CCW11 and an EOQ programmed in CCW15; the second sequence starts at CCW16, with a pause after CCW17 and an EOQ programmed in CCW39.

With BQ2[6:0] set to CCW10 and the continuous-scan mode selected, queue execution begins. When the pause is encountered in CCW11, a software interrupt routine can redefine BQ2[6:0] to be CCW16. Therefore, after the end-of-queue is recognized in CCW15, an internal retrigger event is generated and execution restarts at CCW16. When the pause software interrupt occurs again, software can change BQ2 back to CCW10. After the end-of-queue is recognized in CCW39, an internal retrigger event is created and execution now restarts at CCW10.

If BQ2[6:0] is changed while queue 1 is active, the effect of BQ2[6:0] as an end-of-queue indication for queue 1 is immediate. However, beware of the risk of losing the end-of-queue 1 when changing BQ2[6:0]. Using EOQ (chan63) to end queue 1 is recommended.

NOTE: *If BQ2[6:0] was assigned to the CCW that queue 1 is currently working on, then that conversion is completed before BQ2[6:0] takes effect.*

Each time a CCW is read for queue 1, the CCW location is compared with the current value of the BQ2[6:0] pointer to detect a possible end-of-queue condition. For example, if BQ2[6:0] is changed to CCW3 while queue 1 is converting CCW2, queue 1 is terminated after the conversion is completed. However, if BQ2[6:0] is changed to CCW1 while queue 1 is converting CCW2, the QADC would not recognize a BQ2[6:0] end-of-queue condition until queue 1 execution reached CCW1 again, presumably on the next pass through the queue.

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18.8.6 Status Registers

This subsection describes the QADC status registers.

18.8.6.1 QADC Status Register 0

The QADC status register 0 (QASR0) contains information about the state of each queue and the current A/D conversion.

Stop mode resets the register ($0000)

Address: 0x00ca_0010 and 0x00ca_0011

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	CF1	PF1	CF2	PF2	TOR1	TOR2	QS9	QS8
Write:								
Reset:	0	0	0	0	0	0	0	0
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	QS7	QS6	CWP5	CWP4	CWP3	CWP2	CWP1	CWP0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 18-11. QADC Status Register 0 (QASR0)

Read: Anytime

Write:

For flag bits (CF1, PF1, CF2, PF2, TOR1, TOR2): Writing a 1 has no effect, write a 0 to clear.

For QA[9:6] and CWP: Write has no effect.

Never in stop mode

CF1 — Queue 1 Completion Flag

CF1 indicates that a queue 1 scan has been completed. The scan completion flag is set by the QADC when the input channel sample requested by the last CCW in queue 1 is converted, and the result is stored in the result table.

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The end-of-queue 1 is identified when execution is complete on the CCW in the location prior to that pointed to by BQ2, when the current CCW contains an end-of-queue code instead of a valid channel number, or when the currently completed CCW is in the last location of the CCW RAM.

When CF1 is set and interrupts are enabled for that queue completion flag, the QADC asserts an interrupt request. The software reads the completion flag during an interrupt service routine to identify the interrupt request. The interrupt request is cleared when the software writes a 0 to the completion flag bit, when the bit was previously read as a 1. Once set, only software or reset can clear CF1.

CF1 is maintained by the QADC regardless of whether the corresponding interrupt is enabled. The software polls for CF1 bit to see if it is set. This allows the software to recognize that the QADC is finished with a queue 1 scan. The software acknowledges that it has detected the completion flag being set by writing a 0 to the completion flag after the bit was read as a 1.

PF1 — Queue 1 Pause Flag

PF1 indicates that a queue 1 scan has reached a pause. PF1 is set by the QADC when the current queue 1 CCW has the pause bit set, the selected input channel has been converted, and the result has been stored in the result table.

Once PF1 is set, the queue enters the paused state and waits for a trigger event to allow queue execution to continue. However, if the CCW with the pause bit set is the last CCW in a queue, the queue execution is complete. The queue status becomes idle, not paused, and both the pause and completion flags are set. Another exception occurs in software controlled mode, where the PF1 can be set but queue 1 never enters the pause state since queue 1 continues without pausing.

When PF1 is set and interrupts are enabled for the corresponding queue, the QADC asserts an interrupt request. The software may read PF1 during an interrupt service routine to identify the interrupt request. The interrupt request is cleared when the software writes a 0 to PF1, when the bit was previously read as a 1. Once set, only software or reset can clear PF1.

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In external gated single-scan and continuous-scan mode, the definition of PF1 has been redefined. When the gate closes before the end-of-queue 1 is reached, PF1 becomes set to indicate that an incomplete scan has occurred. In single-scan mode, setting PF1 can be used to cause an interrupt and software can then determine if queue 1 should be enabled again. In either external gated mode, setting PF1 indicates that the results for queue 1 have not been collected during one scan (coherently).

NOTE: *If a pause in a CCW is encountered in external gated mode for either single-scan and continuous-scan mode, the pause flag will not set, and execution continues without pausing. This has allowed for the added definition of PF1 in the external gated modes.*

PF1 is maintained by the QADC regardless of whether the corresponding interrupts are enabled. The software may poll PF1 to find out when the QADC has reached a pause in scanning a queue.The software acknowledges that it has detected a pause flag being set by writing a 0 to PF1 after the bit was last read as a 1.

1 = Queue 1 has reached a pause or gate closed before end-of-queue in gated mode.

0 = Queue 1 has not reached a pause or gate has not closed before end-of-queue in gated mode.

See **Table 18-7** for a summary of pause response in all scan modes.

Table 18-7. Pause Response

Scan Mode	Queue Operation	PF Asserts?
External trigger single-scan	Pauses	Yes
External trigger continuous-scan	Pauses	Yes
Interval timer trigger single-scan	Pauses	Yes
Interval timer continuous-scan	Pauses	Yes
Software-initiated single-scan	Continues	Yes
Software-initiated continuous-scan	Continues	Yes
External gated single-scan	Continues	No
External gated continuous-scan	Continues	No

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CF2 — Queue 2 Completion Flag

CF2 indicates that a queue 2 scan has been completed. CF2 is set by the QADC when the input channel sample requested by the last CCW in queue 2 is converted, and the result is stored in the result table.

The end-of-queue 2 is identified when the current CCW contains an end-of-queue code instead of a valid channel number or when the currently completed CCW is in the last location of the CCW RAM.

When CF2 is set and interrupts are enabled for that queue completion flag, the QADC asserts an interrupt request. The software reads CF2 during an interrupt service routine to identify the interrupt request. The interrupt request is cleared when the software writes a 0 to the CF2 bit, when the bit was previously read as a 1. Once set, only software or reset can clear CF2.

CF2 is maintained by the QADC regardless of whether the corresponding interrupts are enabled. The software polls for CF2 to see if it is set. This allows the software to recognize that the QADC is finished with a queue 2 scan. The software acknowledges that it has detected the completion flag being set by writing a 0 to the completion flag after the bit was read as a 1.

PF2 — Queue 2 Pause Flag

PF2 indicates that a queue 2 scan has reached a pause. PF2 is set by the QADC when the current queue 2 CCW has the pause bit set, the selected input channel has been converted, and the result has been stored in the result table.

Once PF2 is set, the queue enters the paused state and waits for a trigger event to allow queue execution to continue. However, if the CCW with the pause bit set is the last CCW in a queue, the queue execution is complete. The queue status becomes idle, not paused, and both the pause and completion flags are set. Another exception occurs in software controlled mode, where the PF2 can be set but queue 2 never enters the pause state.

When PF2 is set and interrupts are enabled for the corresponding queue, the QADC asserts an interrupt request. The software reads PF2 during an interrupt service routine to identify the interrupt request. The interrupt request is cleared when the software writes a 0 to PF2, when the bit was previously read as a 1. Once set, only software or reset can clear PF2.

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PF2 is maintained by the QADC regardless of whether the corresponding interrupts are enabled. The software may poll PF2 to find out when the QADC has reached a pause in scanning a queue. The software acknowledges that it has detected a pause flag being set by writing a 0 to PF2 after the bit was last read as a 1.

1 = queue 2 has reached a pause.
0 = queue 2 has not reached a pause.

See **Table 18-7** for a summary of pause response in all scan modes.

TOR1 — Queue 1 Trigger Overrun

TOR1 indicates that an unexpected trigger event has occurred for queue 1. TOR1 can be set only while queue 1 is in the active state.

A trigger event generated by a transition on the external trigger pin or by the periodic/interval timer may be captured as a trigger overrun. TOR1 cannot occur when the software-initiated single-scan mode or the software-initiated continuous-scan mode are selected.

TOR1 occurs when a trigger event is received while a queue is executing and before the scan has completed or paused. TOR1 has no effect on the queue execution.

After a trigger event has occurred for queue 1, and before the scan has completed or paused, additional queue 1 trigger events are not retained. Such trigger events are considered unexpected, and the QADC sets the TOR1 error status bit. An unexpected trigger event may be a system overrun situation, indicating a system loading mismatch.

In external gated continuous-scan mode, the definition of TOR1 has been redefined. In the case when queue 1 reaches an end-of-queue condition for the second time during an open gate, TOR1 becomes set. This is considered an overrun condition. In this case CF1 has been set for the first end-of-queue 1 condition and then TOR1 becomes set for the second end-of-queue 1 condition. For TOR1 to be set, software must not clear CF1 before the second end-of-queue 1.

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The software acknowledges that it has detected a trigger overrun being set by writing a 0 to the trigger overrun, after the bit was read as a 1. Once set, only software or reset can clear TOR1.

1 = At least one unexpected queue 1 trigger event has occurred or queue 1 reaches an end-of-queue condition for the second time in gated mode

0 = No unexpected queue 1 trigger events have occurred

TOR2 — Queue 2 Trigger Overrun Flag

TOR2 indicates that an unexpected trigger event has occurred for queue 2. TOR2 can be set when queue 2 is in the active, suspended, and trigger pending states.

The TOR2 trigger overrun can occur only when using an external trigger mode or a periodic/interval timer mode. Trigger overruns cannot occur when the software-initiated single-scan mode and the software-initiated continuous-scan mode are selected.

TOR2 occurs when a trigger event is received while queue 2 is executing, suspended, or a trigger is pending. TOR2 has no effect on the queue execution. A trigger event that causes a trigger overrun is not retained since it is considered unexpected.

An unexpected trigger event may be a system overrun situation, indicating a system loading mismatch. The software acknowledges that it has detected a trigger overrun being set by writing a 0 to the trigger overrun, after the bit was read as a 1. Once set, only software or reset can clear TOR2.

1 = At least one unexpected queue 2 trigger event has occurred.

0 = No unexpected queue 2 trigger events have occurred.

QS[9:6] — Queue Status Field

The 4-bit read-only QS field indicates the current condition of queue 1 and queue 2. There are five queue status conditions:

- Idle
- Active
- Paused
- Suspended
- Trigger pending

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The two most significant bits are associated primarily with queue 1, and the remaining two bits are associated with queue 2. Since the priority scheme between the two queues causes the status to be interlinked, the status bits are considered as one 4-bit field.

Table 18-8 shows the bits in the QS field and how they affect the status of queue 1 and queue 2.

One or both queues may be in the idle state. When a queue is idle, CCWs are not being executed for that queue, the queue is not in the pause state, and there is not a trigger pending.

The idle state occurs when a queue is disabled, when a queue is in a reserved mode, or when a queue is in a valid queue operating mode awaiting a trigger event to initiate queue execution.

Table 18-8. Queue Status

QS[9:6]	Queue 1/Queue 2 States
0000	Queue 1 idle, queue 2 idle
0001	Queue 1 idle, queue 2 paused
0010	Queue 1 idle, queue 2 active
0011	Queue 1 idle, queue 2 trigger pending
0100	Queue 1 paused, queue 2 idle
0101	Queue 1 paused, queue 2 paused
0110	Queue 1 paused, queue 2 active
0111	Queue 1 paused, queue 2 trigger pending
1000	Queue 1 active, queue 2 idle
1001	Queue 1 active, queue 2 paused
1010	Queue 1 active, queue 2 suspended
1011	Queue 1 active, queue 2 trigger pending
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

A queue is in the active state when a valid queue operating mode is selected, when the selected trigger event has occurred, or when the QADC is performing a conversion specified by a CCW from that queue.

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Only one queue can be active at a time. Either or both queues can be in the paused state. A queue is paused when the previous CCW executed from that queue had the pause bit set. The QADC does not execute any CCWs from the paused queue until a trigger event occurs. Consequently, the QADC can service queue 2 while queue 1 is paused.

Only queue 2 can be in the suspended state. When a trigger event occurs on queue 1 while queue 2 is executing, the current queue 2 conversion is aborted. The queue 2 status is reported as suspended. Queue 2 transitions back to the active state when queue 1 becomes idle or paused.

A trigger pending state is required since both queues cannot be active at the same time. The status of queue 2 is changed to trigger pending when a trigger event occurs for queue 2 while queue 1 is active. In the opposite case, when a trigger event occurs for queue 1 while queue 2 is active, queue 2 is aborted and the status is reported as queue 1 active, queue 2 suspended. So due to the priority scheme, only queue 2 can be in the trigger pending state.

Two transition cases cause the queue 2 status to be trigger pending before queue 2 is shown to be in the active state. When queue 1 is active and there is a trigger pending on queue 2, after queue 1 completes or pauses, queue 2 continues to be in the trigger pending state for a few clock cycles. The fleeting status conditions are:

- queue 1 idle with queue 2 trigger pending
- queue 1 paused with queue 2 trigger pending

Figure 18-12 displays the status conditions of the queue status field as the QADC goes through the transition from queue 1 active to queue 2 active.

The queue status field is affected by the stop mode. Since all of the analog logic and control registers are reset, the queue status field is reset to queue 1 idle, queue 2 idle.

During the debug mode, the queue status field is not modified. The queue status field retains the status it held prior to freezing. As a result, the queue status can show queue 1 active, queue 2 idle, even though neither queue is being executed during freeze.

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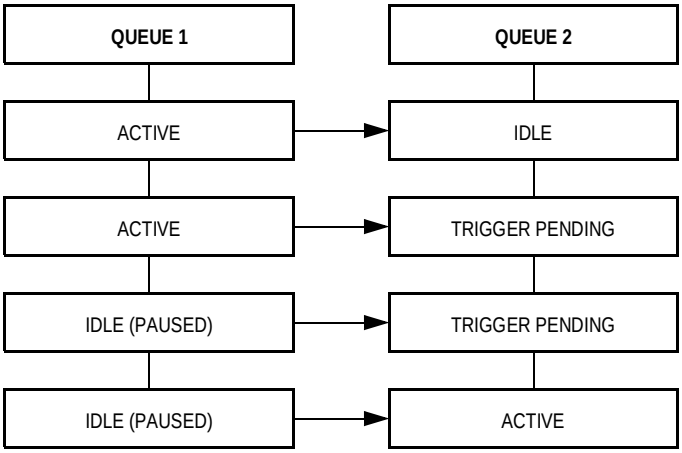

Figure 18-12. Queue Status Transition

CWP[5:0] — Command Word Pointer Field

The CWP allows the software to know which CCW is executing at present, or was last completed. The command word pointer is a software read-only field, and write operations have no effect. The CWP allows software to monitor the progress of the QADC scan sequence. The CWP field is a CCW word pointer with a valid range of 0 to 63.

When a queue enters the paused state, the CWP points to the CCW with the pause bit set. While in pause, the CWP value is maintained until a trigger event occurs on the same queue or the other queue. Usually, the CWP is updated a few clock cycles before the queue status field shows that the queue has become active. For example, software may read a CWP pointing to a CCW in queue 2, and the status field shows queue 1 paused, queue 2 trigger pending.

When the QADC finishes the scan of the queue, the CWP points to the CCW where the end-of-queue condition was detected. Therefore, when the end-of-queue condition is a CCW with the EOQ code (channel 63), the CWP points to the CCW containing the EOQ.

When the last CCW in a queue is in the last CCW table location (CCW63), and it does not contain the EOQ code, the end-of-queue is detected when the following CCW is read, so the CWP points to word CCW0.

Finally, when queue 1 operation is terminated after a CCW is read that is defined as BQ2, the CWP points to the same CCW as BQ2.

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During the stop mode, the CWP is reset to 0, since the control registers and the analog logic are reset. When the debug mode is entered, the CWP is unchanged; it points to the last executed CCW.

18.8.6.2 QADC Status Register 1

Stop mode resets the register ($3f3f)

Address: 0x00ca_0012 and 0x00ca_0013

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	CWPQ15	CWPQ14	CWPQ13	CWPQ12	CWPQ11	CWPQ10
Write:								
Reset:	0	0	1	1	1	1	1	1
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	CWPQ25	CWPQ24	CWPQ23	CWPQ22	CWPQ21	CWPQ20
Write:								
Reset:	0	0	1	1	1	1	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 18-13. QADC Status Register 1 (QASR1)

Read: Anytime

Write: Never

CWPQ1[5:0] — Queue 1 Command Word Pointer Field

CWPQ1[5:0] allows the software to know what CCW was last completed for queue 1. This field is a software read-only field, and write operations have no effect. CWPQ1 allows software to read the last executed CCW in queue 1, regardless of which queue is active. The CWPQ1[5:0] field is a CCW word pointer with a valid range of 0 to 63 (0x3f).

In contrast to CWP, CPWQ1 is updated when the conversion result is written. When the QADC finishes a conversion in queue 1, both the result register is written and the CWPQ1 is updated.

Finally, when queue 1 operation is terminated after a CCW is read that is defined as BQ2, CWP points to BQ2 while CWPQ1 points to the last CCW queue 1.

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During the stop mode, the CWPQ1 is reset to 63 (0x3f), since the control registers and the analog logic are reset. When the debug mode is entered, the CWPQ1 is unchanged; it points to the last executed CCW in queue 1.

CWPQ2[5:0] — Queue 2 Command Word Pointer Field

CWPQ2[5:0] allows the software to know what CCW was last completed for queue 2. This field is a software read-only field, and write operations have no effect. CWPQ2[5:0] allows software to read the last executed CCW in queue 2, regardless which queue is active. The CWPQ2[5:0] field is a CCW word pointer with a valid range of 0 to 63.

In contrast to CWP, CPWQ2 is updated when the conversion result is written. When the QADC finishes a conversion in queue 2, both the result register is written and the CWPQ2 are updated.

During the stop mode, the CWPQ2 is reset to 63, since the control registers and the analog logic are reset. When the debug mode is entered, the CWP is unchanged; it points to the last executed CCW in queue 2.

18.8.7 Conversion Command Word Table

Address: 0x00ca_0200 through 0x00ca_027e

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	0	0	0	0	P	BYP
Write:								
Reset:	0	0	0	0	0	0	U	U

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IST1	IST0	CHAN5	CHAN4	CHAN3	CHAN2	CHAN1	CHAN0
Write:								
Reset:	U	U	U	U	U	U	U	U

= Writes have no effect and the access terminates without a transfer error exception.

U = Unaffected

Figure 18-14. Conversion Command Word Table (CCW)

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Read: Anytime except reads during stop mode are invalid

Write: Anytime except stop mode

P — Pause Bit

The pause bit allows software to create subqueues within queue 1 and queue 2. The QADC performs the conversion specified by the CCW with the pause bit set, and then the queue enters the pause state. Another trigger event causes execution to continue from the pause to the next CCW.

1 = Enter pause state after execution of current CCW
0 = Do not enter pause state after execution of current CCW

NOTE: *The P bit does not cause the queue to pause in the software controlled modes or external gated modes.*

BYP — Sample Amplifier Bypass Bit

Setting the BYP field in the CCW enables the amplifier bypass mode for a conversion and subsequently changes the timing. The initial sample time is eliminated, reducing the potential conversion time by two QCLKs. However, due to internal RC effects, a minimum final sample time of four QCLKs must be allowed. When using this mode, the external circuit should be of low source impedance. Loading effects of the external circuitry need to be considered, since the benefits of the sample amplifier are not present.

1 = Amplifier bypass mode enabled
0 = Amplifier bypass mode disabled

NOTE: *BYP is maintained for software compatibility but has no functional benefit to this version of the module.*

IST[0:1] — Input Sample Time Field

The IST field allows software to specify the length of the sample window. Provision is made to vary the input sample time, through software control, to offer flexibility in the source impedance of the circuitry providing the QADC analog channel inputs. Longer sample times permit more accurate A/D conversions of signals with higher source impedances.

Table 18-9 shows the four selectable input sample times.

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Table 18-9. Input Sample Times

IST[0:1]	Input Sample Times
00	Input sample time = QCLK period × 2
01	Input sample time = QCLK period × 4
10	Input sample time = QCLK period × 8
11	Input sample time = QCLK period × 16

The programmable sample time can also be used to increase the time interval between conversions to adjust the queue execution time or the sampling rate.

CHAN[5:0] — Channel Number Field

The CHAN field selects the input channel number. The software programs the channel field of the CCW with the channel number corresponding to the analog input pin to be sampled and converted. The analog input pin channel number assignments and the pin definitions vary depending on whether the multiplexed or non-multiplexed mode is used by the application. As far as the queue scanning operations are concerned, there is no distinction between an internally or externally multiplexed analog input.

Table 18-10 shows the channel number assignments for the non-multiplexed mode. **Table 18-11** shows the channel number assignments for the multiplexed mode.

The channel field is programmed for channel 63 to indicate the end of the queue. Channels 60 to 62 are special internal channels. When one of the special channels is selected, the sampling amplifier is not used. The value of V_{RL}, V_{RH}, or $(V_{RH}–V_{RL})/2$ is placed directly onto the converter. Also for the internal special channels, programming any input sample time other than two has no benefit except to lengthen the overall conversion time.

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Table 18-10. Non-Multiplexed Channel Assignments and Pin Designations

Non-Multiplexed Input Pins				Channel Number(1) in CCW CHAN Field	
Port Pin Name	**Analog Pin Name**	**Other Functions**	**Pin Type**	**Binary**	**Decimal**
PQB0 PQB1 PQB2 PQB3	AN0 AN1 AN2 AN3	— — — —	Input Input Input Input	000000 000001 000010 000011	0 1 2 3
PQA0 PQA1	AN52 AN53	— —	Input/output Input/output	110100 110101	52 53
PQA3 PQA4	AN55 AN56	ETRIG1 ETRIG2	Input/output Input/output	110111 111000	55 56
V_{RL} V_{RH} —	Low reference High reference —	— — $(V_{RH}–V_{RL})/2$	Input Input —	111100 111101 111110	60 61 62
—	—	End-of-queue code	—	111111	63

1. All channels not listed are reserved or unimplemented and return undefined results.

Table 18-11. Multiplexed Channel Assignments and Pin Designations

Multiplexed Input Pins				Channel Number(1) in CCW CHAN Field	
Port Pin Name	**Analog Pin Name**	**Other Functions**	**Pin Type**	**Binary**	**Decimal**
PQB0 PQB1 PQB2 PQB3	ANw ANx ANy ANz	— — — —	Input Input Input Input	000XX0 000XX1 010XX0 010XX1	0, 2, 4, 6 1, 3, 5, 7 16, 18, 20, 22 17, 19, 21, 23
PQA0 PQA1	— —	MA0 MA1	Output Output	110100 110101	52 53
PQA3 PQA4	AN55 AN56	ETRIG1 ETRIG2	Input/output Input/output	110111 111000	55 56
V_{RL} V_{RH} —	Low reference High reference —	— — $(V_{RH}–V_{RL})/2$	Input Input —	111100 111101 111110	60 61 62
—	—	End-of-queue code	—	111111	63

1. All channels not listed are reserved or unimplemented and return undefined results.

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18.8.8 Result Registers

This subsection describes the result registers.

18.8.8.1 Right-Justified Unsigned Result Register

Address: 0x00ca_0280 through 0x00ca_02fe

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	0	0	0	0	0	0	RESULT	
Write:								
Reset:	0	0	0	0	0	0		

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RESULT							
Write:								
Reset:								

= Writes have no effect and the access terminates without a transfer error exception.

Figure 18-15. Right-Justified Unsigned Result Register (RJURR)

Read: Anytime except reads during stop mode are invalid

Write: Anytime except stop mode

RESULT[9:0] — Result Field

The conversion result is unsigned, right-justified data.

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18.8.8.2 Left-Justified Signed Result Register

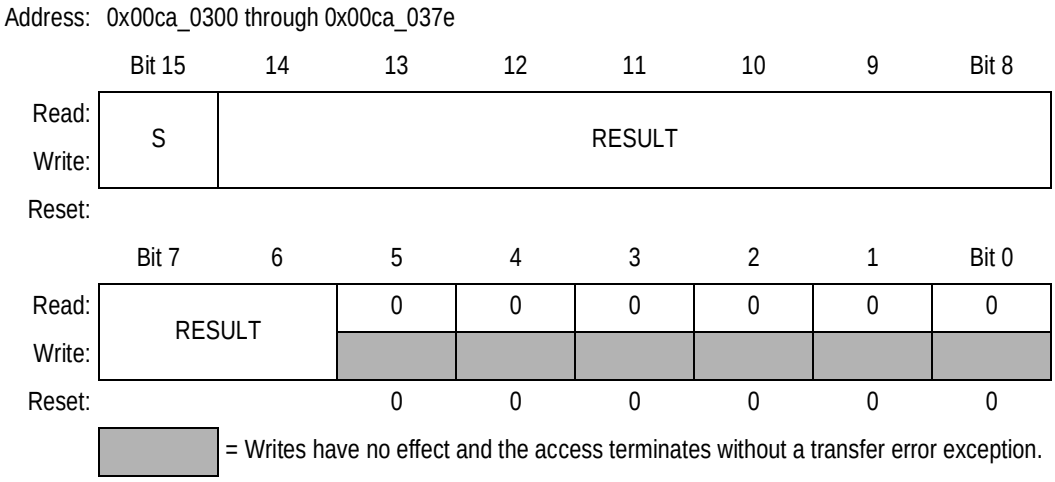

Figure 18-16. Left-Justified Signed Result Register (LJSRR)

S — Sign Bit

RESULT[14:6] — Result Field

The conversion result is signed, left-justified data.

18.8.8.3 Left-Justified Unsigned Result Register

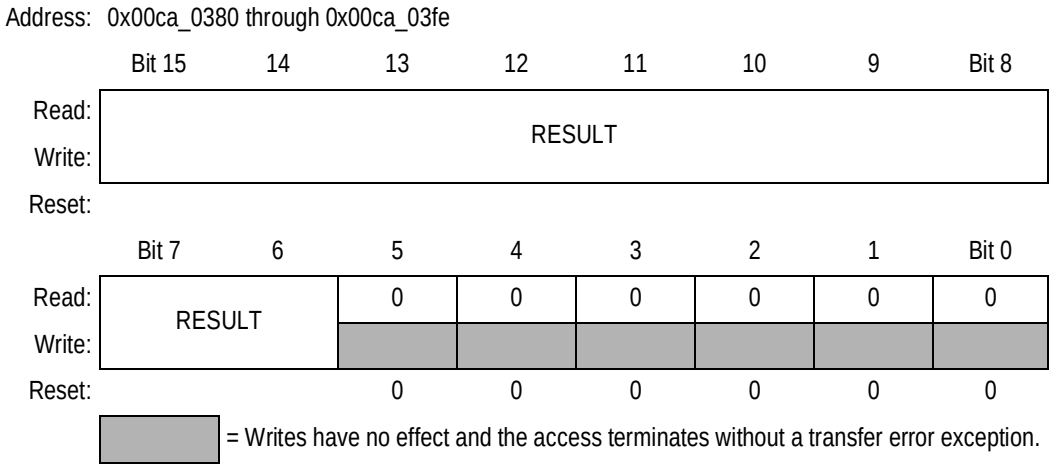

Figure 18-17. Left-Justified Unsigned Result Register (LJURR)

RESULT[15:6] — Result Field

The conversion result is unsigned, left-justified data.

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18.9 Functional Description

This subsection provides a functional description of the QADC.

18.9.1 QADC Bus Accessing

Coherency of results read across multiple cycles is not guaranteed.

18.9.2 External Multiplexing

External multiplexer chips concentrate a number of analog signals onto a few inputs to the analog converter. This is helpful in applications that need to convert more analog signals than the A/D converter can normally provide. External multiplexing also puts the multiplexed chip closer to the signal source. This minimizes the number of analog signals that need to be shielded due to the proximity to noisy high speed digital signals at the microcontroller chip.

For example, four 4-input multiplexer chips can be put at the connector where the analog signals first arrive on the computer board. As a result, only four analog signals need to be shielded from noise as they approach the microcontroller chip, rather than having to protect 16 analog signals. However, external multiplexer chips may introduce additional noise and errors if not properly utilized. Therefore, it is necessary to maintain low “on” resistance (the impedance of an analog switch when active within a multiplexed chip) and insert a low pass filter (R/C) on the input side of the multiplexed chip.

18.9.2.1 External Multiplexing Operation

The QADC can use from one to four or two dual external multiplexer chips to expand the number of analog signals that may be converted. Up to 16 analog channels can be converted through external multiplexer selection. The externally multiplexed channels are automatically selected from the channel field of the conversion command word (CCW) table, the same as internally multiplexed channels. The software selects the external multiplexed mode by setting the MUX bit in control register 0 (QACR0).

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Figure 18-18 shows the maximum configuration of four external multiplexer chips connected to the QADC. The external multiplexer chips select one of four analog inputs and connect it to one analog output, which becomes an input to the QADC. The QADC provides two multiplexed address signals — MA[1:0] — to select one of four inputs. These inputs are connected to all four external multiplexer chips. The analog output of the four multiplex chips are each connected to separate QADC inputs (ANw, ANx, ANy, and ANz) as shown in Figure 18-18.

When the external multiplexed mode is selected, the QADC automatically creates the MA output signals from the channel number in each CCW. The QADC also converts the proper input channel (ANw, ANx, ANy, and ANz) by interpreting the CCW channel number. As a result, up to 16 externally multiplexed channels appear to the conversion queues as directly connected signals. The software simply puts the channel number of externally multiplexed channels into CCWs.

Figure 18-18 shows that the two MA signals may also be analog input pins. When external multiplexing is selected, none of the MA pins can be used for analog or digital inputs. They become multiplexed address outputs and are unaffected by DDRQA[1:0].

18.9.2.2 Module Version Options

The number of available analog channels varies, depending on whether external multiplexing is used. A maximum of 16 analog channels are supported by the internal multiplexing circuitry of the converter. Table 18-12 shows the total number of analog input channels supported with 0 to four external multiplexer chips.

Table 18-12. Analog Input Channels

Number of Analog Input Channels Available Directly Connected + External Multiplexed = Total Channels(1), (2)				
No External Mux	**One External Mux**	**Two External Muxes**	**Three External Muxes**	**Four External Muxes**
8	5 + 4 = 9	4 + 8 = 12	3 + 12 = 15	2 + 16 = 18

1. The external trigger inputs are not shared with two analog input pins.
2. When external multiplexing is used, two input channels can be configured as multiplexed address outputs, and for each external multiplexer chip, one input channel is a multiplexed analog input.

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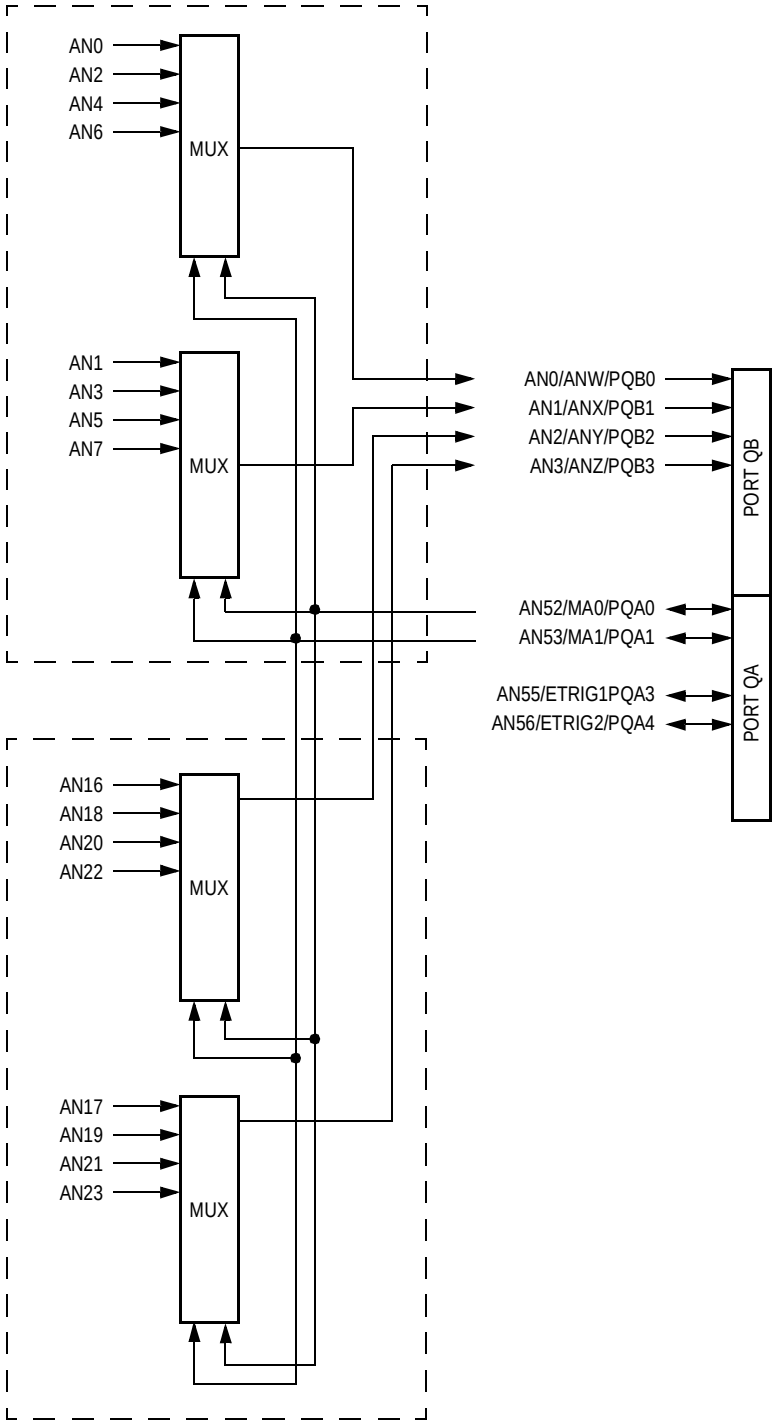

Figure 18-18. External Multiplexing Configuration

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18.9.2.3 External Multiplexed Address Configuration

The QADC can drive external multiplexed addresses. If configured to drive external addresses, the external address pins MA[1:0] will function as address pins and will not maintain analog input functions in external address mode.

18.9.3 Analog Subsystem

This section describes the QADC analog subsystem, which includes the front-end analog multiplexer and analog-to-digital converter.

18.9.3.1 Analog-to-Digital Converter Operation

The analog subsystem consists of the path from the input pins to the A/D converter block. Signals from the queue control logic are fed to the multiplexer and state machine. The end-of-conversion (EOC) signal and the successive-approximation register (SAR) reflect the result of the conversion. **Figure 18-19** shows a block diagram of the QADC analog subsystem.

NOTE: *The following description assumes the use of a buffer amplifier.*

18.9.3.2 Conversion Cycle Times

Total conversion time is made up of initial sample time, final sample time, and resolution time. Initial sample time refers to the time during which the selected input channel is coupled through the buffer amplifier to the sample capacitor. This buffer is used to quickly reproduce its input signal on the sample capacitor and minimize charge sharing errors. During the final sampling period the amplifier is bypassed, and the multiplexer input charges the sample capacitor array directly for improved accuracy. During the resolution period, the voltage in the sample capacitor is converted to a digital value and stored in the SAR.

Initial sample time is fixed at two QCLK cycles. Final sample time can be 2, 4, 8, or 16 QCLK cycles, depending on the value of the IST field in the CCW. Resolution time is 10 QCLK cycles.

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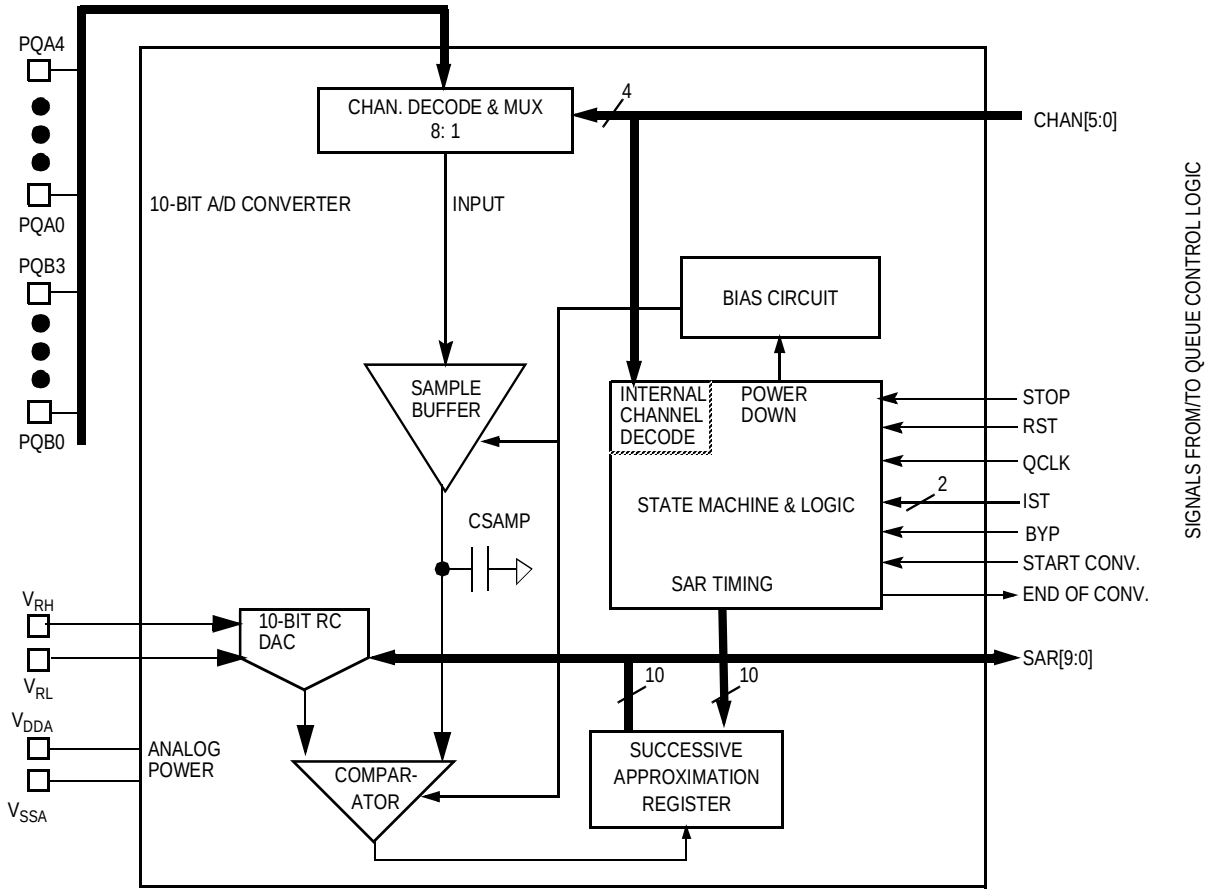

Figure 18-19. QADC Analog Subsystem Block Diagram

Therefore, conversion time requires a minimum of 14 QCLK clocks (7 µs with a 2.0-MHz QCLK). If the maximum final sample time period of 16 QCLKs is selected, the total conversion time is 28 QCLKs or 14 µs (with a 2.0-MHz QCLK).

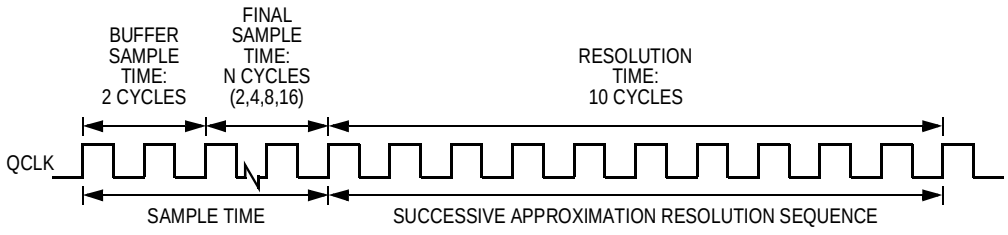

Figure 18-20. Conversion Timing

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If the amplifier bypass mode is enabled for a conversion by setting the amplifier bypass (BYP) field in the CCW, the timing changes to that shown in **Figure 18-21**. See **18.8.7 Conversion Command Word Table** for more information on the BYP field. The initial sample time is eliminated, reducing the potential conversion time by two QCLKs. When using the bypass mode, the external circuit should be of low source impedance (typically less than 10 kΩ). Also, the loading effects to the external circuitry by the QADC need to be considered, since the benefits of the sample amplifier are not present.

NOTE: *Because of internal RC time constants, it is not recommended to use a sample time of two QCLKs in bypass mode for high-frequency operation.*

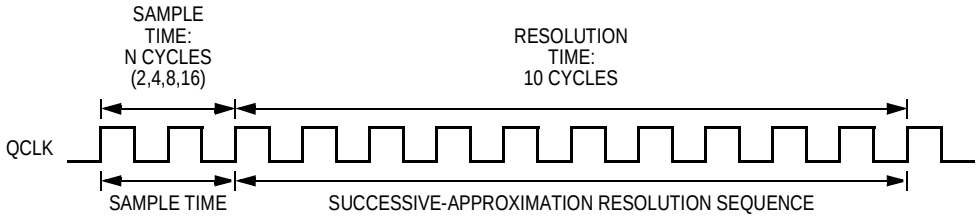

Figure 18-21. Bypass Mode Conversion Timing

18.9.3.3 Channel Decode and Multiplexer

The internal multiplexer selects one of the eight analog input pins for conversion. The selected input is connected to the Sample Buffer Amplifier or to the sample capacitor. The multiplexer also includes positive and negative stress protection circuitry, which prevents deselected channels from affecting the selected channel when current is injected into the deselected channels.

18.9.3.4 Sample Buffer

The sample buffer is used to raise the effective input impedance of the A/D converter, so that external components (higher bandwidth or higher impedance) are less critical to accuracy. The input voltage is buffered onto the sample capacitor to reduce crosstalk between channels.

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18.9.3.5 Digital-to-Analog Converter (DAC) Array

The digital-to-analog converter (DAC) array consists of binary-weighted capacitors and a resistor-divider chain. The reference voltages, VRH and VRL, are used by the DAC to perform ratiometric conversions. The DAC also converts the following three internal channels:

- V_{RH} — reference voltage high
- V_{RL} — reference voltage low
- $(V_{RH}–V_{RL})/2$ — reference voltage

The DAC array serves to provide a mechanism for the successive approximation A/D conversion.

Resolution begins with the most significant bit (MSB) and works down to the least significant bit (LSB). The switching sequence is controlled by the comparator and SAR logic. The sample capacitor samples and holds the voltage to be converted.

18.9.3.6 Comparator

During the approximation process, the comparator senses whether the digitally selected arrangement of the DAC array produces a voltage level higher or lower than the sampled input. The comparator output feeds into the SAR which accumulates the A/D conversion result sequentially, beginning with the MSB.

18.9.3.7 Bias

The bias circuit is controlled by the STOP signal to power-up and power-down all the analog circuits.

18.9.3.8 Successive-Approximation Register

The input of the SAR is connected to the comparator output. The SAR sequentially receives the conversion value one bit at a time, starting with the MSB. After accumulating the 10 bits of the conversion result, the SAR data is transferred to the appropriate result location, where it may be read from the IPbus by user software.

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18.9.3.9 State Machine

The state machine receives the QCLK, RST, STOP, IST[1:0], BYP, CHAN[5:0], and START CONV. signals, from which it generates all timing to perform an A/D conversion. The start-conversion signal (START CONV.) indicates to the A/D converter that the desired channel has been sent to the MUX. IST[1:0] indicates the desired sample time. BYP indicates whether to bypass the sample amplifier. The end-of-conversion (EOC) signal notifies the queue control logic that a result is available for storage in the result RAM.

18.10 Digital Control

The digital control subsystem includes the control logic to sequence the conversion activity, the clock and periodic/interval timer, control and status registers, the conversion command word table RAM, and the result word table RAM.

The central element for control of the QADC conversions is the 64-entry conversion command word (CCW) table. Each CCW specifies the conversion of one input channel. Depending on the application, one or two queues can be established in the CCW table. A queue is a scan sequence of one or more input channels. By using a pause mechanism, subqueues can be created in the two queues. Each queue can be operated using one of several different scan modes. The scan modes for queue 1 and queue 2 are programmed in the control registers QACR1 and QACR2. Once a queue has been started by a trigger event (any of the ways to cause the QADC to begin executing the CCWs in a queue or subqueue), the QADC performs a sequence of conversions and places the results in the result word table.

18.10.1 Queue Priority Timing Examples

This subsection describes the QADC priority scheme when trigger events on two queues overlap or conflict.

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18.10.1.1 Queue Priority

Queue 1 has priority over queue 2 execution. These cases show the conditions under which queue 1 asserts its priority:

- When a queue is not active, a trigger event for queue 1 or queue 2 causes the corresponding queue execution to begin.
- When queue 1 is active and a trigger event occurs for queue 2, queue 2 cannot begin execution until queue 1 reaches completion or the paused state. The status register records the trigger event by reporting the queue 2 status as trigger pending. Additional trigger events for queue 2, which occur before execution can begin, are captured as trigger overruns.
- When queue 2 is active and a trigger event occurs for queue 1, the current queue 2 conversion is aborted. The status register reports the queue 2 status as suspended. Any trigger events occurring for queue 2 while queue 2 is suspended are captured as trigger overruns. Once queue 1 reaches the completion or the paused state, queue 2 begins executing again. The programming of the RESUME bit in QACR2 determines which CCW is executed in queue 2.
- When simultaneous trigger events occur for queue 1 and queue 2, queue 1 begins execution and the queue 2 status is changed to trigger pending.
- Subqueues that are paused

The pause feature can be used to divide queue 1 and/or queue 2 into multiple subqueues. A subqueue is defined by setting the pause bit in the last CCW of the subqueue.

Figure 18-22 shows the CCW format and an example of using pause to create subqueues. Queue 1 is shown with four CCWs in each subqueue and queue 2 has two CCWs in each subqueue.

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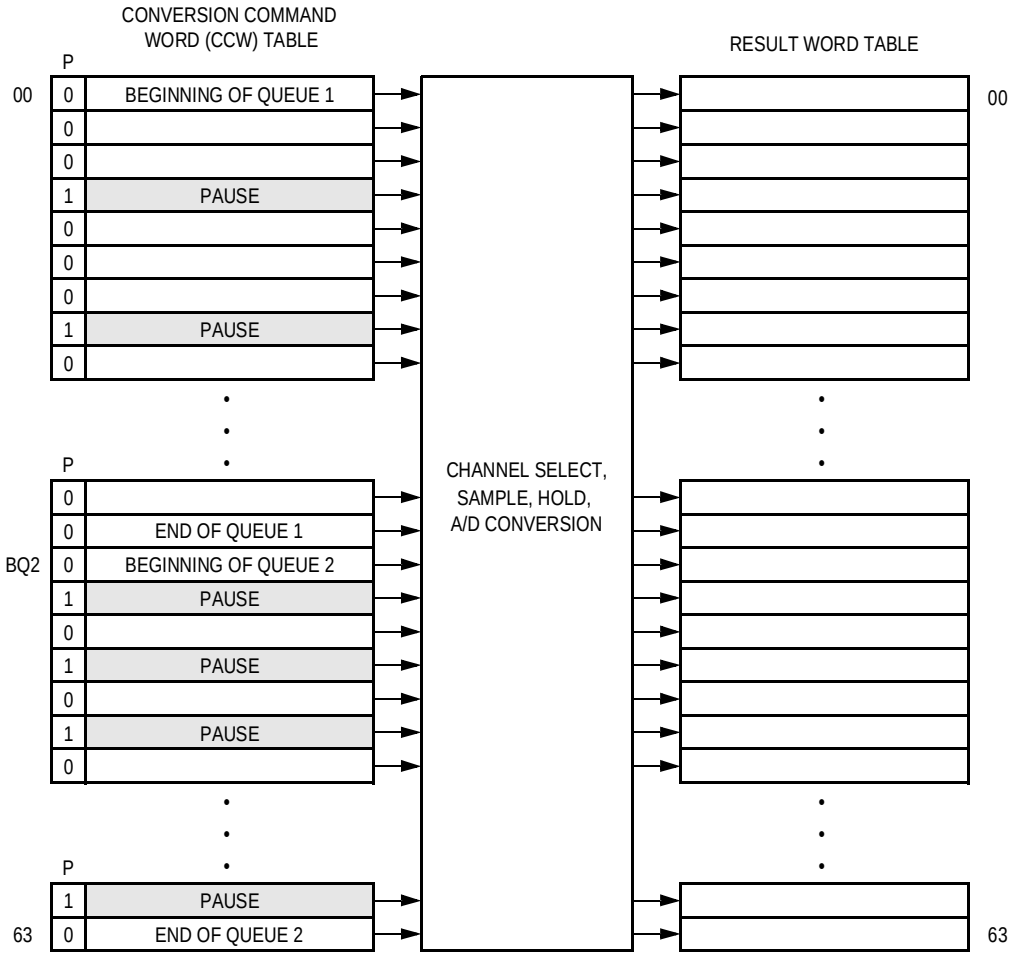

Figure 18-22. QADC Queue Operation with Pause

The queue operating mode selected for queue 1 determines what type of trigger event causes the execution of each of the subqueues within queue 1. Similarly, the queue operating mode for queue 2 determines the type of trigger event required to execute each of the subqueues within queue 2.

For example, when the external trigger rising edge continuous-scan mode is selected for queue 1, and there are six subqueues within queue 1, a separate rising edge is required on the external trigger pin after every pause to begin the execution of each subqueue (refer to **Figure 18-22**).

The choice of single-scan or continuous-scan applies to the full queue, and is not applied to each subqueue. Once a subqueue is initiated, each

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CCW is executed sequentially until the last CCW in the subqueue is executed and the pause state is entered. Execution can only continue with the next CCW, which is the beginning of the next subqueue. A subqueue cannot be executed a second time before the overall queue execution has been completed.

Trigger events which occur during the execution of a subqueue are ignored, except that the trigger overrun flag is set. When a continuous-scan mode is selected, a trigger event occurring after the completion of the last subqueue (after the queue completion flag is set), causes the execution to continue with the first subqueue, starting with the first CCW in the queue.

When the QADC encounters a CCW with the pause bit set, the queue enters the paused state after completing the conversion specified in the CCW with the pause bit. The pause flag is set and a pause software interrupt may optionally be issued. The status of the queue is shown to be paused, indicating completion of a subqueue. The QADC then waits for another trigger event to again begin execution of the next subqueue.

18.10.1.2 Queue Priority Schemes

Since there are two conversion command queues and only one A/D converter, there is a priority scheme to determine which conversion is to occur. Each queue has a variety of trigger events that are intended to initiate conversions, and they can occur asynchronously in relation to each other and other conversions in progress. For example, a queue can be idle awaiting a trigger event, a trigger event can have occurred, but the first conversion has not started, a conversion can be in progress, a pause condition can exist awaiting another trigger event to continue the queue, and so on.

The following paragraphs and figures outline the prioritizing criteria used to determine which conversion occurs in each overlap situation.

NOTE: *Each situation in **Figure 18-23** through **Figure 18-33** are labeled S1 through S19. In each diagram, time is shown increasing from left to right. The execution of queue 1 and queue 2 (Q1 and Q2) is shown as a string of rectangles representing the execution time of each CCW in the queue. In most of the situations, there are four CCWs (labeled C1 to C4) in both queue 1 and queue 2. In some of the situations, CCW C2 is presumed*

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to have the pause bit set, to show the similarities of pause and end-of-queue as terminations of queue execution.

Trigger events are described in **Table 18-13**.

Table 18-13. Trigger Events

Trigger	Events
T1	Events that trigger queue 1 execution (external trigger, software-initiated single-scan enable bit, or completion of the previous continuous loop)
T2	Events that trigger queue 2 execution (external trigger, software-initiated single-scan enable bit, timer period/interval expired, or completion of the previous continuous loop)

When a trigger event causes a CCW execution in progress to be aborted, the aborted conversion is shown as a ragged end of a shortened CCW rectangle.

The situation diagrams also show when key status bits are set. **Table 18-14** describes the status bits.

Table 18-14. Status Bits

Bit	Function
CF flag	Set when the end of the queue is reached
PF flag	Set when a queue completes execution up through a pause bit
Trigger overrun error (TOR)	Set when a new trigger event occurs before the queue is finished serving the previous trigger event

Below the queue execution flows are three sets of blocks that show the status information that is made available to the software. The first two rows of status blocks show the condition of each queue as:

- Idle
- Active
- Pause
- Suspended (queue 2 only)
- Trigger pending

The third row of status blocks shows the 4-bit QS status register field that encodes the condition of the two queues. Two transition status cases,

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QS = 0011 and QS = 0111, are not shown because they exist only very briefly between stable status conditions.

The first three examples in **Figure 18-23** through **Figure 18-25** (S1, S2, and S3) show what happens when a new trigger event is recognized before the queue has completed servicing the previous trigger event on the same queue.

In situation S1 (**Figure 18-23**), one trigger event is being recognized on each queue while that queue is still working on the previously recognized trigger event. The trigger overrun error status bit is set, and otherwise, the premature trigger event is ignored. A trigger event which occurs before the servicing of the previous trigger event is through does not disturb the queue execution in progress.

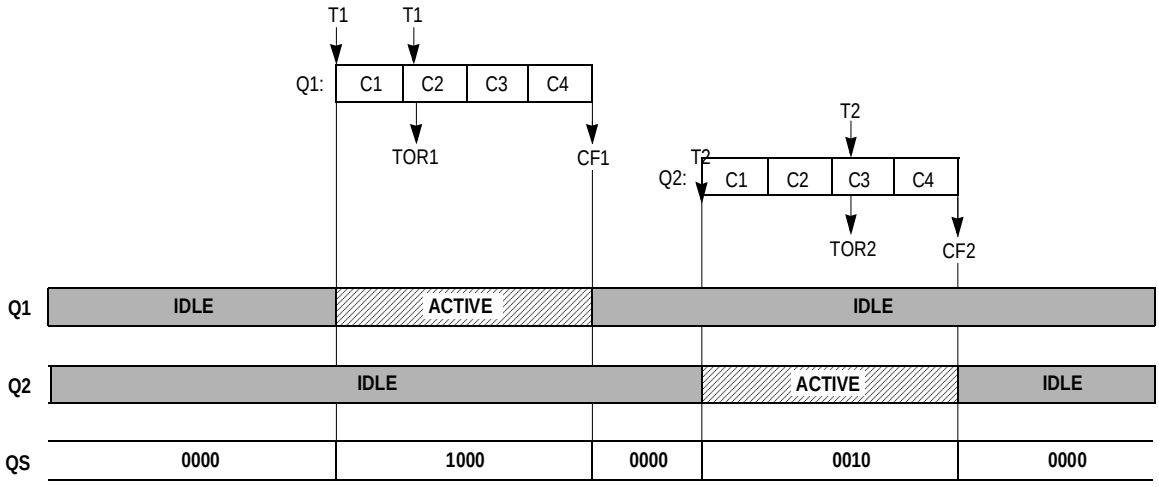

Figure 18-23. CCW Priority Situation 1

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In situation S2 (**Figure 18-24**), more than one trigger event is recognized before servicing of a previous trigger event is complete, the trigger overrun bit is again set, but otherwise, the additional trigger events are ignored. After the queue is complete, the first newly detected trigger event causes queue execution to begin again. When the trigger event rate is high, a new trigger event can be seen very soon after completion of the previous queue, leaving software little time to retrieve the previous results. Also, when trigger events are occurring at a high rate for queue 1, the lower priority queue 2 channels may not get serviced at all.

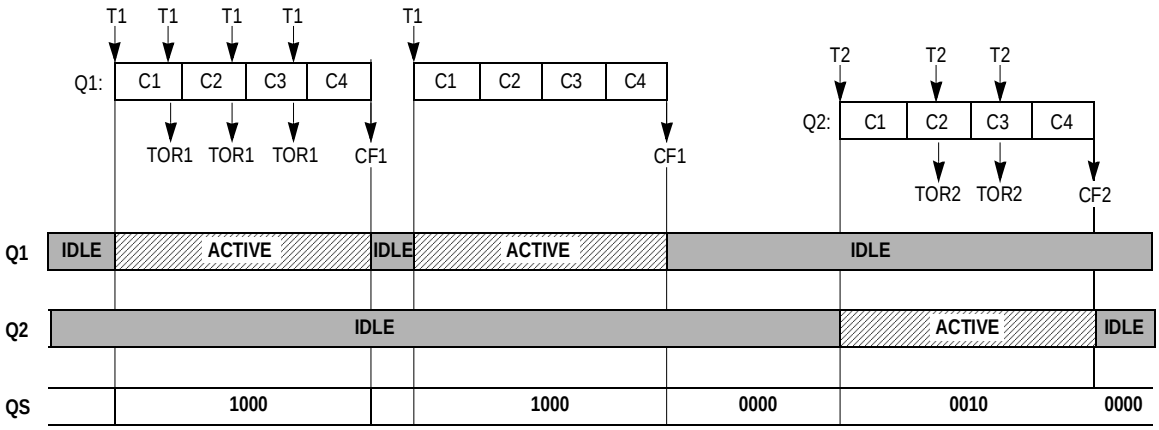

Figure 18-24. CCW Priority Situation 2

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Situation S3 (**Figure 18-25**) shows that when the pause feature is in use, the trigger overrun error status bit is set the same way, and that queue execution continues unchanged.

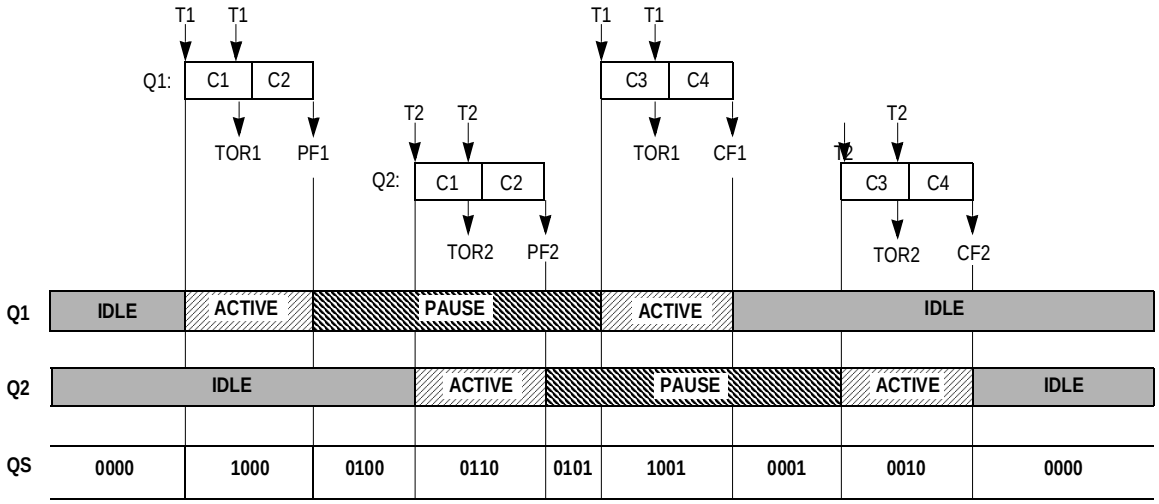

Figure 18-25. CCW Priority Situation 3

The next two situations consider trigger events that occur for the lower priority queue 2, while queue 1 is actively being serviced.

Situation S4 (**Figure 18-26**) shows that a queue 2 trigger event that is recognized while queue 1 is active is saved, and as soon as queue 1 is finished, queue 2 servicing begins.

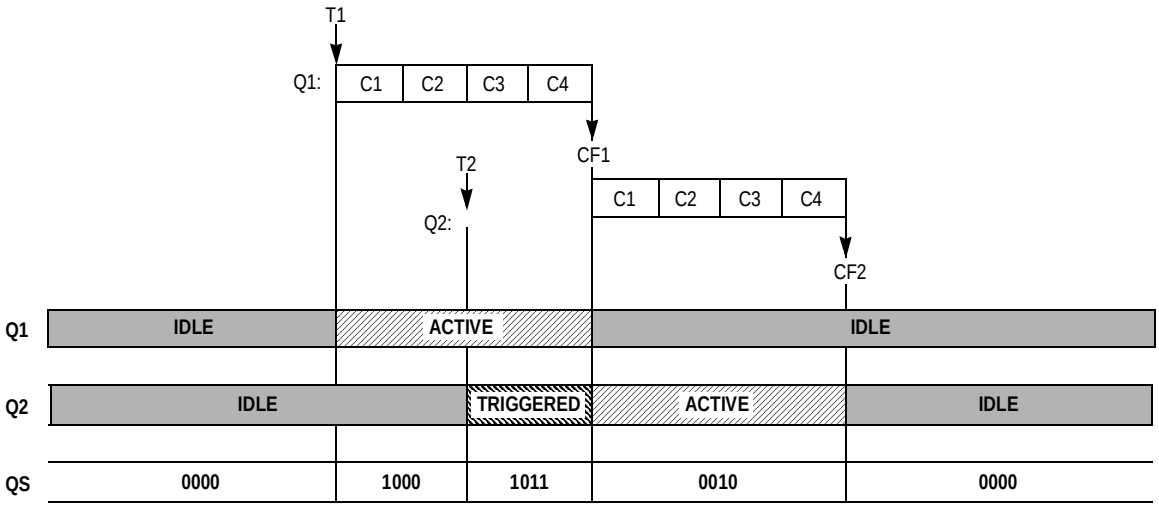

Figure 18-26. CCW Priority Situation 4

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Situation S5 (**Figure 18-27**) shows that when multiple queue 2 trigger events are detected while queue 1 is busy, the trigger overrun error bit is set, but queue 1 execution is not disturbed. Situation S5 also shows that the effect of queue 2 trigger events during queue 1 execution is the same when the pause feature is in use in either queue.

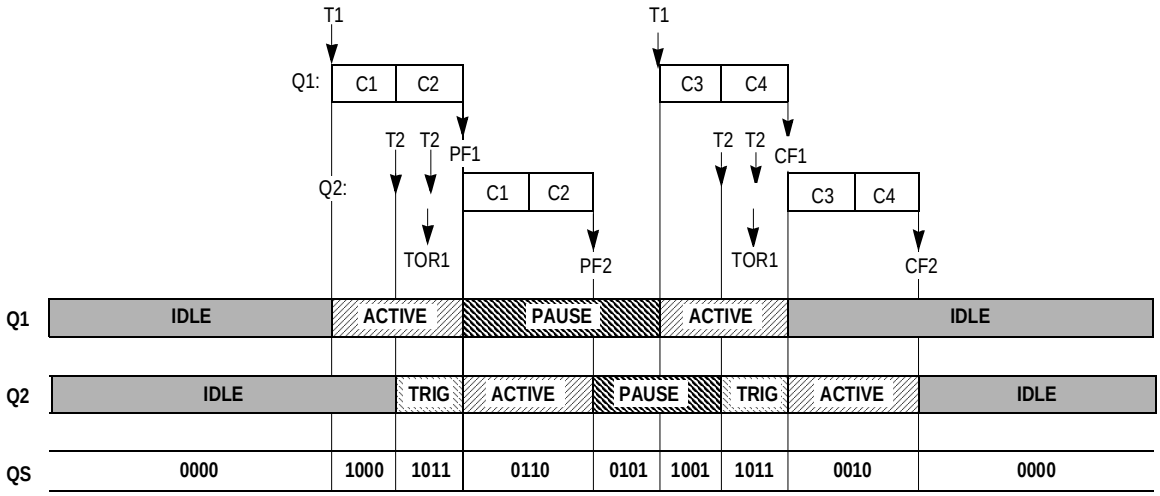

Figure 18-27. CCW Priority Situation 5

The remaining situations, S6 through S11, show the impact of a queue 1 trigger event occurring during queue 2 execution. Queue 1 is higher in priority, the conversion taking place in queue 2 is aborted, so that there is not a variable latency time in responding to queue 1 trigger events.

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In situation 6 (**Figure 18-28**), the conversion initiated by the second CCW in queue 2 is aborted just before the conversion is complete, so that queue 1 execution can begin. Queue 2 is considered suspended. After queue 1 is finished, queue 2 starts over with the first CCW, when the RES (resume) control bit is set to 0. Situation S7 (**Figure 18-29**) shows that when pause operation is not in use with queue 2, queue 2 suspension works the same way.

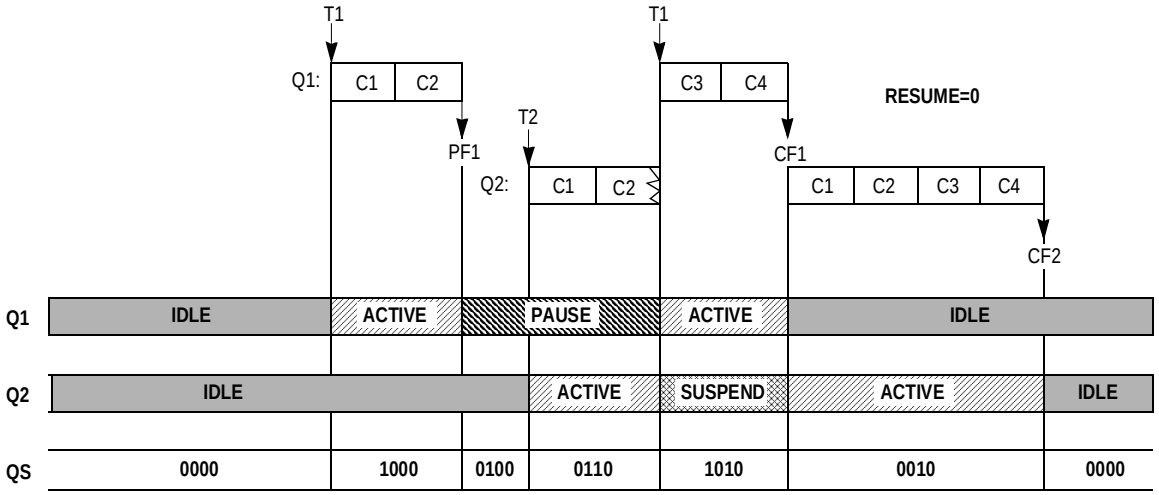

Figure 18-28. CCW Priority Situation 6

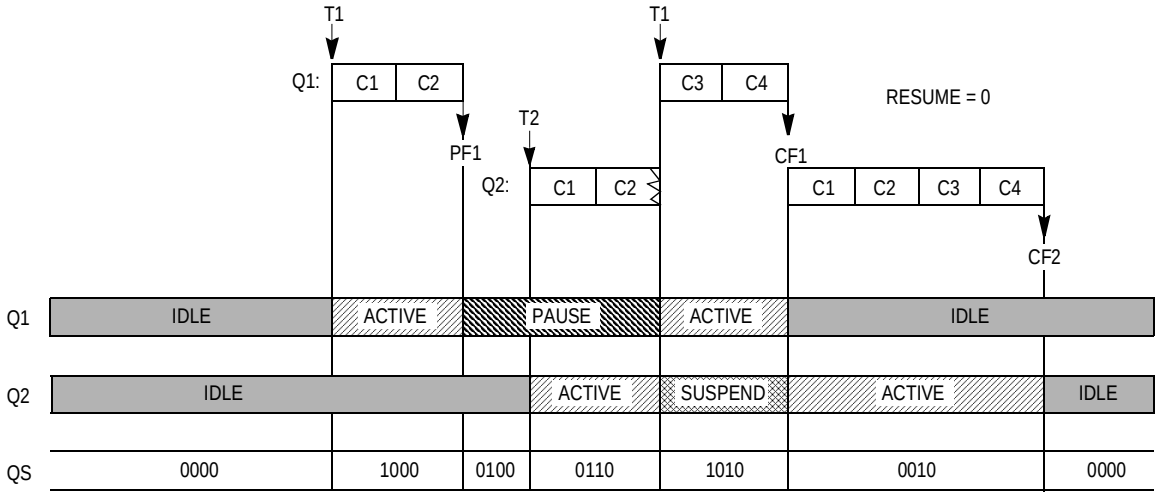

Figure 18-29. CCW Priority Situation 7

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Situations S8 and S9 (**Figure 18-30** and **Figure 18-31**) repeat the same two situations with the RESUME bit set to a 1. When the RES bit is set, following suspension, queue 2 resumes execution with the aborted CCW, not the first CCW in the queue.

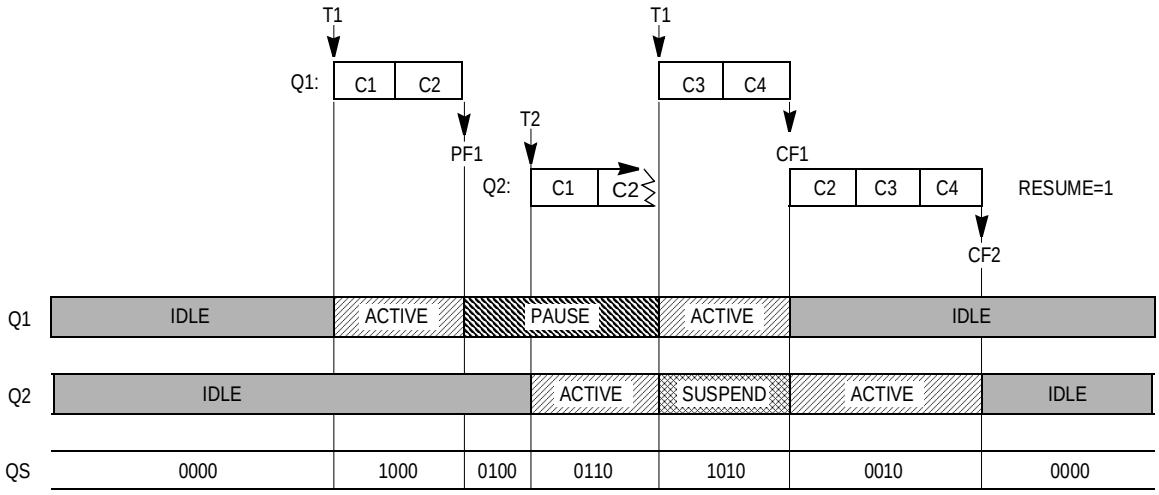

Figure 18-30. CCW Priority Situation 8

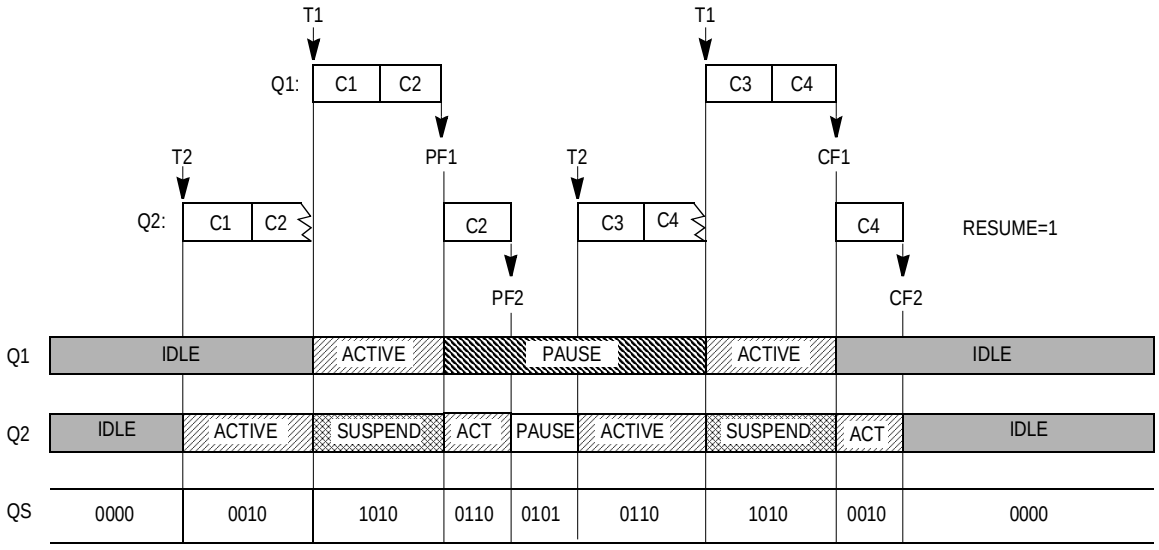

Figure 18-31. CCW Priority Situation 9

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Situations S10 and S11 (**Figure 18-32** and **Figure 18-33**) show that when an additional trigger event is detected for queue 2 while the queue is suspended, the trigger overrun error bit is set, the same as if queue 2 were being executed when a new trigger event occurs. Trigger overrun on queue 2 thus permits the software to know that queue 1 is taking up so much QADC time that queue 2 trigger events are being lost.

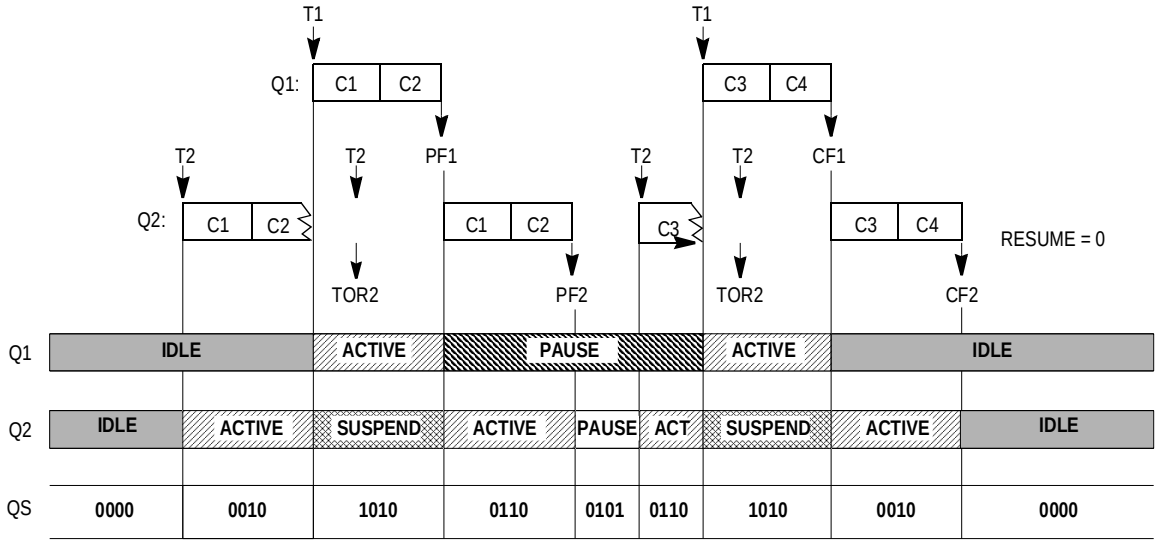

Figure 18-32. CCW Priority Situation 10

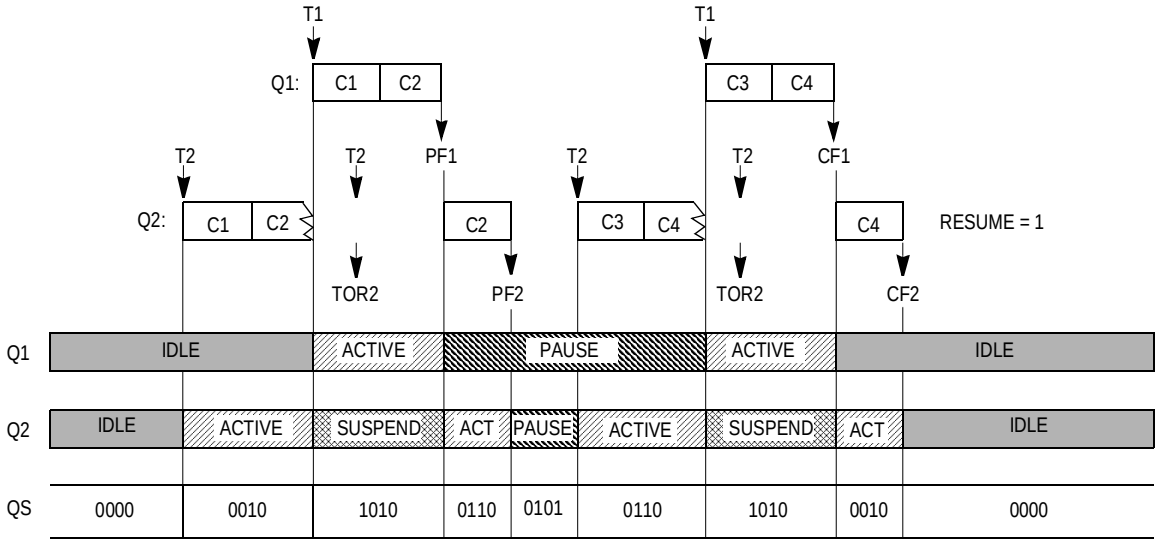

Figure 18-33. CCW Priority Situation 11

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The previous situations cover normal overlap conditions that arise with asynchronous trigger events on the two queues. An additional conflict to consider is that the freeze condition can arise while the QADC is actively executing CCWs. The conventional use for the debug mode is for software/hardware debugging. When the CPU background debug mode is enabled and a breakpoint occurs, the freeze signal is issued, which can cause peripheral modules to stop operation. When freeze is detected, the QADC completes the conversion in progress, unlike queue 1 suspending queue 2. After the freeze condition is removed, the QADC continues queue execution with the next CCW in sequence.

Trigger events that occur during freeze are not captured. When a trigger event is pending for queue 2 before freeze begins, that trigger event is remembered when the freeze is passed. Similarly, when freeze occurs while queue 2 is suspended, after freeze, queue 2 resumes execution as soon as queue 1 is finished.

Situations 12 through 19 (**Figure 18-34** to **Figure 18-41**) show examples of all of the freeze situations.

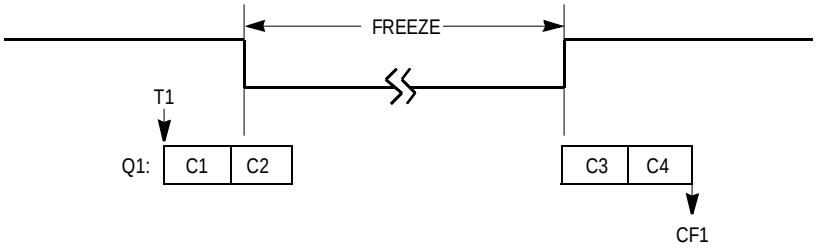

Figure 18-34. CCW Freeze Situation 12

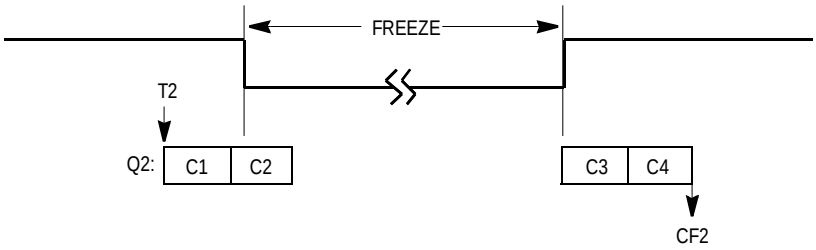

Figure 18-35. CCW Freeze Situation 13

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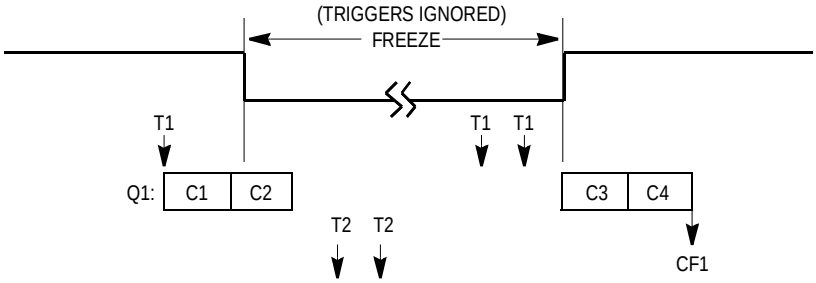

Figure 18-36. CCW Freeze Situation 14

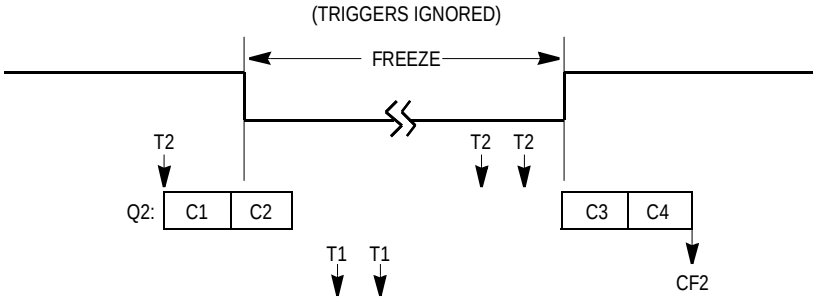

Figure 18-37. CCW Freeze Situation 15

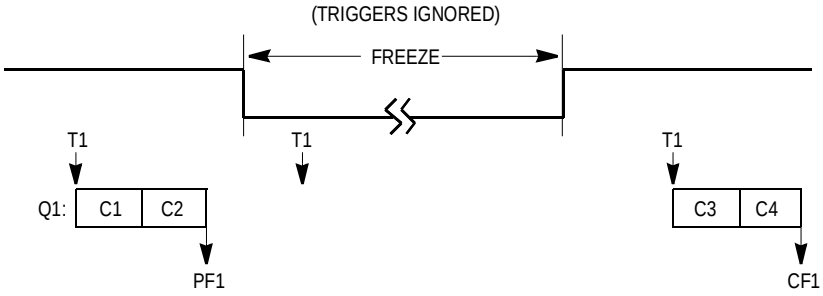

Figure 18-38. CCW Freeze Situation 16

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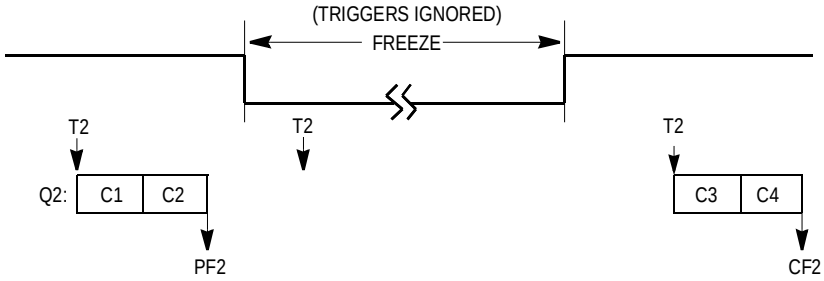

Figure 18-39. CCW Freeze Situation 17

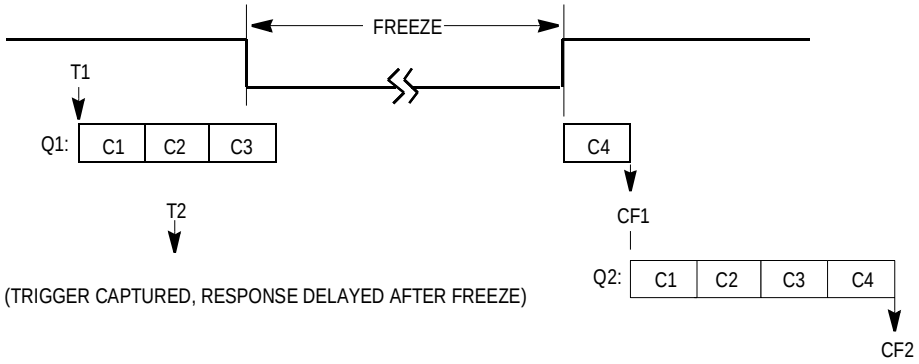

Figure 18-40. CCW Freeze Situation 18

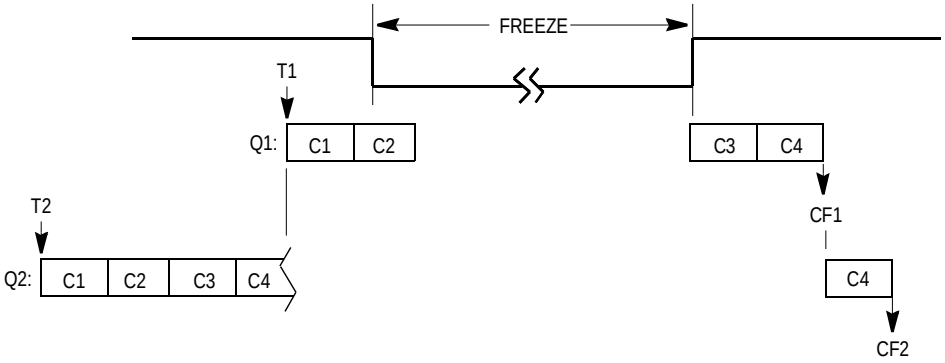

Figure 18-41. CCW Freeze Situation 19

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18.10.2 Boundary Conditions

The queue operation boundary conditions are:

- The first CCW in a queue contains channel 63, the end-of-queue (EOQ) code. The queue becomes active and the first CCW is read. The end-of-queue is recognized, the completion flag is set, and the queue becomes idle. A conversion is not performed.
- BQ2 (beginning of queue 2) is set at the end of the CCW table (63) and a trigger event occurs on queue 2. The end-of-queue condition is recognized, a conversion is performed, the completion flag is set, and the queue becomes idle.
- BQ2 is set to CCW0 and a trigger event occurs on queue 1. After reading CCW0, the end-of-queue condition is recognized, the completion flag is set, and the queue becomes idle. A conversion is not performed.
- BQ2 (beginning of queue 2) is set beyond the end of the CCW table (64–127) and a trigger event occurs on queue 2. The end-of-queue condition is recognized immediately, the completion flag is set, and the queue becomes idle. A conversion is not performed.

NOTE: *Multiple end-of-queue conditions may be recognized simultaneously, although there is no change in the QADC behavior. For example, if BQ2 is set to CCW0, CCW0 contains the EOQ code, and a trigger event occurs on queue 1, the QADC reads CCW0 and detects both end-of-queue conditions. The completion flag is set and queue 1 becomes idle.*

Boundary conditions also exist for combinations of pause and end-of-queue. One case is when a pause bit is in one CCW and an end-of-queue condition is in the next CCW. The conversion specified by the CCW with the pause bit set completes normally. The pause flag is set. However, since the end-of-queue condition is recognized, the completion flag is also set and the queue status becomes idle, not paused. Examples of this situation include:

- The pause bit is set in CCW5 and the channel 63 (EOQ) code is in CCW6.
- The pause is in CCW63.
- During queue 1 operation, the pause bit is set in CCW20 and BQ2 points to CCW21.

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Another pause and end-of-queue boundary condition occurs when the pause and an end-of-queue condition occur in the same CCW. Both the pause and end-of-queue conditions are recognized simultaneously. The end-of-queue condition has precedence so a conversion is not performed for the CCW and the pause flag is not set. The QADC sets the completion flag and the queue status becomes idle. Examples of this situation are:

- The pause bit is set in CCW10 and EOQ is programmed into CCW10.
- During queue 1 operation, the pause bit set in CCW32, which is also BQ2.

18.10.3 Scan Modes

The QADC queuing mechanism allows the application to utilize different requirements for automatically scanning input channels.

In single-scan mode, a single pass through a sequence of conversions defined by a queue is performed. In continuous-scan mode, multiple passes through a sequence of conversions defined by a queue are executed. The possible modes are:

- Disabled mode and reserved mode
- Software-initiated single-scan mode
- External trigger single-scan mode
- External gated single-scan mode
- Interval timer single-scan mode
- Software-initiated continuous-scan mode
- External trigger continuous-scan mode
- External gated continuous-scan mode
- Periodic timer continuous-scan mode

These paragraphs describe single-scan and continuous-scan operations.

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18.10.4 Disabled Mode

When the disabled mode is selected, the queue is not active. Trigger events cannot initiate queue execution. When both queue 1 and queue 2 are disabled, wait states are not encountered for IPbus accesses of the RAM. When both queues are disabled, it is safe to change the QCLK prescaler values.

18.10.5 Reserved Mode

Reserved mode allows for future mode definitions. When the reserved mode is selected, the queue is not active. It functions the same as disabled mode.

18.10.6 Single-Scan Modes

When the application software wants to execute a single pass through a sequence of conversions defined by a queue, a single-scan queue operating mode is selected. By programming the MQ field in QACR1 or QACR2, these modes can be selected:

- Software-initiated single-scan mode
- External trigger single-scan mode
- External gated single-scan mode
- Interval timer single-scan mode

NOTE: *Queue 2 cannot be programmed for external gated single-scan mode.*

In all single-scan queue operating modes, the software must also enable the queue to begin execution by writing the single-scan enable bit to a 1 in the queue's control register. The single-scan enable bits, SSE1 and SSE2, are provided for queue 1 and queue 2 respectively.

Until the single-scan enable bit is set, any trigger events for that queue are ignored. The single-scan enable bit may be set to a 1 during the write cycle, which selects the single-scan queue operating mode. The single-scan enable bit is set through software, but will always read as a 0. Once set, writing the single-scan enable bit to 0 has no effect. Only the QADC can clear the single-scan enable bit. The completion flag,

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completion interrupt, or queue status are used to determine when the queue has completed.

After the single-scan enable bit is set, a trigger event causes the QADC to begin execution with the first CCW in the queue. The single-scan enable bit remains set until the queue is completed. After the queue reaches completion, the QADC resets the single-scan enable bit to 0. If the single-scan enable bit is written to a 1 or a 0 by the software before the queue scan is complete, the queue is not affected. However, if the software changes the queue operating mode, the new queue operating mode and the value of the single-scan enable bit are recognized immediately. The conversion in progress is aborted and the new queue operating mode takes effect.

In the software-initiated single-scan mode, the writing of a 1 to the single-scan enable bit causes the QADC to generate a trigger event internally and the queue execution begins immediately. In the other single-scan queue operating modes, once the single-scan enable bit is written, the selected trigger event must occur before the queue can start. The single-scan enable bit allows the entire queue to be scanned once. A trigger overrun is captured if a trigger event occurs during queue execution in an edge-sensitive external trigger mode or a periodic/interval timer mode.

In the interval timer single-scan mode, the next expiration of the timer is the trigger event for the queue. After the queue execution is complete, the queue status is shown as idle. The software can restart the queue by setting the single-scan enable bit to a 1. Queue execution begins with the first CCW in the queue.

18.10.6.1 Software-Initiated Single-Scan Mode

Software can initiate the execution of a scan sequence for queues 1 or 2 by selecting the software-initiated single-scan mode, and writing the single-scan enable bit in QACR1 or QACR2. A trigger event is generated internally and the QADC immediately begins execution of the first CCW in the queue. If a pause occurs, another trigger event is generated internally, and then execution continues without pausing.

The QADC automatically performs the conversions in the queue until an end-of-queue condition is encountered. The queue remains idle until the software again sets the single-scan enable bit. While the time to

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internally generate and act on a trigger event is very short, software can momentarily read the status conditions, indicating that the queue is paused. The trigger overrun flag is never set while in the software-initiated single-scan mode.

The software-initiated single-scan mode is useful in these applications:

- Allows software complete control of the queue execution
- Allows the software to easily alternate between several queue sequences

18.10.6.2 External Trigger Single-Scan Mode

The external trigger single-scan mode is available on both queue 1 and queue 2. The software programs the polarity of the external trigger edge that is to be detected, either a rising or a falling edge. The software must enable the scan to occur by setting the single-scan enable bit for the queue.

The first external trigger edge causes the queue to be executed one time. Each CCW is read and the indicated conversions are performed until an end-of-queue condition is encountered. After the queue is completed, the QADC clears the single-scan enable bit. Software may set the single-scan enable bit again to allow another scan of the queue to be initiated by the next external trigger edge.

The external trigger single-scan mode is useful when the input trigger rate can exceed the queue execution rate. Analog samples can be taken in sync with an external event, even though the software is not interested in data taken from every edge. The software can start the external trigger single-scan mode and get one set of data, and at a later time, start the queue again for the next set of samples.

When a pause bit is encountered during external trigger single-scan mode, another trigger event is required for queue execution to continue. Software involvement is not needed to enable queue execution to continue from the paused state.

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18.10.6.3 External Gated Single-Scan Mode

The QADC provides external gating for queue 1 only. When external gated single-scan mode is selected, the input level on the associated external trigger pin enables and disables queue execution. The polarity of the external gated signal is fixed so only a high level opens the gate and a low level closes the gate. Once the gate is open, each CCW is read and the indicated conversions are performed until the gate is closed. Software must enable the scan to occur by setting the single-scan enable bit for queue 1. If a pause in a CCW is encountered, the pause flag does not become set, and execution continues without pausing.

While the gate is open, queue 1 executes one time. Each CCW is read and the indicated conversions are performed until an end-of-queue condition is encountered. When queue 1 completes, the QADC sets the completion flag (CF1) and clears the single-scan enable bit. Software may set the single-scan enable bit again to allow another scan of queue 1 to be initiated during the next open gate.

If the gate closes before queue 1 completes execution, the current CCW completes, execution of queue 1 stops, the single-scan enable bit is cleared, and the PF1 bit is set. Software can read the CWPQ1 to determine the last valid conversion in the queue. Software must set the single-scan enable bit again and should clear the PF1 bit before another scan of queue 1 is initiated during the next open gate. The start of queue 1 is always the first CCW in the CCW table.

Since the condition of the gate is only sampled after each conversion during queue execution, closing the gate for a period less than a conversion time interval does not guarantee the closure will be captured.

18.10.6.4 Interval Timer Single-Scan Mode

Both queues can use the periodic/interval timer in a single-scan queue operating mode. The timer interval can range from 128 to 128 KQCLK cycles in binary multiples. When the interval timer single-scan mode is selected and the software sets the single-scan enable bit in QACR1(2), the timer begins counting. When the time interval elapses, an internal trigger event is created to start the queue and the QADC begins execution with the first CCW.

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The QADC automatically performs the conversions in the queue until a pause or an end-of-queue condition is encountered. When a pause occurs, queue execution stops until the timer interval elapses again, and queue execution continues. When the queue execution reaches an end-of-queue situation, the single-scan enable bit is cleared. Software may set the single-scan enable bit again, allowing another scan of the queue to be initiated by the interval timer.

The interval timer generates a trigger event whenever the time interval elapses. The trigger event may cause the queue execution to continue following a pause, or may be considered a trigger overrun. Once the queue execution is completed, the single-scan enable bit must be set again to enable the timer to count again.

Normally, only one queue will be enabled for interval timer single-scan mode and the timer will reset at the end-of-queue. However, if both queues are enabled for either single-scan or continuous interval timer mode, the end-of-queue condition will not reset the timer while the other queue is active. In this case, the timer will reset when both queues have reached end-of-queue. See **18.10.9 Periodic/Interval Timer** for a definition of interval timer reset conditions.

The interval timer single-scan mode can be used in applications which need coherent results, for example:

- When it is necessary that all samples are guaranteed to be taken during the same scan of the analog pins.
- When the interrupt rate in the periodic timer continuous-scan mode would be too high.
- In sensitive battery applications, where the single-scan mode uses less power than the software-initiated continuous-scan mode.

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18.10.7 Continuous-Scan Modes

When the application software wants to execute multiple passes through a sequence of conversions defined by a queue, a continuous-scan queue operating mode is selected. By programming the MQ1(2) field in QACR1(2), these software-initiated modes can be selected:

- Software-initiated continuous-scan mode
- External trigger continuous-scan mode
- External gated continuous-scan mode
- Periodic timer continuous-scan mode

When a queue is programmed for a continuous-scan mode, the single-scan enable bit in the queue control register does not have any meaning or effect. As soon as the queue operating mode is programmed, the selected trigger event can initiate queue execution.

In the case of the software-initiated continuous-scan mode, the trigger event is generated internally and queue execution begins immediately. In the other continuous-scan queue operating modes, the selected trigger event must occur before the queue can start. A trigger overrun is captured if a trigger event occurs during queue execution in the external trigger continuous-scan mode and the periodic timer continuous-scan mode.

After the queue execution is complete, the queue status is shown as idle. Since the continuous-scan queue operating modes allow the entire queue to be scanned multiple times, software involvement is not needed to enable queue execution to continue from the idle state. The next trigger event causes queue execution to begin again, starting with the first CCW in the queue.

NOTE: *Coherent samples are guaranteed. The time between consecutive conversions has been designed to be consistent. However, there is one exception. For queues that end with a CCW containing EOQ code (channel 63), the last queue conversion to the first queue conversion requires one additional CCW fetch cycle. Therefore continuous samples are not coherent at this boundary.*

In addition, the time from trigger to first conversion can not be guaranteed since it is a function of clock synchronization, programmable trigger events, queue priorities, and so on.

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18.10.7.1 Software-Initiated Continuous-Scan Mode

When the software-initiated continuous-scan mode is programmed, the trigger event is generated automatically by the QADC. Queue execution begins immediately. If a pause is encountered, another trigger event is generated internally, and then execution continues without pausing. When the end-of-queue is reached, another internal trigger event is generated and queue execution begins again from the beginning of the queue.

While the time to internally generate and act on a trigger event is very short, software can momentarily read the status conditions, indicating that the queue is idle. The trigger overrun flag is never set while in the software-initiated continuous-scan mode.

The software-initiated continuous-scan mode keeps the result registers updated more frequently than any of the other queue operating modes. The software can always read the result table to get the latest converted value for each channel. The channels scanned are kept up to date by the QADC without software involvement. Software can read a result value at any time.

The software-initiated continuous-scan mode may be chosen for either queue, but is normally used only with queue 2. When the software-initiated continuous-scan mode is chosen for queue 1, that queue operates continuously and queue 2, being lower in priority, never gets executed. The short interval of time between a queue 1 completion and the subsequent trigger event is not sufficient to allow queue 2 execution to begin.

The software-initiated continuous-scan mode is a useful choice with queue 2 for converting channels that do not need to be synchronized to anything, or for the slow-to-change analog channels. Interrupts are normally not used with the software-initiated continuous-scan mode. Rather, the software reads the latest conversion result from the result table at any time. Once initiated, software action is not needed to sustain conversions of channel.

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18.10.7.2 External Trigger Continuous-Scan Mode

The QADC provides external trigger pins for both queues. When the external trigger software-initiated continuous-scan mode is selected, a transition on the associated external trigger pin initiates queue execution. The polarity of the external trigger signal is programmable, so that the software can select a mode which begins queue execution on the rising or falling edge. Each CCW is read and the indicated conversions are performed until an end-of-queue condition is encountered. When the next external trigger edge is detected, the queue execution begins again automatically. Software initialization is not needed between trigger events.

When a pause bit is encountered in external trigger continuous-scan mode, another trigger event is required for queue execution to continue. Software involvement is not needed to enable queue execution to continue from the paused state.

Some applications need to synchronize the sampling of analog channels to external events. There are cases when it is not possible to use software initiation of the queue scan sequence, since interrupt response times vary.

18.10.7.3 External Gated Continuous-Scan Mode

The QADC provides external gating for queue 1 only. When external gated continuous-scan mode is selected, the input level on the associated external trigger pin enables and disables queue execution. The polarity of the external gated signal is fixed so a high level opens the gate and a low level closes the gate. Once the gate is open, each CCW is read and the indicated conversions are performed until the gate is closed. When the gate opens again, the queue execution automatically begins again from the beginning of the queue. Software initialization is not needed between trigger events. If a pause in a CCW is encountered, the pause flag does not become set, and execution continues without pausing.

The purpose of external gated continuous-scan mode is to continuously collect digitized samples while the gate is open and to have the most recent samples available. It is up to the programmer to ensure that the queue is large enough so that a maximum gate open time will not reach

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an end-of-queue. However it is useful to take advantage of a smaller queue in the manner described in the next paragraph.

In the event that the queue completes before the gate closes, a completion flag will be set and the queue will roll over to the beginning and continue conversions until the gate closes. If the gate remains open and the completion flag is not cleared, when the queue completes a second time the trigger overrun flag will be set and the queue will roll-over again. The queue will continue to execute until the gate closes or the mode is disabled.

If the gate closes before queue 1 completes execution, the current CCW completes execution of queue 1 stops and QADC sets the PF1 bit to indicate an incomplete queue. Software can read the CWPQ1 to determine the last valid conversion in the queue. In this mode, if the gate opens again, execution of queue 1 begins again. The start of queue 1 is always the first CCW in the CCW table. Since the condition of the gate is only sampled after each conversion during queue execution, closing the gate for a period less than a conversion time interval does not guarantee the closure will be captured.

18.10.7.4 Periodic Timer Continuous-Scan Mode

The QADC includes a dedicated periodic timer for initiating a scan sequence on queue 1 and/or queue 2. Software selects a programmable timer interval ranging from 128 to 128K times the QCLK period in binary multiples. The QCLK period is prescaled down from the IPbus MCU clock.

When a periodic timer continuous-scan mode is selected for queue 1 and/or queue 2, the timer begins counting. After the programmed interval elapses, the timer generated trigger event starts the appropriate queue. Meanwhile, the QADC automatically performs the conversions in the queue until an end-of-queue condition or a pause is encountered. When a pause occurs, the QADC waits for the periodic interval to expire again, then continues with the queue. Once end-of-queue has been detected, the next trigger event causes queue execution to begin again with the first CCW in the queue.

The periodic timer generates a trigger event whenever the time interval elapses. The trigger event may cause the queue execution to continue following a pause or queue completion, or may be considered a trigger

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overrun. As with all continuous-scan queue operating modes, software action is not needed between trigger events. Since both queues may be triggered by the periodic/interval timer, see **18.10.9 Periodic/Interval Timer** for a summary of periodic/interval timer reset conditions.

Software enables the completion interrupt when using the periodic timer continuous-scan mode. When the interrupt occurs, the software knows that the periodically collected analog results have just been taken. The software can use the periodic interrupt to obtain nonanalog inputs as well, such as contact closures, as part of a periodic look at all inputs.

18.10.8 QADC Clock (QCLK) Generation

Figure 18-42 is a block diagram of the clock subsystem. The QCLK provides the timing for the A/D converter state machine which controls the timing of the conversion. The QCLK is also the input to a 17-stage binary divider which implements the periodic/interval timer. To retain the specified analog conversion accuracy, the QCLK frequency (f_{QCLK}) must be within the tolerance specified in **Section 22. Electrical Specifications**.

Before using the QADC, the software must initialize the prescaler with values that put the QCLK within the specified range. Though most software applications initialize the prescaler once and do not change it, write operations to the prescaler fields are permitted.

NOTE: *For software compatibility with earlier versions of QADC, the definition of PSL, PSH, and PSA have been maintained. However, the requirements on minimum time and minimum low time no longer exist.*

CAUTION: *A change in the prescaler value while a conversion is in progress is likely to corrupt the result from any conversion in progress. Therefore, any prescaler write operation should be done only when both queues are in the disabled modes.*

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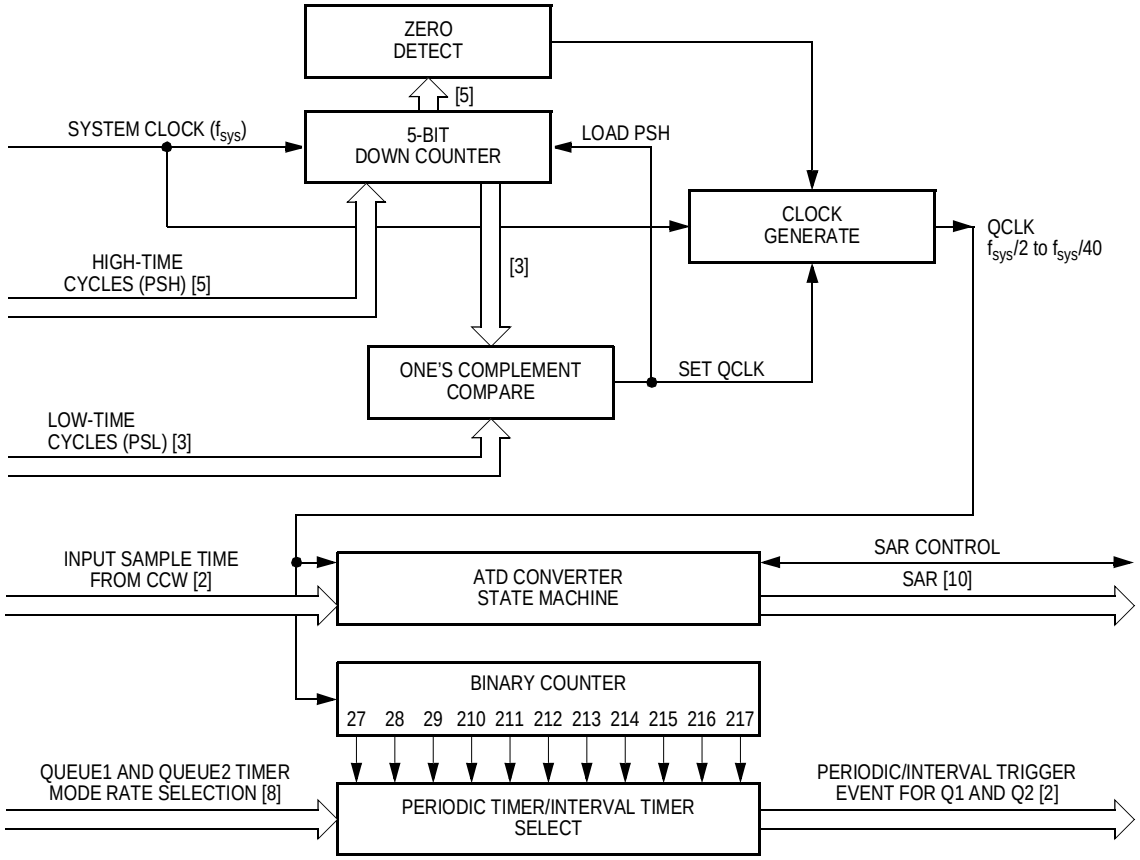

Figure 18-42. QADC Clock Subsystem Functions

To accommodate wide variations of the main MCU clock frequency (IPbus system clock – f_{sys}), QCLK is generated by a programmable prescaler which divides the MCU system clock. To allow the A/D conversion time to be maximized across the spectrum of system clock frequencies, the QADC prescaler permits the frequency of QCLK to be software selectable. It also allows the duty cycle of the QCLK waveform to be programmable.

The software establishes the basic high phase of the QCLK waveform with the PSH (prescaler clock high time) field in QACR0 and selects the basic low phase of QCLK with the PSL (prescaler clock low time) field. The combination of the PSH and PSL parameters establishes the frequency of the QCLK.

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NOTE: *The guideline for selecting PSH and PSL is to maintain approximately 50 percent duty cycle; for prescaler values less than 16 or PSH ~=PSL. For prescaler values greater than 16, keep PSL as large as possible.*

Figure 18-42 shows that the prescaler is essentially a variable pulse width signal generator. A 5-bit down counter, clocked at the system clock rate, is used to create both the high phase and the low phase of the QCLK signal. At the beginning of the high phase, the 5-bit counter is loaded with the 5-bit PSH value. When the 0 detector finds that the high phase is finished, the QCLK is reset. A 3-bit comparator looks for a one's complement match with the 3-bit PSL value, which is the end of the low phase of the QCLK.

These equations define QCLK frequency:

$$\text{high QCLK time} = (\text{PSH} + 1) \div f_{sys}$$

$$\text{low QCLK time} = (\text{PSL} + 1) \div f_{sys}$$

$$f_{QCLK} = 1 \div (\text{high QCLK time} + \text{low QCLK time})$$

Where:

PSH = 0 to 31, the prescaler QCLK high cycles in QACR0
PSL = 0 to 7, the prescaler QCLK low cycles in QACR0
f_{sys} = system clock frequency
f_{QCLK} = QCLK frequency

These are equations for calculating the QCLK high and low phases in example 1:

$$\text{high QCLK time} = (11 + 1) \div 40 \times 10^6 = 300 \text{ ns}$$

$$\text{low QCLK time} = (7 + 1) \div 40 \times 10^6 = 200 \text{ ns}$$

$$f_{QCLK} = 1/(300 + 200) = 2 \text{ MHz}$$

These are equations for calculating the QCLK high and low phases in example 2:

$$\text{high QCLK time} = (7 + 1) \div 32 \times 10^6 = 250 \text{ ns}$$

$$\text{low QCLK time} = (7 + 1) \div 32 \times 10^6 = 250 \text{ ns}$$

$$f_{QCLK} = 1/(250 + 250) = 2 \text{ MHz}$$

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Figure 18-43 and Table 18-15 show examples of QCLK programmability. The examples include conversion times based on this assumption:

Input sample time is as fast as possible (IST = 0, 2 QCLK cycles).

Figure 18-43 and Table 18-15 also show the conversion time calculated for a single conversion in a queue. For other MCU system clock frequencies and other input sample times, the same calculations can be made.

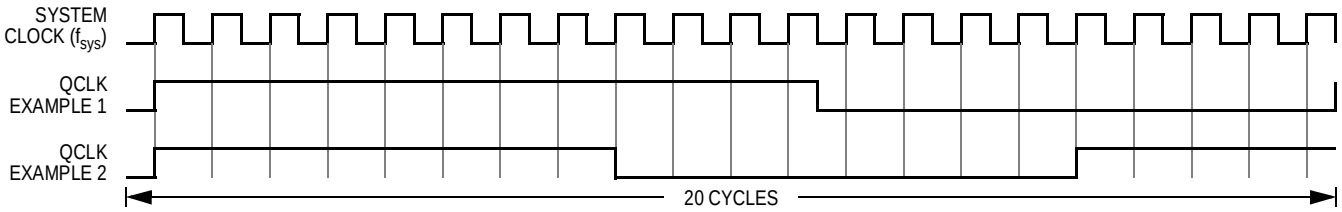

Figure 18-43. QADC Clock Programmability Examples

Table 18-15. QADC Clock Programmability

Control Register 0 Information				Input Sample Time IST = Binary 00	
Example Number	Frequency	PSH	PSL	QCLK (MHz)	Conversion Time (μs)
1	40 MHz	11	7	2.0	7.0
2	32 MHz	7	7	2.0	7.0

NOTE: *PSA is maintained for software compatibility but has no functional benefit to this version of the module.*

The MCU system clock frequency is the basis of the QADC timing. The QADC requires that the system clock frequency be at least twice the QCLK frequency. The QCLK frequency is established by the combination of the PSH and PSL parameters in QACR0. The 5-bit PSH field selects the number of system clock cycles in the high phase of the QCLK wave. The 3-bit PSL field selects the number of system clock cycles in the low phase of the QCLK wave.

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Example 1 in **Figure 18-43** shows that when PSH = 11, the QCLK remains high for 12 cycles of the system clock. It also shows that when PSL = 7, the QCLK remains low for eight system clock cycles. In Example 2, PSH = 7, and the QCLK remains high for eight cycles of the system clock. It also shows that when PSL = 7, the QCLK remains low for eight system clock cycles.

18.10.9 Periodic/Interval Timer

The on-chip periodic/interval timer can be used to generate trigger events at a programmable interval, initiating execution of queue 1 and/or queue 2. The periodic/interval timer stays reset under these conditions:

- Both queue 1 and queue 2 are programmed to any mode which does not use the periodic/interval timer.
- IPbus system reset is asserted.
- Stop mode is selected.
- Debug mode is selected.

NOTE: *Interval timer single-scan mode does not use the periodic/interval timer until the single-scan enable bit is set.*

These conditions will cause a pulsed reset of the periodic/interval timer during use:

- A queue 1 operating mode change to a mode which uses the periodic/interval timer, even if queue 2 is already using the timer
- A queue 2 operating mode change to a mode which uses the periodic/interval timer, provided queue 1 is not in a mode which uses the periodic/interval timer
- Roll over of the timer

During the low-power stop mode, the periodic/interval timer is held in reset. Since low-power stop mode causes QACR1 and QACR2 to be reset to 0, a valid periodic or interval timer mode must be written after stop mode is exited to release the timer from reset.

When the IPbus internal FREEZE line is asserted and a periodic or interval timer mode is selected, the timer counter is reset after the conversion in progress completes. When the periodic or interval timer

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mode has been enabled (the timer is counting), but a trigger event has not been issued, the debug mode takes effect immediately, and the timer is held in reset. When the internal FREEZE line is negated, the timer counter starts counting from the beginning. Refer to **18.5.1 Debug Mode** for more information.

18.10.10 Conversion Command Word Table

The conversion command word (CCW) table is a RAM, 64 words long on 16-bit address boundaries where 10 bits of each entry are implemented. A CCW can be programmed by the software to request a conversion of one analog input channel. The CCW table is written by software and is not modified by the QADC. Each CCW requests the conversion of an analog channel to a digital result. The CCW specifies the analog channel number, the input sample time, and whether the queue is to pause after the current CCW. The 10 implemented bits of the CCW word are read/write data, where they may be written when the software initializes the QADC. The remaining six bits are unimplemented so these read as 0s, and write operations have no effect. Each location in the CCW table corresponds to a location in the result word table. When a conversion is completed for a CCW entry, the 10-bit result is written in the corresponding result word entry. The QADC provides 64 CCW table entries.

The beginning of queue 1 is the first location in the CCW table. The first location of queue 2 is specified by the beginning of queue 2 pointer (BQ2) in QACR2. To dedicate the entire CCW table to queue 1, queue 2 is programmed to be in the disabled mode, and BQ2 is programmed to 64 or greater. To dedicate the entire CCW table to queue 2, queue 1 is programmed to be in the disabled mode, and BQ2 is specified as the first location in the CCW table.

Figure 18-44 illustrates the operation of the queue structure.

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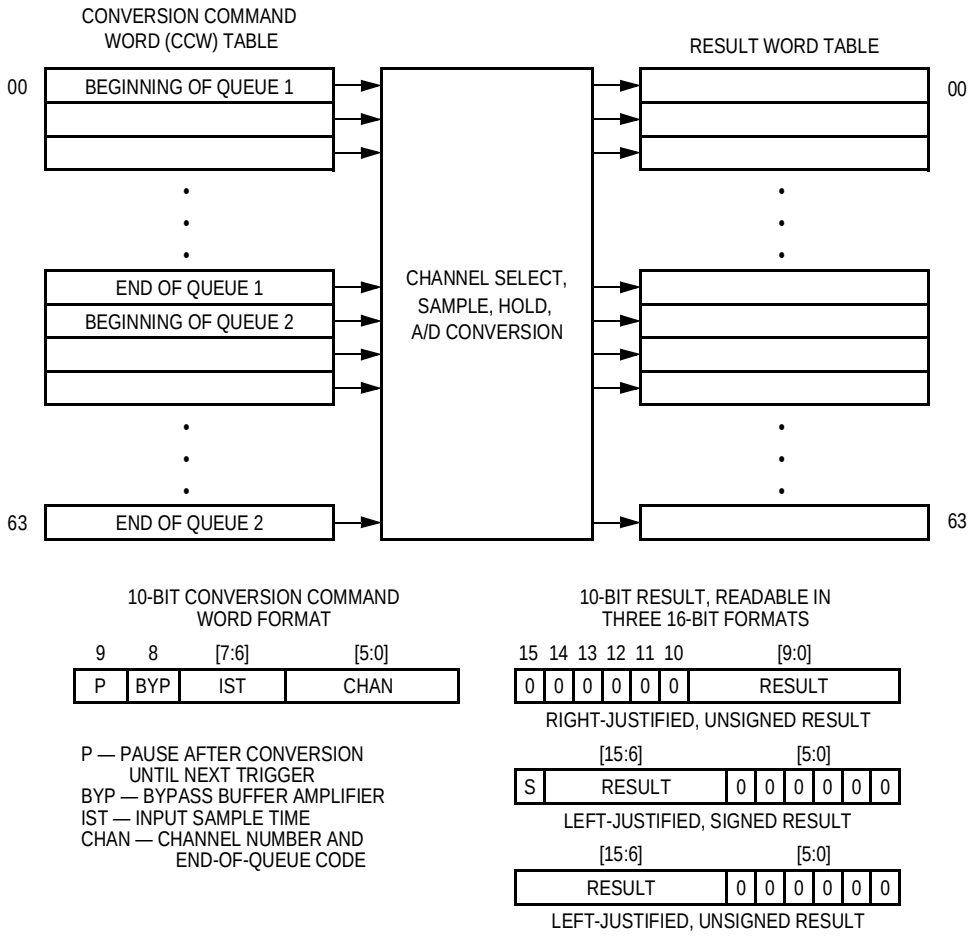

Figure 18-44. QADC Conversion Queue Operation

To prepare the QADC for a scan sequence, the software writes to the CCW table to specify the desired channel conversions. The software also establishes the criteria for initiating the queue execution by programming the queue operating mode. The queue operating mode determines what type of trigger event causes queue execution to begin. A trigger event refers to any of the ways to cause the QADC to begin executing the CCWs in a queue or subqueue. An external trigger is only one of the possible trigger events.

A scan sequence may be initiated by:

- A software command
- Expiration of the periodic/interval timer
- External trigger signal
- External gated signal (queue 1 only)

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The software also specifies whether the QADC is to perform a single pass through the queue or is to scan continuously. When a single-scan mode is selected, the software selects the queue operating mode and sets the single-scan enable bit. When a continuous-scan mode is selected, the queue remains active in the selected queue operating mode after the QADC completes each queue scan sequence.

During queue execution, the QADC reads each CCW from the active queue and executes conversions in four stages:

- Initial sample
- Final sample
- Resolution

During initial sample, a buffered version of the selected input channel is connected to the sample capacitor at the input of the sample buffer amplifier.

During the final sample period, the sample buffer amplifier is bypassed, and the multiplexer input charges the sample capacitor directly. Each CCW specifies a final input sample time of 2, 4, 8, or 16 QCLK cycles. When an analog-to-digital conversion is complete, the result is written to the corresponding location in the result word table. The QADC continues to sequentially execute each CCW in the queue until the end of the queue is detected or a pause bit is found in a CCW.

When the pause bit is set in the current CCW, the QADC stops execution of the queue until a new trigger event occurs. The pause status flag bit is set, which may cause an interrupt to notify the software that the queue has reached the pause state. After the trigger event occurs, the paused state ends and the QADC continues to execute each CCW in the queue until another pause is encountered or the end of the queue is detected.

The end-of-queue condition is indicated by:

- The CCW channel field is programmed with 63 ($3F) to specify the end of the queue.
- The end-of-queue 1 is implied by the beginning of queue 2, which is specified in the BQ2 field in QACR2.
- The physical end of the queue RAM space defines the end of either queue.

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When any of the end-of-queue conditions is recognized, a queue completion flag is set, and if enabled, an interrupt is issued to the software. These situations prematurely terminate queue execution:

- Since queue 1 is higher in priority than queue 2, when a trigger event occurs on queue 1 during queue 2 execution, the execution of queue 2 is suspended by aborting the execution of the CCW in progress, and the queue 1 execution begins. When queue 1 execution is completed, queue 2 conversions restart with the first CCW entry in queue 2 or the first CCW of the queue 2 subqueue being executed when queue 2 was suspended. Alternately, conversions can restart with the aborted queue 2 CCW entry. The RESUME bit in QACR2 allows the software to select where queue 2 begins after suspension. By choosing to re-execute all of the suspended queue 2 queue and subqueue CCWs, all of the samples are guaranteed to have been taken during the same scan pass. However, a high trigger event rate for queue 1 can prohibit the completion of queue 2. If this occurs, the software may choose to begin execution of queue 2 with the aborted CCW entry.
- Software can change the queue operating mode to disabled mode. Any conversion in progress for that queue is aborted. Putting a queue into the disabled mode does not power down the converter.
- Software can change the queue operating mode to another valid mode. Any conversion in progress for that queue is aborted. The queue restarts at the beginning of the queue, once an appropriate trigger event occurs.
- For low-power operation, software can set the stop mode bit to prepare the module for a loss of clocks. The QADC aborts any conversion in progress when the stop mode is entered.
- When the freeze enable bit is set by software and the IPbus internal FREEZE line is asserted, the QADC freezes at the end of the conversion in progress. When internal FREEZE is negated, the QADC resumes queue execution beginning with the next CCW entry. Refer to **18.5.1 Debug Mode** for more information.

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18.10.11 Result Word Table

The result word table is a RAM, 64 words long and 10 bits wide. An entry is written by the QADC after completing an analog conversion specified by the corresponding CCW table entry. Software can read or write the result word table, but in normal operation, the software reads the result word table to obtain analog conversions from the QADC. Unimplemented bits are read as 0s, and write operations do not have any effect.

While there is only one result word table, the data can be accessed in three different data formats:

- Right justified in the 16-bit word, with 0s in the higher order unused bits
- Left justified, with the most significant bit inverted to form a sign bit, and 0s in the unused lower order bits
- Left justified, with 0s in the lower order unused bits

The left justified, signed format corresponds to a half-scale, offset binary, two's complement data format. The data is routed onto the IPbus according to the selected format. The address used to access the table determines the data alignment format. All write operations to the result word table are right justified.

The three result data formats are produced by routing the RAM bits onto the data bus. The software chooses among the three formats by reading the result at the memory address which produces the desired data alignment.

The result word table is read/write accessible by software. During normal operation, applications software only needs to read the result table. Write operations to the table may occur during test or debug breakpoint operation. When locations in the CCW table are not used by an application, software could use the corresponding locations in the result word table as scratch pad RAM, remembering that only 10 bits are implemented. The result alignment is only implemented for software read operations. Since write operations are not the normal use for the result registers, only one write data format is supported, which is right justified data.

NOTE: *Some write operations, like bit manipulation, may not operate as expected because the hardware cannot access a true 16-bit value.*

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18.11 Pin Connection Considerations

The QADC requires accurate, noise-free input signals for proper operation. This section discusses the design of external circuitry to maximize QADC performance.

18.11.1 Analog Reference Pins

No A/D converter can be more accurate than its analog reference. Any noise in the reference can result in at least that much error in a conversion. The reference for the QADC, supplied by pins V_{RH} and V_{RL}, should be low-pass filtered from its source to obtain a noise-free, clean signal. In many cases, simple capacitive bypassing may suffice. In extreme cases, inductors or ferrite beads may be necessary if noise or RF energy is present. Series resistance is not advisable since there is an effective dc current requirement from the reference voltage by the internal resistor string in the RC DAC array. External resistance may introduce error in this architecture under certain conditions. Any series devices in the filter network should contain a minimum amount of DC resistance.

For accurate conversion results, the analog reference voltages must be within the limits defined by V_{DDA} and V_{SSA}, as explained in this subsection.

18.11.2 Analog Power Pins

The analog supply pins (V_{DDA} and V_{SSA}) define the limits of the analog reference voltages (V_{RH} and V_{RL}) and of the analog multiplexer inputs. **Figure 18-45** is a diagram of the analog input circuitry.

Since the sample amplifier is powered by V_{DDA} and V_{SSA}, it can accurately transfer input signal levels up to but not exceeding V_{DDA} and down to but not below V_{SSA}. If the input signal is outside of this range, the output from the sample amplifier is clipped.

In addition, V_{RH} and V_{RL} must be within the range defined by V_{DDA} and V_{SSA}. As long as V_{RH} is less than or equal to V_{DDA} and V_{RL} is greater than or equal to V_{SSA} and the sample amplifier has accurately transferred the input signal, resolution is ratiometric within the limits

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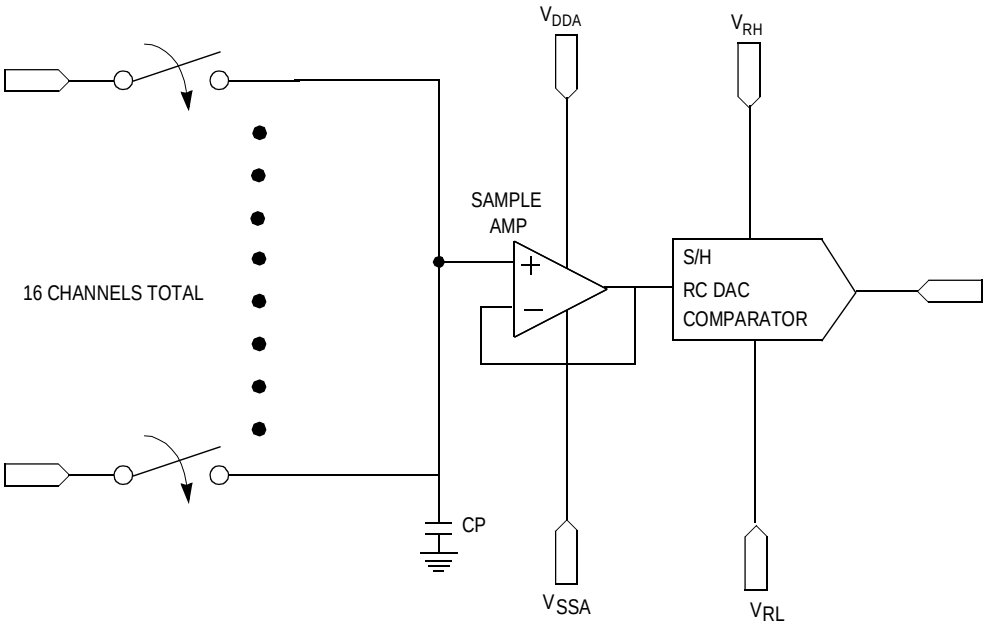

Figure 18-45. Equivalent Analog Input Circuitry

defined by V_{RL} and V_{RH}. If V_{RH} is greater than V_{DDA}, the sample amplifier can never transfer a full-scale value. If V_{RL} is less than V_{SSA}, the sample amplifier can never transfer a 0 value.

In addition, V_{RH} and V_{RL} must be within the range defined by V_{DDA} and V_{SSA}. As long as V_{RH} is less than or equal to V_{DDA} and V_{RL} is greater than or equal to V_{SSA} and the sample amplifier has accurately transferred the input signal, resolution is ratiometric within the limits defined by V_{RL} and V_{RH}. If V_{RH} is greater than V_{DDA}, the sample amplifier can never transfer a full-scale value. If V_{RL} is less than V_{SSA}, the sample amplifier can never transfer a 0 value.

Figure 18-46 shows the results of reference voltages outside the range defined by V_{DDA} and V_{SSA}. At the top of the input signal range, V_{DDA} is 10 mV lower than V_{RH}. This results in a maximum obtainable 10-bit conversion value of $3FE. At the bottom of the signal range, V_{SSA} is 15 mV higher than V_{RL}, resulting in a minimum obtainable 10-bit conversion value of three.

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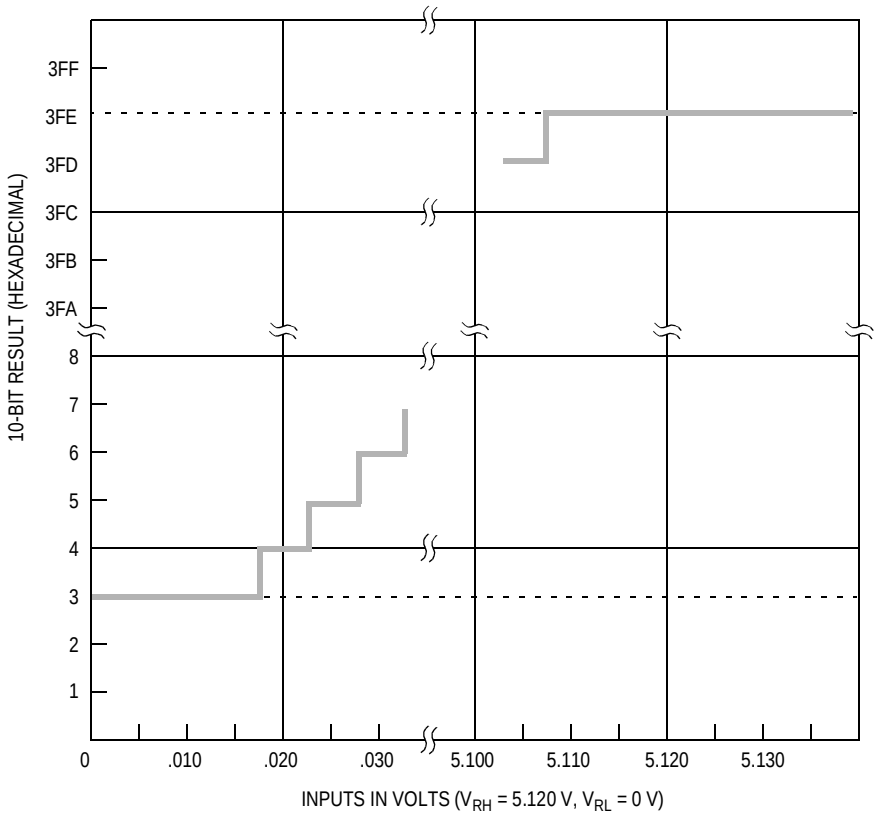

Figure 18-46. Errors Resulting from Clipping

18.11.3 Conversion Timing Schemes

This section contains some conversion timing examples. **Figure 18-47** shows the timing for basic conversions where it is assumed that:

- Q1 begins with CCW0 and ends with CCW3.
- CCW0 has pause bit set.
- CCW1 does not have pause bit set.
- External trigger rise edge for Q1.
- CCW4 = BQ2 and Q2 is disabled.
- Q1 Res shows relative result register updates.

Recall that when QS = 0, both queues are disabled, when QS = 8, queue 1 is active and queue 2 is idle, and when QS = 4, queue 1 is paused and queue 2 is disabled.

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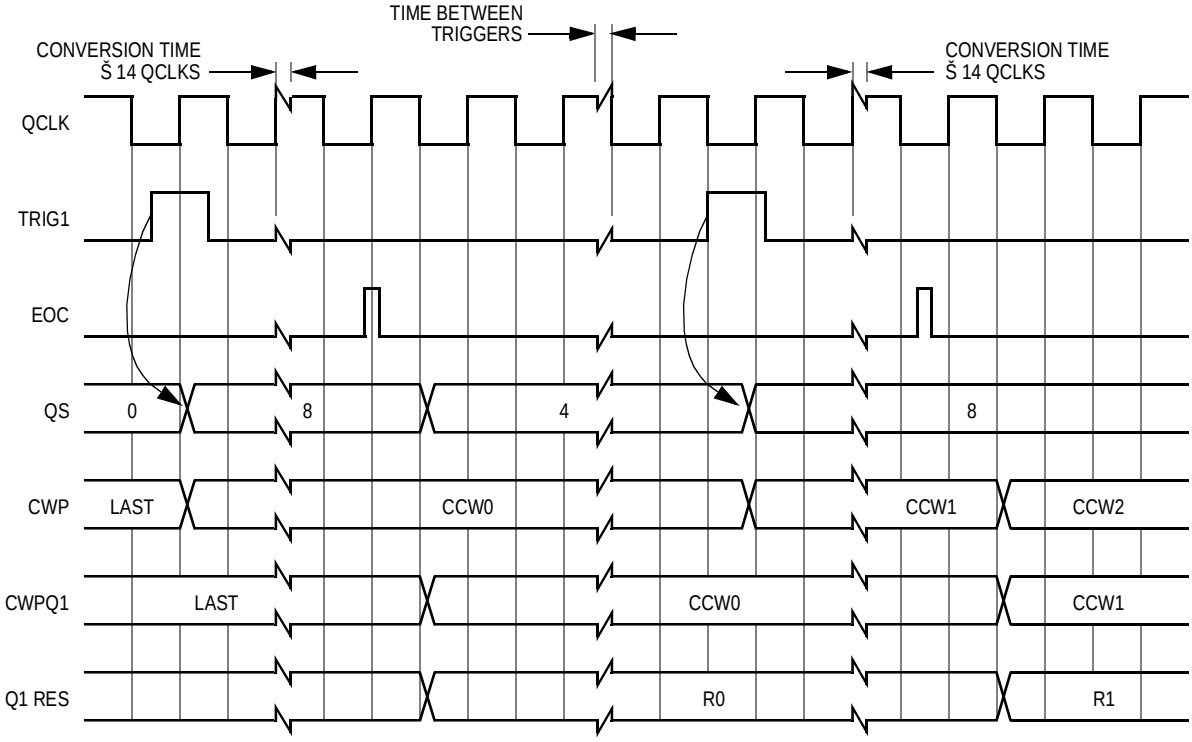

Figure 18-47. External Positive Edge Trigger Mode Timing With Pause

A time separator is provided between the triggers and the end of conversion (EOC). The relationship to QCLK displayed is not guaranteed.

CWPQ1 and CWPQ2 typically lag CWP and only match CWP when the associated queue is inactive. Another way to view CWPQ1(2) is that these registers update when EOC triggers the result register to be written.

In the case with the pause bit set (CCW0), CWP does not increment until triggered. In the case with the pause bit clear (CCW1), the CWP increments with the EOC.

The conversion results Q1 Res(x) show the result associated with CCW(x). So that R0 represents the result associated with CCW0.

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Figure 18-48 shows the timing for conversions in gated mode single scan with same assumptions in example 1 except:

- No pause bits set in any CCW
- External trigger gated mode single scan for Q1
- Single scan bit is set.

When the gate closes and opens again, the conversions start with the first CCW in Q1.

When the gate closes, the active conversion completes before the queue goes idle.

When Q1 completes both the CF1 bit sets and the SSE bit clears.

A proposed amended definition for the PF bit in this mode, to reflect the condition that a gate closing occurred before the queue completed, is under consideration.

Figure 18-49 shows the timing for conversions in gated mode continuous scan with the same assumptions as in Figure 18-48.

At the end of Q1, the completion flag CF1 sets and the queue restarts. If the queue starts a second time and completes, the trigger overrun flag TOR1 sets.

18.11.4 Analog Supply Filtering and Grounding

Two important factors influencing performance in analog integrated circuits are supply filtering and grounding. Generally, digital circuits use bypass capacitors on every V_{DD}/V_{SS} pin pair. This applies to analog subsystems or submodules also. Equally important as bypassing is the distribution of power and ground.

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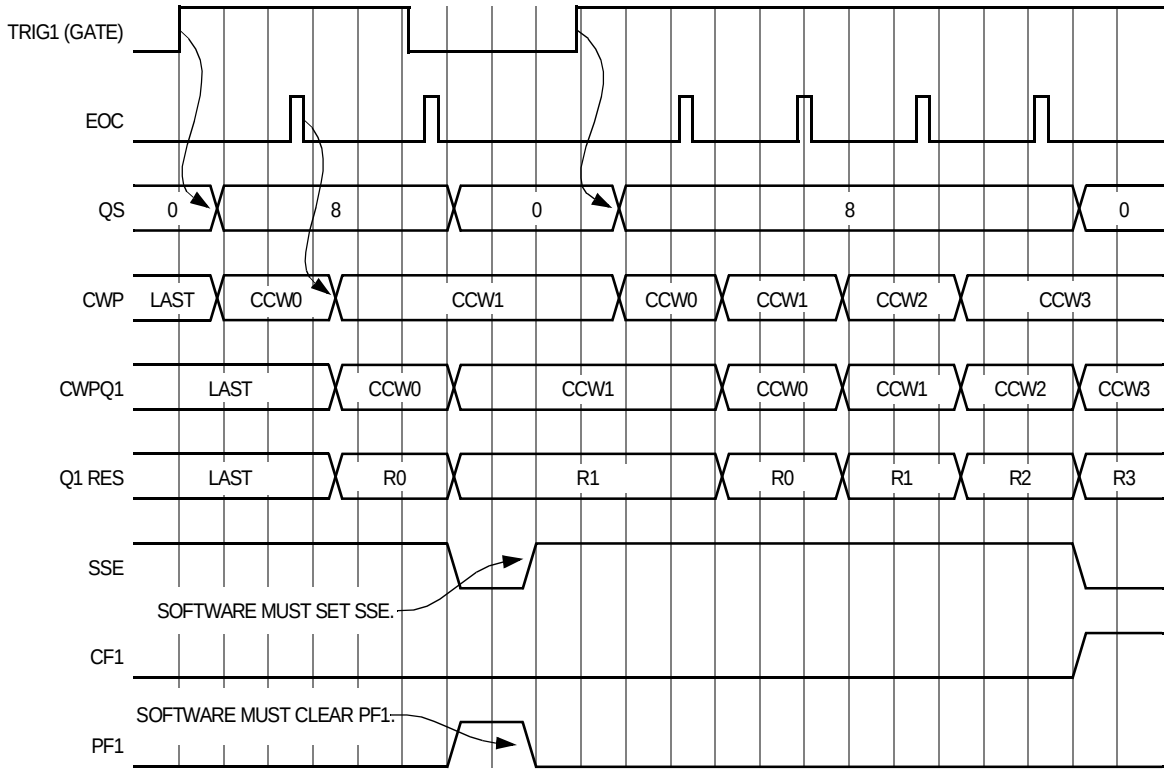

Figure 18-48. Gated Mode, Single Scan Timing

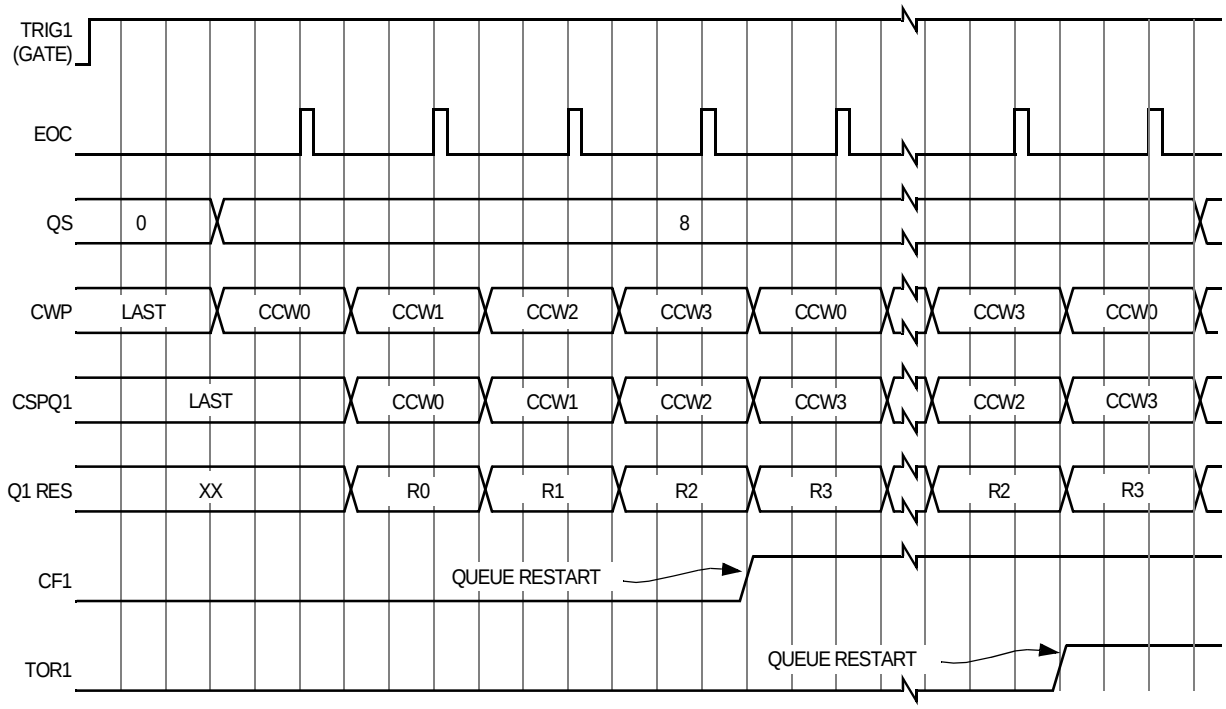

Figure 18-49. Gated Mode, Continuous Scan Timing

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Analog supplies should be isolated from digital supplies as much as possible. This necessity stems from the higher performance requirements often associated with analog circuits. Therefore, deriving an analog supply from a local digital supply is not recommended. However, if for economic reasons digital and analog power are derived from a common regulator, filtering of the analog power is recommended in addition to the bypassing of the supplies already mentioned. For example, an RC low pass filter could be used to isolate the digital and analog supplies when generated by a common regulator. If multiple high precision analog circuits are locally employed (for example, two A/D converters), the analog supplies should be isolated from each other as sharing supplies introduces the potential for interference between analog circuits.

Grounding is the most important factor influencing analog circuit performance in mixed signal systems (or in standalone analog systems). Close attention must be paid not to introduce additional sources of noise into the analog circuitry. Common sources of noise include ground loops, inductive coupling, and combining digital and analog grounds together inappropriately.

The problem of how and when to combine digital and analog grounds arises from the large transients which the digital ground must handle. If the digital ground is not able to handle the large transients, the current from the large transients can return to ground through the analog ground. It is the excess current overflowing into the analog ground which causes performance degradation by developing a differential voltage between the true analog ground and the microcontroller's ground pin. The end result is that the ground observed by the analog circuit is no longer true ground and often ends in skewed results.

Two similar approaches designed to improve or eliminate the problems associated with grounding excess transient currents involve star-point ground systems. One approach is to star-point the different grounds at the power supply origin, thus keeping the ground isolated. Refer to **Figure 18-50**.

Another approach is to star-point the different grounds near the analog ground pin on the microcontroller by using small traces for connecting the non-analog grounds to the analog ground. The small traces are meant only to accommodate dc differences, not ac transients.

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NOTE: *This star-point scheme still requires adequate grounding for digital and analog subsystems in addition to the star-point ground.*

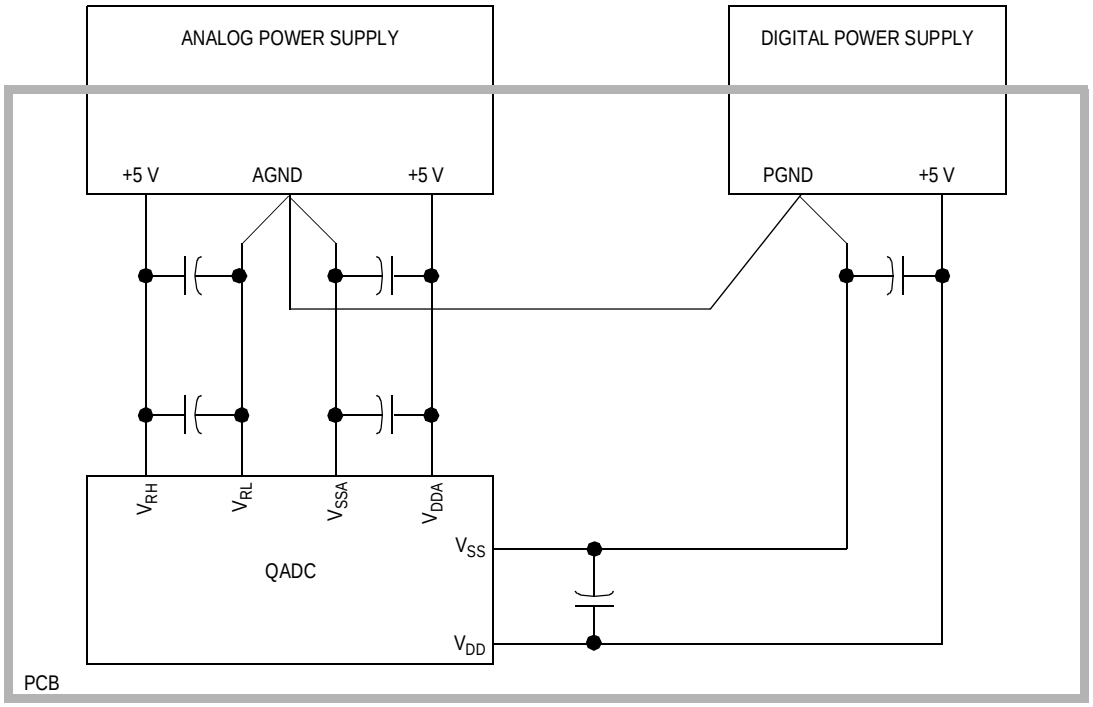

Figure 18-50. Star-Ground at the Point of Power Supply Origin

Other suggestions for PCB layout in which the QADC is employed include:

- Analog ground must be low impedance to all analog ground points in the circuit.
- Bypass capacitors should be as close to the power pins as possible.
- The analog ground should be isolated from the digital ground. This can be done by cutting a separate ground plane for the analog ground.
- Non-minimum traces should be utilized for connecting bypass capacitors and filters to their corresponding ground/power points.
- Minimum distance for trace runs when possible.

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18.11.5 Accommodating Positive/Negative Stress Conditions

Positive or negative stress refers to conditions which exceed nominally defined operating limits. Examples include applying a voltage exceeding the normal limit on an input (for example, voltages outside of the suggested supply/reference ranges) or causing currents into or out of the pin which exceed normal limits. QADC specific considerations are voltages greater than V_{DDA}, V_{RH}, or less than V_{SSA} applied to an analog input which cause excessive currents into or out of the input. Refer to **Section 22. Electrical Specifications** for more information on exact magnitudes.

Either stress conditions can potentially disrupt conversion results on neighboring inputs. Parasitic devices, associated with CMOS processes, can cause an immediate disruptive influence on neighboring pins. Common examples of parasitic devices are diodes to substrate and bipolar devices with the base terminal tied to substrate (V_{SSI}/V_{SSA} ground). Under stress conditions, current injected on an adjacent pin can cause errors on the selected channel by developing a voltage drop across the selected channel's impedances.

Figure 18-51 shows an active parasitic bipolar NPN transistor when an input pin is subjected to negative stress conditions. **Figure 18-52** shows positive stress conditions can activate a similar PNP transistor.

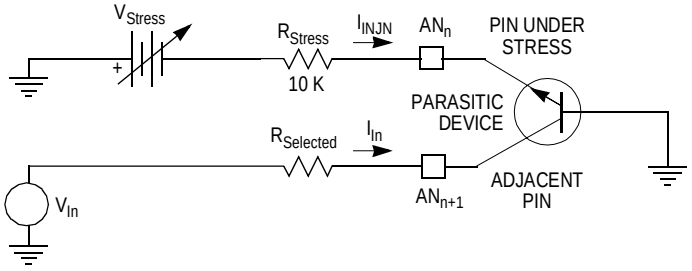

Figure 18-51. Input Pin Subjected to Negative Stress

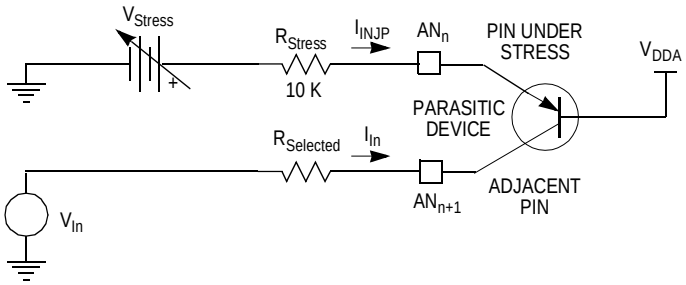

Figure 18-52. Input Pin Subjected to Positive Stress

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The current into the pin (I_{INJN} or I_{INJP}) under negative or positive stress is determined by these equations:

$$I_{INJN} = \frac{-(V_{Stress} - V_{BE})}{R_{Stress}}$$

$$I_{INJP} = \frac{V_{Stress} - V_{EB} - V_{DDA}}{R_{Stress}}$$

where:

V_{Stress} = Adjustable voltage source

V_{EB} = Parasitic PNP emitter/base voltage

V_{BE} = Parasitic NPN base/emitter voltage

R_{Stress} = Source impedance (10 K resistor in **Figure 18-51** and **Figure 18-52** on stressed channel)

$R_{Selected}$ = Source impedance on channel selected for conversion

The current into (I_{In}) the neighboring pin is determined by the K_N (current coupling ratio) of the parasitic bipolar transistor ($K_N << 1$). The I_{In} can be expressed by this equation:

$$I_{In} = -K_N * I_{INJ}$$

where:

I_{INJ} is either I_{INJN} or I_{INJP}.

A method for minimizing the impact of stress conditions on the QADC is to strategically allocate QADC inputs so that the lower accuracy inputs are adjacent to the inputs most likely to see stress conditions.

Also, suitable source impedances should be selected to meet design goals and minimize the effect of stress conditions.

18.11.6 Analog Input Considerations

The source impedance of the analog signal to be measured and any intermediate filtering should be considered whether external multiplexing is used or not. **Figure 18-53** shows the connection of eight typical analog signal sources to one QADC analog input pin through a separate multiplexer chip. Also, an example of an analog signal source connected directly to a QADC analog input channel is displayed.

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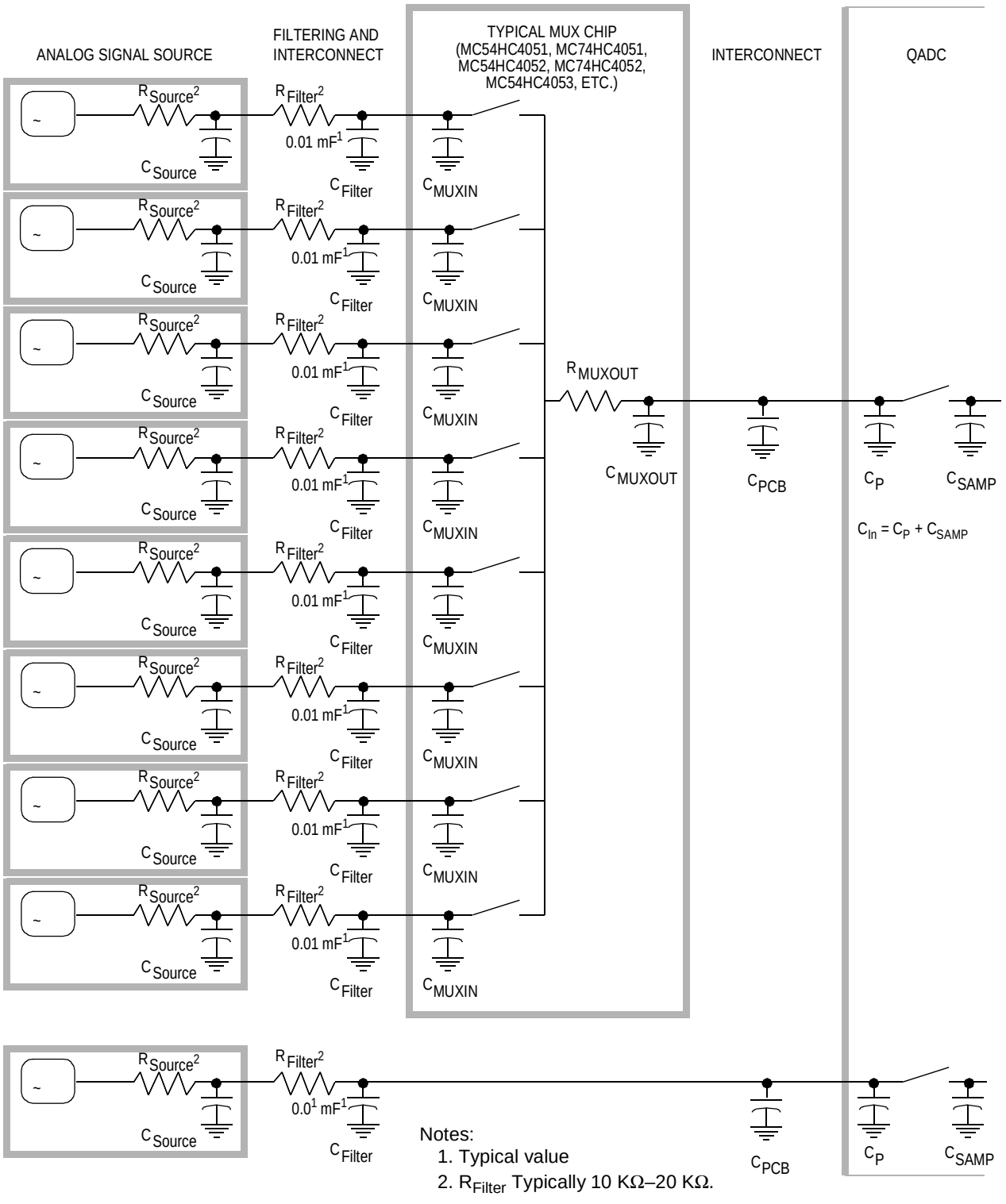

Figure 18-53. External Multiplexing of Analog Signal Sources

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18.11.7 Analog Input Pins

Analog inputs should have low ac impedance at the pins. Low ac impedance can be realized by placing a capacitor with good high frequency characteristics at the input pin of the part. Ideally, that capacitor should be as large as possible (within the practical range of capacitors that still have good high-frequency characteristics). This capacitor has two effects:

- It helps attenuate any noise that may exist on the input.
- It sources charge during the sample period when the analog signal source is a high-impedance source.

Series resistance can be used with the capacitor on an input pin to implement a simple RC filter. The maximum level of filtering at the input pins is application dependent and is based on the bandpass characteristics required to accurately track the dynamic characteristics of an input. Simple RC filtering at the pin may be limited by the source impedance of the transducer or circuit supplying the analog signal to be measured. (See **18.11.7.2 Error Resulting from Leakage**). In some cases, the size of the capacitor at the pin may be very small.

Figure 18-54 is a simplified model of an input channel. Refer to this model in the following discussion of the interaction between the external circuitry and the circuitry inside the QADC.

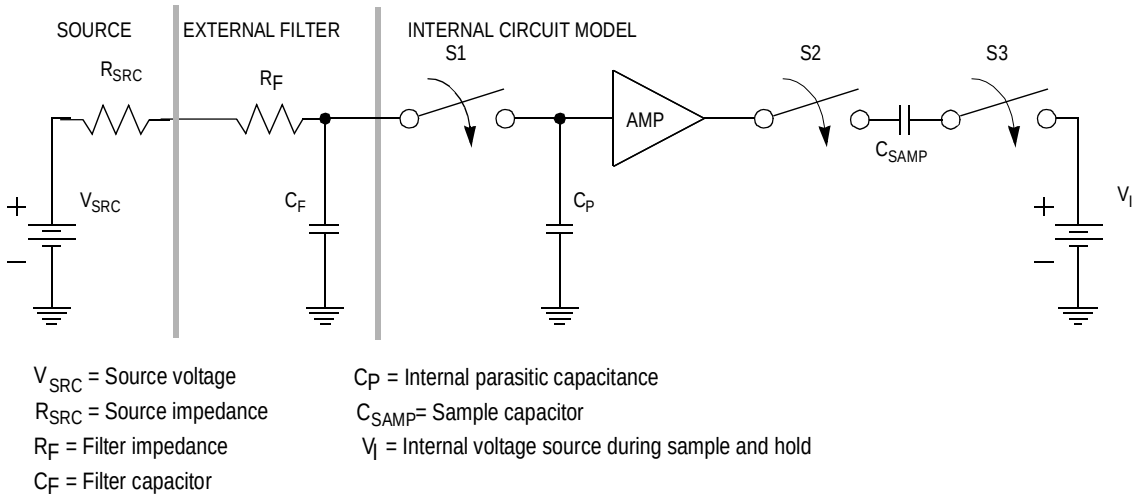

Figure 18-54. Electrical Model of an A/D Input Pin

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In **Figure 18-54**, R_F, R_{SRC} and C_F comprise the external filter circuit. C_P is the internal parasitic capacitor. C_{Samp} is the capacitor array used to sample and hold the input voltage. V_I is an internal voltage source used to provide charge to C_{samp} during sample phase.

The following paragraphs provide a simplified description of the interaction between the QADC and the user's external circuitry. This circuitry is assumed to be a simple RC low-pass filter passing a signal from a source to the QADC input pin. These simplifying assumptions are made:

- The external capacitor is perfect (no leakage, no significant dielectric absorption characteristics, etc.)
- All parasitic capacitance associated with the input pin is included in the value of the external capacitor.
- Inductance is ignored.
- The "on" resistance of the internal switches is 0 ohms and the "off" resistance is infinite.

18.11.7.1 Settling Time for the External Circuit

The values for R_{SRC}, R_F, and C_F in the user's external circuitry determine the length of time required to charge C_F to the source voltage level (V_{SRC}). At time t = 0, V_{src} changes in **Figure 18-54** while S1 is open, disconnecting the internal circuitry from the external circuitry. Assume that the initial voltage across C_F is 0. As C_F charges, the voltage across it is determined by the equation, where t is the total charge time:

$$V_{CF} = V_{SRC} (1 - e^{-t/(RF + RSRC)\ CF})$$

As t approaches infinity, V_{CF} will equal V_{SRC}. (This assumes no internal leakage.) With 10-bit resolution, 1/2 of a count is equal to 1/2048 full-scale value. Assuming worst case (V_{SRC} = full scale), **Table 18-16** shows the required time for C_F to charge to within 1/2 of a count of the actual source voltage during 10-bit conversions. **Table 18-16** is based on the RC network in **Figure 18-54**.

NOTE: *The following times are completely independent of the A/D converter architecture (assuming the QADC is not affecting the charging).*

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Table 18-16. External Circuit Settling Time to 1/2 LSB (10-Bit Conversions)

Filter Capacitor (C_F)	Source Resistance ($R_F + R_{SRC}$)			
	100 Ω	**1 kΩ**	**10 kΩ**	**100 kΩ**
1 µF	760 µs	7.6 ms	76 ms	760 ms
0.1 µF	76 µs	760 µs	7.6 ms	76 ms
0.01 µF	7.6 µs	76 µs	760 µs	7.6 ms
0.001 µF	760 ns	7.6 µs	76 µs	760 µs
100 pF	76 ns	760 ns	7.6 µs	76 µs

The external circuit described in **Table 18-16** is a low-pass filter. A user interested in measuring an ac component of the external signal must take the characteristics of this filter into account.

18.11.7.2 Error Resulting from Leakage

A series resistor limits the current to a pin therefore, input leakage acting through a large source impedance can degrade A/D accuracy. The maximum input leakage current is specified in **Section 22. Electrical Specifications**. Input leakage is greater at higher operating temperatures. In the temperature range from 125°C to 50°C, the leakage current is halved for every 8°C to 12°C reduction in temperature.

Assuming V_{RH}–V_{RL} = 5.12 V, 1 count (with 10-bit resolution) corresponds to 5 mV of input voltage. A typical input leakage of 200 nA acting through 10 kΩ of external series resistance results in an error of 0.4 count (2.0 mV). If the source impedance is 100 kΩ and a typical leakage of 100 nA is present, an error of 2 counts (10 mV) is introduced.

In addition to internal junction leakage, external leakage (for example, if external clamping diodes are used) and charge sharing effects with internal capacitors also contribute to the total leakage current. **Table 18-17** illustrates the effect of different levels of total leakage on accuracy for different values of source impedance. The error is listed in terms of 10-bit counts.

CAUTION: *Leakage from the part below 200 nA is obtainable only within a limited temperature range.*

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Table 18-17. Error Resulting From Input Leakage (I_{Off})

Source Impedance	Leakage Value (10-Bit Conversions)			
	100 nA	200 nA	500 nA	1000 nA
1 kΩ	—	—	0.1 counts	0.2 counts
10 kΩ	0.2 counts	0.4 counts	1 counts	2 counts
100 kΩ	2 counts	4 count	10 counts	20 counts

18.12 Interrupts

The four interrupt lines are outputs of the module and have no priority or arbitration within the module.

18.12.1 Interrupt Operation

QADC inputs can be monitored by polling or by using interrupts. When interrupts are not needed, software can disable the pause and completion interrupts and monitor the completion flag and the pause flag for each queue in the status register (QASR). In other words, flag bits can be polled to determine when new results are available.

Table 18-18 shows the status flag and interrupt enable bits which correspond to queue 1 and queue 2 activity.

Table 18-18. QADC Status Flags and Interrupt Sources

Queue	Queue Activity	Status Flag	Interrupt Enable Bit
Queue 1	Result written to last CCW in queue 1	CF1	CIE1
	Result written for a CCW with pause bit set in queue 1	PF1	PIE1
Queue 2	Result written to last CCW in queue 2	CF2	CIE2
	Result written for a CCW with pause bit set in queue 2	PF2	PIE2

If interrupts are enabled for an event, the QADC requests interrupt service when the event occurs. Using interrupts does not require continuously polling the status flags to see if an event has taken place.

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However, status flags must be cleared after an interrupt is serviced, in to disable the interrupt request

In both polled and interrupt-driven operating modes, status flags must be re-enabled after an event occurs. Flags are re-enabled by clearing appropriate QASR bits in a particular sequence. The register must first be read, then 0s must be written to the flags that are to be cleared. If a new event occurs between the time that the register is read and the time that it is written, the associated flag is not cleared.

18.12.2 Interrupt Sources

The QADC includes four sources of interrupt requests, each of which is separately enabled. Each time the result is written for the last conversion command word (CCW) in a queue, the completion flag for the corresponding queue is set, and when enabled, an interrupt request is generated. In the same way, each time the result is written for a CCW with the pause bit set, the queue pause flag is set, and when enabled, an interrupt request is generated. Refer to **Table 18-18**.

The pause and complete interrupts for queue 1 and queue 2 have separate interrupt vector levels, so that each source can be separately serviced.

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Section 19. External Bus Interface Module (EBI)

19.1 Contents

19.2 Introduction 504
19.3 Signal Descriptions 505
19.3.1 Data Bus (D[31:0]) 506
19.3.2 Show Cycle Strobe (SHS) 506
19.3.3 Transfer Acknowledge (TA) 506
19.3.4 Transfer Error Acknowledge (TEA) 506
19.3.5 Emulation Mode Chip Selects (CSE[1:0]) 506
19.3.6 Transfer Code (TC[2:0]) 506
19.3.7 Read/Write (R/W) 507
19.3.8 Address Bus (A[22:0]) 507
19.3.9 Enable Byte (EB[3:0]) 507
19.3.10 Chip Selects (CS[3:0]) 507
19.3.11 Output Enable (OE) 507
19.3.12 Transfer Size (TSIZ[1:0]) 507
19.3.13 Processor Status (PSTAT[3:0]) 507
19.4 Memory Map and Registers 508
19.5 Operand Transfer 508
19.6 Enable Byte Pins (EB[3:0]) 510
19.7 Bus Master Cycles 510
19.7.1 Read Cycles 511
19.7.1.1 State 1 (X1) 512
19.7.1.2 Optional Wait States (X2W) 512
19.7.1.3 State 2 (X2) 512
19.7.2 Write Cycles 513
19.7.2.1 State 1 (X1) 514
19.7.2.2 Optional Wait States (X2W) 514
19.7.2.3 State 2 (X2) 514

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19.8 Bus Exception Operation 516
19.8.1 Transfer Error Termination 516
19.8.2 Transfer Abort Termination 516
19.9 Emulation Support 516
19.9.1 Emulation Chip-Selects (CSE[1:0]) 516
19.9.2 Internal Data Transfer Display (Show Cycles) 517
19.9.3 Show Strobe (SHS) 518
19.10 Bus Monitor. 519
19.11 Interrupts. 520

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19.2 Introduction

The external bus interface (EBI) module is responsible for controlling the transfer of information between the internal M•CORE local bus and external address space. The external bus has 23 address lines and 32 data lines.

In master mode and emulation mode, the EBI functions as a bus master and allows internal bus cycles to access external resources. In single-chip mode, the EBI is active, but the external data bus is not available, and no external data or termination signals are transferred to the internal bus.

The EBI supports data transfers to both 32-bit and 16-bit ports. Chip-select channels are programmed to define the port size for specific address ranges. When no chip-select is active during an external data transfer, the port size is assumed to be 32 bits.

The EBI supports a variable length external bus cycle to accommodate the access speed of any device. During an external data transfer, the EBI drives the address pins, byte enable pins, output enable pins, size pins, and read/write pins. Wait states are inserted until the bus cycle is terminated by the assertion of the internal transfer acknowledge signal by a chip-select channel or by the assertion of the external $\overline{TA}$ or $\overline{TEA}$ pins. The minimum external bus cycle is one clock.

The EBI also drives the address, size, and read/write pins during internal data transfers, but the output enable and byte enable pins are not asserted. To see the internal data bus on the external pins, show cycles must be enabled.

Only internal sources can terminate internal data transfers. Chip-select channels, external $\overline{TA}$ assertion, and external $\overline{TEA}$ assertion cannot terminate internal data transfers.

19.3 Signal Descriptions

Table 19-1 provides an overview of the signal properties which are discussed in this subsection.

Table 19-1. Signal Properties

Name	Port	Function	Pullup
D[31:0]	PA, PB, PC, PD	Data bus	—
$\overline{SHS}$	PE7	Show cycle strobe	Active
$\overline{TA}$	PE6	Transfer acknowledge	Active
$\overline{TEA}$	PE5	Transfer error acknowledge	Active
CSE[1:0]	PE[4:3]	Emulation chip selects	Active
TC[2:0]	PE[2:0]	Transfer code	Active
R/$\overline{W}$	PF7	Read/write	Active
A[22:0]	PF[6:0], PG, PH	Address bus	Active
EB[3:0]	PI[7:4]	Enable byte	Active
$\overline{CS[3:0]}$	PI[3:0]	Chip selects	Active
$\overline{OE}$	—	Output enable	—
TSIZ[1:0]	—	Transfer size	—
PSTAT[3:0]	—	Processor status	—

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19.3.1 Data Bus (D[31:0])

The three-state bidirectional data bus (D[31:0]) signals are the general-purpose data path between the microcontroller unit (MCU) and all other devices.

19.3.2 Show Cycle Strobe ($\overline{\text{SHS}}$)

In emulation mode, show cycle strobe ($\overline{\text{SHS}}$) is the strobe for capturing address, controls, and data during show cycles.

19.3.3 Transfer Acknowledge ($\overline{\text{TA}}$)

The transfer acknowledge ($\overline{\text{TA}}$) signal indicates that the external data transfer is complete. During a read cycle, when the processor recognizes $\overline{\text{TA}}$, it latches the data and then terminates the bus cycle. During a write cycle, when the processor recognizes $\overline{\text{TA}}$, the bus cycle is terminated. $\overline{\text{TA}}$ is an input in master and emulation modes.

19.3.4 Transfer Error Acknowledge ($\overline{\text{TEA}}$)

The transfer error acknowledge ($\overline{\text{TEA}}$) indicates an error condition exists for the bus transfer. The bus cycle is terminated and the CPU begins execution of the access error exception. $\overline{\text{TEA}}$ is an input in master and emulation modes.

19.3.5 Emulation Mode Chip Selects (CSE[1:0])

The emulation mode chip selects (CSE[1:0]) output signals provide information for development support.

19.3.6 Transfer Code (TC[2:0])

The transfer code (TC[2:0]) output signals indicate the data transfer code for the current bus cycle.

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19.3.7 Read/Write (R/$\overline{W}$)

The read/write (R/$\overline{W}$) output signal indicates the direction of the data transfer on the bus. A logic 1 indicates a read from a slave device and a logic 0 indicates a write to a slave device.

19.3.8 Address Bus (A[22:0])

The address bus (A[22:0]) output signals provide the address for the current bus transfer.

19.3.9 Enable Byte ($\overline{EB}$[3:0])

The enable byte ($\overline{EB}$[3:0]) output signals indicate which byte of data is valid during external cycles.

19.3.10 Chip Selects ($\overline{CS}$[3:0])

The chip selects ($\overline{CS}$[3:0]) output signals select external devices for external bus transactions.

19.3.11 Output Enable ($\overline{OE}$)

The output enable ($\overline{OE}$) signal indicates when an external device can drive data during external read cycles.

19.3.12 Transfer Size (TSIZ[1:0])

TSIZ[1:0] provides an indication of the M•CORE transfer size.

19.3.13 Processor Status (PSTAT[3:0])

PSTAT[3:0] provides an indication of the M•CORE processor status.

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19.4 Memory Map and Registers

The EBI is not memory-mapped and has no software-accessible registers.

19.5 Operand Transfer

The possible operand accesses for the internal M•CORE bus are:

- Byte
- Aligned upper half-word
- Aligned lower half-word
- Aligned word

No misaligned transfers are supported. The EBI controls the byte, half-word, or word operand transfers between the M•CORE bus and a 16-bit or 32-bit port. “Port” refers to the width of the data path that an external device uses during a data transfer. Each port is assigned to particular bits of the data bus. A 16-bit port is assigned to pins D[31:16] and a 32-bit port is assigned to pins D[31:0].

In the case of a word (32-bit) access to a 16-bit port, the EBI runs two external bus cycles to complete the transfer. During the first external bus cycle, the A[1:0] pins are driven low, and the TSIZ[1:0] pins are driven to indicate word size. During the second cycle, A1 is driven high to increment the external address by two bytes, A0 is still driven low, and the TSIZ[1:0] pins are driven to indicate half-word size.

During any word-size transfer, the EBI always drives the A[1:0] pins low during a word transfer (except on the second cycle of a word to half-word port transfer in which A1 is incremented).

Table 19-2 shows each possible transfer size, alignment, and port width. The data bytes shown in the table represent external data pins. This data is multiplexed and driven to the external data bus as shown. The bytes labeled with a dash are not required; the M•CORE will ignore them on read transfers, and drive them with undefined data on write transfers.

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Table 19-2. Data Transfer Cases

Transfer Size	Port Width	External Pins				Data Bus Transfer			
		TSIZ1	TSIZ0	A1	A0				
Byte	16	0	1	0	0	D[31:24]	—	—	—
	32					D[31:24]	—	—	—
	16			0	1	—	D[23:16]	—	—
	32					—	D[23:16]	—	—
	16			1	0	—	—	D[31:24]	—
	32					—	—	D[15:8]	—
	16			1	1	—	—	—	D[23:16]
	32					—	—	—	D[7:0]
Half-word	16	1	0	0	0	D[31:24]	D[23:16]	—	—
	32					D[31:24]	D[23:16]	—	—
	16			1	0	—	—	D[31:24]	D[23:16]
	32					—	—	D[15:8]	D[7:0]
Word	16[1]	0	0	0	0	D[31:24]	D[23:16]	—	—
		1		1	0	—	—	D[31:24]	D[23:16]
	32	0		0	0	D[31:24]	D[23:16]	D[15:8]	D[7:0]

1. The EBI runs two cycles for word accesses to 16-bit ports. The table shows the data placement for both bus cycles.

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19.6 Enable Byte Pins (EB[3:0])

The enable byte pins (EB[3:0]) are configurable as byte enables for read and write cycles, or as write enables for write cycles only. The default function is byte enable unless there is an active chip-select match with the WE bit set. In all external cycles when one or more EB pins are asserted, the encoding corresponds to the external data pins to be used for the transfer as outlined in **Table 19-3**.

Table 19-3. EB[3:0] Assertion Encoding

EB Pin	External Data Pins
EB0	D[31:24]
EB1	D[23:16]
EB2	D[15:8]
EB3	D[7:0]

19.7 Bus Master Cycles

In this subsection, each EBI bus cycle type is defined in terms of actions associated with a succession of internal states. These internal states are only for reference and may not correspond to any implemented machine states.

Read or write operations may require multiple bus cycles to complete based on the operand size and target port size. Refer to **19.5 Operand Transfer** for more information. In the discussion that follows, it is assumed that only a single bus cycle is required for a transfer.

In the waveform diagrams (**Figure 19-3** through **Figure 19-6**), data transfers are related to clock cycles, independent of the clock frequency. The external bus states are also noted.

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19.7.1 Read Cycles

During a read cycle, the EBI receives data from an external memory or peripheral device. During external read cycles, the $\overline{OE}$ pin is asserted regardless of operand size. See **Figure 19-1**.

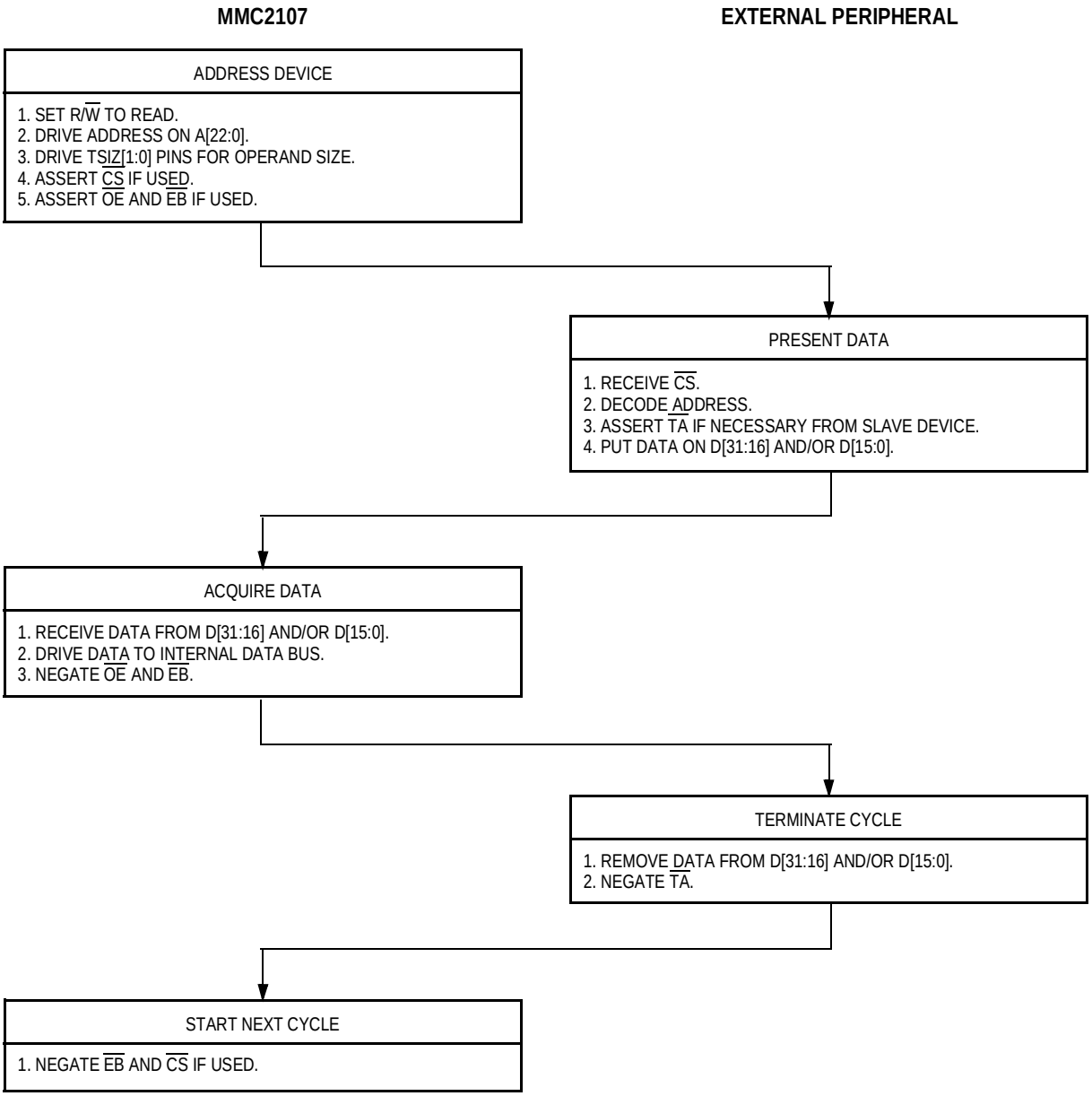

Figure 19-1. Read Cycle Flowchart

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19.7.1.1 State 1 (X1)

The EBI drives the address bus. R/$\overline{W}$ is driven high to indicate a read cycle. The TSIZ[1:0] pins are driven to indicate the number of bytes in the transfer. TC[2:0] pins are driven to indicate the type of access. $\overline{CS}$ may be asserted to drive a device.

Later in state 1, $\overline{OE}$ is asserted. If the $\overline{EB}$ pins are not configured as write enables for this cycle, one or more $\overline{EB}$ pins are also asserted, depending on the size and position of the data to be transferred.

If either the external $\overline{TA}$ pin or internal chip-select transfer acknowledge signal is asserted before the end of state 1, the EBI proceeds to state 2.

19.7.1.2 Optional Wait States (X2W)

Wait states are inserted until the slave asserts the $\overline{TA}$ pin or the internal chip-select transfer acknowledge signal is asserted. Wait states are counted in full clocks.

19.7.1.3 State 2 (X2)

One-half clock later in state 2, the selected device puts its information on D[31:16] and/or D[15:0]. One or both half-words of the external data bus are driven to the internal data bus.

The address bus, R/$\overline{W}$, $\overline{CS}$, $\overline{OE}$, $\overline{EB}$, TC, and TSIZ pins remain valid through state 2 to allow for static memory operation and signal skew.

The slave device asserts data until it detects the negation of $\overline{OE}$, after which it and must remove its data within approximately one-half of a state. Note that the data bus may not become free until state 1.

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19.7.2 Write Cycles

On a write cycle, the EBI transfers data to an external memory or peripheral device. See **Figure 19-2**.

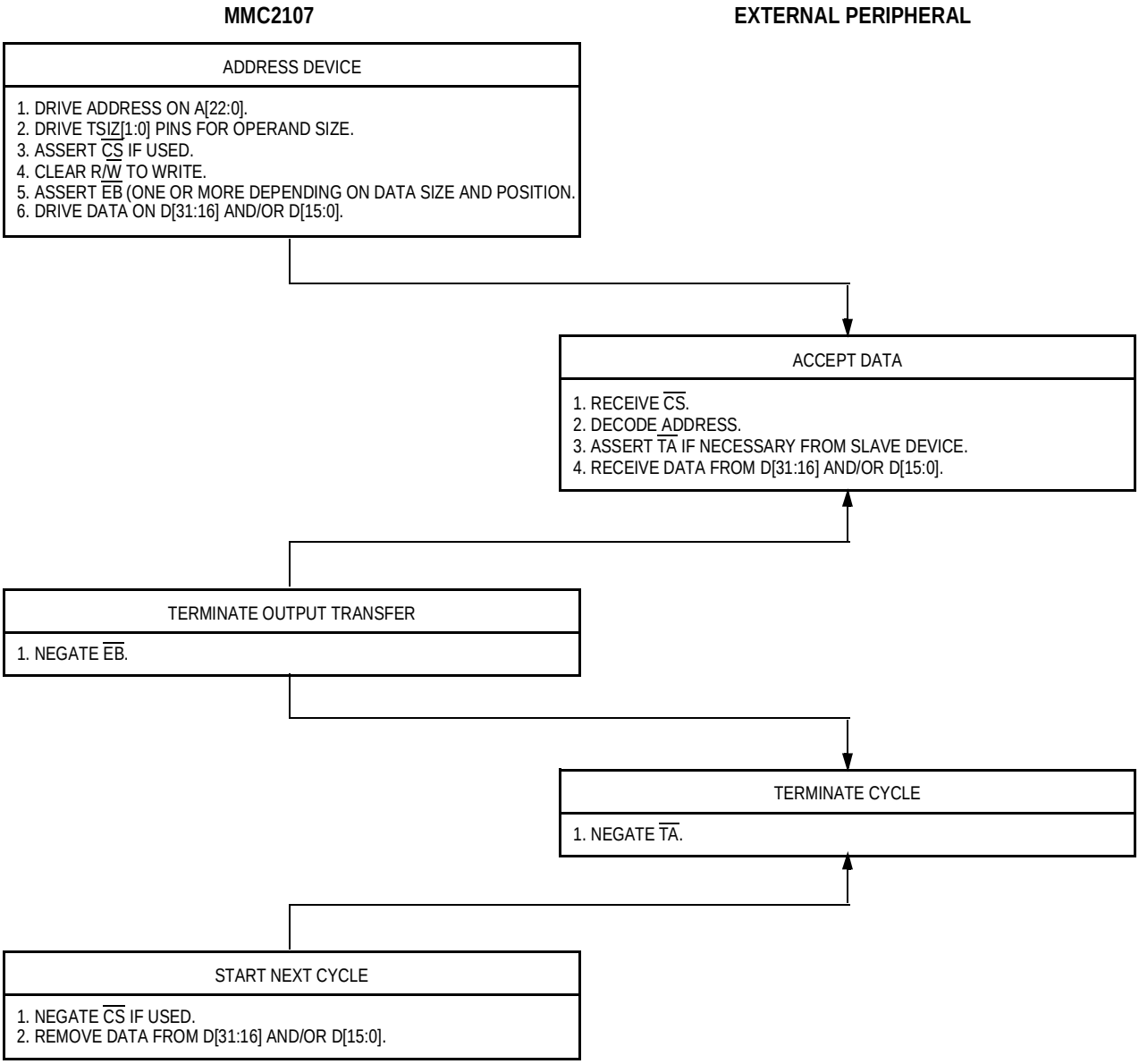

Figure 19-2. Write Cycle Flowchart

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19.7.2.1 State 1 (X1)

The EBI drives the address bus. The TSIZ[1:0] pins are driven to indicate the number of bytes in the transfer. TC[2:0] pins are driven to indicate the type of access. $\overline{CS}$ may be asserted to drive a device. $\overline{OE}$ is negated.

Later in state 1, R/$\overline{W}$ is driven low indicating a write cycle. One or more $\overline{EB}$ pins are asserted, depending on the size and position of the data to be transferred.

If either the external $\overline{TA}$ pin or internal chip-select transfer acknowledge signal is asserted before the end of state 1, the EBI proceeds to state 2.

19.7.2.2 Optional Wait States (X2W)

Wait states are inserted until the slave asserts the $\overline{TA}$ pin or the internal chip-select transfer acknowledge signal is asserted. The EBI drives its data onto data bus lines D[31:16] and/or D[15:0] on the first optional wait state. Wait states are counted in full clocks.

19.7.2.3 State 2 (X2)

If the data was not already driven during optional wait states, the EBI drives its data onto D[31:16] and/or D[15:0] in state 2.

$\overline{EB}$ is negated by the end of state 2. The address bus, data bus, R/$\overline{W}$, $\overline{CS}$, TC[2:0], and TSIZ[1:0] pins remain valid through state 2 to allow for static memory operation and signal skew.

Figure 19-3 and **Figure 19-4** illustrate external bus master cycles with and without wait states and show M•CORE bus activity.

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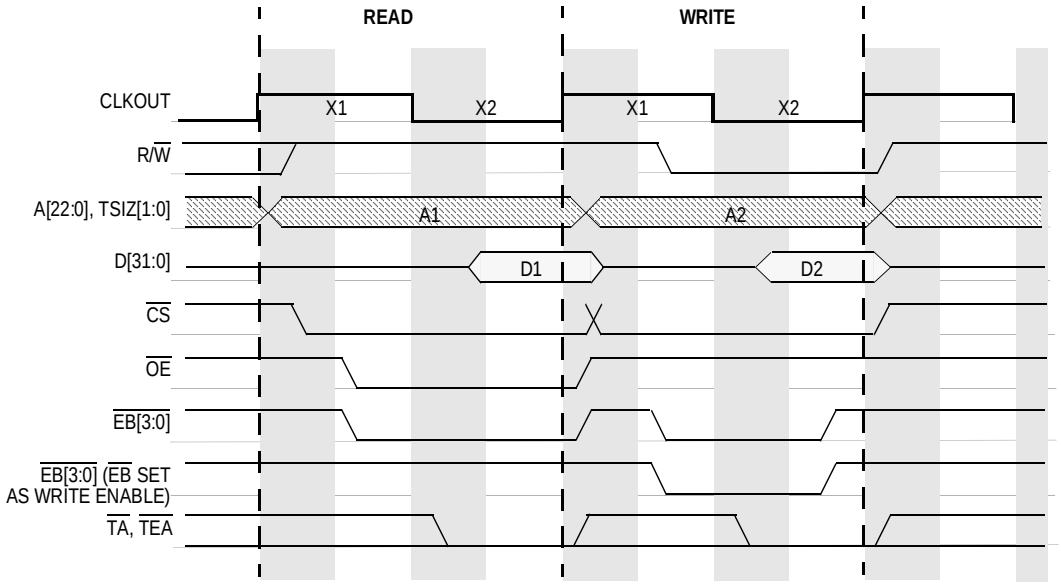

Figure 19-3. Master Mode — 1-Clock Read and Write Cycle

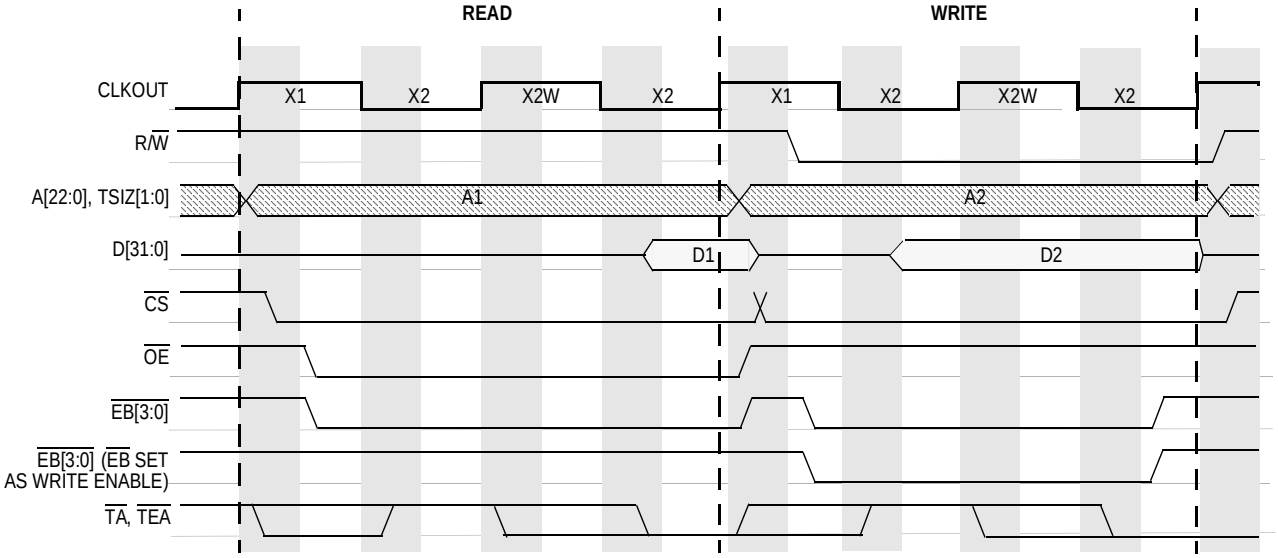

Figure 19-4. Master Mode — 2-Clock Read and Write Cycle

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19.8 Bus Exception Operation

19.8.1 Transfer Error Termination

Normal bus cycle termination requires the assertion of the $\overline{TA}$ pin or the internal transfer acknowledge signal. Minimal bus exception support is provided by transfer error cycle termination. For transfer error cycle termination, the external $\overline{TEA}$ pin or the internal transfer error acknowledge signal is asserted. Transfer error cycle termination takes precedence over normal cycle termination, provided $\overline{TEA}$ assertion meets its timing constraints.

The internal bus monitor will assert the internal transfer error acknowledge signal when $\overline{TA}$ response time is too long.

19.8.2 Transfer Abort Termination

External bus cycles which are aborted by the M•CORE, still have the address, R/$\overline{W}$, TC[2:0], TSIZ[1:0], $\overline{CS}$ (if used), $\overline{OE}$ (reads only), and $\overline{SHS}$ (if used) driven to the external pins.

19.9 Emulation Support

19.9.1 Emulation Chip-Selects (CSE[1:0])

While in emulation mode or master mode, special emulator chip-selects (CSE[1:0]) are driven externally to allow internal/external accesses to be tracked by external hardware See **Table 19-4**.

In emulation mode, all port registers are mapped externally. CSE[1:0] = 10 whenever any emulated port registers are addressed. The lower bits of the address bus indicate the register accessed within the block.

Accesses to the address space which contains the registers for the internal modules (except ports) are indicated by CSE[1:0] = 11.

Internal accesses, other than to the specific module control registers, are indicated by CSE[1:0] = 01. To emulate internal FLASH, the external

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D28 pin is driven low during reset configuration to disable the internal FLASH so that no conflict exists with the external memory device. It should be noted that at higher frequencies writes to external memories emulating the internal memories may require one clock for read accesses and two clocks for write accesses.

Table 19-4. Emulation Mode Chip-Select Summary(1)

CSE1	CSE0	Indication in Emulation Mode
1	1	Internal access to any register space (excluding ports) Reset state (0x00c1_0000:0x00ff_ffff)
1	0	Internal access to ports register space (0x00c0_0000:0x00c0_ffff)
0	1	Internal access not covered by CSE encoding = 11, 10 (0x0000_0000:0x00bf_ffff; 0x0100_0000:0x07ff_ffff)
0	0	External access (0x8000_0000 to 0xffff_ffff)

1. $\overline{\text{CSE}}$[1:0] is valid only for the duration of valid bus cycles or reset. Undefined otherwise.

19.9.2 Internal Data Transfer Display (Show Cycles)

Internal data transfers normally occur without showing the internal data bus activity on the external data bus. For debugging purposes, however, it may be desirable to have internal cycle data appear on the external bus. These external bus cycles are referred to as show cycles and are distinguished from normal external cycles by the fact that $\overline{\text{OE}}$ and $\overline{\text{EB}}$[3:0] remain negated.

Regardless of whether show cycles are enabled, the EBI drives the address bus, TC[2:0], TSIZ[1:0] and R/$\overline{\text{W}}$ signals, indicating the internal cycle activity. When show cycles are disabled, D[31:0] remains in a high impedance state. When show cycles are enabled, $\overline{\text{OE}}$ and $\overline{\text{EB}}$[3:0] remain negated while the internal data is presented on D[31:0] on the first clock tick after the termination of the internal cycle.

Show cycles are always enabled in emulation mode. In master mode, show cycles are disabled coming out of reset and must be enabled by writing to the SHEN bit in the chip configuration register (CCR).

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NOTE: *The PEPA and PCDPA bits in the ports must also be set to 1 to obtain full visibility. The waveforms shown in **Figure 19-5** describe show cycles.*

19.9.3 Show Strobe ($\overline{\text{SHS}}$)

The show strobe ($\overline{\text{SHS}}$) pin provides an indication to an external device (emulator or logic analyzer) when to latch address, TC[2:0], TSIZ[1:0], R/$\overline{\text{W}}$, CSE, PSTAT, and data from the external pins. The $\overline{\text{SHS}}$ pin is enabled coming out of reset in emulation mode. In master mode, the $\overline{\text{SHS}}$ pin may be enabled by writing to the port E pin assignment register (PEPAR).

For any external cycle or show cycle, the $\overline{\text{SHS}}$ pin is driven low to indicate valid address, TC, TSIZ, R/$\overline{\text{W}}$, CSE, and PSTAT are present at the pins, and driven back high to indicate valid data. The $\overline{\text{SHS}}$ pin is driven low and back high only once per external bus cycle. See **Figure 19-5** and **Figure 19-6**.

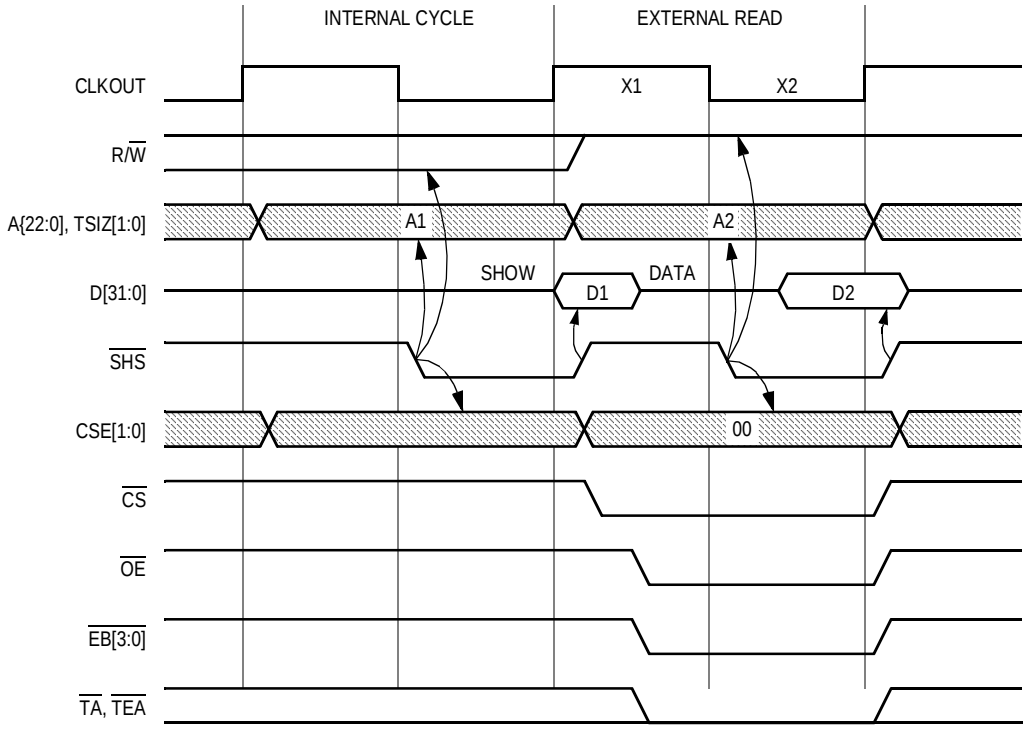

Figure 19-5. Internal (Show) Cycle Followed by External 1-Clock Read

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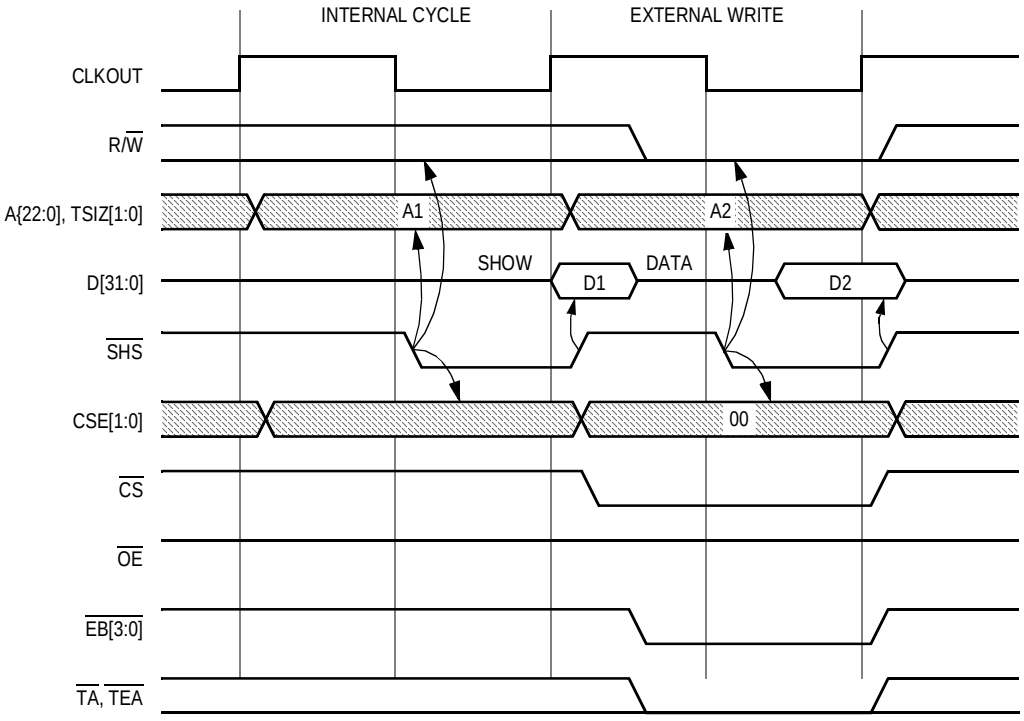

Figure 19-6. Internal (Show) Cycle Followed by External 1-Clock Write

19.10 Bus Monitor

The bus monitor can be set detects excessively long bus access termination response times. Whenever an undecoded address is accessed or a peripheral is inoperative, the access is not terminated and the bus is potentially locked up while it waits for the required response.

The bus monitor monitors the cycle termination response times during a bus cycle. If the cycle termination response time exceeds a programmed count, the bus monitor asserts an internal bus error.

The bus monitor monitors the cycle termination response time (in system clock cycles) by using a programmable maximum allowable response period. There are four selectable response time periods for the bus monitor, selectable among 8, 16, 32, and 64 system clock cycles. The periods are selectable with the BMT[1:0] field in the chip configuration module CCR. The programmability of the timeout allows for varying external peripheral response times. The monitor is cleared and restarted

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on all bus accesses. If the cycle is not terminated within the selected response time, a timeout occurs and the bus monitor terminates the bus cycle.

The bus monitor can be configured with the BME bit in the chip configuration module CCR to monitor only internal bus accesses or both internal and external bus accesses. Also, the bus monitor can be disabled during debug mode for both internal and external accesses.

Two external bus cycles are required for a single 32-bit access to a 16-bit port. If the bus monitor is enabled to monitor external accesses, then the bus monitor views the 32-bit access as two separate external bus cycles and not as one internal bus cycle.

19.11 Interrupts

The EBI does not generate interrupt requests.

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Section 20. Chip Select Module

20.1 Contents

20.2 Introduction 521
20.3 Features 522
20.4 Block Diagram 523
20.5 Signals 524
20.6 Memory Map and Registers 524
20.6.1 Memory Map 524
20.6.2 Registers 525
20.7 Functional Description 530
20.8 Interrupts. 531

20.2 Introduction

The chip select module provides chip enable signals for external memory and peripheral devices. The chip selects can also be programmed to terminate bus cycles. Up to four asynchronous chip select signals are available.

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20.3 Features

Features of the chip select module include:

- Reduced system complexity — No external glue logic required for typical systems if chip selects are used.
- Four programmable asynchronous active-low chip selects ($\overline{CS}$[3:0]) — Chip selects can be independently programmed with various features.
- Control for external boot device — $\overline{CS0}$ can be enabled at reset to select an external boot device.
- Fixed base addresses with 8-Mbyte block sizes
- Support for emulating internal memory space — When the EMINT bit is set in the chip configuration register (CCR), $\overline{CS1}$ matches only addresses in the internal memory space.
- Support for 16-bit and 32-bit external devices — The external port size can be programmed to be 16 or 32 bits.
- Programmable write protection — Each chip select address range can be designated for read access only.
- Programmable access protection — Each chip select address range can be designated for supervisor access only.
- Write-enable selection — The enable byte pins ($\overline{EB}$[3:0]) can be configured as byte enables (assert on both external read and write accesses) or write enables (only assert on external write accesses).
- Bus cycle termination — This option allows the chip select logic to terminate the bus cycle.
- Programmable wait states — To interface with various devices, up to seven wait states can be programmed before the access is terminated.
- Programmable extra wait state for write accesses — One wait state can be added to write accesses to allow writing to memories that require additional data setup time.

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20.4 Block Diagram

Figure 20-1 shows a programmable asynchronous chip select. All asynchronous chip selects have the same structure. All signals used to generate chip select signals are taken from the internal bus. Each chip select has a chip select control register to individually program the chip select characteristics.

All the chip selects share the same cycle termination generator. The active chip select for a particular bus cycle determines the number of wait states produced by the cycle termination generator before the cycle is terminated.

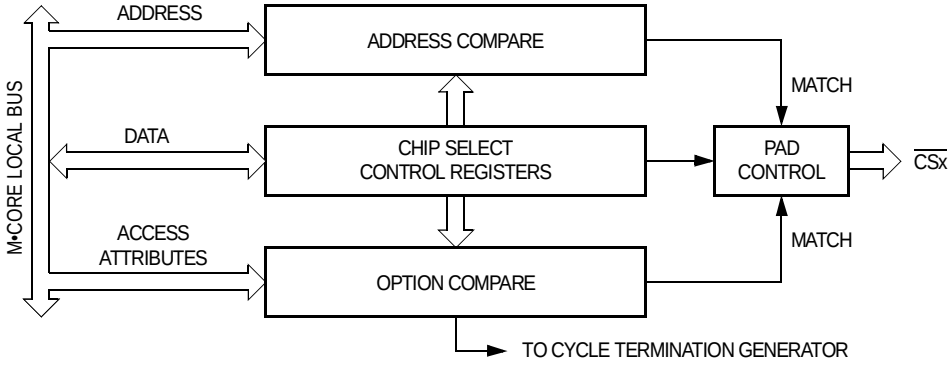

Figure 20-1. Chip Select Block Diagram

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20.5 Signals

Table 20-1 provides an overview of the signals described here.

Table 20-1. Signal Properties

Name	Function	Reset State	Pullup
$\overline{CS0}$	Chip select 0 pin	1	Active
$\overline{CS1}$	Chip select 1 pin	1	Active
$\overline{CS2}$	Chip select 2 pin	1	Active
$\overline{CS3}$	Chip select 3 pin	1	Active

$\overline{CS}$[3:0] are chip-select outputs. $\overline{CS}$[3:0] are available for general-purpose input/output (I/O) when not configured for chip select operation.

20.6 Memory Map and Registers

Table 20-2 shows the chip select memory map. The registers are described in 20.6.2 Registers.

20.6.1 Memory Map

Table 20-2. Chip Select Memory Map

Address	Bits 31–16	Bits 15–0	Access(1), (2)
0x00c2_0000	CSCR0 — chip select control register 0	CSCR1 — chip select control register 1	S
0x00c2_0004	CSCR2 — chip select control register 2	CSCR3 — chip select control register 3	S

1. User mode accesses to supervisor-only address locations have no effect and result in a cycle termination transfer error.
2. S = CPU supervisor mode access only.

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20.6.2 Registers

The chip programming model consists of four chip select control registers (CSCR0–CSCR3), one for each chip select (CS[3:0]). CSCR0–CSCR3 are read/write always and define the conditions for asserting the chip select signals.

All the chip select control registers are the same except for the reset states of the CSEN and PS bits in CSCR0 and the CSEN bit in CSCR1. This allows CS0 to be enabled at reset with either a 16-bit or 32-bit port size for selecting an external boot device and allows CS1 to be used to emulate internal memory.

Address: 0x00c2_0000 and 0x00c2_0001

	Bit 15	14	13	12	11	10	9	Bit 8
Read: / Write:	SO	RO	PS	WWS	WE	WS2	WS1	WS0
Reset:	0	0	See note	1	1	1	1	1
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	TAEN	CSEN
Write:								
Reset:	0	0	0	0	0	0	1	See note

= Writes have no effect and the access terminates without a transfer error exception.

Note: Reset state determined during reset configuration.

Figure 20-2. Chip Select Control Register 0 (CSCR0)

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Address: 0x00c2_0002 and 0x00c2_0003

	Bit 15	14	13	12	11	10	9	Bit 8
Read: / Write:	SO	RO	PS	WWS	WE	WS2	WS1	WS0
Reset:	0	0	1	1	1	1	1	1
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	TAEN	CSEN
Write:								
Reset:	0	0	0	0	0	0	1	See note

= Writes have no effect and the access terminates without a transfer error exception.

Note: Reset state determined during reset configuration.

Figure 20-3. Chip Select Control Register 1 (CSCR1)

Address: 0x00c2_0004 and 0x00c2_0005

	Bit 15	14	13	12	11	10	9	Bit 8
Read: / Write:	SO	RO	PS	WWS	WE	WS2	WS1	WS0
Reset:	0	0	1	1	1	1	1	1
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	TAEN	CSEN
Write:								
Reset:	0	0	0	0	0	0	1	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-4. Chip Select Control Register 2 (CSCR2)

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Address: 0x00c2_00006 and 0x00c2_0007

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	SO	RO	PS	WWS	WE	WS2	WS1	WS0
Reset:	0	0	1	1	1	1	1	1
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	TAEN	CSEN
Write:								
Reset:	0	0	0	0	0	0	1	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-5. Chip Select Control Register 3 (CSCR3)

SO — Supervisor-Only Bit

The SO bit restricts user mode access to the address range defined by the corresponding chip select. If the SO bit is 1, only supervisor mode access is permitted. If the SO bit is 0, both supervisor and user level accesses are permitted.

When an access is made to a memory space assigned to the chip select, the chip select logic compares the SO bit with bit 2 of the internal transfer code, which indicates whether the access is at the supervisor or user level. If the chip select logic detects a protection violation, the access is ignored.

1 = Only supervisor mode accesses allowed; user mode accesses ignored by chip select logic
0 = Supervisor and user mode accesses allowed

RO — Read-Only Bit

The RO bit restricts write accesses to the address range defined by the corresponding chip select. If the RO bit is 1, only read access is permitted. If the RO bit is 0, both read and write accesses are permitted.

When an access is made to a memory space assigned to the chip select, the chip select logic compares the RO bit with the internal

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read/write signal, which indicates whether the access is a read (read/write = 1) or a write (read/write = 0). If the chip select logic detects a violation (RO = 1 with read/write = 0), the access is ignored.

1 = Only read accesses allowed; write accesses ignored by the chip select logic
0 = Read and write accesses allowed

PS — Port Size Bit

The PS bit defines the width of the external data port supported by the chip select as either 16-bit or 32-bit. When a chip select is programmed as a 16-bit port, the external device must be connected to D[31:16]. For 32-bit accesses to 16-bit ports, the external memory interface initiates two bus cycles and multiplexes data as needed to complete the data transfer.

1 = 32 bit port
0 = 16 bit port

WWS — Write Wait State Bit

The WWS bit determines if an additional wait state is required for write cycles. WWS does not affect read cycles.

1 = One additional wait state added for write cycles
0 = No additional wait state added for write cycles

WE — Write Enable Bit

The WE bit defines when the enable byte output pins ($\overline{EB[3:0]}$) are asserted. When WE is 0, $\overline{EB[3:0]}$ are configured as byte enables and assert for both external read and external write accesses. When WE is 1, $\overline{EB[3:0]}$ are configured as write enables and assert only for external write accesses.

1 = $\overline{EB[3:0]}$ configured as write enables
0 = $\overline{EB[3:0]}$ configured as byte enables

NOTE: *The WE bit has no effect on the $\overline{EB[3:0]}$ pin function if the chip select is not active. If the chip select is not active, the $\overline{EB[3:0]}$ pin function is byte enable by default.*

WS[2:0] — Wait States Field

The WS field determines the number of wait states for the chip select logic to insert before asserting the internal cycle termination signal. One wait state is equal to one system clock cycle. If WS is configured for zero wait states, then the internal cycle termination signal is

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asserted in the clock cycle following the start of the cycle access, resulting in one-clock transfers. A WS configured for one wait state means that the internal cycle termination signal is asserted two clock cycles after the start of the cycle access.

Since the internal cycle termination signal is asserted internally after the programmed number of wait states, software can adjust the bus timing to accommodate the access speed of the external device. With up to seven possible wait states, even slow devices can be interfaced with the MCU.

Table 20-3. Chip Select Wait States Encoding

WS[2:0]	Number of Wait States			
	WWS = 0		WWS = 1	
	Read Access	Write Access	Read Access	Write Access
000	0	0	0	1
001	1	1	1	2
010	2	2	2	3
011	3	3	3	4
100	4	4	4	5
101	5	5	5	6
110	6	6	6	7
111	7	7	7	8

TAEN — Transfer Acknowledge Enable Bit

The TAEN bit determines whether the internal cycle termination signal is asserted by the chip select logic when accesses occur to the address range defined by the corresponding chip select. When TAEN is 0, an external device is responsible for asserting the external $\overline{TA}$ pin to terminate the bus access. When TAEN is 1, the chip select logic asserts the internal cycle termination signal after a time determined by the programmed number of wait states. When TAEN is 1, external logic can still terminate the access before the internal cycle termination signal is asserted by asserting the external $\overline{TA}$ pin.

1 = Internal cycle termination signal asserted by chip select logic
0 = Internal cycle termination signal asserted by external logic

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CSEN — Chip Select Enable Bit

The CSEN bit enables the chip select logic. When the chip select function is disabled, the $\overline{CSx}$ signal is negated high.

1 = Chip select function enabled
0 = Chip select function disabled

20.7 Functional Description

Each chip select can provide a chip enable signal for an external device and assert the internal bus cycle termination signal.

Setting the CSEN bit in CSCR enables the chip select to provide an external chip enable.

Setting both the CSEN and TAEN bits in CSCR enables the chip select to generate the internal bus cycle termination signal.

Both the chip select pin assertion and the bus cycle termination function depend on an initial address/option match for activation. During the matching process, the fixed base address of each chip select is compared to the corresponding address for the bus cycle to determine whether an address match has occurred. This match is further qualified by comparing the internal read/write indication and access type with the programmed values in CSCR of each chip select. When the address and option information match the current cycle, the chip select is activated. If no chip select matches the bus cycle information for the current access, the chip select logic does not respond in any way.

Only one chip select can be active for a given bus cycle. The configuration of the active chip select, determined by the wait state (WS/WWS) field, the port size (PS) field, and the write enable (WE) field, is used for the access.

NOTE: *WWS and WS are valid only if the TAEN bit is 1 for the active chip select.*

When no chip select pin is available, the active chip select can still terminate the bus cycle. If both the CSEN and TAEN bits are 1 and the address/options match the chip select configuration, then the chip select logic asserts the internal termination signal; the bus cycle terminates after the programmed number of wait states. If the external $\overline{TA}$ or $\overline{TEA}$

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pin is asserted before the chip select logic asserts the internal cycle termination signal, then the bus cycle is terminated early.

If internal address bit 31 is 0, then the access is internal. If internal address bit 31 is 1, then the access is external.

NOTE: *Chip select logic does not decode internal address bits A[30:25].*

Table 20-4. Chip Select Address Range Encoding

Chip Select	Block Size	Address Bits Compared (A[31:23])[1]
$\overline{CS0}$	8 MB	1XXX_XXX0_0
$\overline{CS1}$	8 MB	1XXX_XXX0_1[2]
$\overline{CS2}$	8 MB	1XXX_XXX1_0
$\overline{CS3}$	8 MB	1XXX_XXX1_1

1. The chip selects do not decode A[30:25]. Thus, the total 32-Mbyte block size is repeated/mirrored in external memory space.
2. If the EMINT bit in the chip configuration module CCR is set, then $\overline{CS1}$ matches only internal accesses to the 8-MB block starting at address 0 to support emulation of internal memory. Thus, A[31:23] match 0xxx_xxx0_0.

20.8 Interrupts

The chip select module does not generate interrupt requests.

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Section 21. JTAG Test Access Port and OnCE

21.1 Contents

21.2 Introduction 535
21.3 Top-Level Test Access Port (TAP) 537
21.3.1 Test Clock (TCLK) 538
21.3.2 Test Mode Select (TMS) 538
21.3.3 Test Data Input (TDI) 538
21.3.4 Test Data Output (TDO) 538
21.3.5 Test Reset ($\overline{\text{TRST}}$) 538
21.3.6 Debug Event ($\overline{\text{DE}}$) 538
21.4 Top-Level TAP Controller 540
21.5 Instruction Shift Register 541
21.5.1 EXTEST Instruction 541
21.5.2 IDCODE Instruction 542
21.5.3 SAMPLE/PRELOAD Instruction 543
21.5.4 ENABLE_MCU_ONCE Instruction 543
21.5.5 HIGHZ Instruction 544
21.5.6 CLAMP Instruction 544
21.5.7 BYPASS Instruction 544
21.6 IDCODE Register 545
21.7 Bypass Register 546
21.8 Boundary SCAN Register 546
21.9 Restrictions 546
21.10 Non-Scan Chain Operation 547
21.11 Boundary Scan 547
21.12 Low-Level TAP (OnCE) Module 553
21.13 Signal Descriptions 555
21.13.1 Debug Serial Input (TDI) 555
21.13.2 Debug Serial Clock (TCLK) 555
21.13.3 Debug Serial Output (TDO) 555

Freescale Semiconductor, Inc.

21.13.4 Debug Mode Select (TMS) 556
21.13.5 Test Reset (TRST) 556
21.13.6 Debug Event (DE) 556
21.14 Functional Description 556
21.14.1 Operation 557
21.14.2 OnCE Controller and Serial Interface 558
21.14.3 OnCE Interface Signals 559
21.14.3.1 Internal Debug Request Input (IDR) 559
21.14.3.2 CPU Debug Request (DBGRQ) 560
21.14.3.3 CPU Debug Acknowledge (DBGACK) 560
21.14.3.4 CPU Breakpoint Request (BRKRQ) 560
21.14.3.5 CPU Address, Attributes (ADDR, ATTR) 560
21.14.3.6 CPU Status (PSTAT) 560
21.14.3.7 OnCE Debug Output (DEBUG) 560
21.14.4 OnCE Controller Registers 561
21.14.4.1 OnCE Command Register 561
21.14.4.2 OnCE Control Register 564
21.14.4.3 OnCE Status Register 568
21.14.5 OnCE Decoder (ODEC) 570
21.14.6 Memory Breakpoint Logic 570
21.14.6.1 Memory Address Latch (MAL) 571
21.14.6.2 Breakpoint Address Base Registers 571
21.14.7 Breakpoint Address Mask Registers 571
21.14.7.1 Breakpoint Address Comparators 572
21.14.7.2 Memory Breakpoint Counters 572
21.14.8 OnCE Trace Logic 572
21.14.8.1 OnCE Trace Counter 573
21.14.8.2 Trace Operation 574
21.14.9 Methods of Entering Debug Mode 574
21.14.9.1 Debug Request During RESET 574
21.14.9.2 Debug Request During Normal Activity 575
21.14.9.3 Debug Request During Stop, Doze, or Wait Mode . . . 575
21.14.9.4 Software Request During Normal Activity 575
21.14.10 Enabling OnCE Trace Mode 575
21.14.11 Enabling OnCE Memory Breakpoints 576
21.14.12 Pipeline Information and Write-Back Bus Register 576
21.14.12.1 Program Counter Register 577
21.14.12.2 Instruction Register 577

Freescale Semiconductor, Inc.

21.14.12.3 Control State Register 577
21.14.12.4 Writeback Bus Register 579
21.14.12.5 Processor Status Register 579
21.14.13 Instruction Address FIFO Buffer (PC FIFO) 580
21.14.14 Reserved Test Control Registers 581
21.14.15 Serial Protocol 581
21.14.16 OnCE Commands 582
21.14.17 Target Site Debug System Requirements 582
21.14.18 Interface Connector for JTAG/OnCE Serial Port 582

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21.2 Introduction

The MMC2107 has two JTAG (Joint Test Action Group) TAP (test access port) controllers:

1. A top-level controller that allows access to the MMC2107's boundary scan (external pins) register, IDCODE register, and bypass register
2. A low-level OnCE (on-chip emulation) controller that allows access to MMC2107's central processor unit (CPU) and debugger-related registers

At power-up, only the top-level TAP controller will be visible. If desired, a user can then enable the low-level OnCE controller which will in turn disable the top-level TAP controller. The top-level TAP controller will remain disabled until either power is removed and reapplied to the MMC2107 or until the test reset signal, $\overline{\text{TRST}}$, is asserted (logic 0).

The OnCE TAP controller can be enabled in either of two ways:

1. With the top-level TAP controller in its test-logic-reset state:
   a. Deassert $\overline{\text{TRST}}$, test reset (logic1)
   b. Assert $\overline{\text{DE}}$, the debug event (logic 0) for two TCLK, test clock, cycles
2. Shift the ENABLE_MCU_ONCE instruction, 0x3, into the top-level TAP controller's instruction register (IR) and pass through the TAP controller state update-IR.

Refer to **Figure 21-1**.

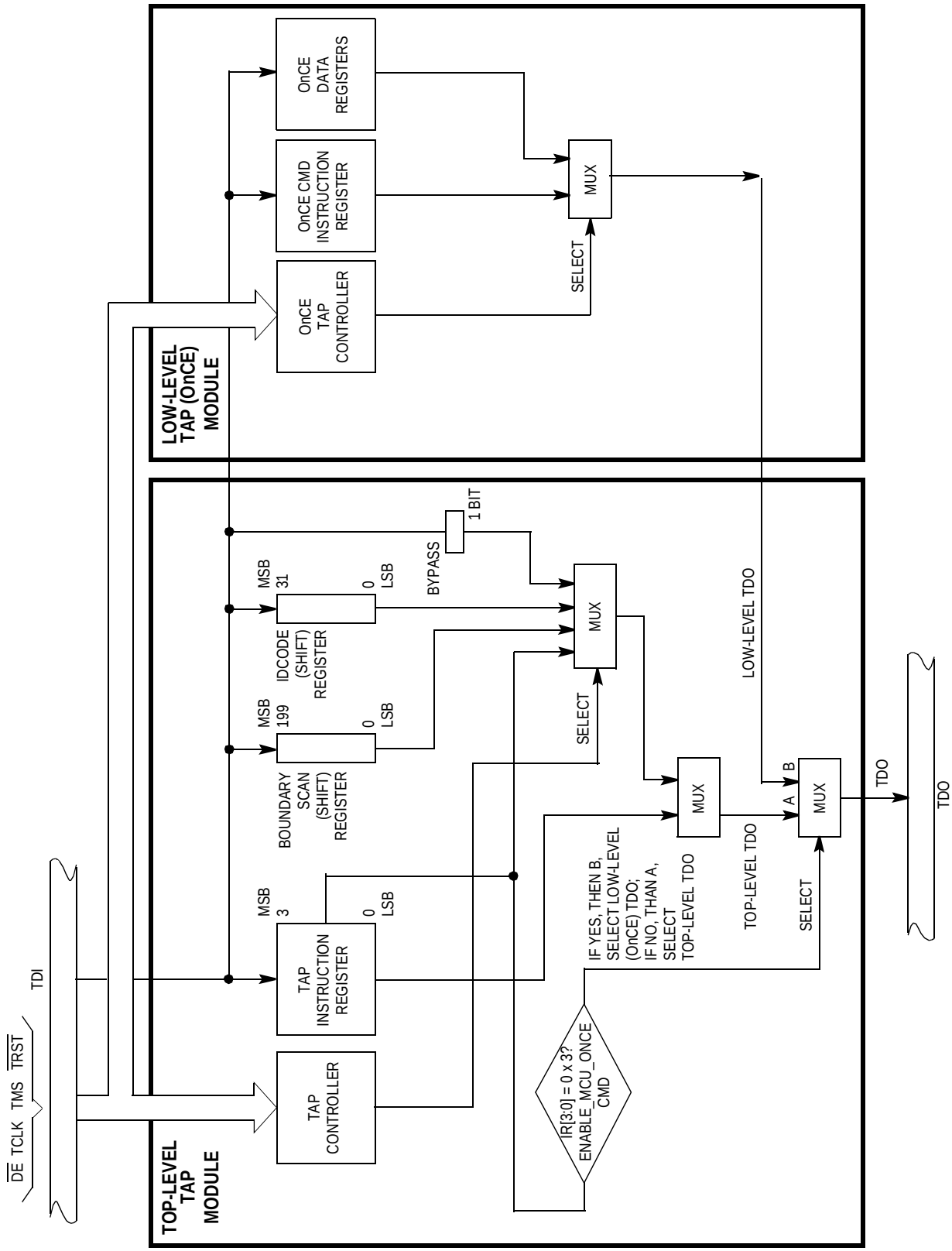

Figure 21-1. Top-Level Tap Module and Low-Level (OnCE) TAP Module

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21.3 Top-Level Test Access Port (TAP)

The MMC2107 provides a dedicated user-accessible test access port (TAP) that is fully compatible with the *IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture*. Problems associated with testing high-density circuit boards have led to development of this proposed standard under the sponsorship of the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The MMC2107 implementation supports circuit-board test strategies based on this standard.

The top-level TAP consists of five dedicated signal pins, a 16-state TAP controller, an instruction register, and three data registers, a boundary scan register for monitoring and controlling the device's external pins, a device identification register, and a 1-bit bypass (do nothing) register.

The top-level TAP provides the ability to:

1. Perform boundary scan (external pin) drive and monitor operations to test circuitry external to the MMC2107
2. Disable the MMC2107's output pins
3. Read the MMC2107's IDCODE device identification register

CAUTION: *Certain precautions must be observed to ensure that the top-level TAP module does not interfere with non-test operation. See* ***21.10 Non-Scan Chain Operation*** *for details.*

The MMC2107's top-level TAP module includes a TAP controller, a 4-bit instruction register, and three test data registers (a 1-bit bypass register, a 200-bit boundary scan register, and a 32-bit IDCODE register). The top-level tap controller and the low-level (OnCE) TAP controller share the external signals described here.

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21.3.1 Test Clock (TCLK)

TCLK is a test clock input to synchronize the test logic. TCLK is independent of the MMC2107 processor clock. It includes an internal pullup resistor.

21.3.2 Test Mode Select (TMS)

TMS is a test mode select input (with an internal pullup resistor) that is sampled on the rising edge of TCLK to sequence the TAP controller's state machine.

21.3.3 Test Data Input (TDI)

TDI is a serial test data input (with an internal pullup resistor) that is sampled on the rising edge of TCLK.

21.3.4 Test Data Output (TDO)

TDO is a three-state test data output that is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.

21.3.5 Test Reset ($\overline{\text{TRST}}$)

$\overline{\text{TRST}}$ is an active low asynchronous reset with an internal pullup resistor that forces the TAP controller into the test-logic-reset state.

21.3.6 Debug Event ($\overline{\text{DE}}$)

This is a bidirectional, active-low signal.

As an output, this signal will be asserted for three system clocks, synchronous to the rising CLKOUT edge, to acknowledge that the CPU has entered debug mode as a result of a debug request or a breakpoint condition.

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As an input, this signal provides multiple functions such as:

- The main function is a means of entering debug mode from an external command controller. This signal, when asserted, causes the CPU to finish the current instruction being executed, save the instruction pipeline information, enter debug mode, and wait for commands to be entered from the serial debug input line. This input must be asserted for at least three system clocks, sampled with the rising CLKOUT edge. This function is ignored during reset. While the processor is in debug mode, this signal is still sampled but has no effect until debug mode is exited.
- Another input function is to enable OnCE. This is an alternate method to the ENABLE_MCU_ONCE JTAG command to enable the OnCE logic to be accessible via the JTAG interface. This input signal must be asserted low (while in the test-logic-reset state with POR/$\overline{\text{TRST}}$ not asserted) for at least two TCLK rising edges. Once enabled, the OnCE will remain enabled until the next POR or $\overline{\text{TRST}}$ resets.
- Another input function is as a wake-up event from a low-power mode of operation. Asynchronously asserting this signal will cause the clock controller to restart. This signal must be held asserted until the M•CORE receives three valid rising edges on the system clock. Then the processor will exit the low-power mode and go into debug mode.

NOTE: *If used to enter debug mode, $\overline{DE}$ must be pulled negated before the processor exits debug mode to prevent a still low signal from being unintentionally recognized as another debug request. Also, asserting this signal to enter debug mode may prevent external logic from seeing the processor output acknowledgment since the external pullup may not be able to pull the signal negated before the handshake is asserted. Finally, if using this signal to enable OnCE outside of reset it may be seen as a request to enter debug mode.*

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21.4 Top-Level TAP Controller

The top-level TAP controller is responsible for interpreting the sequence of logical values on the TMS signal. It is a synchronous state machine that controls the operation of the JTAG logic. The machine's states are shown in **Figure 21-2**. The value shown adjacent to each arc represents the value of the TMS signal sampled on the rising edge of the TCLK signal.

The top-level TAP controller can be asynchronously reset to the test-logic-reset state by asserting TRST, test reset. As **Figure 21-2** shows, holding TMS high (to logic 1) while clocking TCLK through at least five rising edges will also cause the state machine to enter its test-logic-reset state.

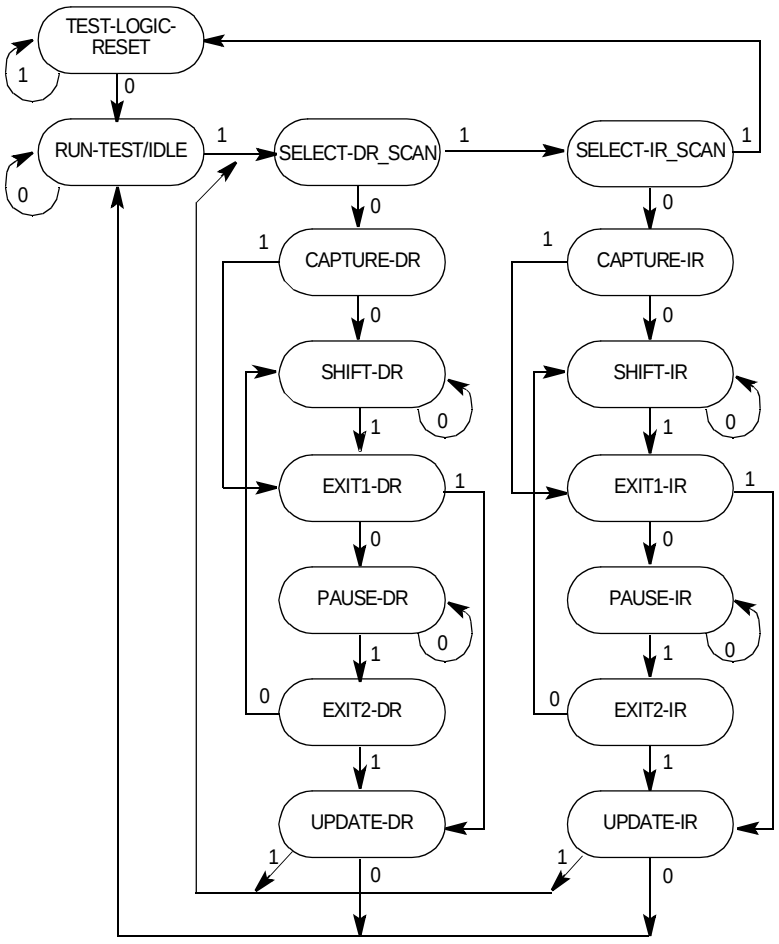

Figure 21-2. Top-Level TAP Controller State Machine

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21.5 Instruction Shift Register

The MMC2107 top-level TAP module uses a 4-bit instruction shift register with no parity. This register transfers its value to a parallel hold register and applies an instruction on the falling edge of TCLK when the TAP state machine is in the update-IR state. To load the instructions into the shift portion of the register, place the serial data on the TDI pin prior to each rising edge of TCLK. The MSB of the instruction shift register is the bit closest to the TDI pin and the LSB is the bit closest to the TDO pin.

Table 21-1 lists the instructions supported along with their opcodes, IR3–IR0. The last three instructions in the table are reserved for manufacturing purposes only.

Unused opcodes are currently decoded to perform the BYPASS operation, but Motorola reserves the right to change their decodings in the future.

21.5.1 EXTEST Instruction

The external test instruction (EXTEST) selects the boundary-scan register. The EXTEST instruction forces all output pins and bidirectional pins configured as outputs to the preloaded fixed values (with the SAMPLE/PRELOAD instruction) and held in the boundary-scan update registers. The EXTEST instruction can also configure the direction of bidirectional pins and establish high-impedance states on some pins. EXTEST also asserts internal reset for the MMC2107 system logic to force a predictable internal state while performing external boundary scan operations.

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Table 21-1. JTAG Instructions

Instruction	IR3–IR0	Instruction Summary
EXTEST	0000	Selects the boundary scan register while applying fixed values to output pins and asserting functional reset
IDCODE	0001	Selects IDCODE register for shift
SAMPLE/PRELOAD	0010	Selects the boundary scan register for shifting, sampling, and preloading without disturbing functional operation
ENABLE_MCU_ONCE	0011	Instruction to enable the M•CORE TAP controller
HIGHZ	1001	Selects the bypass register while three-stating all output pins and asserting functional reset
CLAMP	1100	Selects bypass while applying fixed values to output pins and asserting functional reset
BYPASS	1111	Selects the bypass register for data operations
Reserved	0100 0110	Instruction for chip manufacturing purposes only
Reserved	0101	Instruction for chip manufacturing purposes only(1)
Reserved	0111–1000 1101–1110 1010–1011	Decoded to select bypass register(2)

1. To exit this instruction, the $\overline{\text{TRST}}$ pin must be asserted or power-on reset.
2. Motorola reserves the right to change the decoding of the unused opcodes in the future.

21.5.2 IDCODE Instruction

The IDCODE instruction selects the 32-bit IDCODE register for connection as a shift path between the TDI pin and the TDO pin. This instruction allows interrogation of the MMC2107 to determine its version number and other part identification data. The IDCODE register has been implemented in accordance with the IEEE 1149.1 standard so that the least significant bit of the shift register stage is set to logic 1 on the rising edge of TCLK following entry into the capture-DR state. Therefore, the first bit to be shifted out after selecting the IDCODE register is always

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a logic 1. The remaining 31 bits are also set to fixed values on the rising edge of TCLK following entry into the capture-DR state.

IDCODE is the default instruction placed into the instruction register when the top-level TAP resets. Thus, after a TAP reset, the IDCODE (data) register will be selected automatically.

21.5.3 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction provides two separate functions.

First, it obtains a sample of the system data and control signals present at the MMC2107 input pins and just prior to the boundary scan cell at the output pins. This sampling occurs on the rising edge of TCLK in the capture-DR state when an instruction encoding of hex 2 is resident in the instruction register. The user can observe this sampled data by shifting it through the boundary scan register to the output TDO by using the shift-DR state. Both the data capture and the shift operation are transparent to system operation.

NOTE: *The user is responsible for providing some form of external synchronization to achieve meaningful results because there is no internal synchronization between TCLK and the system clock.*

The second function of the SAMPLE/PRELOAD instruction is to initialize the boundary scan register update cells before selecting EXTEST or CLAMP. This is achieved by ignoring the data being shifted out of the TDO pin while shifting in initialization data. The update-DR state in conjunction with the falling edge of TCLK can then transfer this data to the update cells. This data will be applied to the external output pins when EXTEST or CLAMP instruction is applied.

21.5.4 ENABLE_MCU_ONCE Instruction

The ENABLE_MCU_ONCE is a public instruction to enable the M•CORE OnCE TAP controller. When the OnCE TAP controller is enabled, the top-level TAP controller connects the internal OnCE TDO to the pin TDO and remains in the run-test/idle state. It will remain in this state until TRST is asserted. While the OnCE TAP controller is enabled, the top-level JTAG remains transparent.

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21.5.5 HIGHZ Instruction

The HIGHZ instruction is provided as a manufacturer's optional public instruction to prevent having to backdrive the output pins during circuit-board testing. When HIGHZ is invoked, all output drivers, including the 2-state drivers, are turned off (for example, high impedance). The instruction selects the bypass register. HIGHZ also asserts internal reset for the MMC2107 system logic to force a predictable internal state.

21.5.6 CLAMP Instruction

The CLAMP instruction selects the bypass register and asserts internal reset while simultaneously forcing all output pins and bidirectional pins configured as outputs to the fixed values that are preloaded and held in the boundary scan update register. This instruction enhances test efficiency by reducing the overall shift path to a single bit (the bypass register) while conducting an EXTEST type of instruction through the boundary scan register.

21.5.7 BYPASS Instruction

The BYPASS instruction selects the single-bit bypass register, creating a single-bit shift register path from the TDI pin to the bypass register to the TDO pin. This instruction enhances test efficiency by reducing the overall shift path when a device other than the MMC2107 processor becomes the device under test on a board design with multiple chips on the overall IEEE 1149.1 standard defined boundary scan chain. The bypass register has been implemented in accordance with IEEE 1149.1 standard so that the shift register state is set to logic 0 on the rising edge of TCLK following entry into the capture-DR state. Therefore, the first bit to be shifted out after selecting the bypass register is always a logic 0 (to differentiate a part that supports an IDCODE register from a part that supports only the bypass register).

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21.6 IDCODE Register

An IEEE 1149.1 standard compliant JTAG identification register (IDCODE) has been included on the MMC2107.

Bit 31	30	29	28	27	26	25	Bit 24
0	0	0	0	0	1	0	1
Bit 23	22	21	20	19	18	17	Bit 16
1	1	0	0	0	0	0	1
Bit 15	14	13	12	11	10	9	Bit 8
0	1	1	1	0	0	0	0
Bit 7	6	5	4	3	2	1	Bit 0
0	0	0	1	1	1	0	1

Figure 21-3. IDCODE Register Bit Specification

Bits 31–28 — Version Number (Part Revision Number)

This is equivalent to the lower four bits of the PRN of the chip identification register located in the chip configuration module.

Bits 27–22 — Design Center

Indicates the Motorola Microcontroller Division

Bits 21–12 — Device Number (Part Identification Number)

Bits 19-12 are equivalent to the PIN of the chip identification register located in the chip configuration module.

Bits 11–1 — JEDEC ID

Indicates the reduced JEDEC ID for Motorola. JEDEC refers to the Joint Electron Device Engineering Council. Refer to JEDEC publication 106-A and chapter 11 of the IEEE 1149.1 standard for further information on this field.

Bit 0

Differentiates this register as the JTAG IDCODE register (as opposed to the bypass register), according to the IEEE 1149.1 standard

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21.7 Bypass Register

The MMC2107 includes an IEEE 1149.1 standard-compliant bypass register, which creates a single bit shift register path from TDI to the bypass register to TDO when the BYPASS instruction is selected.

21.8 Boundary SCAN Register

MMC2107 includes an IEEE 1149.1 standard-compliant boundary-scan register. The boundary-scan register is connected between TDI and TDO when the EXTEST or SAMPLE/PRELOAD instructions are selected. This register captures signal pin data on the input pins, forces fixed values on the output signal pins, and selects the direction and drive characteristics (a logic value or high impedance) of the bidirectional and three-state signal pins.

21.9 Restrictions

The test logic is implemented using static logic design, and TCLK can be stopped in either a high or low state without loss of data. The system logic, however, operates on a different system clock which is not synchronized to TCLK internally. Any mixed operation requiring the use of the IEEE 1149.1 standard test logic, in conjunction with system functional logic that uses both clocks, must have coordination and synchronization of these clocks done externally.

The control afforded by the output enable signals using the boundary scan register and the EXTEST instruction requires a compatible circuit-board test environment to avoid device-destructive configurations. The user must avoid situations in which MMC2107 output drivers are enabled into actively driven networks.

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MMC2107 features a low-power stop mode. The interaction of the scan chain interface with low-power stop mode is:

1. The TAP controller must be in the test-logic-reset state to either enter or remain in the low-power stop mode. Leaving the test-logic-reset state negates the ability to achieve low-power, but does not otherwise affect device functionality.
2. The TCLK input is not blocked in low-power stop mode. To consume minimal power, the TCLK input should be externally connected to V_{DD}.
3. The TMS, TDI, $\overline{\text{TRST}}$ pins include on-chip pullup resistors. In low-power stop mode, these three pins should remain either unconnected or connected to V_{DD} to achieve minimal power consumption.

21.10 Non-Scan Chain Operation

Keeping the TAP controller in the test-logic-reset state will ensure that the scan chain test logic is kept transparent to the system logic. It is recommended that TMS, TDI, TCLK, and $\overline{\text{TRST}}$ be pulled up. $\overline{\text{TRST}}$ could be connected to ground. However, since there is a pullup on $\overline{\text{TRST}}$, some amount of current will result. JTAG will be initialized to the test-logic-reset state on power-up without $\overline{\text{TRST}}$ asserted low due to the JTAG power-on-reset internal input. The low-level TAP module in the M•CORE also has the power-on-reset input.

21.11 Boundary Scan

The MMC2107 boundary-scan register contains 200 bits. This register can be connected between TDI and TDO when EXTEST or SAMPLE/PRELOAD instructions are selected. This register is used for capturing signal pin data on the input pins, forcing fixed values on the output signal pins, and selecting the direction and drive characteristics (a logic value or high impedance) of the bidirectional and three-state signal pins.

This IEEE 1149.1 standard-compliant boundary-scan register contains bits for bonded-out and non-bonded signals excluding JTAG signals, analog signals, power supplies, compliance enable pins, and clock

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signals.To maintain JTAG compliance, TEST should be held to logic 0 and $\overline{DE}$ should be held to logic 1. These non-scanned pins are shown in **Table 21-2**.

Table 21-2. List of Pins Not Scanned in JTAG Mode

Pin Name	Pin Type
EXTAL	Clock/analog
XTAL	Clock/analog
V_{DDSYN}	Supply
V_{SSSYN}	Supply
PQA4–PQA3 and PQA1–PQA0	Analog
PQB3–PQB0	Analog
V_{RH}	Supply
V_{RL}	Supply
V_{DDA}	Supply
V_{SSA}	Supply
V_{DDH}	Supply
$\overline{TRST}$	JTAG
TCLK	JTAG
TMS	JTAG
TDI	JTAG
TDO	JTAG
DE	JTAG compliance enable
TEST	JTAG compliance enable
V_{pp}	Supply
V_{DDF}	Supply
V_{SSF}	Supply
V_{STBY}	Supply
V_{DD}	Supply
V_{SS}	Supply

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Table 21-3 defines the boundary-scan register.

- The first column shows bit numbers assigned to each of the register's cells. The bit nearest to TDO (the first to be shifted in) is defined as bit 0.
- The second column lists the logical state bit for each MMC2107 pin alternately with the read/write direction control bit for that pin. The logic state bits are non-inverting with respect to their associated pins, so that a 1 logical state bit equates to a logical high voltage on its corresponding pin. A direction control bit value of 1 causes a pin's logical state to be expressed by its logic state bit, a read of a pin. A direction control bit value of 0 causes a pin's logical voltage to follow the state of its logical state bit, a write to a pin.

Table 21-3. Boundary-Scan Register Definition (Sheet 1 of 4)

(Note: Shaded regions indicate optional pins)

Bit	Logical State and Direction Control Bits for Each Pin
0	D31 logical state
1	D31 direction control
2	A12 logical state
3	A12 direction control
4	A13 logical state
5	A13 direction control
6	A14 logical state
7	A14 direction control
8	A15 logical state
9	A15 direction control
10	A16 logical state
11	A16 direction control
12	A17 logical state
13	A17 direction control
14	CLKOUT logical state
15	CLKOUT direction control
16	A18 logical state

Bit	Logical State and Direction Control Bits for Each Pin
17	A18 direction control
18	A19 logical state
19	A19 direction control
20	$\overline{\text{RSTOUT}}$ logical state
21	$\overline{\text{RSTOUT}}$ direction control
22	A20 logical state
23	A20 direction control
24	$\overline{\text{RESET}}$ logical state
25	$\overline{\text{RESET}}$ direction control
26	A21 logical state
27	A21 direction control
28	A22 logical state
29	A22 direction control
30	$\overline{\text{TEA}}$ logical state
31	$\overline{\text{TEA}}$ direction control
32	$\overline{\text{EB0}}$ logical state
33	$\overline{\text{EB0}}$ direction control

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Table 21-3. Boundary-Scan Register Definition (Sheet 2 of 4)

(Note: Shaded regions indicate optional pins)

Bit	Logical State and Direction Control Bits for Each Pin
34	$\overline{\text{EB1}}$ logical state
35	$\overline{\text{EB1}}$ direction control
36	$\overline{\text{TA}}$ logical state
37	$\overline{\text{TA}}$ direction control
38	$\overline{\text{EB2}}$ logical state
39	$\overline{\text{EB2}}$ direction control
40	$\overline{\text{SHS}}$ logical state
41	$\overline{\text{SHS}}$ direction control
42	$\overline{\text{EB3}}$ logical state
43	$\overline{\text{EB3}}$ direction control
44	$\overline{\text{OE}}$ logical state
45	$\overline{\text{OE}}$ direction control
46	$\overline{\text{SS}}$ logical state
47	$\overline{\text{SS}}$ direction control
48	SCK logical state
49	SCK direction control
50	MISO logical state
51	MISO direction control
52	MOSI logical state
53	MOSI direction control
54	$\overline{\text{INT7}}$ logical state
55	$\overline{\text{INT7}}$ direction control
56	$\overline{\text{INT6}}$ logical state
57	$\overline{\text{INT6}}$ direction control
58	$\overline{\text{CS0}}$ logical state
59	$\overline{\text{CS0}}$ direction control
60	$\overline{\text{CS1}}$ logical state
61	$\overline{\text{CS1}}$ direction control
62	$\overline{\text{INT5}}$ logical state
63	$\overline{\text{INT5}}$ direction control

Bit	Logical State and Direction Control Bits for Each Pin
64	$\overline{\text{CS2}}$ logical state
65	$\overline{\text{CS2}}$ direction control
66	$\overline{\text{INT4}}$ logical state
67	$\overline{\text{INT4}}$ direction control
68	$\overline{\text{CS3}}$ logical state
69	$\overline{\text{CS3}}$ direction control
70	TC0 logical state
71	TC0 direction control
72	$\overline{\text{INT3}}$ logical state
73	$\overline{\text{INT3}}$ direction control
74	TC1 logical state
75	TC1 direction control
76	$\overline{\text{INT2}}$ logical state
77	$\overline{\text{INT2}}$ direction control
78	$\overline{\text{INT1}}$ logical state
79	$\overline{\text{INT1}}$ direction control
80	$\overline{\text{INT0}}$ logical state
81	$\overline{\text{INT0}}$ direction control
82	RXD1 logical state
83	RXD1 direction control
84	TXD1 logical state
85	TXD1 direction control
86	RXD2 logical state
87	RXD2 direction control
88	TC2 logical state
89	TC2 direction control
90	TXD2 logical state
91	TXD2 direction control
92	CSE0 logical state
93	CSE0 direction control

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Table 21-3. Boundary-Scan Register Definition (Sheet 3 of 4)

(Note: Shaded regions indicate optional pins)

Bit	Logical State and Direction Control Bits for Each Pin
94	ICOC1_0 logical state
95	ICOC1_0 direction control
96	$\overline{CSE1}$ logical state
97	$\overline{CSE1}$ direction control
98	R/$\overline{W}$ logical state
99	R/$\overline{W}$ direction control
100	ICOC1_1 logical state
101	ICOC1_1 direction control
102	ICOC1_2 logical state
103	ICOC1_2 direction control
104	ICOC1_3 logical state
105	ICOC1_3 direction control
106	ICOC2_0 logical state
107	ICOC2_0 direction control
108	ICOC2_1 logical state
109	ICOC2_1 direction control
110	ICOC2_2 logical state
111	ICOC2_2 direction control
112	ICOC2_3 logical state
113	ICOC2_3 direction control
114	D0 logical state
115	D0 direction control
116	A0 logical state
117	A0 direction control
118	A1 logical state
119	A1 direction control
120	D1 logical state
121	D1 direction control
122	A2 logical state
123	A2 direction control

Bit	Logical State and Direction Control Bits for Each Pin
124	D2 logical state
125	D2 direction control
126	D3 logical state
127	D3 direction control
128	D4 logical state
129	D4 direction control
130	D5 logical state
131	D5 direction control
132	D6 logical state
133	D6 direction control
134	D7 logical state
135	D7 direction control
136	D8 logical state
137	D8 direction control
138	D9 logical state
139	D9 direction control
140	D10 logical state
141	D10 direction control
142	D11 logical state
143	D11 direction control
144	D12 logical state
145	D12 direction control
146	D13 logical state
147	D13 direction control
148	D14 logical state
149	D14 direction control
150	A3 logical state
151	A3 direction control
152	A4 logical state
153	A4 direction control

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Table 21-3. Boundary-Scan Register Definition (Sheet 4 of 4)

(Note: Shaded regions indicate optional pins)

Bit	Logical State and Direction Control Bits for Each Pin
154	D15 logical state
155	D15 direction control
156	A5 logical state
157	A5 direction control
158	D16 logical state
159	D16 direction control
160	A6 logical state
161	A6 direction control
162	A7 logical state
163	A7 direction control
164	D17 logical state
165	D17 direction control
166	D18 logical state
167	D18 direction control
168	D19 logical state
169	D19 direction control
170	D20 logical state
171	D20 direction control
172	D21 logical state
173	D21 direction control
174	D22 logical state
175	D22 direction control
176	A8 logical state
177	A8 direction control
178	A9 logical state
179	A9 direction control
180	D23 logical state
181	D23 direction control
182	A10 logical state
183	A10 direction control
184	D24 logical state
185	D24 direction control
186	D25 logical state
187	D25 direction control
188	A11 logical state
189	A11 direction control
190	D26 logical state
191	D16 direction control
192	D27 logical state
193	D27 direction control
194	D28 logical state
195	D28 direction control
196	D29 logical state
197	D29 direction control
198	D30 logical state
199	D30 direction control

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21.12 Low-Level TAP (OnCE) Module

The low-level TAP (OnCE, on-chip emulation) circuitry provides a simple, inexpensive debugging interface that allows external access to the processor's internal registers and to memory/peripherals. OnCE capabilities are controlled through a serial interface, mapped onto a JTAG test access port (TAP) protocol.

Refer to **Figure 21-4** for a block diagram of the OnCE.

NOTE: *The interface to the OnCE controller and its resources is based on the TAP defined for JTAG in the IEEE 1149.1 standard.*

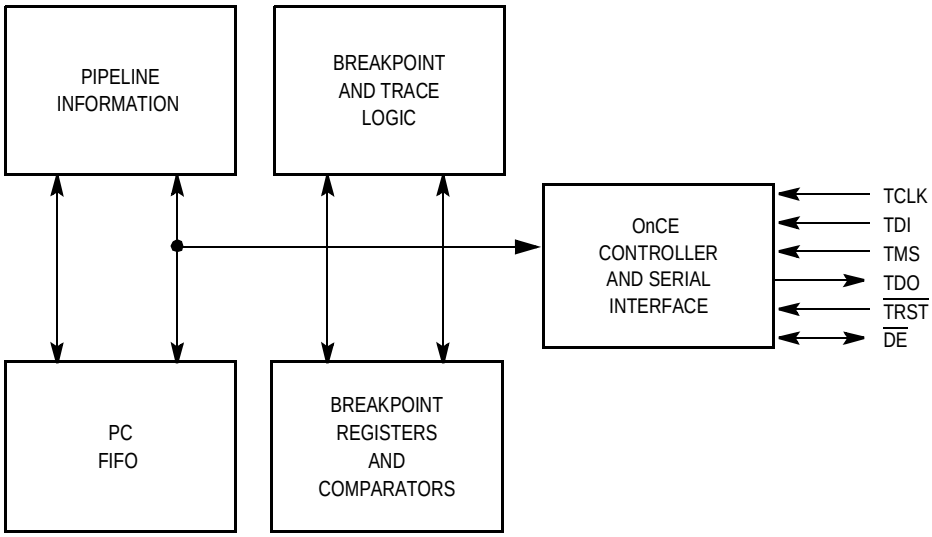

Figure 21-4. OnCE Block Diagram

Figure 21-5 shows the OnCE (low-level TAP module) data registers in the MMC2107.

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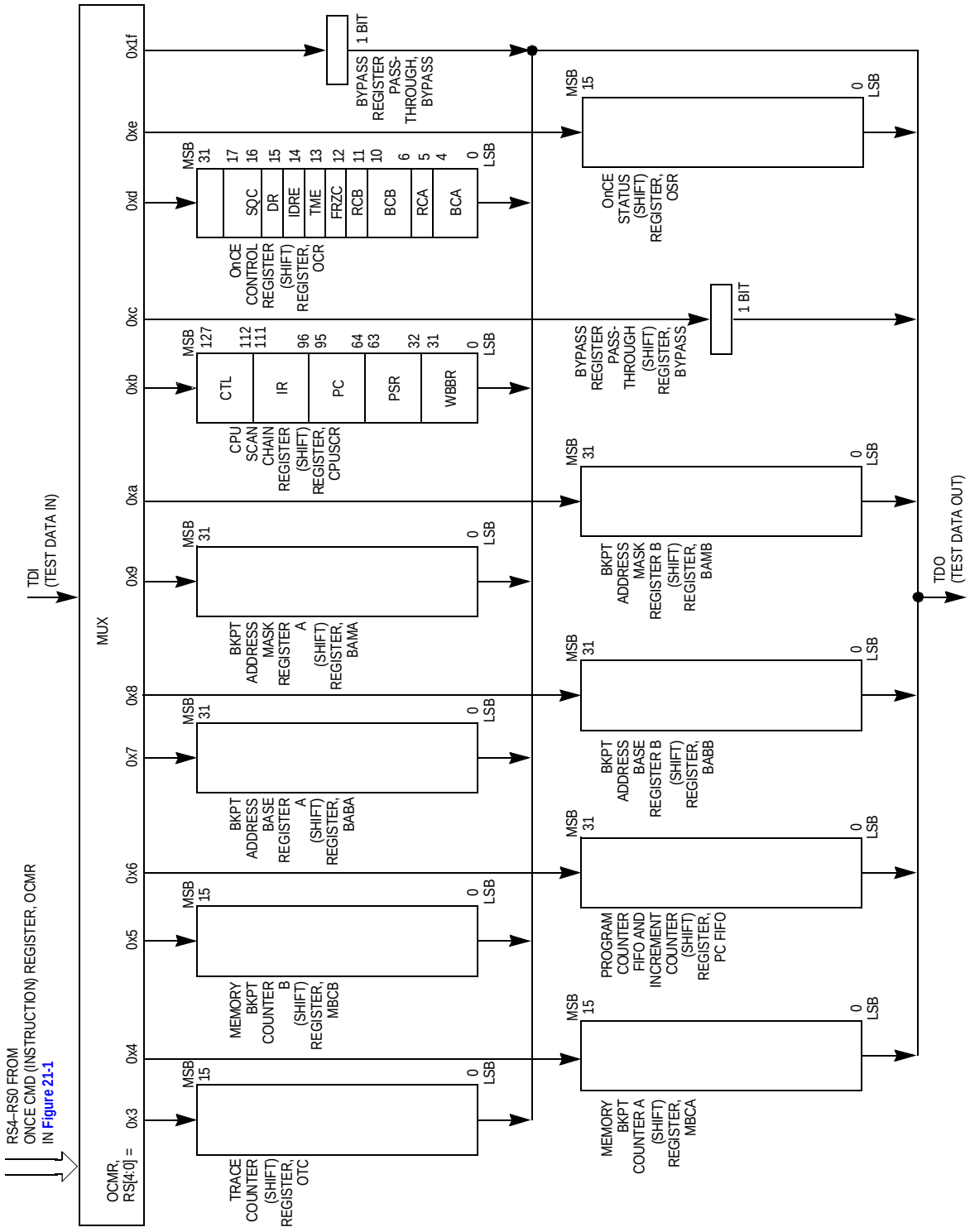

Figure 21-5. Low-Level (OnCE) Tap Module Data Registers (DRs)

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21.13 Signal Descriptions

The OnCE pin interface is used to transfer OnCE instructions and data to the OnCE control block. Depending on the particular resource being accessed, the CPU may need to be placed in debug mode. For resources outside of the CPU block and contained in the OnCE block, the processor is not disturbed and may continue execution. If a processor resource is required, the OnCE controller may assert a debug request ($\overline{\text{DBGRQ}}$) to the CPU. This causes the CPU to finish the instruction being executed, save the instruction pipeline information, enter debug mode, and wait for further commands. Asserting $\overline{\text{DBGRQ}}$ causes the device to exit stop, doze, or wait mode.

21.13.1 Debug Serial Input (TDI)

Data and commands are provided to the OnCE controller through the TDI pin. Data is latched on the rising edge of the TCLK serial clock. Data is shifted into the OnCE serial port least significant bit (LSB) first.

21.13.2 Debug Serial Clock (TCLK)

The TCLK pin supplies the serial clock to the OnCE control block. The serial clock provides pulses required to shift data and commands into and out of the OnCE serial port. (Data is clocked into the OnCE on the rising edge and is clocked out of the OnCE serial port on the falling edge.) The debug serial clock frequency must be no greater than 50 percent of the processor clock frequency.

21.13.3 Debug Serial Output (TDO)

Serial data is read from the OnCE block through the TDO pin. Data is always shifted out the OnCE serial port LSB first. Data is clocked out of the OnCE serial port on the falling edge of TCLK. TDO is three-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.

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21.13.4 Debug Mode Select (TMS)

The TMS input is used to cycle through states in the OnCE debug controller. Toggling the TMS pin while clocking with TCLK controls the transitions through the TAP state controller.

21.13.5 Test Reset ($\overline{\text{TRST}}$)

The $\overline{\text{TRST}}$ input is used to reset the OnCE controller externally by placing the OnCE control logic in a test logic reset state. OnCE operation is disabled in the reset controller and reserved states.

21.13.6 Debug Event ($\overline{\text{DE}}$)

The $\overline{\text{DE}}$ pin is a bidirectional open drain pin. As an input, $\overline{\text{DE}}$ provides a fast means of entering debug mode from an external command controller. As an output, this pin provides a fast means of acknowledging debug mode entry to an external command controller.

The assertion of this pin by a command controller causes the CPU to finish the current instruction being executed, save the instruction pipeline information, enter debug mode, and wait for commands to be entered from the TDI line. If $\overline{\text{DE}}$ was used to enter debug mode, then $\overline{\text{DE}}$ must be negated after the OnCE responds with an acknowledgment and before sending the first OnCE command.

The assertion of this pin by the CPU acknowledges that it has entered debug mode and is waiting for commands to be entered from the TDI line.

21.14 Functional Description

The on-chip emulation (OnCE) circuitry provides a simple, inexpensive debugging interface that allows external access to the processor's internal registers and to memory/peripherals. OnCE capabilities are controlled through a serial interface, mapped onto a JTAG test access port (TAP) protocol. **Figure 21-6** shows the components of the OnCE circuitry.

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The interface to the OnCE controller and its resources are based on the TAP defined for JTAG in the IEEE 1149.1 standard.

21.14.1 Operation

An instruction is scanned into the OnCE module through the serial interface and then decoded. Data may then be scanned in and used to update a register or resource on a write to the resource, or data associated with a resource may be scanned out for a read of the resource.

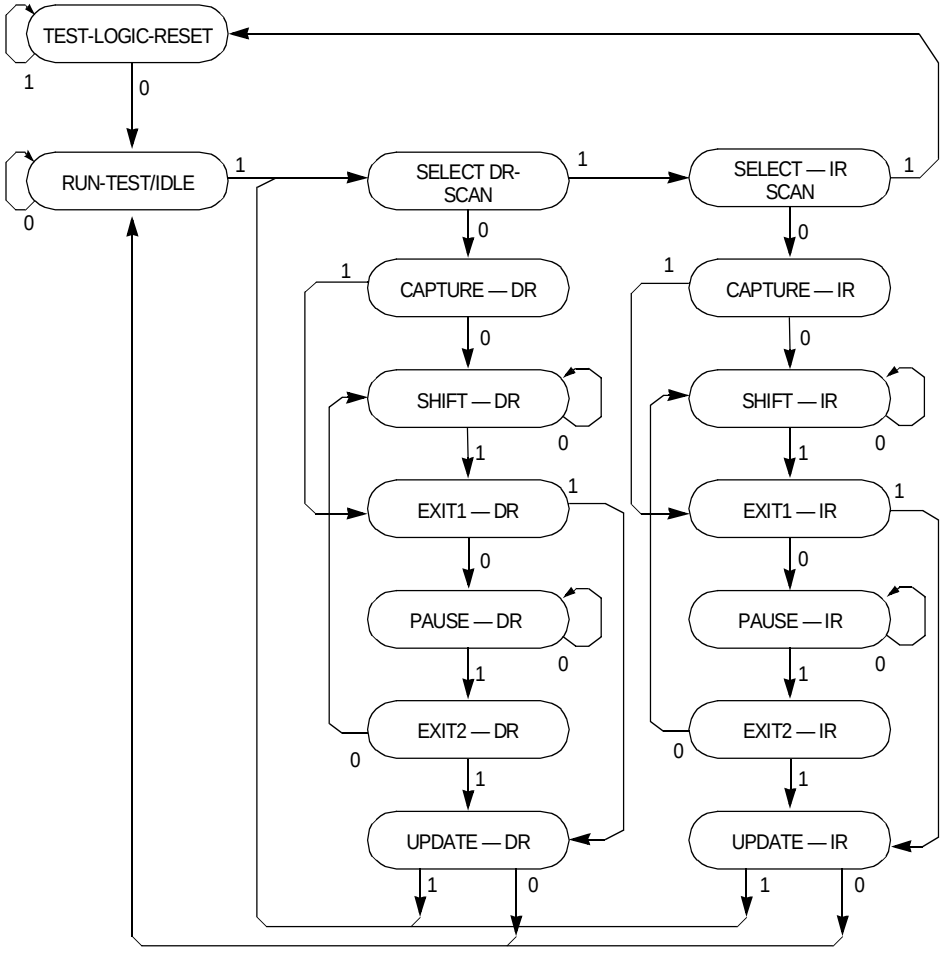

Figure 21-6. OnCE Controller

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For accesses to the CPU internal state, the OnCE controller requests the CPU to enter debug mode via the CPU DBGRQ input. Once the CPU enters debug mode, as indicated by the OnCE status register, the processor state may be accessed through the CPU scan register.

The OnCE controller is implemented as a 16-state finite state machine, with a one-to-one correspondence to the states defined for the JTAG TAP controller.

CPU registers and the contents of memory locations are accessed by scanning instructions and data into and out of the CPU scan chain. Required data is accessed by executing the scanned instructions. Memory locations may be read by scanning in a load instruction to the CPU that references the desired memory location, executing the load instruction, and then scanning out the result of the load. Other resources are accessed in a similar manner.

Resources contained in the OnCE module that do not require the CPU to be halted for access may be controlled while the CPU is executing and do not interfere with normal processor execution. Accesses to certain resources, such as the PC FIFO and the count registers, while not part of the CPU, may require the CPU to be stopped to allow access to avoid synchronization hazards. If it is known that the CPU clock is enabled and running no slower than the TCLK input, there is sufficient synchronization performed to allow reads but not writes of these specific resources. Debug firmware may ensure that it is safe to access these resources by reading the OSR to determine the state of the CPU prior to access. All other cases require the CPU to be in the debug state for deterministic operation.

21.14.2 OnCE Controller and Serial Interface

Figure 21-7 is a block diagram of the OnCE controller and serial interface.

The OnCE command register acts as the instruction register (IR) for the TAP controller. All other OnCE resources are treated as data registers (DR) by the TAP controller. The command register is loaded by serially shifting in commands during the TAP controller shift-IR state, and is loaded during the update-IR state. The command register selects a

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OnCE resource to be accessed as a DR during the TAP controller capture-DR, shift-DR and update-DR states.

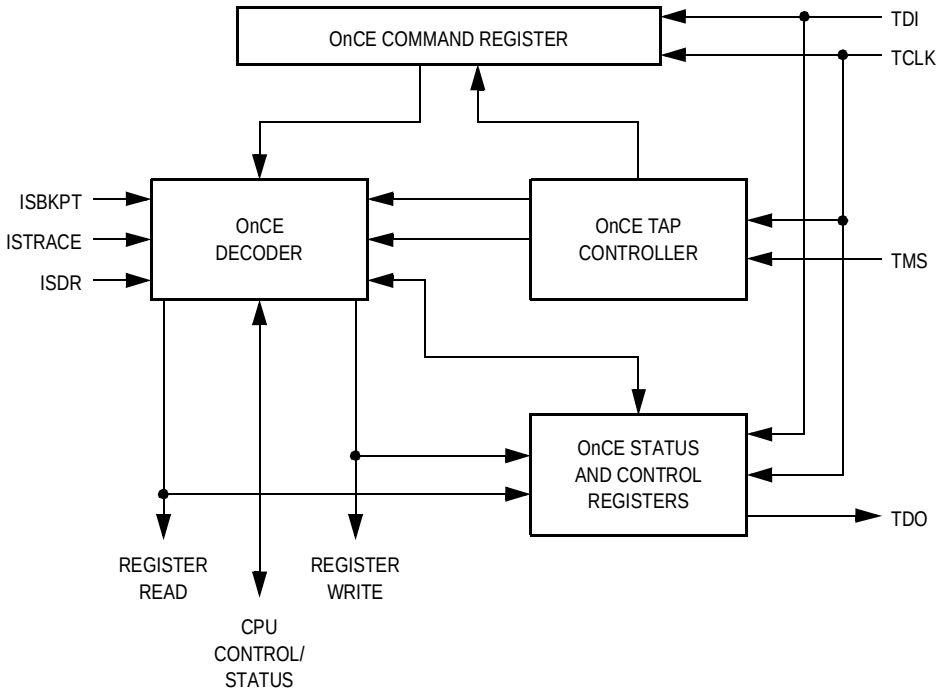

Figure 21-7. OnCE Controller and Serial Interface

21.14.3 OnCE Interface Signals

The following paragraphs describe the OnCE interface signals to other internal blocks associated with the OnCE controller. These signals are not available externally, and descriptions are provided to improve understanding of OnCE operation.

21.14.3.1 Internal Debug Request Input ($\overline{IDR}$)

The internal debug request input is a hardware signal which is used in some implementations to force an immediate debug request to the CPU. If present and enabled, it functions in an identical manner to the control function provided by the DR control bit in the OCR. This input is maskable by a control bit in the OCR.

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21.14.3.2 CPU Debug Request (DBGRQ)

The DBGRQ signal is asserted by the OnCE control logic to request the CPU to enter the debug state. It may be asserted for a number of different conditions. Assertion of this signal causes the CPU to finish the current instruction being executed, save the instruction pipeline information, enter debug mode, and wait for further commands. Asserting DBGRQ causes the device to exit stop, doze, or wait mode.

21.14.3.3 CPU Debug Acknowledge (DBGACK)

The CPU asserts the DBGACK signal upon entering the debug state. This signal is part of the handshake mechanism between the OnCE control logic and the CPU.

21.14.3.4 CPU Breakpoint Request (BRKRQ)

The BRKRQ signal is asserted by the OnCE control logic to signal that a breakpoint condition has occurred for the current CPU bus access.

21.14.3.5 CPU Address, Attributes (ADDR, ATTR)

The CPU address and attribute information may be used in the memory breakpoint logic to qualify memory breakpoints with access address and cycle type information.

21.14.3.6 CPU Status (PSTAT)

The trace logic uses the PSTAT signals to qualify trace count decrements with specific CPU activity.

21.14.3.7 OnCE Debug Output (DEBUG)

The DEBUG signal is used to indicate to on-chip resources that a debug session is in progress. Peripherals and other units may use this signal to modify normal operation for the duration of a debug session. This may involve the CPU executing a sequence of instructions solely for the purpose of visibility/system control. These instructions are not part of the normal instruction stream that the CPU would have executed had it not been placed in debug mode.

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This signal is asserted the first time the CPU enters the debug state and remains asserted until the CPU is released by a write to the OnCE command register with the GO and EX bits set, and a register specified as either no register selected or the CPUSCR. This signal remains asserted even though the CPU may enter and exit the debug state for each instruction executed under control of the OnCE controller.

21.14.4 OnCE Controller Registers

This section describes the OnCE controller registers:

- OnCE command register (OCMR)
- OnCE control register (OCR)
- OnCE status register (OSR)

All OnCE registers are addressed by means of the RS field in the OCMR, as shown in **Table 21-4**.

21.14.4.1 OnCE Command Register

The OnCE command register (OCMR) is an 8-bit shift register that receives its serial data from the TDI pin. This register corresponds to the JTAG IR and is loaded when the update-IR TAP controller state is entered. It holds the 8-bit commands shifted in during the shift-IR controller state to be used as input for the OnCE decoder. The OCMR contains fields for controlling access to a OnCE resource, as well as controlling single-step operation, and exit from OnCE mode.

Although the OCMR is updated during the update-IR TAP controller state, the corresponding resource is accessed in the DR scan sequence of the TAP controller, and as such, the update-DR state must be transitioned through in order for an access to occur. In addition, the update-DR state must also be transitioned through in order for the single-step and/or exit functionality to be performed, even though the command appears to have no data resource requirement associated with it.

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Bit 7	6	5	4	3	2	1	Bit 0
R/W	G	EX	RS4	RS3	RS2	RS1	RS0

Figure 21-8. OnCE Command Register (OCMR)

R/W — Read/Write Bit

1 = Read the data in the register specified by the RS field.
0 = Write the data associated with the command into the register specified by the RS field.

GO — Go Bit

When the GO bit is set, the device executes the instruction in the IR register in the CPUSCR. To execute the instruction, the processor leaves debug mode, executes the instruction, and if the EX bit is cleared, returns to debug mode immediately after executing the instruction. The processor resumes normal operation if the EX bit is set. The GO command is executed only if the operation is a read/write to either the CPUSCR or to “no register selected.” Otherwise, the GO bit has no effect. The processor leaves debug mode after the TAP controller update-DR state is entered.

1 = Execute instruction in IR
0 = Inactive (no action taken)

EX — Exit Bit

When the EX bit is set, the processor leaves debug mode and resumes normal operation until another debug request is generated. The exit command is executed only if the GO bit is set and the operation is a read/write to the CPUSCR or a read/write to “no register selected.” Otherwise, the EX bit has no effect. The processor exits debug mode after the TAP controller update-DR state is entered.

1 = Leave debug mode
0 = Remain in debug mode

RS4–RS0 — Register Select Field

The RS field defines the source for the read operation or the destination for the write operation. **Table 21-4** shows OnCE register addresses.

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Table 21-4. OnCE Register Addressing

RS4–RS0	Register Selected
00000	Reserved
00001	Reserved
00010	Reserved
00011	OTC — OnCE trace counter
00100	MBCA — memory breakpoint counter A
00101	MBCB — memory breakpoint counter B
00110	PC FIFO — program counter FIFO and increment counter
00111	BABA — breakpoint address base register A
01000	BABB — breakpoint address base register B
01001	BAMA — breakpoint address mask register A
01010	BAMB — breakpoint address mask register B
01011	CPUSCR — CPU scan chain register
01100	Bypass — no register selected
01101	OCR — OnCE control register
01110	OSR — OnCE status register
01111	Reserved (factory test control register — do not access)
10000	Reserved (MEM_BIST — do not access)
10001–10110	Reserved (bypass, do not access)
10111	Reserved (LSRL, do not access)
11000–11110	Reserved (bypass, do not access)
11111	Bypass

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21.14.4.2 OnCE Control Register

The 32-bit OnCE control register (OCR) selects the events that put the device in debug mode and enables or disables sections of the OnCE logic.

	Bit 31	30	29	28	27	26	25	Bit 24
Read:	0	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 23	22	21	20	19	18	17	Bit 16
Read:	0	0	0	0	0	0	SQC1	SQC0
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	DR	IDRE	TME	FRZC	RCB	BCB4	BCB3	BCB2
Write:								
Reset:	0	0	0	0	0	0	0	0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BCB1	BCB0	RCA	BCA4	BCA3	BCA2	BCA1	BCA0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or reserved

Figure 21-9. OnCE Control Register (OCR)

SQC1 and SQC0 — Sequential Control Field

The SQC field allows memory breakpoint B and trace occurrences to be suspended until a qualifying event occurs. Test logic reset clears the SQC field. See **Table 21-5**.

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Table 21-5. Sequential Control Field Settings

SQC1 and SQC0	Meaning
00	Disable sequential control operation. Memory breakpoints and trace operation are unaffected by this field.
01	Suspend normal trace counter operation until a breakpoint condition occurs for memory breakpoint B. In this mode, memory breakpoint B occurrences no longer cause breakpoint requests to be generated. Instead, trace counter comparisons are suspended until the first memory breakpoint B occurrence. After the first memory breakpoint B occurrence, trace counter control is released to perform normally, assuming TME is set. This allows a sequence of breakpoint conditions to be specified prior to trace counting.
10	Qualify memory breakpoint B matches with a breakpoint occurrence for memory breakpoint A. In this mode, memory breakpoint A occurrences no longer cause breakpoint requests to be generated. Instead, memory breakpoint B comparisons are suspended until the first memory breakpoint A occurrence. After the first memory breakpoint A occurrence, memory breakpoint B is enabled to perform normally. This allows a sequence of breakpoint conditions to be specified.
11	Combine the 01 and 10 qualifications. In this mode, no breakpoint requests are generated, and trace count operation is enabled once a memory breakpoint B occurrence follows a memory breakpoint A occurrence if TME is set.

DR — Debug Request Bit

DR requests the CPU to enter debug mode unconditionally. The PM bits in the OnCE status register indicate that the CPU is in debug mode. Once the CPU enters debug mode, it returns there even with a write to the OCMR with GO and EX set until the DR bit is cleared. Test logic reset clears the DR bit.

IDRE — Internal Debug Request Enable Bit

The internal debug request ($\overline{\text{IDR}}$) input to the OnCE control logic may not be used in all implementations. In some implementations, the $\overline{\text{IDR}}$ control input may be connected and used as an additional hardware debug request. Test logic reset clears the IDRE bit.

1 = $\overline{\text{IDR}}$ input enabled
0 = $\overline{\text{IDR}}$ input disabled

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TME — Trace Mode Enable Bit

TME enables trace operation. Test logic reset clears the TME bit. Trace operation is also affected by the SQC field.

1 = Trace operation enabled
0 = Trace operation disabled

FRZC — Freeze Control Bit

This control bit is used in conjunction with memory breakpoint B registers to select between asserting a breakpoint condition when a memory breakpoint B occurs or freezing the PC FIFO from further updates when memory breakpoint B occurs while allowing the CPU to continue execution. The PC FIFO remains frozen until the FRZO bit in the OSR is cleared.

1 = Memory breakpoint B occurrence freezes PC FIFO and does not assert breakpoint condition.
0 = Memory breakpoint B occurrence asserts breakpoint condition.

RCB and RCA — Memory Breakpoint B and A Range Control Bits

RCB and RDA condition enabled memory breakpoint occurrences happen when memory breakpoint matches are either within or outside the range defined by memory base address and mask.

1 = Condition breakpoint on access outside of range
0 = Condition breakpoint on access within range

BCB4–BCB0 and BCA4–BCA0 — Memory Breakpoint B and A Control Fields

The BCB and BCA fields enable memory breakpoints and qualify the access attributes to select whether the breakpoint matches are recognized for read, write, or instruction fetch (program space) accesses. Test logic reset clears BCB4–BCB0 and BCA4–BCA0.

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Table 21-6. Memory Breakpoint Control Field Settings

BCB4–BCB0 BCA4–BCA0	Description
00000	Breakpoint disabled
00001	Qualify match with any access
00010	Qualify match with any instruction access
00011	Qualify match with any data access
00100	Qualify match with any change of flow instruction access
00101	Qualify match with any data write
00110	Qualify match with any data read
00111	Reserved
01XXX	Reserved
10000	Reserved
10001	Qualify match with any user access
10010	Qualify match with any user instruction access
10011	Qualify match with any user data access
10100	Qualify match with any user change of flow access
10101	Qualify match with any user data write
10110	Qualify match with any user data read
10111	Reserved
11000	Reserved
11001	Qualify match with any supervisor access
11010	Qualify match with any supervisor instruction access
11011	Qualify match with any supervisor data access
11100	Qualify match with any supervisor change of flow access
11101	Qualify match with any supervisor data write
11110	Qualify match with any supervisor data read
11111	Reserved

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21.14.4.3 OnCE Status Register

The 16-bit OnCE status register (OSR) indicates the reason(s) that debug mode was entered and the current operating mode of the CPU.

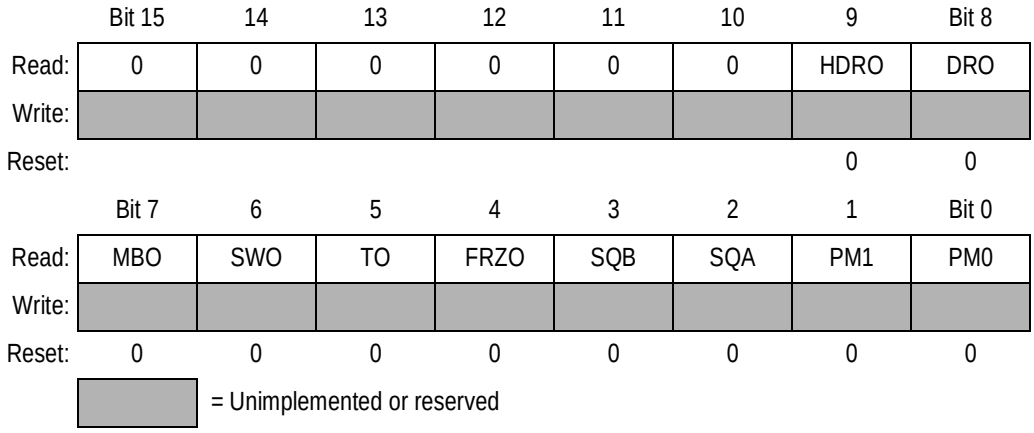

Figure 21-10. OnCE Status Register (OSR)

HDRO — Hardware Debug Request Occurrence Flag

HDRO is set when the processor enters debug mode as a result of a hardware debug request from the IDR signal or the DE pin. This bit is cleared on test logic reset or when debug mode is exited with the GO and EX bits set.

DRO — Debug Request Occurrence Flag

DRO is set when the processor enters debug mode and the debug request (DR) control bit in the OnCE control register is set. This bit is cleared on test logic reset or when debug mode is exited with the GO and EX bits set.

MBO — Memory Breakpoint Occurrence Flag

MBO is set when a memory breakpoint request has been issued to the CPU via the BRKRQ input and the CPU enters debug mode. In some situations involving breakpoint requests on instruction prefetches, the CPU may discard the request along with the prefetch. In this case, this bit may become set due to the CPU entering debug mode for another reason. This bit is cleared on test logic reset or when debug mode is exited with the GO and EX bits set.

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SWO — Software Debug Occurrence Flag

SWO bit is set when the processor enters debug mode of operation as a result of the execution of the BKPT instruction. This bit is cleared on test logic reset or when debug mode is exited with the GO and EX bits set.

TO — Trace Count Occurrence Flag

TO is set when the trace counter reaches zero with the trace mode enabled and the CPU enters debug mode. This bit is cleared on test logic reset or when debug mode is exited with the GO and EX bits set.

FRZO — FIFO Freeze Occurrence Flag

FRZO is set when a FIFO freeze occurs. This bit is cleared on test logic reset or when debug mode is exited with the GO and EX bits set.

SQB — Sequential Breakpoint B Arm Occurrence Flag

SQB is set when sequential operation is enabled and a memory breakpoint B event has occurred to enable trace counter operation. This bit is cleared on test logic reset or when debug mode is exited with the GO and EX bits set.

SQA — Sequential Breakpoint A Arm Occurrence Flag

SQA is set when sequential operation is enabled and a memory breakpoint A event has occurred to enable memory breakpoint B operation. This bit is cleared on test logic reset or when debug mode is exited with the GO and EX bits set.

PM1 and PM0 — Processor Mode Field

These flags reflect the processor operating mode. They allow coordination of the OnCE controller with the CPU for synchronization.

Table 21-7. Processor Mode Field Settings

PM1 and PM0	Meaning
00	Processor in normal mode
01	Processor in stop, doze, or wait mode
10	Processor in debug mode
11	Reserved

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21.14.5 OnCE Decoder (ODEC)

The ODEC receives as input the 8-bit command from the OCMR and status signals from the processor. The ODEC generates all the strobes required for reading and writing the selected OnCE registers.

21.14.6 Memory Breakpoint Logic

Memory breakpoints can be set for a particular memory location or on accesses within an address range. The breakpoint logic contains an input latch for addresses, registers that store the base address and address mask, comparators, attribute qualifiers, and a breakpoint counter. **Figure 21-11** illustrates the basic functionality of the OnCE memory breakpoint logic. This logic is duplicated to provide two independent breakpoint resources.

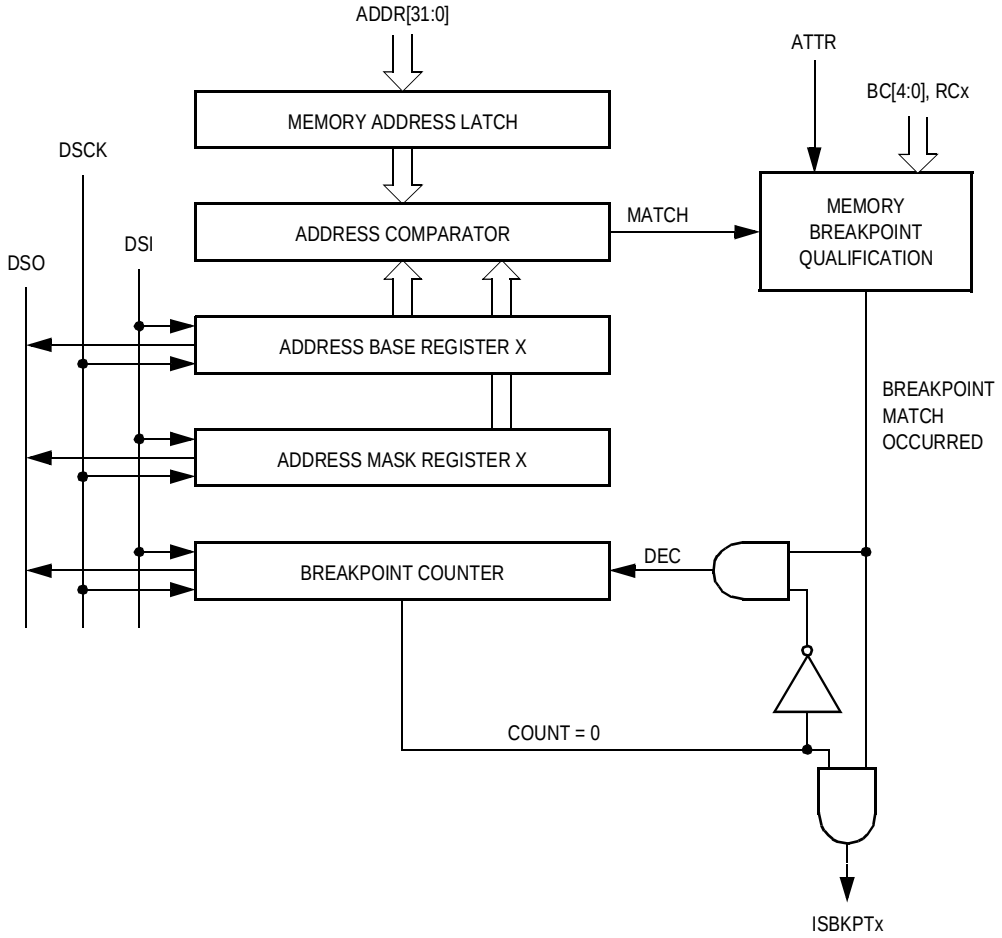

Figure 21-11. OnCE Memory Breakpoint Logic

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Address comparators can be used to determine where a program may be getting lost or when data is being written to areas which should not be written. They are also useful in halting a program at a specific point to examine or change registers or memory. Using address comparators to set breakpoints enables the user to set breakpoints in RAM or ROM in any operating mode. Memory accesses are monitored according to the contents of the OCR.

The address comparator generates a match signal when the address on the bus matches the address stored in the breakpoint address base register, as masked with individual bit masking capability provided by the breakpoint address mask register. The address match signal and the access attributes are further qualified with the RCx4–RCx0 and BCx4–BCx0 control bits. This qualification is used to decrement the breakpoint counter conditionally if its contents are non-zero. If the contents are zero, the counter is not decremented and the breakpoint event occurs (ISBKPTx asserted).

21.14.6.1 Memory Address Latch (MAL)

The MAL is a 32-bit register that latches the address bus on every access.

21.14.6.2 Breakpoint Address Base Registers

The 32-bit breakpoint address base registers (BABA and BABB) store memory breakpoint base addresses. BABA and BABB can be read or written through the OnCE serial interface. Before enabling breakpoints, the external command controller should load these registers.

21.14.7 Breakpoint Address Mask Registers

The 32-bit breakpoint address mask registers (BAMA and BAMB) registers store memory breakpoint base address masks. BAMA and BAMB can be read or written through the OnCE serial interface. Before enabling breakpoints, the external command controller should load these registers.

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21.14.7.1 Breakpoint Address Comparators

The breakpoint address comparators are not externally accessible. Each compares the memory address stored in MAL with the contents of BABx, as masked by BAMx, and signals the control logic when a match occurs.

21.14.7.2 Memory Breakpoint Counters

The 16-bit memory breakpoint counter registers (MBCA and MBCB) are loaded with a value equal to the number of times, minus one, that a memory access event should occur before a memory breakpoint is declared. The memory access event is specified by the RCx4–RCx0 and BCx4–BCx0 bits in the OCR and by the memory base and mask registers. On each occurrence of the memory access event, the breakpoint counter, if currently non-zero, is decremented. When the counter has reached the value of zero and a new occurrence takes place, the $\overline{\text{ISBKPTx}}$ signal is asserted and causes the CPU's $\overline{\text{BRKRQ}}$ input to be asserted. The MBCx can be read or written through the OnCE serial interface.

Anytime the breakpoint registers are changed, or a different breakpoint event is selected in the OCR, the breakpoint counter must be written afterward. This assures that the OnCE breakpoint logic is reset and that no previous events will affect the new breakpoint event selected.

21.14.8 OnCE Trace Logic

The OnCE trace logic allows the user to execute instructions in single or multiple steps before the device returns to debug mode and awaits OnCE commands from the debug serial port. The OnCE trace logic is independent of the M•CORE trace facility, which is controlled through the trace mode bits in the M•CORE processor status register. The OnCE trace logic block diagram is shown in **Figure 21-12**.

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21.14.8.1 OnCE Trace Counter

The OnCE trace counter register (OTC) is a 16-bit counter that allows more than one instruction to be executed in real time before the device returns to debug mode. This feature helps the software developer debug sections of code that are time-critical. The trace counter also enables the user to count the number of instructions executed in a code segment.

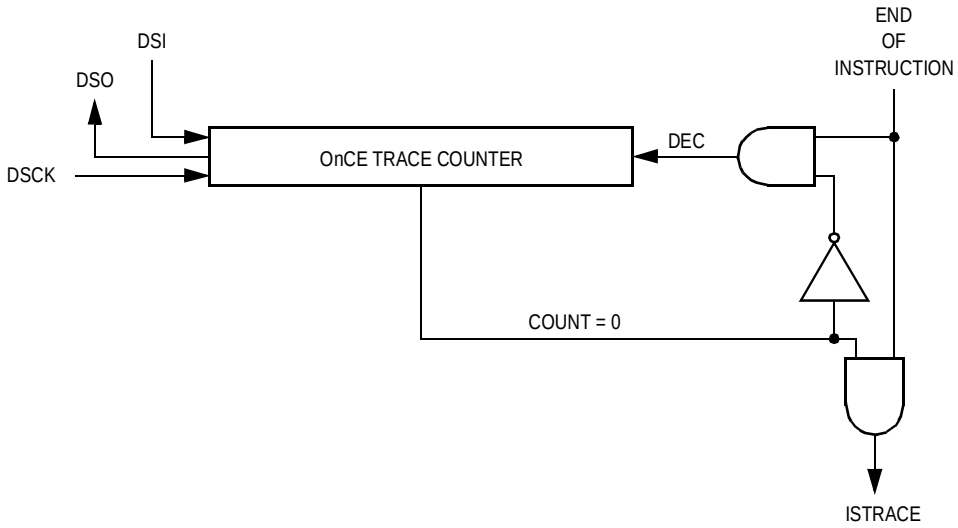

Figure 21-12. OnCE Trace Logic Block Diagram

The OTC register can be read, written, or cleared through the OnCE serial interface. If N instructions are to be executed before entering debug mode, the trace counter should be loaded with N – 1. N must not equal zero unless the sequential breakpoint control capability is being used. In this case a value of zero (indicating a single instruction) is allowed.

A hardware reset clears the OTC.

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21.14.8.2 Trace Operation

To initiate trace mode operation:

1. Load the OTC register with a value. This value must be non-zero, unless sequential breakpoint control operation is enabled in the OCR register. In this case, a value of zero (indicating a single instruction) is allowed.
2. Initialize the program counter and instruction register in the CPUSCR with values corresponding to the start location of the instruction(s) to be executed real-time.
3. Set the TME bit in the OCR.
4. Release the processor from debug mode by executing the appropriate command issued by the external command controller.

When debug mode is exited, the counter is decremented after each execution of an instruction. Interrupts can be serviced, and all instructions executed (including interrupt services) will decrement the trace counter.

When the trace counter decrements to zero, the OnCE control logic requests that the processor re-enter debug mode, and the trace occurrence bit TO in the OSR is set to indicate that debug mode has been requested as a result of the trace count function. The trace counter allows a minimum of two instructions to be specified for execution prior to entering trace (specified by a count value of one), unless sequential breakpoint control operation is enabled in the OCR. In this case, a value of zero (indicating a single instruction) is allowed.

21.14.9 Methods of Entering Debug Mode

The PM status field in the OSR indicates that the CPU has entered debug mode. The following paragraphs discuss conditions that invoke debug mode.

21.14.9.1 Debug Request During $\overline{\text{RESET}}$

When the DR bit in the OCR is set, assertion of $\overline{\text{RESET}}$ causes the device to enter debug mode. In this case the device may fetch the reset

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vector and the first instruction of the reset exception handler but does not execute an instruction before entering debug mode.

21.14.9.2 Debug Request During Normal Activity

Setting the DR bit in the OCR during normal device activity causes the device to finish the execution of the current instruction and then enter debug mode. Note that in this case the device completes the execution of the current instruction and stops after the newly fetched instruction enters the CPU instruction latch. This process is the same for any newly fetched instruction, including instructions fetched by interrupt processing or those that will be aborted by interrupt processing.

21.14.9.3 Debug Request During Stop, Doze, or Wait Mode

Setting the DR bit in the OCR when the device is in stop, doze, or wait mode (for instance, after execution of a STOP, DOZE, or WAIT instruction) causes the device to exit the low-power state and enter the debug mode. Note that in this case, the device completes the execution of the STOP, DOZE, or WAIT instruction and halts after the next instruction enters the instruction latch.

21.14.9.4 Software Request During Normal Activity

Executing the BKPT instruction when the FDB (force debug enable mode) control bit in the control state register is set causes the CPU to enter debug mode after the instruction following the BKPT instruction has entered the instruction latch.

21.14.10 Enabling OnCE Trace Mode

When the OnCE trace mode mechanism is enabled and the trace count is greater than zero, the trace counter is decremented for each instruction executed. Completing execution of an instruction when the trace counter is zero causes the CPU to enter debug mode.

NOTE: *Only instructions actually executed cause the trace counter to decrement. An aborted instruction does not decrement the trace counter and does not invoke debug mode.*

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21.14.11 Enabling OnCE Memory Breakpoints

When the OnCE memory breakpoint mechanism is enabled with a breakpoint counter value of zero, the device enters debug mode after completing the execution of the instruction that caused the memory breakpoint to occur. In case of breakpoints on instruction fetches, the breakpoint is acknowledged immediately after the execution of the fetched instruction. In case of breakpoints on data memory addresses, the breakpoint is acknowledged after the completion of the memory access instruction.

21.14.12 Pipeline Information and Write-Back Bus Register

A number of on-chip registers store the CPU pipeline status and are configured in the CPU scan chain register (CPUSCR) for access by the OnCE controller. The CPUSCR is used to restore the pipeline and resume normal device activity upon return from debug mode. The CPUSCR also provides a mechanism for the emulator software to access processor and memory contents. **Figure 21-13** shows the block diagram of the pipeline information registers contained in the CPUSCR.

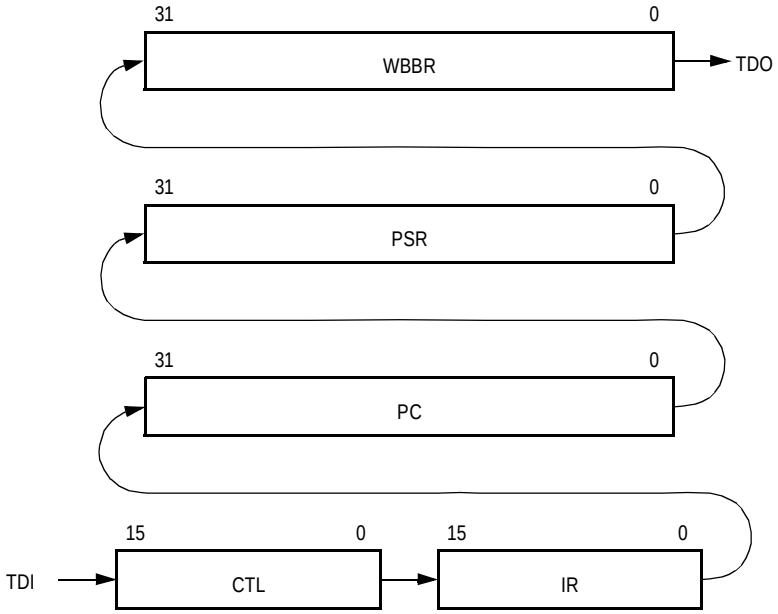

Figure 21-13. CPU Scan Chain Register (CPUSCR)

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21.14.12.1 Program Counter Register

The program counter register (PC) is a 32-bit latch that stores the value in the CPU program counter when the device enters debug mode. The CPU PC is affected by operations performed during debug mode and must be restored by the external command controller when the CPU returns to normal mode.

21.14.12.2 Instruction Register

The instruction register (IR) provides a mechanism for controlling the debug session. The IR allows the debug control block to execute selected instructions; the debug control module provides single-step capability.

When scan-out begins, the IR contains the opcode of the next instruction to be executed at the time debug mode was entered. This opcode must be saved in order to resume normal execution at the point debug mode was entered.

On scan-in, the IR can be filled with an opcode selected by debug control software in preparation for exiting debug mode. Selecting appropriate instructions allows a user to examine or change memory locations and processor registers.

Once the debug session is complete and normal processing is to be resumed, the IR can be loaded with the value originally scanned out.

21.14.12.3 Control State Register

The control state register (CTL) is used to set control values when debug mode is exited. On scan-in, this register is used to control specific aspects of the CPU. Certain bits reflect internal processor status and should be restored to their original values.

The CTL register is a 16-bit latch that stores the value of certain internal CPU state variables before debug mode is entered. This register is affected by the operations performed during the debug session and should be restored by the external command controller when returning to normal mode. In addition to saved internal state variables, the bits are used by emulation firmware to control the debug process.

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Reserved bits represent the internal processor state. Restore these bits to their original value after a debug session is completed, for example, when a OnCE command is issued with the GO and EX bits set and not ignored. Set these bits to 1s while instructions are executed during a debug session.

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	FFY
Reset:								0

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	FDB	SZ1	SZ0	TC2	TC1	TC0	RSVD	RSVD
Reset:	0	0	0	0	0	0		

Figure 21-14. Control State Register (CTL)

FFY — Feed Forward Y Operand Bit

This control bit is used to force the content of the WBBR to be used as the Y operand value of the first instruction to be executed following an update of the CPUSCR. This gives the debug firmware the capability of updating processor registers by initializing the WBBR with the desired value, setting the FFY bit, and executing a MOV instruction to the desired register.

FDB — Force Debug Enable Mode Bit

Setting this control bit places the processor in debug enable mode. In debug enable mode, execution of the BKPT instruction as well as recognition of the $\overline{\text{BRKRQ}}$ input causes the processor to enter debug mode, as if the $\overline{\text{DBGRQ}}$ input had been asserted.

SZ1 and SZ0 — Prefetch Size Field

This control field is used to drive the CPU SIZ1 and SIZ0 outputs on the first instruction pre-fetch caused by issuing a OnCE command with the GO bit set and not ignored. It should be set to indicate a 16-bit size, for example, 0b10. This field should be restored to its original value after a debug session is completed, for example, when a OnCE command is issued with the GO and EX bits set and not ignored.

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TC — Prefetch Transfer Code

This control field is used to drive the CPU TC2–TC0 outputs on the first instruction pre-fetch caused by issuing a OnCE command with the GO bit set and not ignored. It should typically be set to indicate a supervisor instruction access, for example, 0b110. This field should be restored to its original value after a debug session is completed, for example, when a OnCE command is issued with the GO and EX bits set and not ignored.

21.14.12.4 Writeback Bus Register

The writeback bus register (WBBR) is a means of passing operand information between the CPU and the external command controller. Whenever the external command controller needs to read the contents of a register or memory location, it forces the device to execute an instruction that brings that information to WBBR.

For example, to read the content of processor register r0, a MOV r0,r0 instruction is executed, and the result value of the instruction is latched into the WBBR. The contents of WBBR can then be delivered serially to the external command controller.

To update a processor resource, this register is initialized with a data value to be written, and a MOV instruction is executed which uses this value as a write-back data value. The FFY bit in the CTL register forces the value of the WBBR to be substituted for the normal source value of a MOV instruction, thus allowing updates to processor registers to be performed.

21.14.12.5 Processor Status Register

The processor status register (PSR) is a 32-bit latch used to read or write the M•CORE processor status register. Whenever the external command controller needs to save or modify the contents of the M•CORE processor status register, the PSR is used. This register is affected by the operations performed in debug mode and must be restored by the external command controller when returning to normal mode.

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21.14.13 Instruction Address FIFO Buffer (PC FIFO)

To ease debugging activity and keep track of program flow, a first-in-first-out (FIFO) buffer stores the addresses of the last eight instruction change-of-flow prefetches that were issued.

The FIFO is a circular buffer containing eight 32-bit registers and one 3-bit counter. All the registers have the same address, but any read access to the FIFO address causes the counter to increment and point to the next FIFO register. The registers are serially available to the external command controller through the common FIFO address. **Figure 21-15** shows the structure of the PC FIFO.

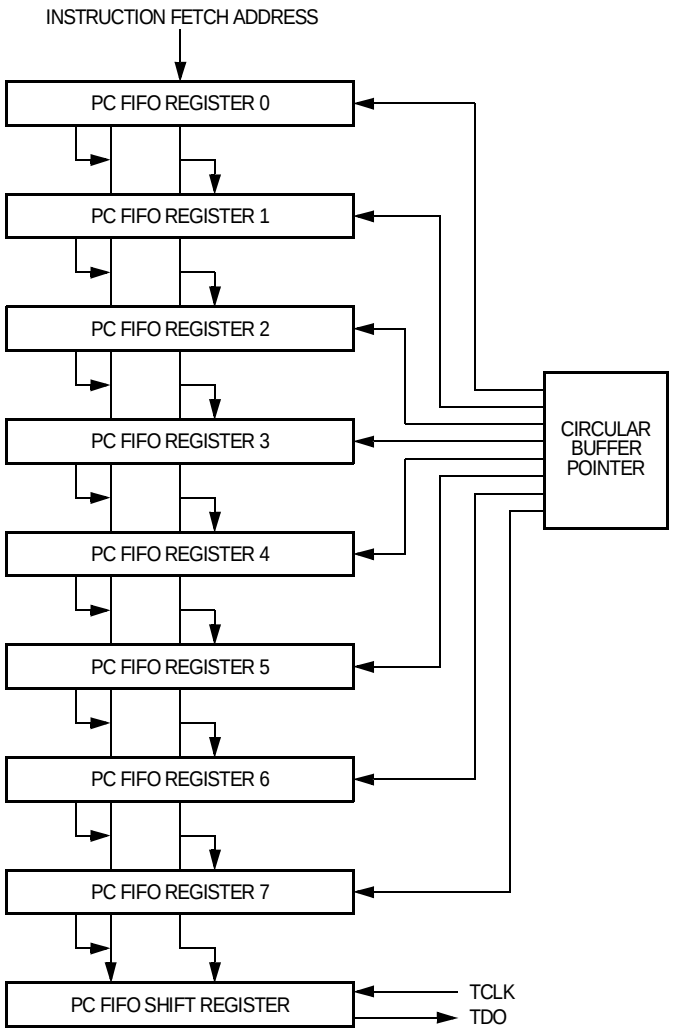

Figure 21-15. OnCE PC FIFO

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The FIFO is not affected by operations performed in debug mode, except for incrementing the FIFO pointer when the FIFO is read. When debug mode is entered, the FIFO counter points to the FIFO register containing the address of the oldest of the eight change-of-flow pre-fetches. The first FIFO read obtains the oldest address, and the following FIFO reads return the other addresses from the oldest to the newest, in order of execution.

To ensure FIFO coherence, a complete set of eight reads of the FIFO must be performed. Each read increments the FIFO pointer, causing it to point to the next location. After eight reads, the pointer points to the same location as before the start of the read procedure.

21.14.14 Reserved Test Control Registers

The reserved test control registers (MEM_BIST, FTCR, and LSRL) are reserved for factory testing.

CAUTION: *To prevent damage to the device or system, do not access these registers during normal operation.*

21.14.15 Serial Protocol

The serial protocol permits an efficient means of communication between the OnCE external command controller and the MCU. Before starting any debugging activity, the external command controller must wait for an acknowledgment that the device has entered debug mode. The external command controller communicates with the device by sending 8-bit commands to the OnCE command register and 16 to 128 bits of data to one of the other OnCE registers. Both commands and data are sent or received LSB first. After sending a command, the external command controller must wait for the processor to acknowledge execution of certain commands before it can properly access another OnCE register.

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21.14.16 OnCE Commands

The OnCE commands can be classified as:

- Read commands (the device delivers the required data)
- Write commands (the device receives data and writes the data in one of the OnCE registers)
- Commands with no associated data transfers

21.14.17 Target Site Debug System Requirements

A typical debug environment consists of a target system in which the MCU resides in the user-defined hardware.

The external command controller acts as the medium between the MCU target system and a host computer. The external command controller circuit acts as a serial debug port driver and host computer command interpreter. The controller issues commands based on the host computer inputs from a user interface program which communicates with the user.

21.14.18 Interface Connector for JTAG/OnCE Serial Port

Figure 21-16 shows the recommended connector pinout and interface requirements for debug controllers that access the JTAG/OnCE port. The connector has two rows of seven pins with 0.1-inch center-to-center spacing between pins in each row and each column.

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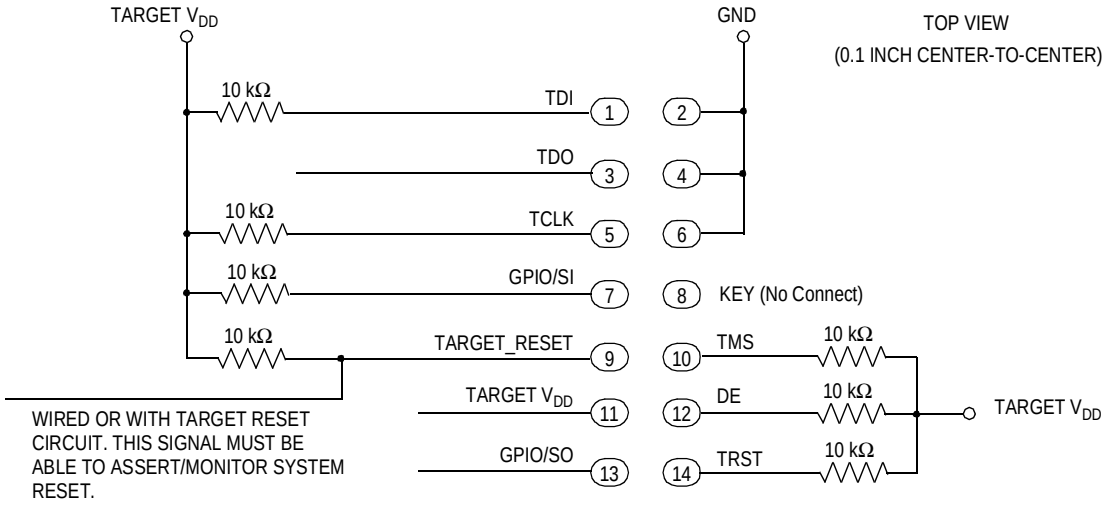

Note: GPIO/SI and GPIO/SO are not required for OnCE operation at this time.
These pins can be used for high-speed downloads with a recommended interface.

Figure 21-16. Recommended Connector Interface to JTAG/OnCE Port

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Section 22. Electrical Specifications

22.1 Contents

22.2 Introduction 585
22.3 Absolute Maximum Ratings 586
22.4 Thermal Characteristics 587
22.5 Power Dissipation 587
22.6 Electrostatic Discharge (ESD) Protection 587
22.7 DC Electrical Specifications 588
22.8 PLL Electrical Specifications 590
22.9 QADC Electrical Characteristics 591
22.10 FLASH Memory Characteristics 594
22.11 External Interface Timing Characteristics 596
22.12 Reset and Configuration Override Timing 601
22.13 SPI Timing Characteristics 602
22.14 OnCE, JTAG, and Boundary Scan Timing 605

22.2 Introduction

This section contains electrical and timing specifications.

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22.3 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it. See **Table 22-1**.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Keep V_{In} and V_{Out} within the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Connect unused inputs to the appropriate voltage level, either V_{SS} or V_{DD}. This device is not guaranteed to operate properly at the maximum ratings. Refer to **22.7 DC Electrical Specifications** for guaranteed operating conditions.

Table 22-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDSYN}	–0.3 to +4.0	V
RAM memory standby supply voltage	V_{STBY}	–0.3 to + 4.0	V
FLASH memory supply voltage	V_{DDF}	–0.3 to +4.0	V
FLASH memory program/erase supply voltage	V_{PP}	–0.3 to + 6.0	V
Analog supply voltage	V_{DDA}	–0.3 to +6.0	V
Analog reference supply voltage	V_{RH}	–0.3 to +6.0	V
Analog ESD protection voltage	V_{DDH}	–0.3 to +6.0	V
Digital input voltage(1)	V_{IN}	–0.3 to + 4.0	V
Analog input voltage	V_{AIN}	–0.3 to + 6.0	V
Instantaneous maximum current single pin limit (applies to all pins)(2), (3)	I_D	25	mA
Operating temperature range (packaged)	T_A (T_L to T_H)	–40 to 85	°C
Storage temperature range	T_{STG}	–65 to 150	°C

1. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
2. All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.
3. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock).

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22.4 Thermal Characteristics

Table 22-2. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance Plastic 100-pin LQFP surface mount Plastic 144-pin LQFP surface mount	θ_{JA}	 43.5 46.1	°C/W

22.5 Power Dissipation

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + P_D \times \theta_{JA} \quad (1)$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{DD} \times V_{DD}$, watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} < P_{INT}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

22.6 Electrostatic Discharge (ESD) Protection

Table 22-3. ESD Protection Characteristics

Parameter[1]	Symbol	Value	Units
ESD target for human body model	HBM	2000	V
ESD target for machine model	MM	200	V
HBM circuit description	R_{Series}	1500	W
	C	100	pF
MM circuit description	R_{Series}	0	W
	C	200	pF

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

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22.7 DC Electrical Specifications

Table 22-4. DC Electrical Specifications
($V_{SS} = V_{SSYN} = V_{SSF} = V_{SSA} = 0$ V, $T_A = T_L$ to T_H)

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	0.7 x V_{DD}	V_{DD} +0.3	V
Input low voltage	V_{IL}	V_{SS} –0.3	0.35 x V_{DD}	V
Input hysteresis	V_{HYS}	0.06 x V_{DD}	—	V
Input leakage current, $V_{in} = V_{DD}$ or V_{SS}, input-only pins	I_{In}	–1.0	1.0	µA
High impedance (off-state) leakage current $V_{in} = V_{DD}$ or V_{SS}, all input/output and output pins	I_{OZ}	–1.0	1.0	µA
Output high voltage I_{OH} = –2.0 mA, all input/output and all output pins	V_{OH}	V_{DD} –0.5	—	V
Output low voltage I_{OL} = 2.0 mA, all input/output and all output pins	V_{OL}	—	0.5	V
Weak internal pullup device current, tested at V_{IL} maximum	I_{APU}	–10	–130	µA
Input capacitance All input-only pins All input/output (three-state) pins	C_{In}	— —	7 7	pF
Load Capacitance 50% partial drive 100% full drive	C_L	— —	25 50	pF
Supply voltage, includes core modules and pads	V_{DD}	2.7	3.6	V
Clock synthesizer supply voltage	V_{DDSYN}	2.7	3.6	V
RAM memory standby supply voltage Normal operation: $V_{DD} > V_{STBY}$ –0.3 V Standby mode: $V_{DD} < V_{STBY}$ –0.3 V	V_{STBY}	0.0 2.7	3.6 3.6	V
FLASH memory supply voltage(1) Read Program or erase	V_{DDF}	2.7 3.135	3.6 3.465	V
FLASH memory program/erase supply voltage Read Program or erase	V_{PP}	V_{DDF} –0.35 4.75	5.25 5.25	V
Operating supply current(2), (4) Master mode Single-chip mode Wait mode Doze mode Stop mode	I_{DD}	 — — — — —	 200 175 75 75 100	 mA mA mA mA µA

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Table 22-4. DC Electrical Specifications (Continued)
(V_{SS} = V_{SSYN} = V_{SSF} = V_{SSA} = 0 V, T_A = T_L to T_H)

Parameter	Symbol	Min	Max	Unit
Clock synthesizer supply current(3) Normal operation 8-MHz crystal, VCO on, Max f_{sys} Stop (OSC and PLL enabled) Stop (OSC enable, PLL disabled) Stop (OSC and PLL disabled)	I_{DDSYN}	 — — — —	 4 2 1 10	 mA mA mA µA
RAM memory standby supply current(4) Normal operation: $V_{DD} > V_{STBY} – 0.3$ V Transient condition: $V_{STBY} –0.3$ V > V_{DD} > V_{SS} + 0.5 V Standby operation: $V_{DD} < V_{SS}$ + 0.5 V	I_{STBY}	 — — —	 10 7 20	 µA mA µA
FLASH memory supply current(4) Read Program or erase Disabled Stop	I_{DDF}	 — — — —	 50 50 20 10	 mA mA mA µA
Flash memory program / erase supply current(4) Read Program or erase Disabled and stop	I_{PP}	 — — —	 100 100 10	 µA mA µA
Analog supply current(4) Normal operation Low-power stop	I_{DDA}	 — —	 15.0 10.0	 mA µA
DC injection current(4), (5), (6) $V_{NEGCLAMP}$ = V_{SS} – 0.3 V, $V_{POSCLAMP}$ = V_{DD} + 0.3 Single pin limit Total MCU limit, includes sum of all stressed pins	I_{IC}	 –1.0 –10	 1.0 10	mA

1. A voltage of at least V_{DDF} –0.35 V must be applied at all times to the V_{PP} pin or damage to the FLASH module can occur The FLASH can be damaged by power on and power off V_{PP} transients. V_{PP} must not rise to programming level while V_{DDF} is below the specified minimum value, and must not fall below the minimum specified value while V_{DDF} is applied.
2. Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.
3. Total device current consumption = I_{DD} + I_{DDSYN} + I_{STBY} + I_{DDF} + I_{PP} + I_{DDA}
4. All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

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22.8 PLL Electrical Specifications

Table 22-5. PLL Electrical Specifications
(V_{DD} and V_{DDSYN} = 2.7 to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Parameter	Symbol	Min	Max	Unit
PLL reference frequency range Crystal reference External reference 1:1 mode	f_{ref}	 2 2 10	 10.0 33.0 33.0	MHz
System frequency(1) External reference On-chip PLL frequency	f_{sys}	 0 f_{ref}/64	 33.0 33.0	MHz
Loss of reference frequency(2)	f_{LOR}	100	250	kHz
Self-clocked mode frequency(3)	f_{SCM}	0.5	15	MHz
EXTAL input high voltage Crystal mode All other modes (1:1, bypass, external)	V_{IHEXT}	 V_{DDSYN} –1.0 2.0	 V_{DDSYN} V_{DDSYN}	V
EXTAL input low voltage Crystal mode All other modes (1:1, bypass, external)	V_{ILEXT}	 V_{SSSYN} V_{SSSYN}	 1.0 0.8	V
PLL lock time(4), (5)	t_{LPLL}	—	200	µs
Powerup-to-lock Time(4), (5) Without crystal reference	t_{LPLK}	—	200	µs
1:1 clock skew (between CLKOUT and EXTAL)(6)	t_{Skew}	–2	2	ns
Duty cycle of reference(4)	t_{dc}	40	60	% f_{sys}
Frequency un-LOCK range	f_{UL}	–1.5	1.5	% f_{sys}
Frequency LOCK range	f_{LCK}	–0.75	0.75	% f_{sys}
CLKOUT period jitter(7) Measured at f_{sys} maximum Peak-to-peak jitter (clock edge to clock edge) Long-term jitter (averaged over 2-ms interval)	C_{Jitter}	 — —	 5 0.01	% f_{sys}

1. All internal registers retain data at 0 Hz.
2. Loss of reference frequency is the reference frequency detected internally, which transitions the PLL into self-clocked mode.
3. Self-clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.
4. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
5. Assuming a reference is available at power-up, lock time is measured from the time V_{DD} and V_{DDSYN} are valid to $\overline{\text{RSTOUT}}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal startup time must be added to the PLL lock time to determine the total startup time.
6. PLL is operating in 1:1 PLL mode.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

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22.9 QADC Electrical Characteristics

The QADC electrical characteristics are shown in **Table 22-6**, **Table 22-7**, and **Table 22-8**.

Table 22-6. QADC Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Analog supply, with reference to V_{SSA}	V_{DDA}	–0.3	6.0	V
Internal digital supply with reference to V_{SS}	V_{DD}	–0.3	4.0	V
Maximum analog reference voltage with respect to V_{RL}	V_{RH}	–0.3	6.0	V
V_{SS} differential voltage	$V_{SS} - V_{SSA}$	–0.1	0.1	V
V_{DD} differential voltage(1)	$V_{DD} - V_{DDA}$	–6.0	4.0	V
V_{REF} differential voltage	$V_{RH} - V_{RL}$	–0.3	6.0	V
V_{RH} to V_{DDA} differential voltage(2)	$V_{RH} - V_{DDA}$	–6.0	6.0	V
V_{RL} to V_{SSA} differential voltage	$V_{RL} - V_{SSA}$	–0.3	0.3	V
V_{DDH} to V_{DDA} differential voltage	$V_{DDH} - V_{DDA}$	–1.0	1.0	V
Maximum input current(2), (3), (4)	I_{MA}	–25	25	mA

1. Refers to allowed random sequencing of power supplies
2. Transitions within the limit do not affect device reliability or cause permanent damage. Exceeding limit may cause permanent conversion error on stressed channels and on unstressed channels.
3. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.3$ V and $V_{NEGCLAMP} = –0.3$ V, then use the larger of the calculated values.
4. Condition applies to one pin at a time.

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Electrical Specifications

Table 22-7. QADC Electrical Specifications
($V_{DDH} = V_{DDA} = 5.0\ V \pm 0.5\ V$, $V_{DD} = 2.7$ to 3.6 V, V_{SS} and $V_{SSA} = 0$ Vdc, $f_{QCLK} = 2.0$ MHz, $T_A = T_L$ to T_H)

Parameter[1]	Symbol	Min	Max	Unit
Analog supply	V_{DDA}	4.5	5.5	V
V_{SS} differential voltage	$V_{SS} - V_{SSA}$	–100	100	mV
Reference voltage low[2]	V_{RL}	V_{SSA}	$V_{SSA} + 0.1$	V
Reference voltage high[3]	V_{RH}	$V_{DDA} - 0.1$	V_{DDA}	V
V_{REF} differential voltage	$V_{RH} - V_{RL}$	4.5	5.5	V
Input voltage	V_{INDC}	$V_{SSA} - 0.3$	$V_{DDA} + 0.3$	V
Input high voltage, PQA and PQB	V_{IH}	$0.7 \times V_{DDH}$	$V_{DDH} + 0.3$	V
Input low voltage, PQA and PQB	V_{IL}	$V_{SSA} - 0.3$	$0.35 \times V_{DDH}$	V
Input hysteresis, PQA and PQB[3]	V_{HYS}	$0.6 \times V_{DDH}$	—	V
Output low voltage, PQA[4] I_{OL} = 5.3 mA I_{OL} = 10.0 µA	V_{OL}	— —	0.4 0.2	V
Output high voltage, PQA[5] I_{OH} = 2.0 mA I_{OH} = 10.0 µA	V_{OH}	$V_{DD} - 0.4$ $V_{DD} - 0.2$	— —	V
Analog supply current Normal operation [5] Low-power stop	I_{DDA}	— —	15.0 10.0	mA µA
Reference supply current, DC Reference supply current, transient	I_{Ref}	— —	250 2.0	µA mA
Load capacitance, PQA	C_L	—	50	pF
Input current, channel off [6] PQA, PQB	I_{Off}	–200 –150	200 150	nA
Total input capacitance PQA not sampling PQB not sampling Incremental capacitance added during sampling	C_{In}	— — —	15 10 5	pF

1. QADC converter specifications are only guaranteed for V_{DDH} and $V_{DDA} = 5.0\ V \pm 0.5\ V$. V_{DDH} and V_{DDA} may be powered down to 2.7 V with only GPIO functions supported.
2. To obtain full-scale, full-range results, $V_{SSA} \le V_{RL} \le V_{INDC} \le V_{RH} \le V_{DDA}$
3. Parameter applies to the following pins: Port A: PQA[7:0]/AN[59:58]/ETRIG[2:1]
   Port B: PQB[7:0]/AN[3:0]/AN[51:48]/AN[Z:W]
4. Full driver (push-pull)
5. Current measured at maximum system clock frequency with QADC active
6. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°C to 12°C, in the ambient temperature range of –40°C to +85°C.

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Table 22-8. QADC Conversion Specifications
(V_{DDH} and V_{DDA} = 5.0 Vdc ± 0.5 V, V_{DD} = 2.7 to 3.6 V, V_{SS} = V_{SSA} = 0 Vdc, V_{RH} – V_{RL} = 5 V ± 0.5 V, T_A = T_L to T_H)

No.	Parameter	Symbol	Min	Max	Unit
1	QADC clock (QCLK) frequency(1)	f_{QCLK}	0.5	2.1	MHz
2	Conversion cycles	CC	14	28	QCLK cycles
3	Conversion time, f_{QCLK} = 2.0 MHz Minimum = CCW/IST =%00 Maximum = CCW/IST =%11	t_{CONV}	7.0	14.0	µs
4	Stop mode recovery time	t_{SR}	—	10	µs
5	Resolution(2)	—	5	—	mV
6	Absolute (total unadjusted) error(3), (4), (5) f_{QCLK} = 2.0 MHz(2), two clock input sample time	AE	–2	2	Counts
7	Disruptive input injection current(6), (7), (8)	I_{INJ}(9)	–1	1	mA
8	Current coupling ratio(10) PQA PQB	K	— —	$8x10^{-5}$ $8x10^{-5}$	m
9	Incremental error due to injection current All channels have same 10 kΩ < R_S <100 kΩ Channel under test has R_S = 10 kΩ, I_{INJ} = I_{INJMAX}, I_{INJMIN}	E_{INJ}	— — —	±1.0 ±1.0 ±1.0	Counts Counts Counts
10	Source impedance at input(11)	R_S	—	100	kΩ
11	Incremental capacitance during sampling(12)	C_{SAMP}	—	5	pF

1. Conversion characteristics vary with f_{QCLK} rate. Reduced conversion accuracy occurs at max f_{QCLK} rate. Using the QADC pins as GPIO functions during conversions may result in degraded results.
2. At V_{RH} – V_{RL} = 5.12 V, one count = 5 mV
3. Accuracy tested and guaranteed at V_{RH} – V_{RL} = 5.0 V ± 0.5 V
4. Absolute error includes 1/2 count (~2.5 mV) of inherent quantization error and circuit (differential, integral, and offset) error. Specification assumes that adequate low-pass filtering is present on analog input pins — capacitive filter with 0.01 µF to 0.1 µF capacitor between analog input and analog ground, typical source isolation impedance of 10 kΩ.
5. Input signals with large slew rates or high frequency noise components cannot be converted accurately. These signals may affect the conversion accuracy of other channels
6. Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.
7. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
8. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP}$ = V_{DDA} + 0.5 V and $V_{NEGCLAMP}$ = – 0.3 V, then use the larger of the calculated values.
9. Condition applies to two adjacent pins.
10. Current coupling ratio, K, is defined as the ratio of the output current, I_{Out}, measured on the pin under test to the injection current, I_{INJ}, when both adjacent pins are overstressed with the specified injection current. K = I_{Out}/ I_{INJ} The input voltage error on the channel under test is calculated as V_{ERR} = I_{INJ} x K x R_S.

— Continued —

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11. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance. Error from junction leakage is a function of external source impedance and input leakage current. In the following expression, expected error in result value due to junction leakage is expressed in voltage (V_{ERRJ}):
    $V_{ERRJ} = R_S \times I_{Off}$
    where:
    I_{Off} is a function of operating temperature.
    Charge-sharing leakage is a function of input source impedance, conversion rate, change in voltage between successive conversions, and the size of the filtering capacitor used. Error levels are best determined empirically. In general, continuous conversion of the same channel may not be compatible with high-source impedance.
12. For a maximum sampling error of the input voltage ≤ 1 LSB, then the external filter capacitor, $C_f \geq 1024 \times C_{SAMP}$. The value of C_{SAMP} in the new design may be reduced.

22.10 FLASH Memory Characteristics

The FLASH memory characteristics are shown in **Table 22-9**, **Table 22-10**, **Figure 22-2**, and **Figure 22-1**.

Table 22-9. FLASH Program and Erase Characteristics
(V_{DDF} = 3.135 to 3.465 V, V_{PP} = 4.75 to 5.25 V, $T_A = T_L$ to T_H)

Parameter	Symbol	Min	Typ	Max	Unit
Number of erase pulses	E_{Pulse}	8	8	20	—
Erase pulse time	t_{Erase}	See **Table 9-11. Required Erase Algorithm** on page 219.			
Erase recovery time	t_{E_Off}	4.0	4.8	6.0	µs
Number of program pulses	P_{Pulse}	—	500	Note 1	—
Program pulse time	t_{PROG}	See **Table 9-9. Required Programming Algorithm** on page 213.			
Program recovery time	t_{P_Off}	4.0	4.8	6.0	µs

1. Maximum pulses vary with V_{PP}.

Table 22-10. FLASH EEPROM Module Life Characteristics
(V_{DDF} = 2.7 to 3.6 V, V_{PP} = 4.75 to 5.25 V, $T_A = T_L$ to T_H)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/ erase cycles(1)	P/E	100(2)	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

1. A program/erase cycle is defined as switching the bits from 1 → 0 → 1.
2. Reprogramming of a FLASH array block prior to erase is not required.

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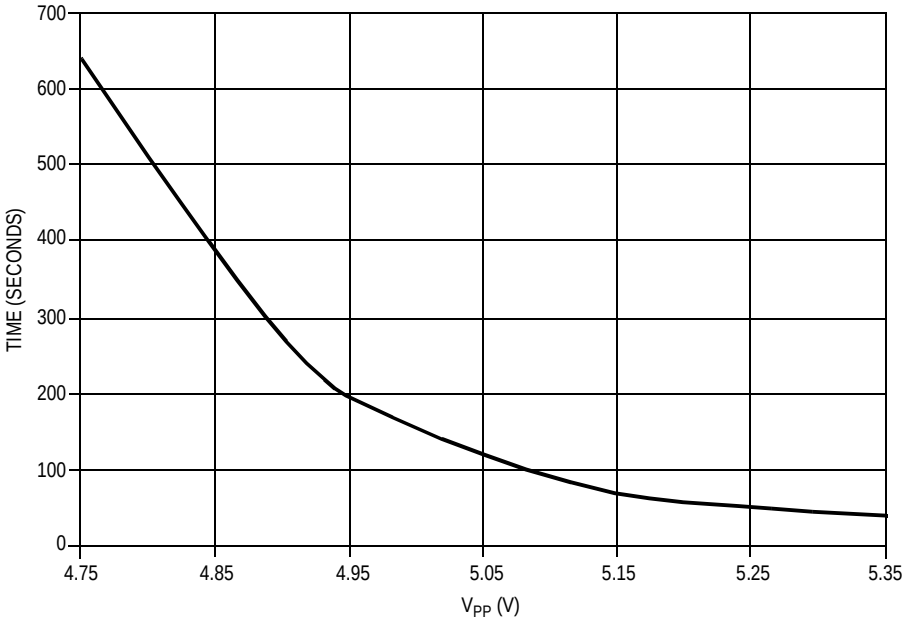

Notes:
1. Data taken with V_{DD} = 3.6 V at 25°C
2. One page at a time programming of full 128-K array
3. Total number of pulses increases with lower V_{PP}. See **Figure 22-2**.

Figure 22-1. V_{PP} versus Programming Time

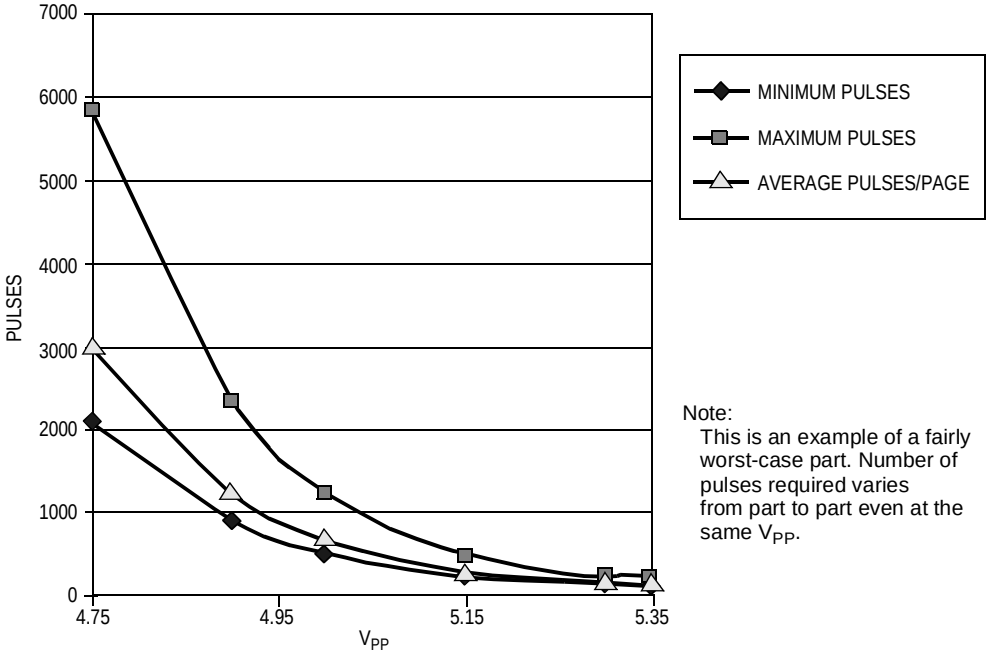

Figure 22-2. V_{PP} versus Programming Pulses

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22.11 External Interface Timing Characteristics

Table 22-11. External Interface Timing Characteristics
(V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)

No.	Characteristic[1], [2]	Symbol	Min	Max	Unit
1	CLKOUT period	t_{cyc}	30	—	ns
2	CLKOUT low pulse width	t_{CLW}	0.5 t_{cyc} – 1	—	ns
3	CLKOUT high pulse width	t_{CHW}	0.5 t_{cyc} – 1	—	ns
4	All rise times	t_{CR}	—	3	ns
5	All fall times	t_{CF}	—	3	ns
6	CLKOUT high to A[22:0], TSIZ[1:0] valid[3]	t_{CHAV}	—	10	ns
7	CLKOUT high to A[22:0], TSIZ[1:0] invalid	t_{CHAI}	0	—	ns
8	CLKOUT high to $\overline{CS[3:0]}$ asserted	t_{CHCA}	—	10	ns
9	CLKOUT high to $\overline{CS[3:0]}$ negated	t_{CHCN}	0	—	ns
10	CLKOUT high to CSE[1:0] valid	t_{CHCEV}	—	10	ns
11	CLKOUT high to CSE[1:0] invalid	t_{CHCEI}	0	—	ns
12	CLKOUT high to TC[2:0], PSTAT[3:0] valid	t_{CHTV}	—	15	ns
13	CLKOUT high to TC[2:0], PSTAT[3:0] invalid	t_{CHTI}	0	—	ns
14	CLKOUT high to R/$\overline{W}$ high hold time	t_{CHRWH}	0	10	ns
15	CLKOUT high to R/$\overline{W}$ valid write	t_{CHRWV}	0.25 t_{cyc}	0.25 t_{cyc} + 9	ns
16	CLKOUT high to $\overline{OE}$, $\overline{EB}$ asserted[4], [5]	t_{CHOEA}	0.25 t_{cyc}	0.25 t_{cyc} + 9	ns
17	CLKOUT high to $\overline{OE}$, $\overline{EB}$ read negated	t_{CHOEN}	0	9	ns
17A	CLKOUT low to $\overline{EB}$ write negated	t_{CLEN}	0.25 t_{cyc}	0.25 t_{cyc} + 10	ns
18	CLKOUT low to $\overline{SHS}$ low	t_{CLSL}	0	10	ns
19	CLKOUT $\overline{High}$ to $\overline{SHS}$ high[6]	t_{CHSH}	0	8	ns
20	CLKOUT low to data-out low impedance write/show	t_{CHDOD}	0	—	ns
21	CLKOUT high to data-out high impedance write/show[7]	t_{CHDOZ}	2	10	ns
22	CLKOUT low to data-out valid write	t_{CLDOVW}	—	12	ns
22A	CLKOUT low to data-out valid show	t_{CLDOVS}	—	12	ns
23	CLKOUT high to data-out invalid write/show	t_{CHDOIW}	10	—	ns

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Table 22-11. External Interface Timing Characteristics (Continued)
(V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)

No.	Characteristic[1], [2]	Symbol	Min	Max	Unit
24	Data-in valid to CLKOUT high read	t_{DIVCH}	22	—	ns
25	CLKOUT high to data-in invalid read	t_{CHDII}	0	—	ns
26	$\overline{TA}$, $\overline{TEA}$ asserted to CLKOUT high	t_{TACH}	0.25 t_{cyc} + 14	—	ns
27	CLKOUT high to $\overline{TA}$, $\overline{TEA}$ negated	t_{CHTN}	0	—	ns

1. All AC timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels, unless otherwise noted.
2. Timing is not guaranteed during the clock cycle of mode and/or setup changes (for example, changing pin function between GPIO and primary function, changing GPIO between input/output functions, changing control registers that affect pin functions).
3. A[22:0], TSIZ[1:0], $\overline{CS[3:0]}$ valid to R/$\overline{W}$ (write), $\overline{OE}$, $\overline{EB}$ asserted (minimum) spec is 0 ns. This parameter is characterized before qualification rather than 100% tested.
4. Write/show data high-Z to $\overline{OE}$ asserted (minimum) or from $\overline{EB}$ negated (write — maximum) spec is 0 ns. This parameter is characterized before qualification rather than 100% tested.
5. To prevent an unintentional assertion glitch of the $\overline{EB}$ pins during a synchronous reset (and before the reset overrides configure the chip in a stable mode), leave the port output data register bits associated with the $\overline{EB}$ GPO default of 1 and do not pull the pins down with a current load.
6. $\overline{SHS}$ high to show data or write data invalid (minimum) spec is 0 ns. This parameter is characterized before qualification rather than 100% tested.
7. Write/show data high-Z and write/show data invalid is 0 ns for synchronous reset conditions.

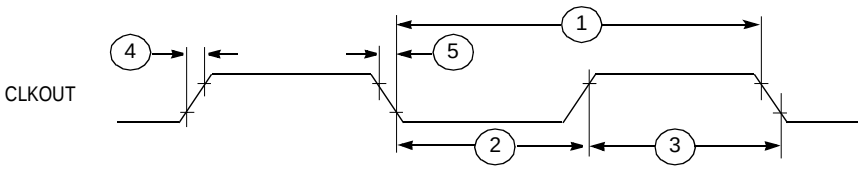

Figure 22-3. CLKOUT Timing

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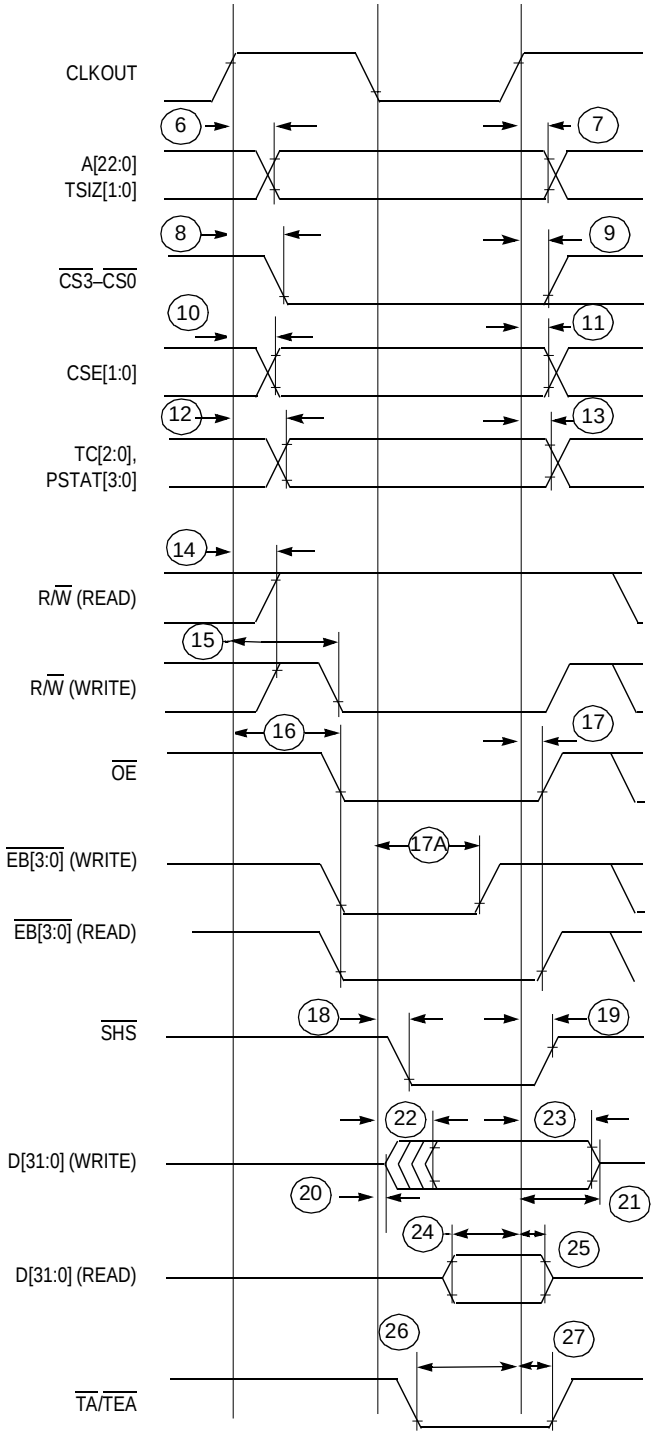

Figure 22-4. Clock Read/Write Cycle Timing

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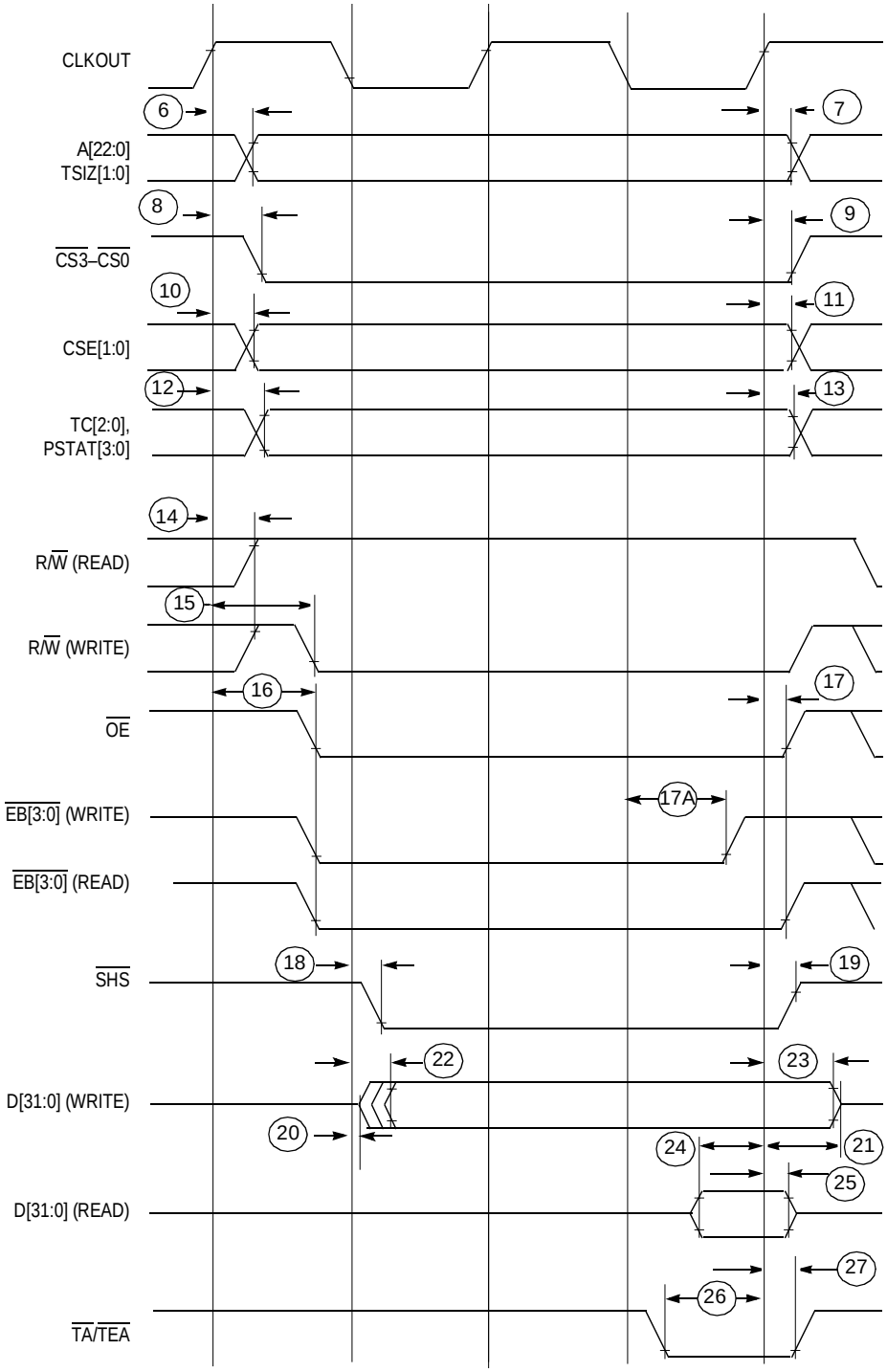

Figure 22-5. Read/Write Cycle Timing with Wait States

Freescale Semiconductor, Inc.

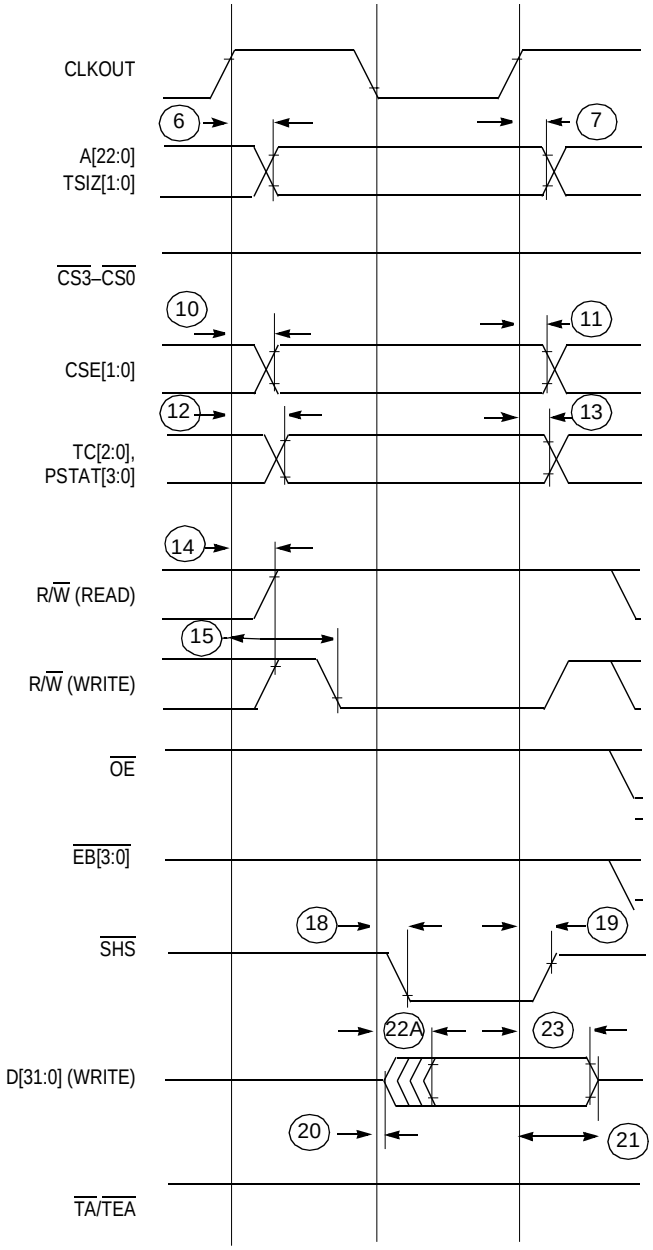

Figure 22-6. Show Cycle Timing

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22.12 Reset and Configuration Override Timing

Table 22-12. Reset and Configuration Override Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)

No.	Parameter[1]	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ input asserted to CLKOUT high	t_{RACH}	10	—	ns
R2	CLKOUT high to $\overline{\text{RESET}}$ input negated	t_{CHRN}	2	—	ns
R3	$\overline{\text{RESET}}$ input assertion time[2]	t_{RIAT}	5	—	t_{cyc}
R4	CLKOUT high to $\overline{\text{RSTOUT}}$ valid[3]	t_{CHROV}	—	20	ns
R5	$\overline{\text{RSTOUT}}$ asserted to config. overrides asserted	t_{ROACA}	0	—	ns
R6	Configuration override setup time to $\overline{\text{RSTOUT}}$ negated	t_{COS}	20	—	t_{cyc}
R7	Configuration override hold time after $\overline{\text{RSTOUT}}$ negated	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ negated to configuration override high impedance	t_{RONCZ}	—	1	t_{cyc}

1. All AC timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels, unless otherwise noted.
2. During low-power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.
3. This parameter also covers the timing of the show interrupt function.

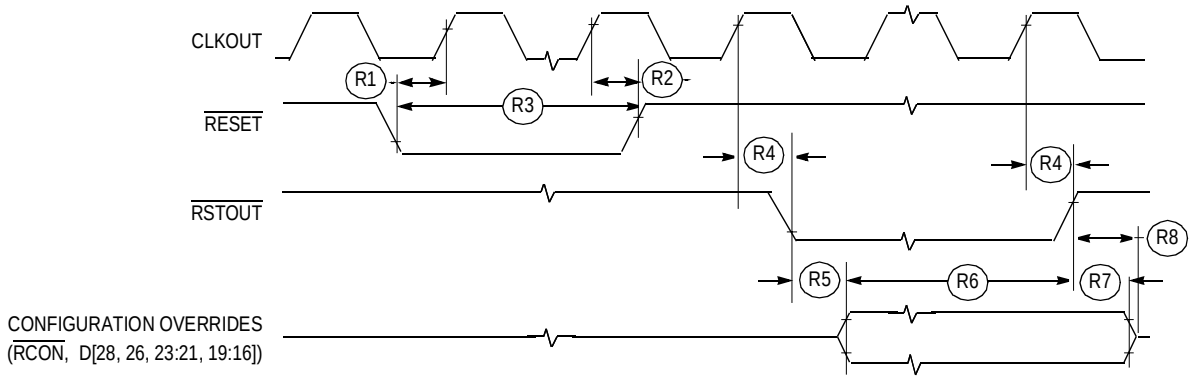

Figure 22-7. $\overline{\text{RESET}}$ and Configuration Override Timing

Freescale Semiconductor, Inc.

22.13 SPI Timing Characteristics

Table 22-13. SPI Timing Characteristics
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)

No.	Function	Symbol	Min	Max	Unit
1	Operating frequency Master Slave	f_{op}	DC DC	1/2 x f_{sys} 1/2 x f_{sys}	System frequency
2	SCK period Master Slave	t_{SCK}	2 2	2048 —	t_{cyc} t_{cyc}
3	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{sck} t_{cyc}
4	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{sck} t_{cyc}
5	Clock (SCK) high or low time Master Slave	t_{WSCK}	t_{cyc} – 30 t_{cyc} – 30	1024 t_{cyc} —	ns
6	Data setup time, inputs Master Slave	t_{SU}	25 25	— —	ns
7	Data hold time, inputs Master Slave	t_{High}	0 25	— —	ns
8	Slave access time	t_A	—	1	t_{cyc}
9	Slave MISO disable time	t_{DIS}	—	1	t_{cyc}
10	Data valid after SCK edge Master Slave	t_V	— —	25 25	ns
11	Data hold time, outputs Master Slave	t_{Hold}	0 0	— —	ns
12	Rise time Input Output	t_{RI} t_{RO}	— —	t_{cyc} – 25 25	ns
13	Fall time Input Output	t_{FI} t_{FO}	— —	t_{cyc} – 25 25	ns

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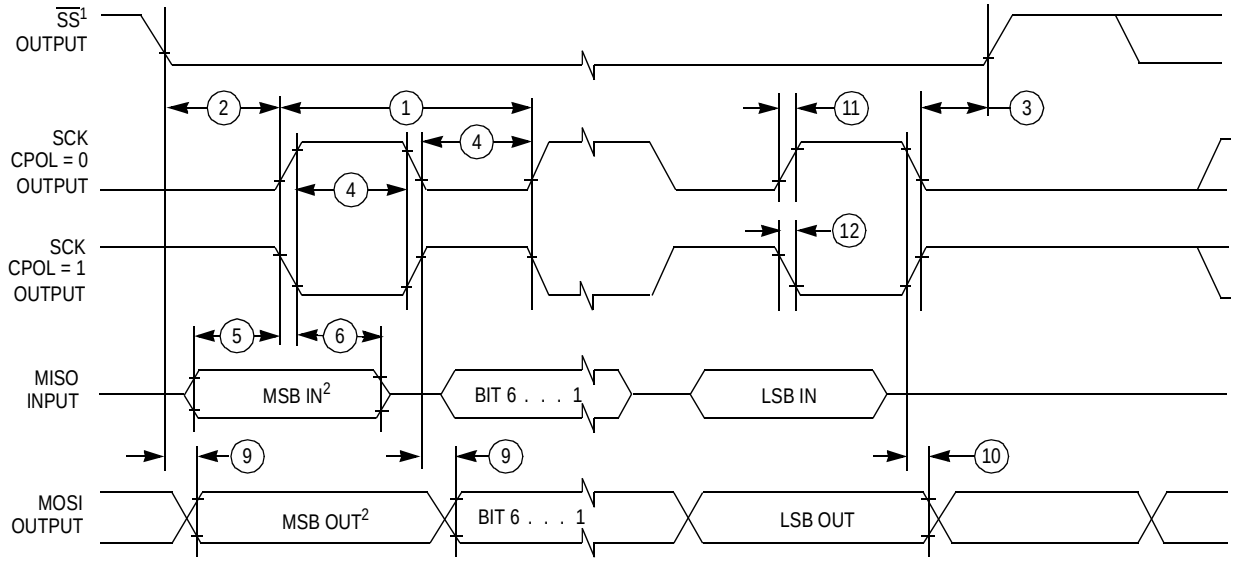
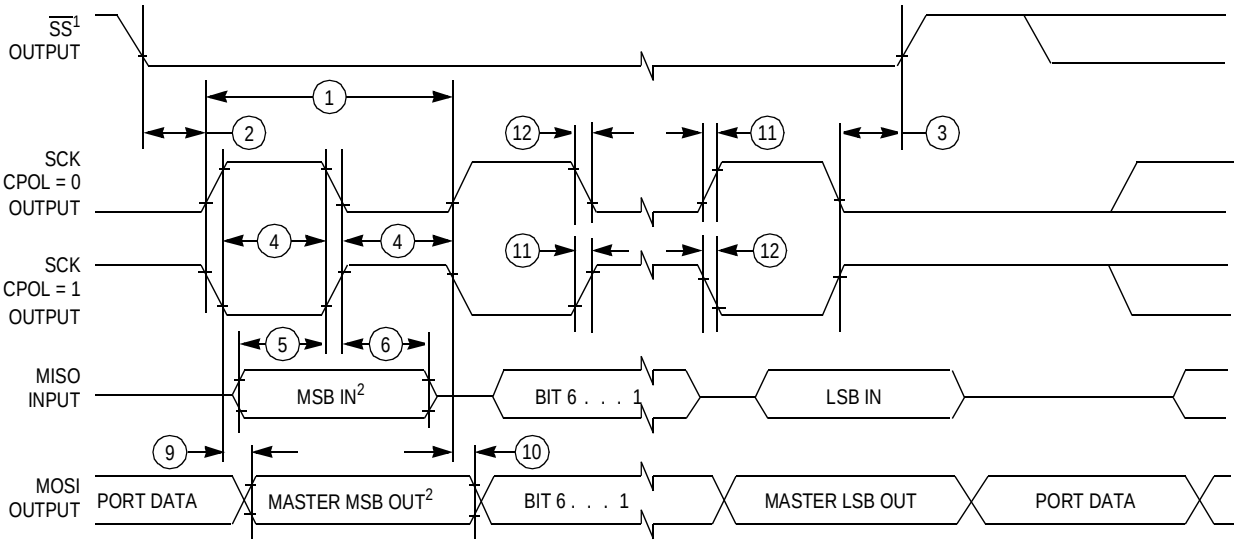


Notes:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1)
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

A) SPI Master Timing (CPHA = 0)



Notes:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1)
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

B) SPI Master Timing (CPHA = 1)

Figure 22-8. SPI Timing Diagram (Sheet 1 of 2)

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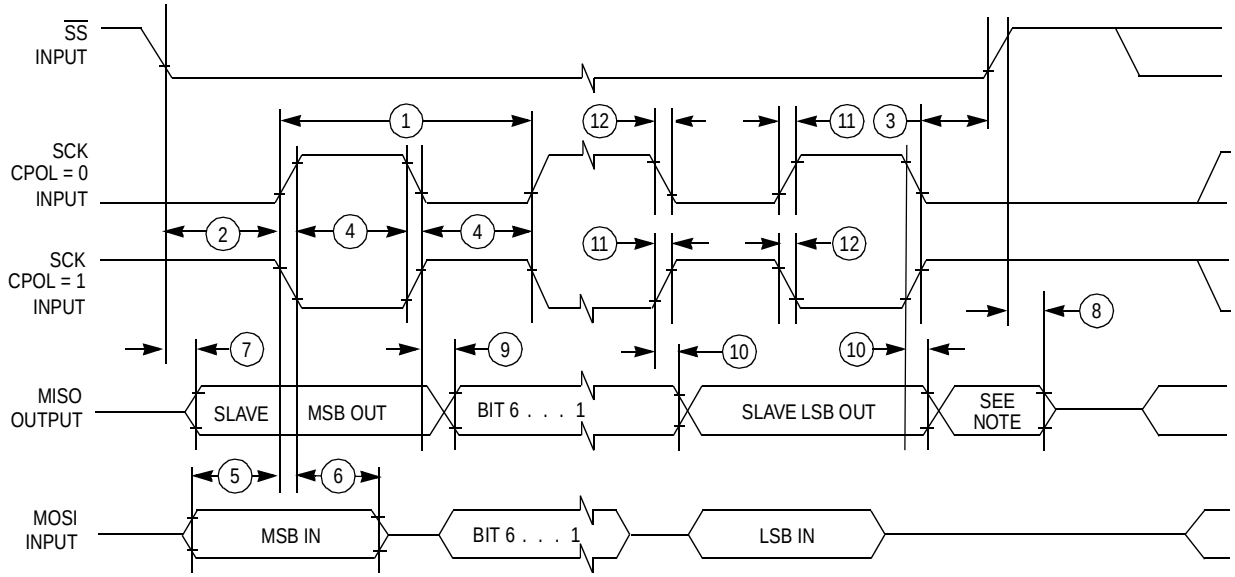
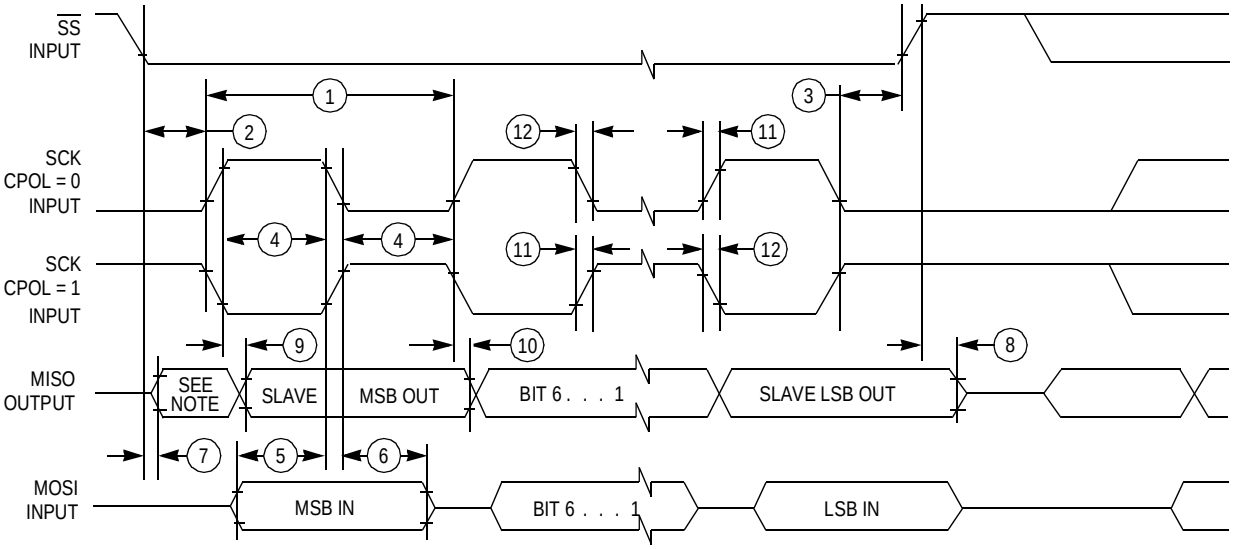
Electrical Specifications



Note: Not defined, but normally MSB of character just received

A) SPI Slave Timing (CPHA = 0)



Note: Not defined, but normally LSB of character just received

B) SPI Slave Timing (CPHA = 1)

Figure 24-7. SPI Timing Diagram (Sheet 2 of 2)

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22.14 OnCE, JTAG, and Boundary Scan Timing

Table 22-14. OnCE, JTAG, and Boundary Scan Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, $T_A = T_L$ to T_H)

No.	Characteristics	Symbol	Min	Max	Unit
1	TCLK frequency of operation	f_{JCYC}	dc	1/2 x f_{sys}	MHz
2	TCLK cycle period	t_{JCYC}	2	—	t_{cyc}
3	TCLK clock pulse width	t_{JCW}	25	—	ns
4	TCLK rise and fall times	t_{JCRF}	0	3	ns
5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	5	—	ns
6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	24	—	ns
7	TCLK low-to-boundary scan output data valid	t_{BSDV}	0	40	ns
8	TCLK low-to-boundary scan output high Z	t_{BSDZ}	0	40	ns
9	TMS, TDI, and $\overline{DE}$ input data setup time to TCLK rise(1)	t_{TAPDST}	7	—	ns
10	TMS, TDI, and $\overline{DE}$ input data hold time after TCLK rise(1)	t_{TAPDHT}	15	—	ns
11	TCLK low to TDO data valid	t_{TDODV}	0	25	ns
12	TCLK low to TDO high Z	t_{TDODZ}	0	9	ns
13	$\overline{TRST}$ assert time	t_{TRSTAT}	100	—	ns
14	$\overline{TRST}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns
15	$\overline{DE}$ input data setup time to CLKOUT rise(1)	t_{DEDST}	10	—	ns
16	$\overline{DE}$ input data hold time after CLKOUT rise(1)	t_{DEDHT}	2	—	ns
17	CLKOUT high to $\overline{DE}$ data valid	t_{DEDV}	0	20	ns
18	CLKOUT high to $\overline{DE}$ high Z	t_{DEDZ}	0	10	ns

1. Parameters 9 and 10 apply to the $\overline{DE}$ pin when used to enable OnCE. Parameters 15 and 16 apply to the $\overline{DE}$ pin when used to request the processor to enter debug mode.

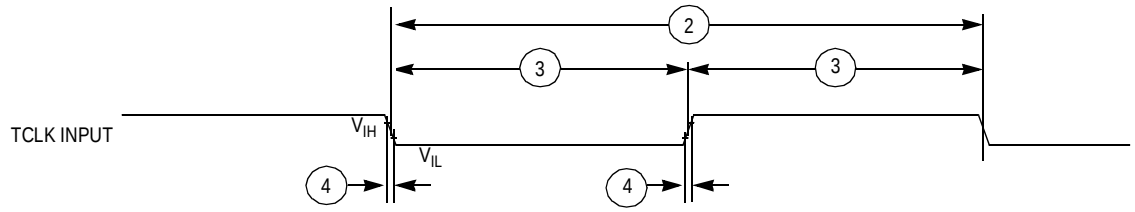

Figure 22-9. Test Clock Input Timing

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Electrical Specifications

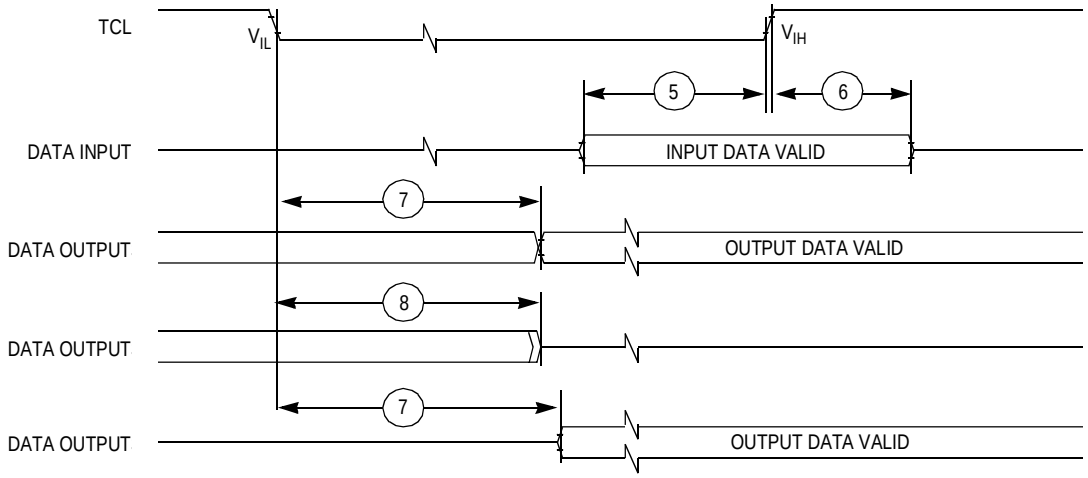

Figure 22-10. Boundary Scan (JTAG) Timing

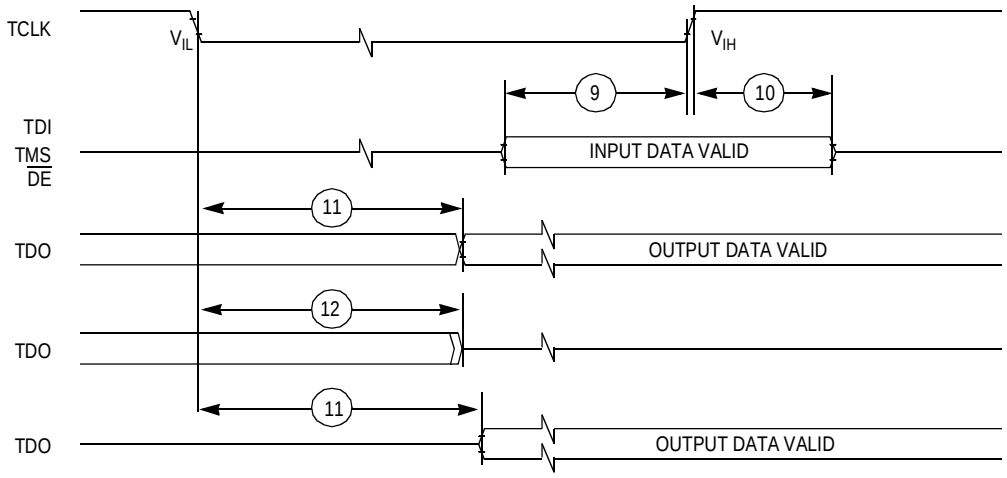

Figure 22-11. Test Access Port Timing

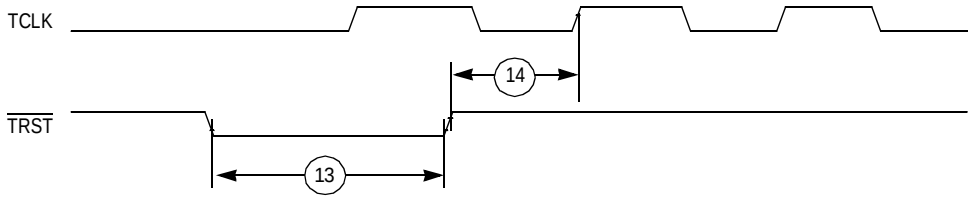

Figure 22-12. $\overline{\text{TRST}}$ Timing

Freescale Semiconductor, Inc.

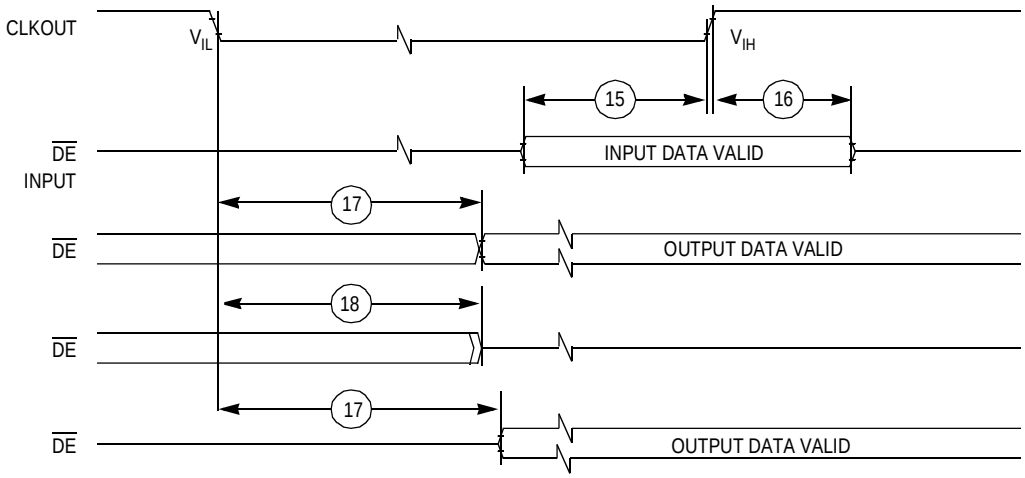

Figure 22-13. Debug Event Pin Timing

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Electrical Specifications

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Section 23. Mechanical Specifications

23.1 Contents

23.2 Introduction 609
23.3 Bond Pins 610
23.4 Package Information for the 144-Pin LQFP 611
23.5 Package Information for the 100-Pin LQFP 611
23.6 144-Pin LQFP Mechanical Drawing 612
23.7 100-Pin LQFP Mechanical Drawing 613

23.2 Introduction

The MMC2107 is available in two types of packages:

1. 100-pin low-profile quad flat pack (LQFP) version supporting single-chip mode of operation
2. 144-pin LQFP version supporting:
   - Single-chip operation with extra general-purpose input/output
   - Expanded master mode for interfacing to external memories
   - Emulation mode for development and debug

This section shows the latest package specifications available at the time of this publication. To make sure that you have the latest information, contact one of the following:

- Local Motorola Sales Office
- World Wide Web at http://www.mcu.motsps.com

Follow the World Wide Web on-line instructions to retrieve the current mechanical specifications.

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23.3 Bond Pins

The MMC2107 die has a total of 144 bond pads. Of these, the pads that are not bonded out in the 100-pin package are distributed around the circumference of the die. This optional group of pins includes:

A[22:0]

R/$\overline{W}$

$\overline{EB}$[3:0]

CSE[1:0]

TC[2:0]

$\overline{OE}$

$\overline{CS}$[3:0]

3 x V_{DD}

3 x V_{SS}

For more detailed information, see **Section 4. Signal Description**.

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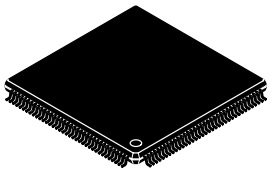
23.4 Package Information for the 144-Pin LQFP

The production 144-pin package characteristics are:

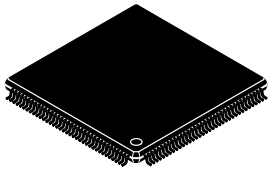
- Joint-Electron Device Engineering Council (JEDEC) standard
- Low-profile quad flat pack (LQFP)
- Dimension: 20 x 20 mm
- Lead pitch: 0.5 mm
- Thin: 1.4 mm
- Case number: 918-03
- Clam shell socket: Yamaichi part #IC51-1444-1354
- Open face socket: Yamaichi part #IC201-1444-034



23.5 Package Information for the 100-Pin LQFP

The production 100-pin package characteristics are:

- JEDEC standard
- Low-profile quad flat pack (LQFP)
- Dimension: 14 x 14 mm
- Lead pitch: 0.5 mm
- Thin: 1.4 mm
- Case number: 983-02
- Clam shell socket: Yamaichi part #IC51-1004-809
- Open face socket: Yamaichi part #IC201-1004-008



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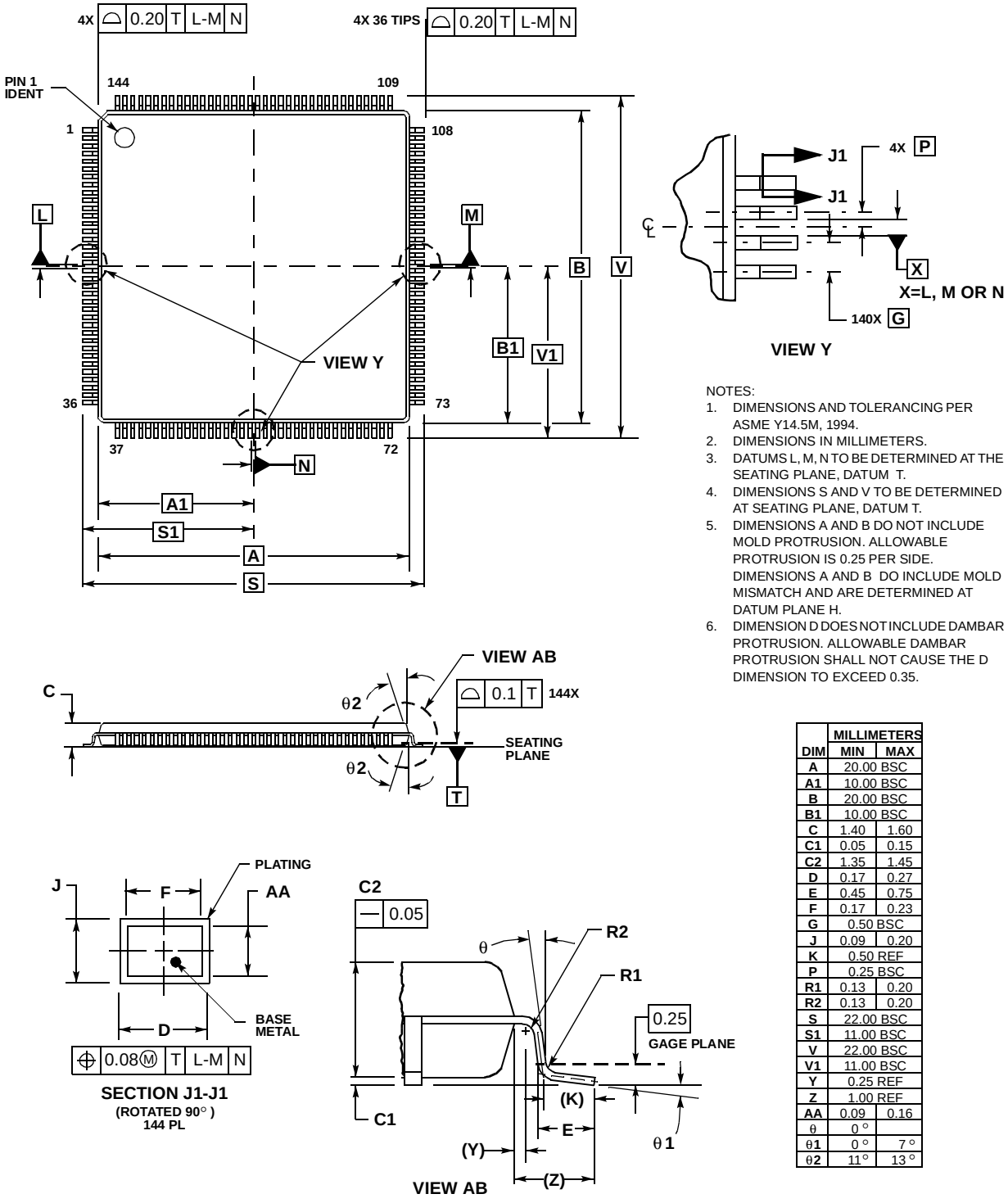
23.6 144-Pin LQFP Mechanical Drawing



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M, N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35.

	MILLIMETERS	
DIM	MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0 °	
θ1	0 °	7 °
θ2	11°	13 °

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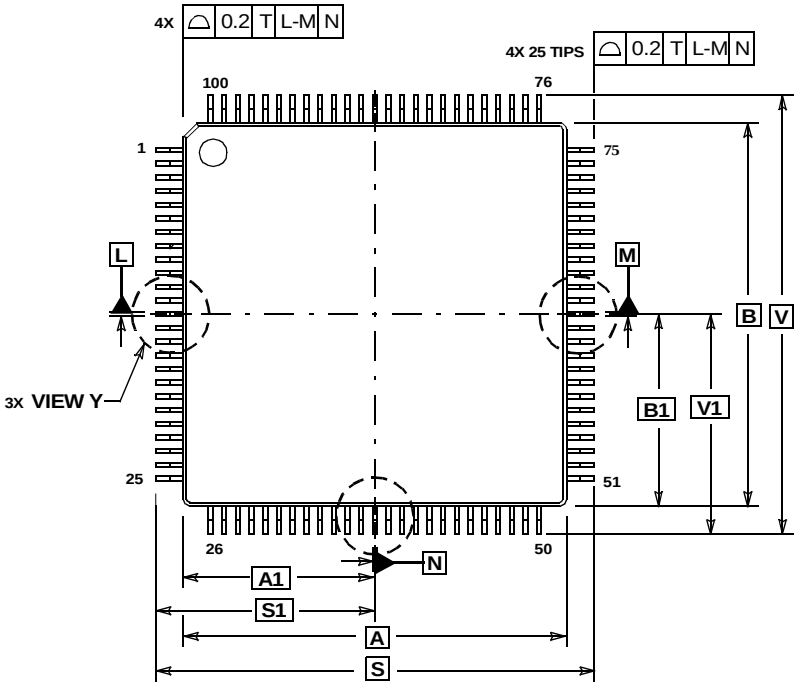
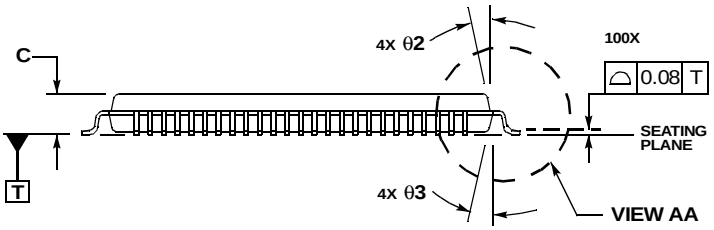
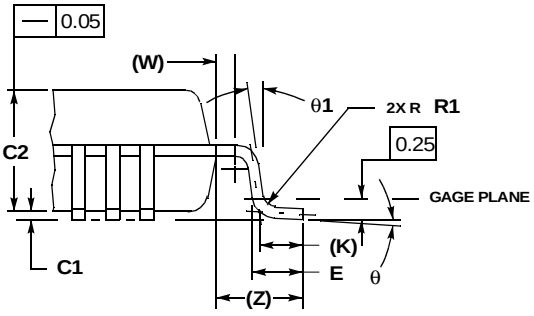
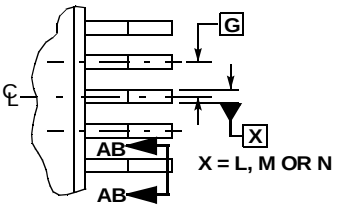
23.7 100-Pin LQFP Mechanical Drawing



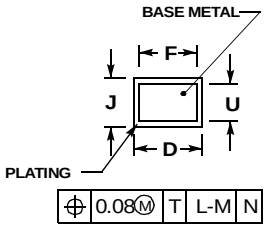




VIEW AA



VIEW Y



SECTION AB-AB
ROTATED 90° CLOCKWISE

NOTES:
1. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

	MILLIMETERS	
DIM	MIN	MAX
A	14.00 BSC	
A1	7.00 BSC	
B	14.00 BSC	
B1	7.00 BSC	
C	---	1.70
C1	0.05	0.20
C2	1.30	1.50
D	0.10	0.30
E	0.45	0.75
F	0.15	0.23
G	0.50 BSC	
J	0.07	0.20
K	0.50 REF	
R1	0.08	0.20
S	16.00 BSC	
S1	8.00 BSC	
U	0.09	0.16
V	16.00 BSC	
V1	8.00 BSC	
W	0.20 REF	
Z	1.00 REF	
θ	0°	7°
θ1	0°	---
θ2	12° REF	
θ3	12° REF	

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Mechanical Specifications

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Section 24. Ordering Information

24.1 Contents

24.2 Introduction 615
24.3 MC Order Numbers 615

24.2 Introduction

This section contains instructions for ordering the MMC2107.

24.3 MC Order Numbers

Table 24-1. MC Order Numbers

MC Order Number[1]	Operating Temperature Range
MMC2107PU	–40°C to +85°C
MMC2107PV	–40 °C to +85 °C

1. PU = 100-pin 14 x 14 mm low-profile quad flat pack (LQFP)
PV = 144-pin 20 x 20 mm LQFP

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Ordering Information

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MMC2107 Technical Data

How to Reach Us:

USA/EUROPE/LOCATIONS NOT LISTED:
Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
1-303-675-2140
1-800-441-2447

TECHNICAL INFORMATION CENTER:
1-800-521-6274

JAPAN:
Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu, Minato-ku
Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:
Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
852-26668334

HOME PAGE:
http://www.motorola.com/semiconductors/

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