

MN103001G / F01K

Type		MN103001G / F01K (under development)	
Command ROM (×64-Bit)		128 KB / 256 KB (Flash)	
Data RAM (×32-Bit)		8 KB	
Minimum Instruction Execution Time		MN103001G:	17 ns (at 3.3 V, 60 MHz)
		MN1030F01K:	25 ns (at 3.3 V, 40 MHz) (under development)
Interrupts		• RESET • IRQ × 8 • NMI • Timer × 18 • SIF × 8 • WDT • A/D • System error	
Timer Counter		Timer Counter 0 to 3: 32-Bit × 1 (Interval Timer, Event Count, Timer Output, Interrupt, Clock Source for Serial I/F, A/D Conversion Trigger) Clock Source . . . IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter Interrupt Source . . . Underflow of Timer Counter 0, 1, 2, 3 Timer Counter 4 to 7: 32-Bit × 1 (Interval Timer, Event Count, Timer Output, PWM Output, Interrupt) Clock Source . . . IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter Interrupt Source . . . Underflow of Timer Counter 4, 5, 6, 7 Timer Counter 8 to B: 32-Bit × 1 (Interval Timer, Event Count, Timer Output, PWM Output, Interrupt, Clock Source for Serial I/F) Clock Source . . . IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter Interrupt Source . . . Underflow of Timer Counter 8, 9, A, B * Each of Timer Counters 0 to 3, 4 to 7, and 8 to B can be Changed to an 8-, 16-, or 24-Bit Timer Counter Timer Counter 10: 16-Bit × 1 (Interval Timer, Event Count, PWM Output, Toggle Output (2 Lines), Interrupt, Input Capture (2 Lines), One-Shot Output) Clock Source . . . IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter Interrupt Source . . . Overflow of Timer Counter 10, Coincidence with Compare Capture (2 Lines) or at Capture Timer Counter 11: 16-Bit × 1 (Interval Timer, Event Count, Toggle Output, Interrupt) Clock Source . . . IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter Interrupt Source . . . Underflow of Timer Counter Timer Counter 12: 16-Bit × 1 (Same Functions as Those of Timer Counter 11) Timer Counter 13: 16-Bit × 1 (Same Functions as Those of Timer Counter 11) Watchdog Timer: 16- to 25-Bit × 1ch	
Serial Interface		Serial 0: 7-, 8-Bit × 1 (Clock Synchronous, Start-Stop Synchronous, I²C Mode) Serial 1, 2: 7-, 8-Bit × 2 (Clock Synchronous Mode) Serial 3: 7-, 8-Bit × 1 (Start-Stop Synchronous Mode) Clock Source . . . (Clock Synchronous Mode, Start-Stop Synchronous Mode) . . . IOCLK, Underflow of Timer Counter, External Clock (I²C Mode) . . . IOCLK, Underflow of Timer Counter	
I/O Pins	I/O	53	• Common use 53
	Output	15	• Common use 15
	Input	4	• Common use 4



A/D	10-Bit × 4ch
PWM	16-Bit × 1ch, 8-Bit × 8ch (Common with Timer)
ICR	16-Bit × 2ch (Common with OCR)
OCR	16-Bit × 2ch, 8-Bit × 8ch (Common Partially with ICR)
Package	LQFP100-P-1414

Electrical Characteristics

MN103001G

Supply Current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating Supply Current	IDD1	VDD, PVDD, AVDD = 3.3 V VI = VDD or VSS Fosc = 15.0 MHz CKSEL pin = Hi level At internal = 60 MHz Output released			180	mA
Supply current at stopping	IDD4	VDD, PVDD, AVDD = 3.465 V VI = VDD or VSS Fosc = Oscillation stopped Output released			100	μA

(Ta = -20 °C to +70 °C)

A/D Conversion Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
A/D conversion absolute Error		VREF+ = 3.3 V A/D conversion clock = 5 MHz			±7	LSB
A/D conversion relative Error					±4	LSB
A/D conversion time			2.8			μs

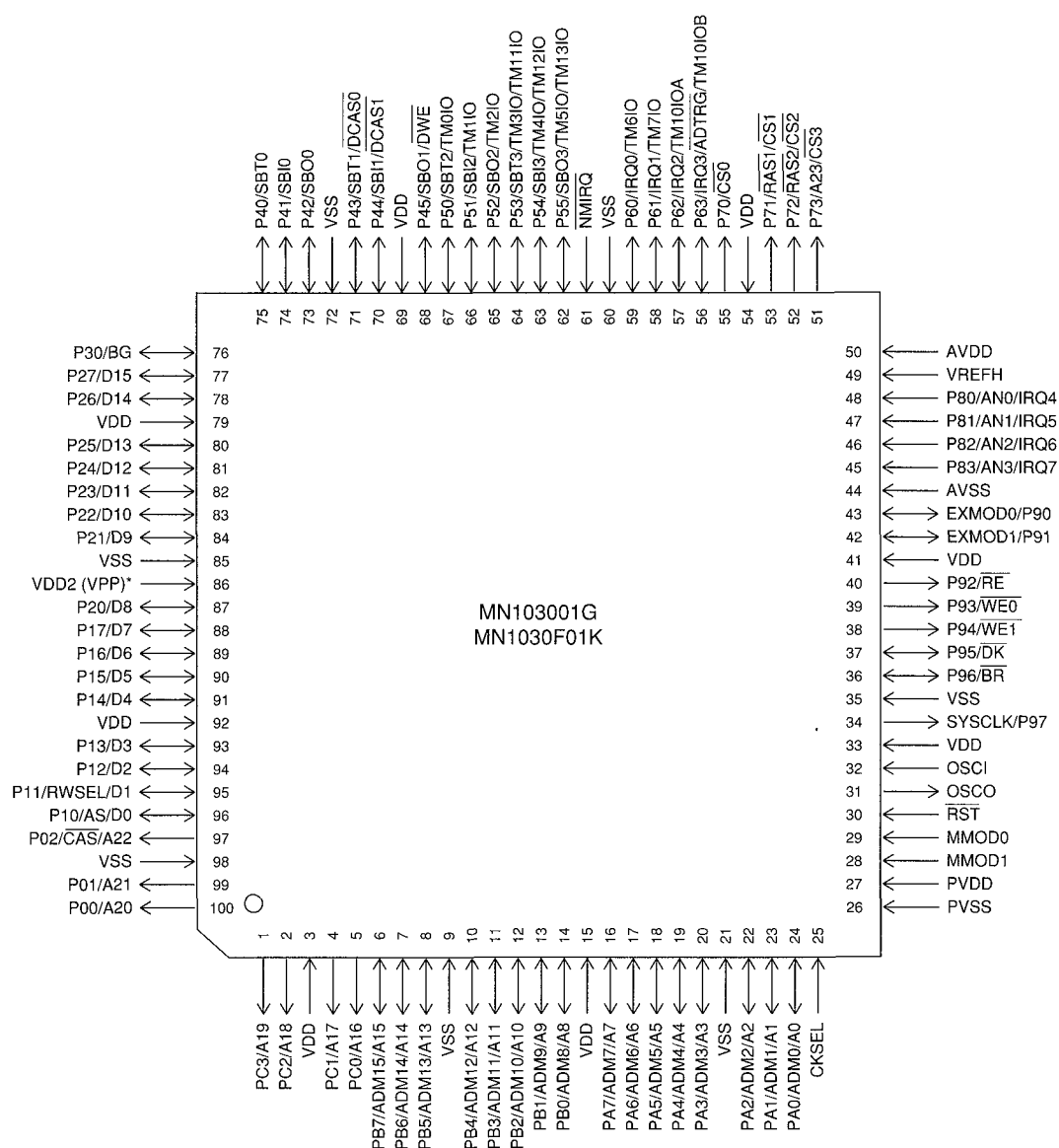
(Ta = -20 °C to +70 °C, AVDD = 3.3 V, AVSS = 0.0 V)

Support Tool

In-Circuit Emulator

PX-ICE103001

Pin Assignment



LQFP100-P-1414

* VDD2 for MN103001G and VPP for MN1030F01K