MN103002A

Type	MN103002A
Command Cache	4 KB (2-Way)
Data Cache	4 KB (2-Way)
Minimum Instruction Execution Time	**15 ns (3.3 V, 66.6 MHz)**
Interrupts	• RESET • IRQ0 to 7 • NMI • Timer 0 to 6 • SIO0 to 2 • DMAC0 to 3 • WDT • System error
Timer Counter	**Timer Counter 0: 8-Bit × 1** (Timer Output, 16-Bit Timer Clock Source, Interval Timer, Event Count, Clock Source for Serial I/F0) Clock Source . . 1/(1, 8, 32) of I/O Clock, External Clock Input, Underflow of Timer 1, 2 Interrupt Source .Underflow of Timer Counter **Timer Counter 1: 8-Bit × 1** (Timer Output, 16-Bit Timer Clock Source, Interval Timer, Event Count, Clock Source for Serial I/F1) Clock Source 1/(1, 8, 32) of I/O Clock, External Clock Input, Output of Timer Counter 0, Underflow of Timer 0, 2 Interrupt Source Underflow of Timer Counter **Timer Counter 2: 8-Bit × 1** (Timer Output, Interval Timer, Event Count, Clock Source for Serial I/F 0, 2, DMA Start) Clock Source 1/(1, 8, 32) of I/O Clock, External Clock Input, Output of Timer Counter 1, Underflow of Timer 0, 1 Interrupt Source Underflow of Timer Counter **Timer Counter 3: 8-Bit × 1** (Timer Output, Interval Timer, Event Count, Clock Source for Serial I/F 1, 2, DMA Start) Clock Source 1/(1, 8, 32) of I/O Clock, External Clock Input, Output of Timer Counter 2, Underflow of Timer 0, 1, 2 Interrupt Source Underflow of Timer Counter **Timer Counter 4: 16-Bit × 1** (Timer Output, Down Count, Interval Timer, Event Count) Clock Source . 1/(1, 8, 32) of I/O Clock, External Clock Input, Underflow of Timer 0, 1, 2 Interrupt Source Underflow of Timer Counter **Timer Counter 5: 16-Bit × 1** (Timer Output, Down Count, Interval Timer, Event Count) Clock Source .. . 1/(1, 8, 32) of I/O Clock, External Clock Input, Output of Timer Counter 4, Underflow of Timer 0, 1, 2 Interrupt Source Underflow of Timer Counter **Timer Counter 6: 16-Bit × 1** (Event Caunt, Input Capture, Toggle Output, PWM Output, High-Speed PWM Output, Up Count, Interval Timer, One-Shot Output) Clock Source 1/(1, 8, 32) of I/O Clock, External Clock Input, Underflow of Timer 0, 1, 2 Interrupt Source Overflow of Timer Counter, Compare Capture A, B **Watchdog Timer × 1** (Watchdog Overflow Output) Clock Source . . . . System Clock Interrupt Source Overflow of Watchdog Timer
DMA Controller	Number of Channels 4 Unit of Transfer 8/16/32 bits Max Transfer Cycles 65536 Starting Factor External Request, Various Types of Interrupt, Software Transfer Method. 2-Bus Cycle Transfer, 1-Bus Cycle Transfer Transfer Modes. Word Transfer, Burst Transfer, Intermittent Transfer

Serial Interface

Serial 0: 8-Bit × 1 (Start-Stop Synchronous Mode, Clock Synchronous Mode, I^2C Mode)
Clock Source . . . I/O Clock, Timer Counter 0, 2, External Clock

Serial 1: 8-Bit × 1 (Start-Stop Synchronous Mode, Clock Synchronous Mode, I^2C Mode)
Clock Source I/O Clock, Timer Counter 1, 3, External Clock

Serial 2: 8-Bit × 1 (Start-Stop Synchronous Mode with CTS Control)
Clock Source . I/O Clock, Timer Counter 2, 3, External Clock

I/O Pins

I/O	26	• Common use 26

Package

QFP160-P-2828B

Electrical Characteristics

Supply Current

Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Operating Supply Current	IDD1	Fosc = 16 6 MHz FRQS pin = Hi level Output released			250	mA
Supply current at SLEEP	IDD2	Fosc = 16 6 MHz FRQS pin = Hi level Output released			50	mA
Supply current at HALT	IDD3	Fosc = 16 6 MHz FRQS pin = Hi level Output released			6	mA
Supply current at stopping	IDD4	Fosc = Stopped Output released			1 25	mA

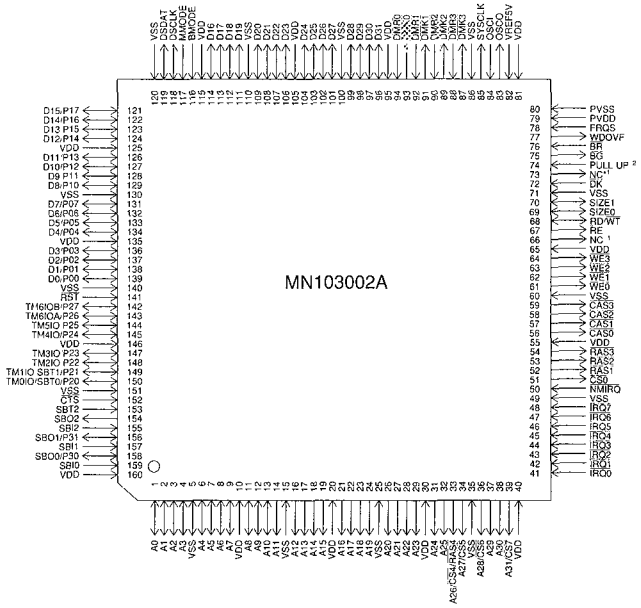
(Ta = –20 °C to +70 °C, VDD = 3.3 V, VSS = 0 V)

Support Tool

In-Circuit Emulator

PX-ICE103002

Pin Assignment



*1· Set to open
*2 Pull up via the resistor