

# DDR SDRAM Registered DIMM

**MT36VDDT12872 – 1GB**
**MT36VDDT25672 – 2GB**
**MT36VDDT51272 – 4GB**

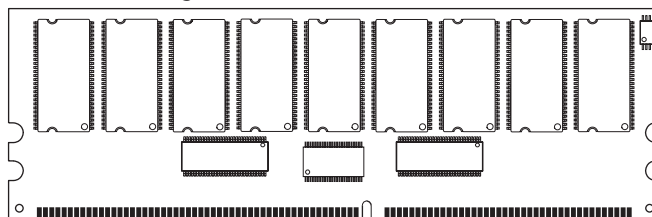
For component specifications, refer to Micron's Web site: [www.micron.com/products/ddrsdram](http://www.micron.com/products/ddrsdram)

## Features

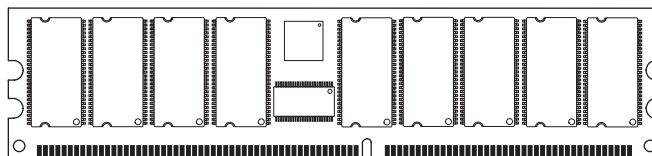
- 184-pin, dual in-line memory module (DIMM)
- Fast data transfer rates: PC2100 and PC2700
- Utilizes 266 MT/s and 333 MT/s DDR SDRAM stacked components
- Supports ECC error detection and correction
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- 1GB (128 Meg x 72), 2GB (256 Meg x 72), and 4GB (512 Meg x 72)
- VDD= VDDQ = +2.5V
- VDDSPD = +2.3V to +3.6V
- 2.5V I/O (SSTL\_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Four internal device banks for concurrent operation
- Selectable burst lengths (BL): 2, 4, or 8
- Auto refresh and self refresh modes
- 7.8125µs maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable READ CAS latency
- Gold edge contacts

**Figure 1: 184-Pin DIMM (MO-206)**

Standard PCB Height 1.7in (43.18mm)



Low Profile PCB Height 1.2in (30.48mm)



## Options

- Package
  - 184-pin DIMM (Standard)
  - 184-pin DIMM (Lead-free)<sup>1</sup>
- Memory Clock, Speed, CAS latency<sup>2</sup>
  - 6ns (167 Mhz), 333 MT/s, CL = 2.5
  - 7.5ns (133 MHz), 266 MT/s, CL = 2
  - 7.5ns (133 MHz), 266 MT/s, CL = 2
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.5
- PCB height
  - Standard 1.7in (43.18mm)
  - Low profile 1.2in (30.48mm)

## Marking

G  
Y

-335  
-262<sup>1</sup>  
-26A<sup>1</sup>  
-265<sup>1</sup>

See note,  
page 2

- Notes: 1. Contact Micron for product availability.  
 2. CL = Device CAS (READ) latency; registered mode adds one clock cycle to CL.



# 1GB, 2GB, 4GB: (x72, DR) 184-Pin DDR RDIMM Features

**Table 1: Address Table**

	1GB	2GB	4GB
Refresh count	8K	8K	8K
Row addressing	8K (A0–A12)	8K (A0–A12)	16K (A0–A13)
Device bank addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Base Device Configuration	256Mb (64 Meg x 4)	512Mb (128 Meg x 4)	1Gb (256 Meg x 4)
Column Addressing	2K (A0–A9, A11)	4K (A0–A9, A11, A12)	4K (A0–A9, A11, A12)
Module Rank Addressing	2 (S0#, S1#)	2 (S0#, S1#)	2 (S0#, S1#)

**Table 2: Part Numbers and Timing Parameters**

Part Number <sup>1</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock, Data Rate	Latency (CL - <sup>t</sup> RCD - <sup>t</sup> RP)
MT36VDDT12872G-335__	1GB	128 Meg x 72	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT36VDDT12872Y-335__	1GB	128 Meg x 72	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT36VDDT12872G-262__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT12872Y-262__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT12872G-26A__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDT12872Y-26A__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDT12872G-265__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT12872Y-265__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT25672G-335__	2GB	256 Meg x 72	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT36VDDT25672Y-335__	2GB	256 Meg x 72	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT36VDDT25672G-262__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT25672Y-262__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT25672G-26A__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDT25672Y-26A__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDT25672G-265__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDT25672Y-265__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDT51272G-335__	4GB	512 Meg x 72	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT36VDDT51272Y-335__	4GB	512 Meg x 72	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT36VDDT51272G-262__	4GB	512 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT51272Y-262__	4GB	512 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT51272G-26A__	4GB	512 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDT51272Y-26A__	4GB	512 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDT51272G-265__	4GB	512 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDT51272Y-265__	4GB	512 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

**NOTE:**

1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT36VDDT12872G-265A1.
2. Contact Micron for product availability.

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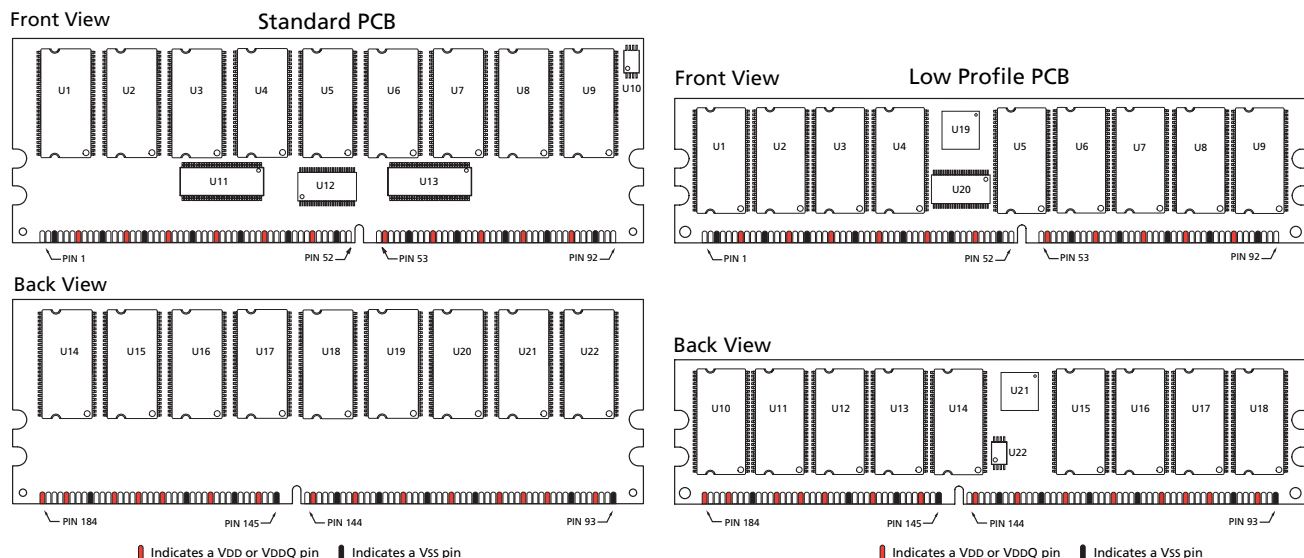
### Pin Assignments and Descriptions

**Table 3: Pin Assignments**

184-Pin DIMM Front								184-Pin DIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	24	DQ17	47	DQS8	70	VDD	93	VSS	116	VSS	139	VSS	162	DQ47
2	DQ0	25	DQS2	48	A0	71	NC	94	DQ4	117	DQ21	140	DQS17	163	NC
3	VSS	26	VSS	49	CB2	72	DQ48	95	DQ5	118	A11	141	A10	164	VDDQ
4	DQ1	27	A9	50	VSS	73	DQ49	96	VDDQ	119	DQS11	142	CB6	165	DQ52
5	DQS0	28	DQ18	51	CB3	74	VSS	97	DQS9	120	VDD	143	VDDQ	166	DQ53
6	DQ2	29	A7	52	BA1	75	DNU	98	DQ6	121	DQ22	144	CB7	167	NC/A13
7	VDD	30	VDDQ	53	DQ32	76	DNU	99	DQ7	122	A8	145	VSS	168	VDD
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ	100	VSS	123	DQ23	146	DQ36	169	DQS15
9	NC	32	A5	55	DQ33	78	DQS6	101	NC	124	VSS	147	DQ37	170	DQ54
10	RESET#	33	DQ24	56	DQS4	79	DQ50	102	NC	125	A6	148	VDD	171	DQ55
11	VSS	34	VSS	57	DQ34	80	DQ51	103	NC	126	DQ28	149	DQS13	172	VDDQ
12	DQ8	35	DQ25	58	VSS	81	VSS	104	VDDQ	127	DQ29	150	DQ38	173	NC
13	DQ9	36	DQS3	59	BA0	82	NC	105	DQ12	128	VDDQ	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DQS12	152	VSS	175	DQ61
15	VDDQ	38	VDD	61	DQ40	84	DQ57	107	DQS10	130	A3	153	DQ44	176	VSS
16	DNU	39	DQ26	62	VDDQ	85	VDD	108	VDD	131	DQ30	154	RAS#	177	DQS16
17	DNU	40	DQ27	63	WE#	86	DQS7	109	DQ14	132	VSS	155	DQ45	178	DQ62
18	VSS	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	VDDQ	179	DQ63
19	DQ10	42	VSS	65	CAS#	88	DQ59	111	CKE1	134	CB4	157	S0#	180	VDDQ
20	DQ11	43	A1	66	VSS	89	VSS	112	VDDQ	135	CB5	158	S1#	181	SA0
21	CKE0	44	CB0	67	DQS5	90	DNU	113	NC	136	VDDQ	159	DQS14	182	SA1
22	VDDQ	45	CB1	68	DQ42	91	SDA	114	DQ20	137	CK0	160	VSS	183	SA2
23	DQ16	46	VDD	69	DQ43	92	SCL	115	A12	138	CK0#	161	DQ46	184	VDDSPD

Notes: 1. Pin 167 is NC for 1GB and 2GB modules, A13 for 4GB module.

**Figure 2: 184-Pin DIMM Pin Locations**



**Table 4: Pin Descriptions**

Pin numbers may not necessarily correlate with symbols; refer to Figure 3 on page 6 for more information

Pin Numbers	Symbol	Type	Description
63, 65, 154	WE#, CAS#,RAS#	Input	Command inputs: RAS#, CAS#, and WE# define the command being entered.
137, 138	CK0, CK0#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
21, 111	CKE0, CKE1	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after VDD is applied and until CKE is first brought HIGH. After CKE is brought HIGH, it becomes an SSTL_2 input only.
157, 158	S0#, S1#	Input	Chip Select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
52, 59	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
27, 29, 32, 37, 41, 43, 48, 115, 118, 122, 125, 130, 141, 167 (4GB)	A0–A12 (1GB, 2GB) A0–A13 (4GB)	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/ WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
10	RESET#	Input	Asynchronously forces all register outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure CKE is LOW and SDRAM DQs are High-Z.
91	SDA	Input/ Output	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
92	SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
181, 182, 183	SA0–SA2	Input	Presence-detect address inputs: These pins are used to configure the presence-detect device.
44, 45, 49, 51, 134, 135, 142, 144	CB0–CB7	Input/ Output	Check bits.
5, 14, 25, 36, 47, 56, 67, 78, 86, 97, 107, 119, 129, 140, 149, 159, 169, 177	DQS0–DQS17	Input/ Output	Data strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data.

**Table 4: Pin Descriptions**

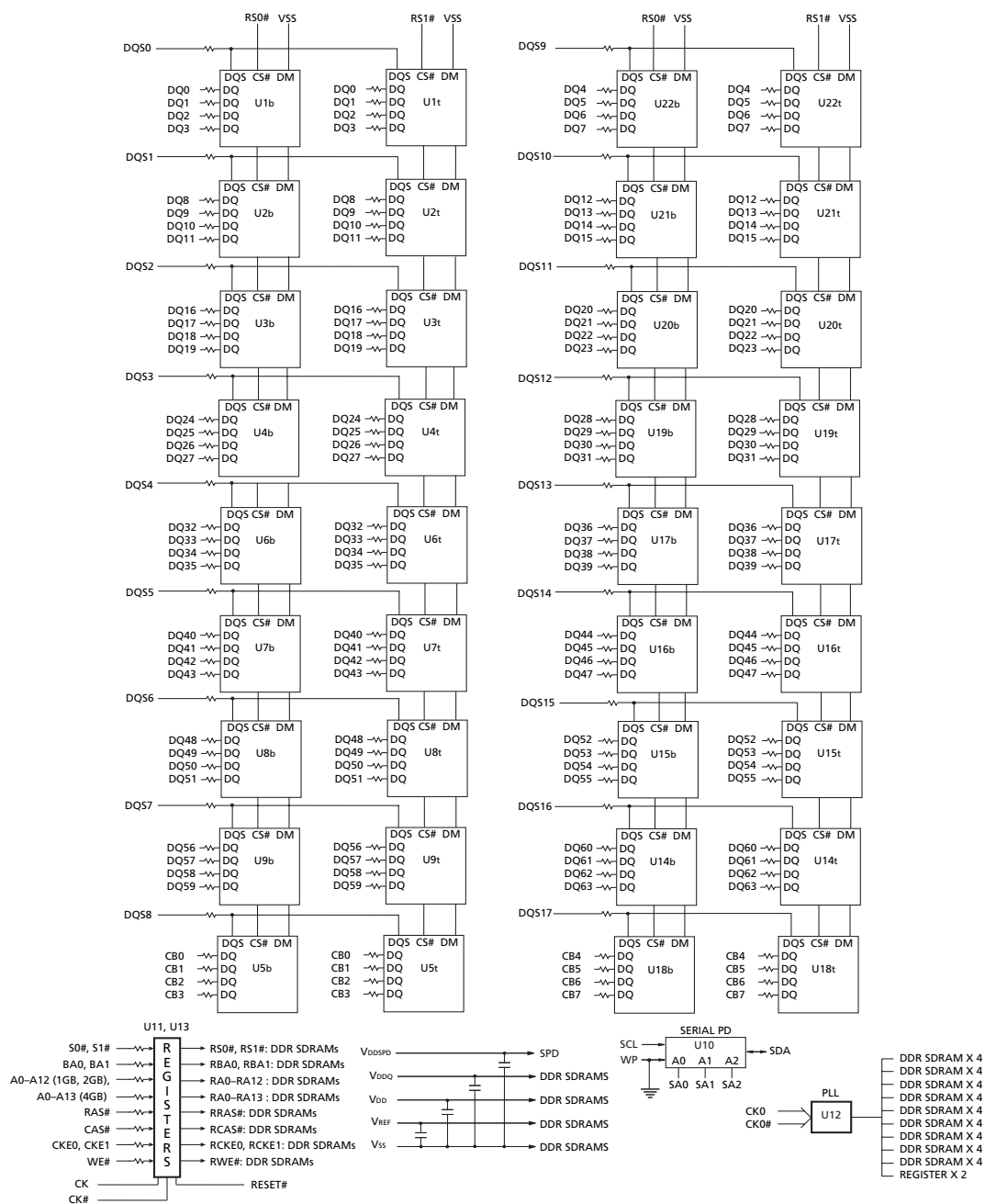
Pin numbers may not necessarily correlate with symbols; refer to Figure 3 on page 6 for more information

Pin Numbers	Symbol	Type	Description
2, 4, 6, 8, 12, 13, 19, 20, 23, 24, 28, 31, 33, 35, 39, 40, 53, 55, 57, 60, 61, 64, 68, 69, 72, 73, 79, 80, 83, 84, 87, 88, 94, 95, 98, 99, 105, 106, 109, 110, 114, 117, 121, 123, 126, 127, 131, 133, 146, 147, 150, 151, 153, 155, 161, 162, 165, 166, 170, 171, 174, 175, 178, 179	DQ0–DQ63	Input/Output	Data I/Os: Data bus.
1	VREF	Supply	SSTL_2 reference voltage.
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	VDDQ	Supply	DQ power supply: +2.5V ±0.2V.
7, 38, 46, 70, 85, 108, 120, 148, 168	VDD	Supply	Power supply: +2.5V ±0.2V.
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	VSS	Supply	Ground.
184	VDDSPD	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V.
9, 71, 82, 101, 102, 103, 113, 163, 167 (1GB, 2GB), 173	NC	–	No connect: These pins should be left unconnected.
16, 17, 75, 76, 90	DNU	–	Do not use: These pins are not connected on this module but are assigned pins on other modules in this product family.

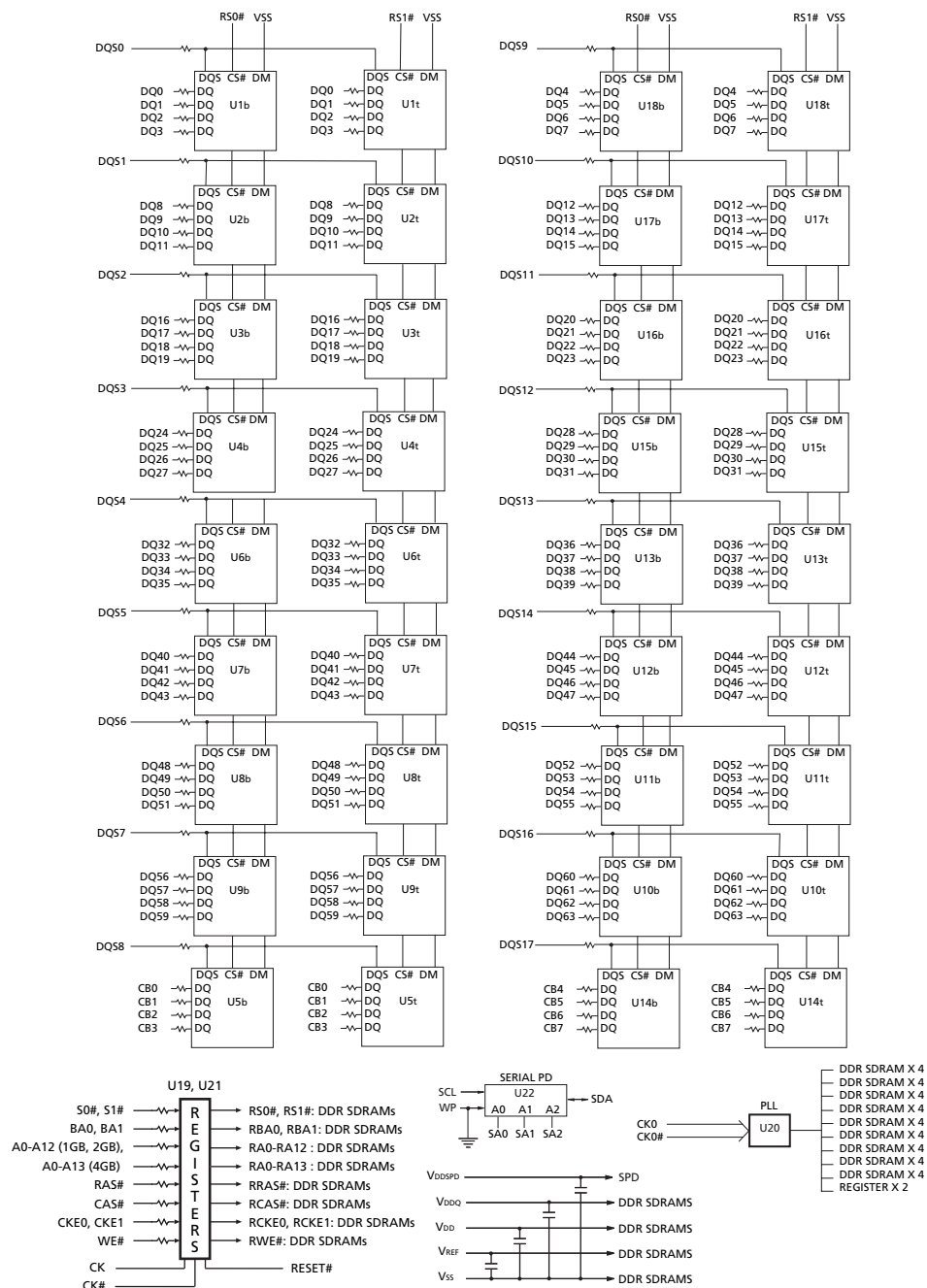


All resistor values are 22Ω unless otherwise specified. Symbol ‘b’ = bottom portion of stacked SDRAM, ‘t’ = top portion of stacked SDRAM. Per industry standard, Micron modules utilize various component speed grades, as referenced in the module part numbering guide at [www.micron.com/numberguide](http://www.micron.com/numberguide).

**Figure 3: Functional Block Diagram (Standard PCB)**



**Figure 4: Functional Block Diagram (Low-Profile PCB)**



- Notes:
1. All resistor values are 22Ω unless otherwise specified'
  2. 'b' = bottom portion of stacked SDRAM, 't' = top portion of stacked SDRAM.
  3. Per industry standard, Micron modules utilize various component speed grades, as referenced in the module part numbering guide at [www.micron.com/numberguide](http://www.micron.com/numberguide).

## General Description

The MT36VDDT12872, MT36VDDT25672 and MT36VDDT51272 are high-speed CMOS, dynamic random-access, 1GB, 2GB, and 4GB registered memory modules organized in a x72 (ECC) configuration. DDR SDRAM modules use internally configured quad-bank DDR SDRAM devices.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. Double data rate architecture is essentially a  $2n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single  $2n$ -bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding  $n$ -bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by DDR SDRAMs during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed [BA0, BA1 select device bank, A0–A12 (1GB, 2GB) or A0–A13 (4GB) select device row]. The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

DDR SDRAM modules provide for programmable read or write burst lengths (BL) of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL\_2. All outputs are SSTL\_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the 256Mb, 512MB, or 1Gb DDR SDRAM component data sheets.

## PLL and Register Operation

DDR SDRAM modules operate in registered mode where the control/address input signals are latched in the register on one rising clock edge and sent to DDR SDRAM devices on the following rising clock edge (data access is delayed by one clock). A phase-lock loop (PLL) on the module is used to redrive the differential clock signals CK and CK# to DDR SDRAM devices to minimize system clock loading.

## Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and

various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I<sup>2</sup>C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

## Mode Register Definition

The mode register is used to define the specific mode of operation of DDR SDRAM devices. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Figure 5 on page 13. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A12 (1GB, 2GB) or A7–A13 (4GB) specify the operating mode.

## Burst Length

Read and write accesses to DDR SDRAM devices are burst oriented, with the burst length being programmable, as shown in Figure 5 on page 13. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A<sub>i</sub> when the burst length is set to two, by A2–A<sub>i</sub> when the burst length is set to four and by A3–A<sub>i</sub> when the burst length is set to eight (where A<sub>i</sub> is the most significant column address bit for a given configuration; see Note 5, of Table 5 on page 14). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

## Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

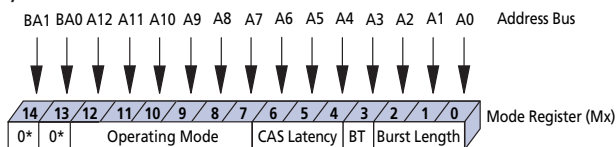
The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 5 on page 14.

## Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2, or 2.5 clocks, as shown in Figure on page 14.

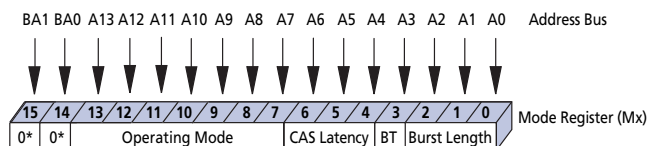
**Figure 5: Mode Register Definition Diagram**

## 1GB, 2GB Module Address Bus



\* M14 and M13 (BA1 and BA0) must be "0, 0" to select the base mode register (vs. the extended mode register).

## 4GB Module Address Bus



\* M15 and M14 (BA1 and BA0) must be "0, 0" to select the base mode register (vs. the extended mode register).

M2 M1 M0			Burst Length
			M3 = 0
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

M13	M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	-	All other states reserved

**Table 5: Burst Definition Table**

Burst Length	Starting Column Address	Order of Accesses within a Burst	
		Type = Sequential	Type = Interleaved
2	<b>A0</b>		
	0	0-1	0-1
	1	1-0	1-0
4	<b>A1 A0</b>		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	<b>A2 A1 A0</b>		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

- Notes:
1. For BL = 2, A1–Ai select the two-data-element block; A0 selects the first access within the block.
  2. For BL = 4, A2–Ai select the four-data-element block; A0–A1 select the first access within the block.
  3. For BL = 8, A3–Ai select the eight-data-element block; A0–A2 select the first access within the block.
  4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
  5.  $i = 9, 11$  (1GB);  
 $i = 9, 11, 12$  (2GB, 4GB)

## CAS Latency Diagram

If a READ command is registered at clock edge  $n$ , and the latency is  $m$  clocks, the data will be available nominally coincident with clock edge  $n + m$ . Figure on page 14, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

## Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7–A12 (1GB, 2GB) or A7–A13 (4GB) each set to zero, and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9–A12 (1GB, 2GB) or A9–A13 (4GB) each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7–A12 (1GB, 2GB) or A7–A13 (4GB) are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

## **Extended Mode Register**

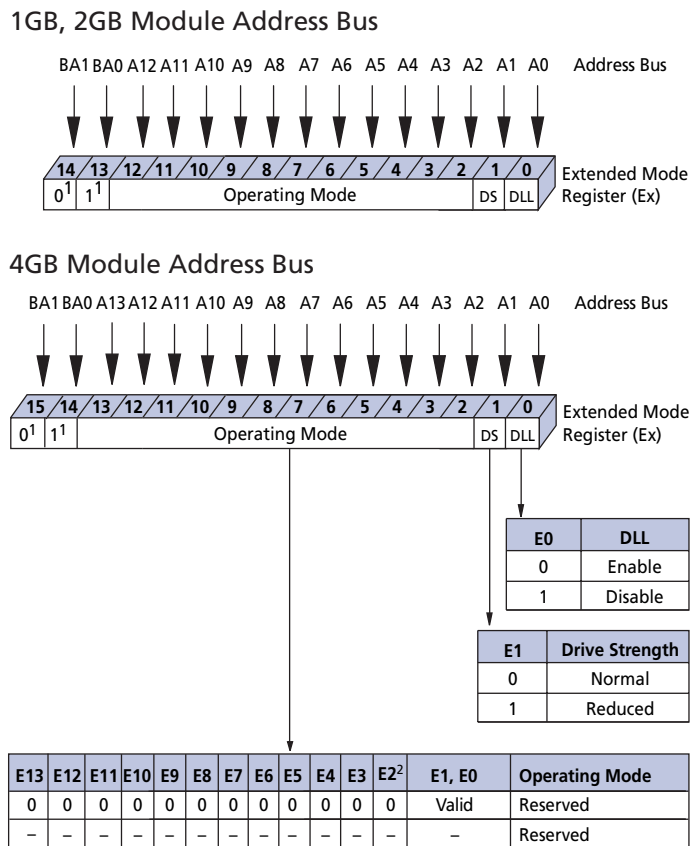
The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable and output drive strength. These functions are controlled via the bits shown in Figure 6 on page 16. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

## **DLL Enable/Disable**

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles with CKE HIGH must occur before a READ command can be issued.

**Figure 6: Extended Mode Register Definition Diagram**



- Notes: 1. BA1 and BA0 (E14 and E13 for 1GB, 2GB; E15 and E14 for 4GB), must be "0, 1" to select the Extended Mode Register (vs. the base Mode Register).
2. The QFC# option is not supported.



## Commands

Table 6 and Table 7 provide a general reference of available commands. For a more detailed description of commands and operations, refer to the Micron 256Mb, 512MB, or 1Gb DDR SDRAM component data sheet.

**Table 6: Commands Truth Table**

CKE is HIGH for all commands shown except SELF REFRESH; all states and sequences not shown are illegal or reserved

Name (Function)	CS#	RAS#	CAS#	WE#	Address	Notes
DESELECT (NOP)	H	X	X	X	X	1
NO OPERATION (NOP)	L	H	H	H	X	1
ACTIVE (Select device bank and activate row)	L	L	H	H	Bank/Row	2
READ (Select device bank and column, and start READ burst)	L	H	L	H	Bank/Col	3
WRITE (Select device bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	3
BURST TERMINATE	L	H	H	L	X	4
PRECHARGE (Deactivate row in device bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	8

- Notes:
1. Deselect and NOP are functionally interchangeable.
  2. BA0–BA1 provide device bank address and A0–A12 (1GB, 2GB) or A0–A13 (4GB) provide row address.
  3. BA0–BA1 provide device bank address; A0–A9, A11 (1GB) or A0–A9, A11, A12 (2GB, 4GB) provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
  4. Applies only to READ bursts with auto precharge disabled; this command is undefined (and should not be used) for read bursts with auto precharge enabled and for write bursts.
  5. A10 LOW: BA0–BA1 determine which device bank is precharged. A10 HIGH: all device banks are precharged and BA0–BA1 are “Don’t Care.”
  6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
  7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
  8. BA0–BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A12 (1GB, 2GB) or A0–A13 (4GB) provide the op-code to be written to the selected mode register.

**Table 7: DM Operation Truth Table**

Used to mask write data; provided coincident with the corresponding data

Name (Function)	DM	DQ
Write enable	L	Valid
Write inhibit	H	X

## Electrical Specifications

### Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

VDD Supply Voltage Relative to VSS	-1V to +3.6V
VDDQ Supply Voltage Relative to VSS	-1V to +3.6V
VREF and Inputs Voltage Relative to VSS	-1V to +3.6V
I/O Pin Voltage Relative to VSS	-0.5V to VDDQ +0.5V
Operating Temperature,	
T <sub>A</sub> (ambient - commercial)	0°C to +70°C
T <sub>A</sub> (ambient - industrial)	-40°C to +85°C
Storage Temperature (plastic)	-55°C to +150°C
Short Circuit Output Current	50mA

**Table 8: DC Electrical Characteristics and Operating Conditions**

Notes: 1–5, 14; notes appear on pages 24–28; 0°C ≤ T<sub>A</sub> ≤ +70°C

Parameter/Condition		Symbol	Min	Max	Units	Notes
Supply voltage		VDD	2.3	2.7	V	32, 36
I/O supply voltage		VDDQ	2.3	2.7	V	32, 36, 39
I/O reference voltage		VREF	0.49 x VDDQ	0.51x VDDQ	V	6, 39
I/O termination voltage (system)		VTT	VREF - 0.04	VREF + 0.04	V	7, 39
Input high (logic 1) voltage		V <sub>IH</sub> (DC)	VREF + 0.15	VDD + 0.3	V	25
Input low (logic 0) voltage		V <sub>IL</sub> (DC)	-0.3	VREF - 0.15	V	25
INPUT LEAKAGE CURRENT Any input 0V ≤ V <sub>IN</sub> ≤ VDD, VREF pin 0V ≤ V <sub>IN</sub> ≤ 1.35V (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE#, S#, CKE	I <sub>I</sub>	-5	5	μA	47
	CK, CK#		-10	10		
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V <sub>OUT</sub> ≤ VDDQ)		I <sub>OZ</sub>	-10	10	μA	47
OUTPUT LEVELS:		I <sub>OH</sub>	-16.8	–	mA	33, 34
High current (V <sub>OUT</sub> = VDDQ - 0.373V, minimum VREF, minimum VTT)		I <sub>OL</sub>	16.8	–	mA	
Low current (V <sub>OUT</sub> = 0.373V, maximum VREF, maximum VTT)						

**Table 9: AC Input Operating Conditions**

Notes: 1–5, 12, 22; notes appear on pages 24–28; 0°C ≤ T<sub>A</sub> ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

Parameter/Condition	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage	V <sub>IH</sub> (AC)	VREF + 0.310	–	V	25, 35
Input low (logic 0) voltage	V <sub>IL</sub> (AC)	–	VREF - 0.310	V	25, 35
I/O reference voltage	VREF (AC)	0.49 x VDDQ	0.51 x VDDQ	V	6

**Table 10: IDD Specifications and Conditions – 1GB**

DDR SDRAM Components Only

Notes: 1–5, 8, 10,12, 48; notes appear on pages 24–28;  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DD} = V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ 

		Max					
Parameter/Condition	Sym	-335	-262	-26A/ -265/	Units	Notes	
OPERATING CURRENT: One device bank; Active-Precharge; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	IDD0 <sup>a</sup>	2,322	2,322	2,232	mA	20, 42	
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 4; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; IOUT = 0mA; Address and control inputs changing once per clock cycle.	IDD1 <sup>a</sup>	3,132	2,952	2,682	mA	20, 42	
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = (LOW).	IDD2P <sup>b</sup>	144	144	144	mA	21, 28, 44	
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM.	IDD2F <sup>b</sup>	1,800	1,620	1,620	mA	45	
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = LOW.	IDD3P <sup>b</sup>	1,080	900	900	mA	21, 28, 44	
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; $t_{RC} = t_{RAS}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	IDD3N <sup>b</sup>	2,160	1,800	1,800	mA	41	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; IOUT = 0mA.	IDD4R <sup>a</sup>	3,222	2,772	2,772	mA	20, 42	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle.	IDD4W <sup>a</sup>	3,222	2,772	2,772	mA	20	
AUTO REFRESH CURRENT	$t_{REFC} = t_{RFC}(\text{MIN})$	IDD5 <sup>b</sup>	9,180	8,460	8,460	mA	20, 42
	$t_{REFC} = 7.81\mu\text{s}$	IDD5A <sup>b</sup>	216	216	216	mA	20, 44
SELF REFRESH CURRENT: CKE ≤ 0.2V	IDD6 <sup>b</sup>	144	144	144	mA	9	
OPERATING CURRENT: Four device bank interleaving READs (BL= 4) with auto precharge with $t_{RC}$ = minimum $t_{RC}$ allowed; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs change only during active READ or WRITE commands.	IDD7 <sup>a</sup>	7,452	6,372	6,372	mA	20, 43	

NOTE:

a: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2p (CKE LOW) mode.

b: Value calculated reflects all module ranks in this operating condition.

**Table 11: IDD Specifications and Conditions – 2GB**

DDR SDRAM Components Only

Notes: 1–5, 8, 10,12, 48; notes appear on pages 24–28;  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DD} = V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ 

		Max					
Parameter/Condition	Sym	-335	-262	-26A/ -265/	Units	Notes	
OPERATING CURRENT: One device bank; Active-Precharge; $t_{RC} = t_{RC}$ (MIN); $t_{CK} = t_{CK}$ (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	IDD0 <sup>a</sup>	2,430	2,430	2,160	mA	20, 42	
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 4; $t_{RC} = t_{RC}$ (MIN); $t_{CK} = t_{CK}$ (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle.	IDD1 <sup>a</sup>	2,970	2,970	2,700	mA	20, 42	
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; $t_{CK} = t_{CK}$ (MIN); CKE = (LOW).	IDD2P <sup>b</sup>	180	180	180	mA	21, 28, 44	
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK}$ MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM.	IDD2F <sup>b</sup>	1,620	1,620	1,440	mA	45	
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; $t_{CK} = t_{CK}$ (MIN); CKE = LOW.	IDD3P <sup>b</sup>	1,260	1,260	1,080	mA	21, 28, 44	
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; $t_{RC} = t_{RAS}$ (MAX); $t_{CK} = t_{CK}$ (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	IDD3N <sup>b</sup>	1,800	2,160	1,800	mA	41	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}$ (MIN); IOUT = 0mA.	IDD4R <sup>a</sup>	3,060	3,060	2,700	mA	20, 42	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle.	IDD4W <sup>a</sup>	3,240	2,880	2,520	mA	20	
AUTO REFRESH CURRENT	$t_{REFC} = t_{RFC}$ (MIN)	IDD5 <sup>b</sup>	10,440	10,440	10,080	mA	20, 42
	$t_{REFC} = 7.81\mu s$	IDD5A <sup>b</sup>	360	360	360	mA	20, 44
SELF REFRESH CURRENT: CKE ≤ 0.2V	IDD6 <sup>b</sup>	180	180	180	mA	9	
OPERATING CURRENT: Four device bank interleaving READs (BL= 4) with auto precharge with $t_{RC}$ = minimum $t_{RC}$ allowed; $t_{CK} = t_{CK}$ (MIN); Address and control inputs change only during active READ or WRITE commands.	IDD7 <sup>a</sup>	7,380	7,290	6,390	mA	20, 43	

NOTE:

a: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2p (CKE LOW) mode.

b: Value calculated reflects all module ranks in this operating condition.

**Table 12: IDD Specifications and Conditions – 4GB**

DDR SDRAM Components Only

Notes: 1–5, 8, 10,12, 48; notes appear on pages 24–28;  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DD} = V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ 

		Max					
Parameter/Condition	Sym	-335	-262	-26A/ -265/	Units	Notes	
OPERATING CURRENT: One device bank; Active-Precharge; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	IDD0 <sup>a</sup>	2,430	2,430	2,790	mA	20, 42	
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 4; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; IOUT = 0mA; Address and control inputs changing once per clock cycle.	IDD1 <sup>a</sup>	2,970	2,970	3,420	mA	20, 42	
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = (LOW).	IDD2P <sup>b</sup>	180	180	360	mA	21, 28, 44	
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM.	IDD2F <sup>b</sup>	1,620	1,620	2,160	mA	45	
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = LOW.	IDD3P <sup>b</sup>	1,260	1,260	1,080	mA	21, 28, 44	
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; $t_{RC} = t_{RAS}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	IDD3N <sup>b</sup>	1,620	1,620	1,620	mA	41	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; IOUT = 0mA.	IDD4R <sup>a</sup>	3,060	3,060	3,780	mA	20, 42	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle.	IDD4W <sup>a</sup>	2,880	2,880	3,960	mA	20	
AUTO REFRESH CURRENT	$t_{REFC} = t_{RFC}(\text{MIN})$	IDD5 <sup>b</sup>	10,440	10,440	11,880	mA	20, 42
	$t_{REFC} = 7.81\mu\text{s}$	IDD5A <sup>b</sup>	360	360	360	mA	20, 44
SELF REFRESH CURRENT: CKE ≤ 0.2V	IDD6 <sup>b</sup>	180	180	324	mA	9	
OPERATING CURRENT: Four device bank interleaving READs (BL= 4) with auto precharge with $t_{RC} = \text{minimum } t_{RC} \text{ allowed}$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs change only during active READ or WRITE commands.	IDD7 <sup>a</sup>	7,380	7,380	8,910	mA	20, 43	

NOTE:

a: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2p (CKE LOW) mode.

b: Value calculated reflects all module ranks in this operating condition.

**Table 13: Capacitance**

Note: 11; notes appear on pages 24–28

Parameter	Symbol	Min	Max	Units
Input/Output capacitance: DQ, DQS	CIO	8.0	10.0	pF
Input capacitance: command and address, CKE, CK, CK#	CI1	2.5	3.5	pF



# 1GB, 2GB, 4GB: (x72, SR) 184-Pin DDR RDIMM Electrical Specifications

**Table 14: DDR Device Electrical Characteristics and Recommended AC Operating Conditions**

Notes: 1–5, 12–15, 29; notes appear on pages 24–28;  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DD} = V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$

AC Characteristics		-335		-262		-26A/-265		Units	Notes
Parameter	Sym	Min	Max	Min	Max	Min	Max		
Access window of DQ from CK/CK#	$t_{AC}$	-0.7	+0.7	-0.70	+0.70	-0.75	+0.75	ns	
CK high-level width	$t_{CH}$	0.45	0.55	0.45	0.55	0.45	0.55	$t_{CK}$	26
CK low-level width	$t_{CL}$	0.45	0.55	0.45	0.55	0.45	0.55	$t_{CK}$	26
Clock cycle time	CL = 2.5 $t_{CK} (2.5)$	6	13	6	13	7.5	13	ns	40, 46
	CL = 2 $t_{CK} (2)$	7.5	13	7.5	13	10/7.5	13	ns	40, 46
DQ and DM input hold time relative to DQS	$t_{DH}$	0.45		0.45		0.5		ns	23, 27
DQ and DM input setup time relative to DQS	$t_{DS}$	0.45		0.45		0.5		ns	23, 27
DQ and DM input pulse width (for each input)	$t_{DIPW}$	1.75		1.75		1.75		ns	27
Access window of DQS from CK/CK#	$t_{DQSCK}$	-0.60	+0.60	-0.65	+0.6	-0.75	+0.75	ns	
DQS input high pulse width	$t_{DQSH}$	0.35		0.35		0.35		$t_{CK}$	
DQS input low pulse width	$t_{DQSL}$	0.35		0.35		0.35		$t_{CK}$	
DQS-DQ skew, DQS to last DQ valid, per group, per access	$t_{DQSQ}$		0.45		0.45		0.5	ns	22, 23
Write command to first DQS latching transition	$t_{DQSS}$	0.75	1.25	0.75	1.25	0.75	1.25	$t_{CK}$	
DQS falling edge to CK rising - setup time	$t_{DSS}$	0.2		0.2		0.2		$t_{CK}$	
DQS falling edge from CK rising - hold time	$t_{DSH}$	0.2		0.2		0.2		$t_{CK}$	
Half clock period	$t_{HP}$	$t_{CH}, t_{CL}$		$t_{CH}, t_{CL}$		$t_{CH}, t_{CL}$		ns	30
Data-out high-impedance window from CK/CK#	$t_{HZ}$		+0.70		+0.7		+0.75	ns	16, 37
Data-out low-impedance window from CK/CK#	$t_{LZ}$	-0.70		-0.7		-0.75		ns	16, 37
Address and control input hold time (fast slew rate)	$t_{IH_f}$	0.75		0.75		0.90		ns	12
Address and control input setup time (fast slew rate)	$t_{IS_f}$	0.75		0.75		0.90		ns	12
Address and control input hold time (slow slew rate)	$t_{IH_s}$	0.80		0.8		1		ns	
Address and control input setup time (slow slew rate)	$t_{IS_s}$	0.80		0.8		1		ns	
Address and Control input pulse width (for each input)	$t_{IPW}$	2.2		2.2		2.2		ns	
LOAD MODE REGISTER command cycle time	$t_{MRD}$	12		15		15		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	$t_{QH}$	$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$		ns	22, 23
Data Hold Skew Factor	$t_{QHS}$		0.55		0.75		0.75	ns	
ACTIVE to PRECHARGE command	$t_{RAS}$	42	70,000	40	120,000	40	120,000	ns	31, 49
ACTIVE to READ with Auto precharge command	$t_{RAP}$	15		15		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period	$t_{RC}$	60		60		65		ns	
AUTO REFRESH command period	1GB, 2GB 4GB $t_{RFC}$	72		75		75		ns	44
		120		120		120		ns	44
ACTIVE to READ or WRITE delay	$t_{RCD}$	15		15		20		ns	
PRECHARGE command period	$t_{RP}$	15		15		20		ns	
DQS read preamble	$t_{RPRE}$	0.9	1.1	0.9	1.1	0.9	1.1	$t_{CK}$	38
DQS read postamble	$t_{RPST}$	0.4	0.6	0.4	0.6	0.4	0.6	$t_{CK}$	38

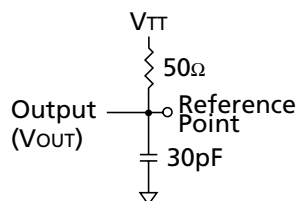
**Table 14: DDR Device Electrical Characteristics and Recommended AC Operating Conditions (Continued)**

AC Characteristics		-335		-262		-26A/-265		Units	Notes
Parameter	Sym	Min	Max	Min	Max	Min	Max		
ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command	$t_{RRD}$	12		15		15		ns	
DQS write preamble	$t_{WPRE}$	0.25		0.25		0.25		$t_{CK}$	
DQS write preamble setup time	$t_{WPRES}$	0		0		0		ns	18, 19
DQS write postamble	$t_{WPST}$	0.4	0.6	0.4	0.6	0.4	0.6	$t_{CK}$	17
Write recovery time	$t_{WR}$	15		15		15		ns	
Internal WRITE to READ command delay	$t_{WTR}$	1		1		1		$t_{CK}$	
Data valid output window (DVW)	na	$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		ns	22
REFRESH to REFRESH command interval	$t_{REFC}$		70.3		70.3		70.3	$\mu s$	21
Average periodic refresh interval	$t_{REFI}$		7.8		7.8		7.8	$\mu s$	21
Terminating voltage delay to $V_{DD}$	$t_{VTD}$	0		0		0		ns	
Exit SELF REFRESH to non-READ command	1GB, 2GB	$t_{XSNR}$	75		75		75	ns	
	4GB		127.5		127.5		127.5	ns	
Exit SELF REFRESH to READ command	$t_{XSRD}$	200		200		200		$t_{CK}$	



## Notes

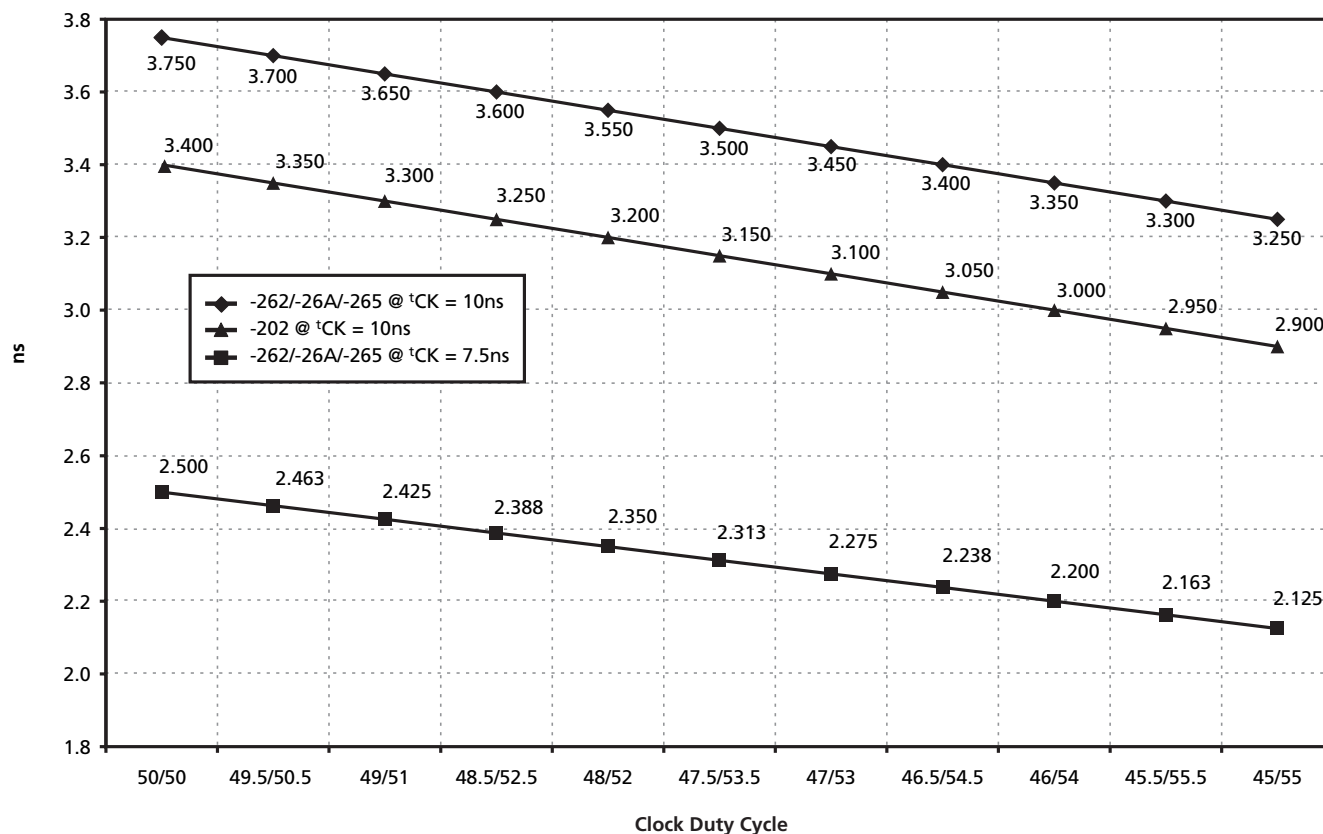
1. All voltages referenced to VSS.
2. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between VIL(AC) and VIH(AC).
5. The AC and DC input level specifications are as defined in the SSTL\_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on VREF may not exceed  $\pm 2$  percent of the DC value, so Vref is allowed  $\pm 25$ mV for DC error and  $\pm 25$ mV for AC noise from VDDQ/2. Measurement taken at the nearest VREF bypass capacitor.
7. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
8. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at -335 and with the outputs open.
9. Enables on-chip refresh and address counters.
10. IDD specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. VDD = +2.5V  $\pm 0.2$ V, VDDQ = +2.5V  $\pm 0.2$ V, VREF = VSS, f = 100 MHz, TA = 25°C, VOUT(DC) = VDDQ/2, VOUT (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. For slew rates less than 1 V/ns and greater than or equal to 0.5 V/ns. If slew rate is less than 0.5 V/ns, timing must be derated: tIS has an additional 50ps per each 100 mV/ns reduction in slew rate from 500 mV/ns, while tIH is unaffected. If slew rate exceeds 4.5 V/ns, functionality is uncertain. For -335, slew rates must be  $\geq 0.5$  V/ns.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is VREF.
14. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE  $\leq 0.3 \times$  VDDQ is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is VTT.



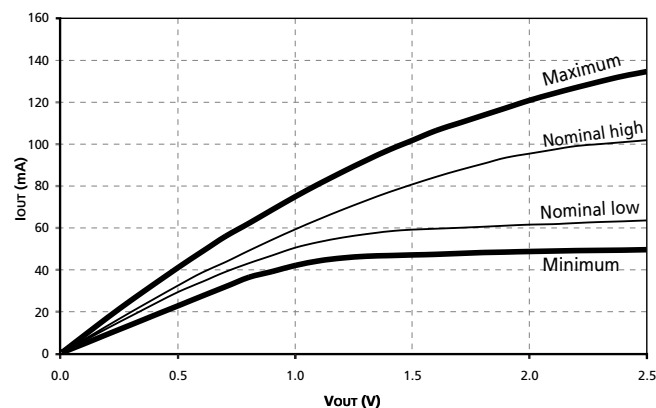
16.  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The intent of the “Don’t Care” state after completion of the postamble is the DQS-driven signal should either be HIGH, LOW, or High-Z and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions high [above  $V_{IH\ DC}$  (MIN)] then it must not transition LOW (below  $V_{IH[DC]}$ ) prior to  $t_{DQSH}$  (MIN).
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on  $t_{DQSS}$ .
20. MIN ( $t_{RC}$  or  $t_{RFC}$ ) for IDD measurements is the smallest multiple of  $t_{CK}$  that meets the minimum absolute value for the respective parameter.  $t_{RAS}$  (MAX) for IDD measurements is the largest multiple of  $t_{CK}$  that meets the maximum absolute value for  $t_{RAS}$ .
21. The refresh period 64ms. This equates to an average refresh rate of 7.8125 $\mu$ s. However, an AUTO REFRESH command must be asserted at least once every 70.3 $\mu$ s; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
22. The valid data window is derived by achieving other specifications:  $t_{HP}$  ( $t_{CK}/2$ ),  $t_{DQSQ}$ , and  $t_{QH}$  ( $t_{QH} = t_{HP} - t_{QHS}$ ). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, beyond which functionality is uncertain. Figure 7 on page 26, shows derating curves for duty cycles ranging between 50/50 and 45/55.
23. Each DQ byte lane has a corresponding DQS.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period ( $t_{RFC}$  [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
  - a. Sustain a constant slew rate from the current AC level through to the target AC level,  $V_{IL(AC)}$  or  $V_{IH(AC)}$ .
  - b. Reach at least the target AC level.
  - c. After the AC target level is reached, continue to maintain at least the target DC level,  $V_{IL(DC)}$  or  $V_{IH(DC)}$ .
26. JEDEC specifies CK and CK# input slew rate must be  $\geq 1V/ns$  (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to  $t_{DS}$  and  $t_{DH}$  for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.
28. VDD must not vary more than 4 percent if CKE is not active while any bank is active.
29. The clock is allowed up to  $\pm 150ps$  of jitter. Each timing parameter is allowed to vary by the same amount.
30.  $t_{HP}$  min is the lesser of  $t_{CL}$  minimum and  $t_{CH}$  minimum actually applied to the device CK and CK# inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until  $t_{RAS(MIN)}$  can be satisfied prior to the internal precharge command being issued.

**Figure 7: Derating Data Valid Window ( $t_{QH} - t_{DQSQ}$ )**


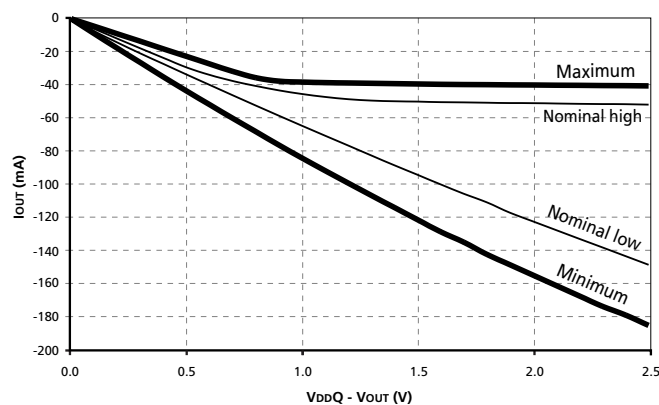
32. Any positive glitch must be less than 1/3 of the clock and not more than +400mV or 2.9V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2V, whichever is more positive.
33. Normal Output Drive Curves:
  - a. The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 8 on page 27.
  - b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 8 on page 27.
  - c. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 9 on page 27.
  - d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 9 on page 27.
  - e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature.
  - f. The full variation in the ratio of the nominal pull-up to pull-down current should be unity  $\pm 10$  percent, for device drain-to-source voltages from 0.1V to 1.0V.
34. The voltage levels used are derived from a minimum VDD level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.

35.  $V_{IH}$  overshoot:  $V_{IH}(MAX) = V_{DDQ} + 1.5V$  for a pulse width  $\leq 3ns$  and the pulse width can not be greater than 1/3 of the cycle rate.  $V_{IL}$  undershoot:  $V_{IL}(MIN) = -1.5V$  for a pulse width  $\leq 3ns$  and the pulse width can not be greater than 1/3 of the cycle rate.
36.  $V_{DD}$  and  $V_{DDQ}$  must track each other.
37.  $t_{HZ}$  (MAX) will prevail over  $t_{DQSCK}$  (MAX) +  $t_{RPST}$  (MAX) condition.  $t_{LZ}$  (MIN) will prevail over  $t_{DQSCK}$  (MIN) +  $t_{RPRE}$  (MAX) condition.
38.  $t_{RPST}$  end point and  $t_{RPRE}$  begin point are not referenced to a specific voltage level but specify when the device output is no longer driving ( $t_{RPST}$ ), or begins driving ( $t_{RPRE}$ ).
39. During initialization,  $V_{DDQ}$ ,  $V_{TT}$ , and  $V_{REF}$  must be equal to or less than  $V_{DD} + 0.3V$ . Alternatively,  $V_{TT}$  may be 1.35V maximum during power up, even if  $V_{DD}/V_{DDQ}$  are 0.0V, provided a minimum of  $42\Omega$  of series resistance is used between the  $V_{TT}$  supply and the input pin.
40. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
41. For the -335, -262, -26A, and -265 speed grades,  $I_{DD3N}$  is specified to be 35mA per DDR SDRAM device.
42. Random addressing changing and 50 percent of data changing at every transfer.
43. Random addressing changing and 100 percent of data changing at every transfer.

**Figure 8: Pull-Down Characteristics**



**Figure 9: Pull-Up Characteristics**



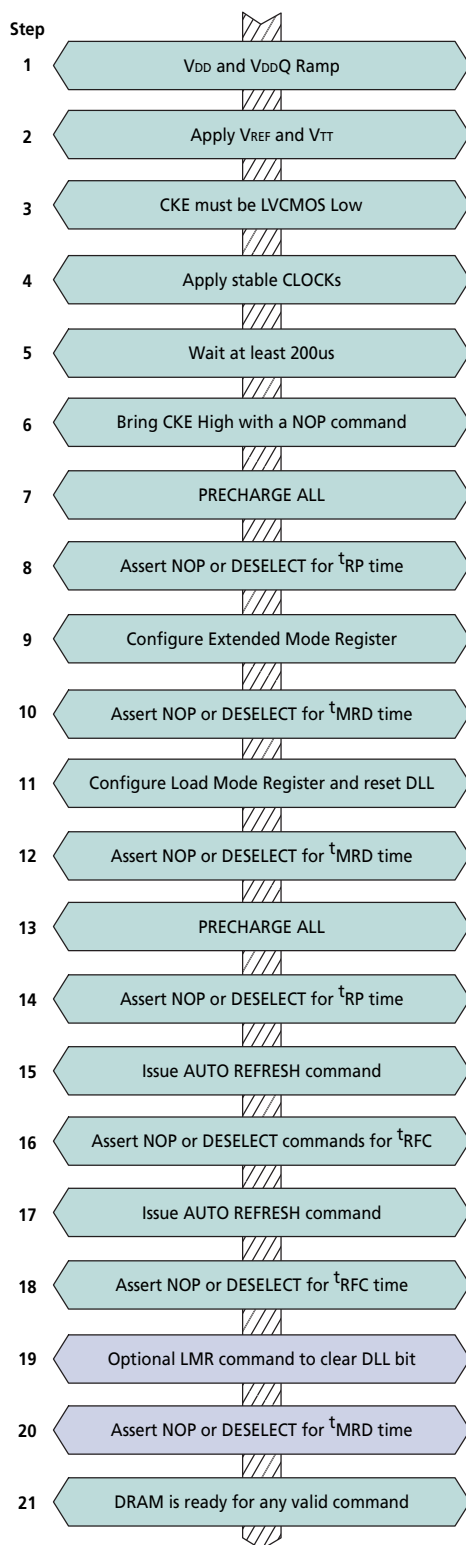
44. CKE must be active (HIGH) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until  $t_{REF}$  later.
45. IDD2N specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is “worst case.”
46. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles.
47. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
48. When an input signal is HIGH or LOW, it is defined as a steady state logic HIGH or LOW.
49. The -335 speed grade will operate with  $t_{RAS} (MIN) = 40ns$  and  $t_{RAS} (MAX) = 120,000ns$  at any slower frequency.

## Initialization

To ensure device operation, DDR devices must be initialized as described below:

1. Simultaneously apply power to VDD and VDDQ.
2. Apply VREF and then VTT power.
3. Assert and hold CKE at a LVCMOS logic low.
4. Provide stable CLOCK signals.
5. Wait at least 200µs.
6. Bring CKE HIGH and provide at least one NOP or DESELECT command. At this point the CKE input changes from a LVCMOS input to a SSTL2 input only and will remain a SSTL\_2 input unless a power cycle occurs.
7. Perform a PRECHARGE ALL command.
8. Wait at least  $t_{RP}$  time, during this time NOP or DESELECT commands must be given.
9. Using the LMR command program the extended mode register (E0 = 0 to enable the DLL and E1 = 0 for normal drive or E1 = 1 for reduced drive, E2 through En must be set to 0; where n = most significant bit).
10. Wait at least  $t_{MRD}$  time; only NOP or DESELECT commands are allowed.
11. Using the LMR command program the mode register to set operating parameters and to reset the DLL. At least 200 clock cycles are required between a DLL reset and any READ command.
12. Wait at least  $t_{MRD}$  time, only NOP or DESELECT commands are allowed.
13. Issue a PRECHARGE ALL command.
14. Wait at least  $t_{RP}$  time, only NOP or DESELECT commands are allowed.
15. Issue an AUTO REFRESH command (this may be moved prior to step 13).
16. Wait at least  $t_{RFC}$  time; only NOP or DESELECT commands are allowed.
17. Issue an AUTO REFRESH command (this may be moved prior to step 13).
18. Wait at least  $t_{RFC}$  time; only NOP or DESELECT commands are allowed.
19. Although not required by the Micron device, JEDEC requires a LMR command to clear the DLL bit (set M8 = 0). If a LMR command is issued the same operating parameters should be utilized as in step 11.
20. Wait at least  $t_{MRD}$  time; only NOPs or DESELECT commands are allowed.
21. At this point the DDR devices are ready for any valid command. Note that 200 clock cycles are required between step 11 (DLL Reset) and any READ command.

**Figure 10: Initialization Flow Diagram**



## PLL and Register Specifications

**Table 15: Register Timing Requirements and Switching Characteristics**

Note: 1

Register	Symbol	Parameter	Conditions	0°C ≤ T <sub>A</sub> ≤ +70°C V <sub>DD</sub> = +2.5V ±0.2V		Units	Notes
				Min	Max		
SSTL (bit pattern by JESD82-3 or JESD82-4)	t <sub>CK</sub>	Clock frequency		60	170	MHz	
	t <sub>PD</sub>	Clock to output time	30pF to GND and 50Ω to V <sub>TT</sub>	1.1	2.7	ns	
	t <sub>RST</sub>	Reset to output time		–	5	ns	
	t <sub>SL</sub>	Output slew rate		0.5	4	V/ns	
	t <sub>su</sub>	Setup time, fast slew rate (see notes 1 and 3)		–	0.75	ns	2, 4
		Setup time, slow slew rate (see notes 2 and 3)		–	0.9	ns	3, 4
	t <sub>h</sub>	Hold time, fast slew rate (see notes 1 and 3)		–	0.75	ns	2, 4
		Hold time, slow slew rate (see notes 2 and 3)		–	0.9	ns	3, 4
	C <sub>IN</sub> (CK)	Clock input capacitance		2.5	3.5	pF	
	C <sub>IN</sub> (data)	Data input capacitance		2.5	3.5	pF	

Notes: 1. The timing specifications for the register listed above are critical for proper operation of DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information on this part has been shown at the JEDEC JC-40 Committee. Please contact Micron Technology's module applications team if further information on the specific register model is required.

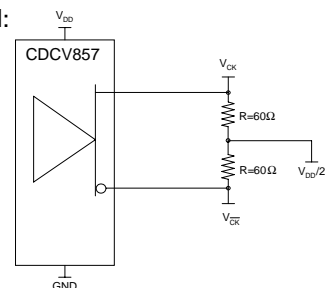
2. For data signal, input slew rate ≥ 1 V/ns.
3. For data signal, input slew rate ≥ 0.5 V/ns and < 1 V/ns.
4. For CK and CK# signals, input slew rates are ≥ 1 V/ns.

**Table 16: PLL Clock Driver Timing Requirements and Switching Characteristics**

Note: 1; specifications for the PLL component used on the module

Parameter	Symbol	Test Conditions	0°C ≤ T <sub>A</sub> ≤ +70°C V <sub>DD</sub> = +2.5V ±0.2V			Units	Notes
			Min	Nom	Max		
Clock frequency	f <sub>C</sub>		66		167	MHz	2, 3
Input clock duty cycle			40%		60%		
Stabilization time <sup>1</sup>					0.1	ms	4
Low-to high level propagation delay time	t <sub>PLH</sub>	CK mode/CK to any output	1.5	3.5	6	ns	
High-to low level propagation delay time	t <sub>PHL</sub>	CK mode/CK to any output	1.5	3.5	6	ns	5
Output enable time	t <sub>en</sub>	CK mode/G to any Y output		3		ns	
Output disable time	t <sub>dis</sub>	CK mode/G to any Y output		3		ns	6
Jitter (peak-to-peak)	t <sub>(jitter)</sub>	66 MHz			120	ps	6
		100/125/133/167 MHz			75		
Jitter (cycle-to-cycle)	t <sub>(jitter)</sub>	66 MHz			110	ps	7
		100/125/133/167 MHz			65		2, 3
Phase error	t <sub>(phase error)</sub>	Terminated with 120Ω/16pF	-150		150	ns	
							4
Output skew	t <sub>skew(o)</sub>	Terminated with 120Ω/16pF			100	ns	
Pulse skew	t <sub>dis</sub>	Terminated with 120Ω/16pF			100	ns	5
Duty cycle		66 MHz to 100 MHz	49.5%		50.5%		

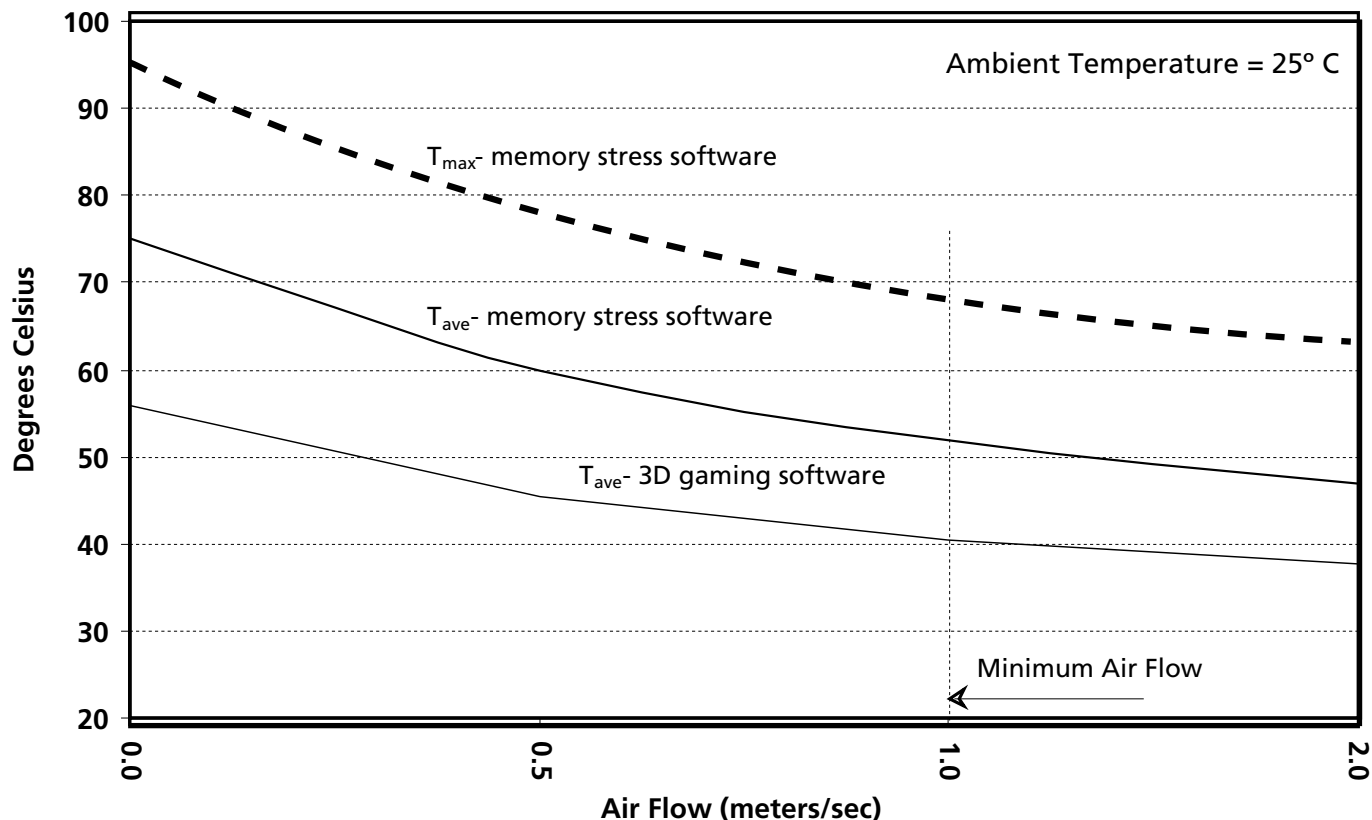
- Notes: 1. The timing and switching specifications for the PLL listed above are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this PLL is available in JEDEC Standard JESD82.
2. The PLL must be able to handle spread spectrum induced skew.
3. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low-speed system debug.)
4. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up.
5. Static Phase Offset does not include Jitter.
6. Period jitter and half-period jitter specifications are separate specifications that must be met independently of each other.
7. The output slew rate is determined from the IBIS model:





## Thermal Specifications

Figure 11: Component Case Temperature Vs. Air Flow



- Notes:
1. Micron Technology, Inc., recommends a minimum air flow of 1 meter/second (~197 LFM) across all modules when installed in a system.
  2. The component case temperature measurements shown above were obtained experimentally. The typical system to be used for experimental purposes is a dual-processor 600 MHz work station, fully loaded, with four comparable registered memory modules. Case temperatures charted represent worst-case component locations on modules installed in the internal slots of the system.
  3. Temperature versus air speed data is obtained by performing experiments with the system motherboard removed from its case and mounted in a Eiffel-type low air speed wind tunnel. Peripheral devices installed on the system motherboard for testing are the processor(s) and video card, all other peripheral devices are mounted outside of the wind tunnel test chamber.
  4. The memory diagnostic software used for determining worst-case component temperatures is a memory diagnostic software application developed for internal use by Micron Technology, Inc.

## Serial Presence-Detect

### SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 12 on page 34, and Figure 13 on page 35).

### SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

### SPD Stop Condition

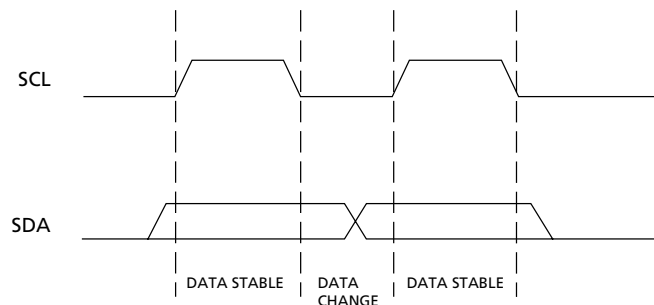
All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

### SPD Acknowledge

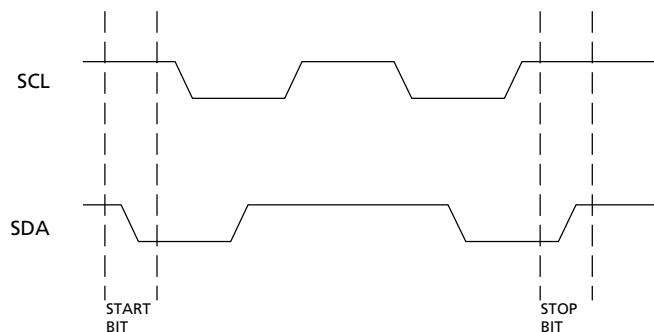
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 14 on page 35).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

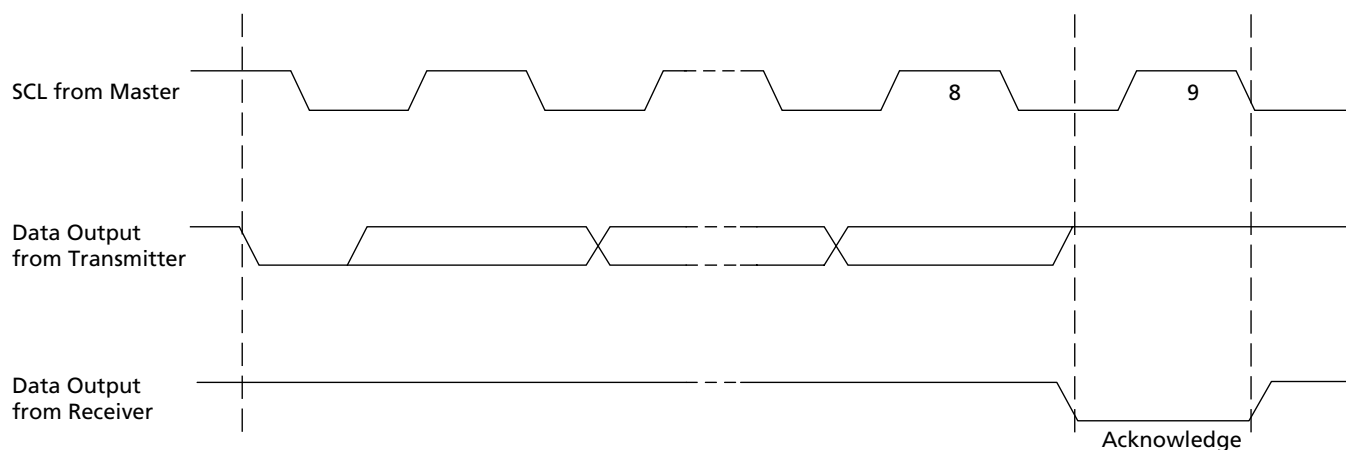
**Figure 12: Data Validity**



**Figure 13: Definition of Start and Stop**



**Figure 14: Acknowledge Response from Receiver**



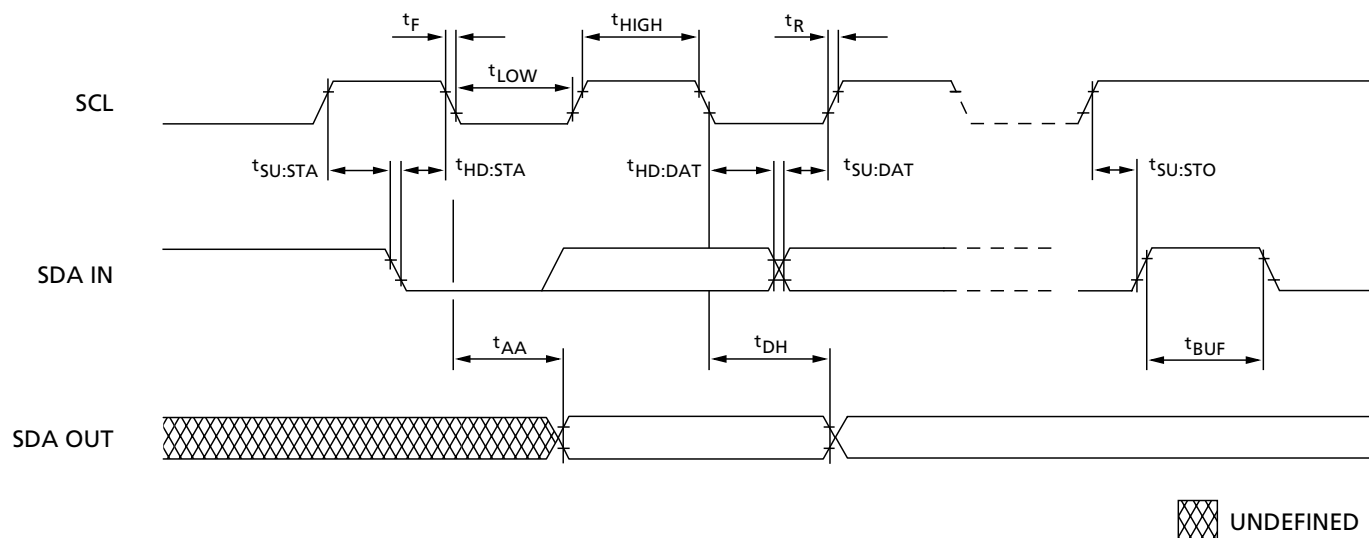
**Table 17: EEPROM Device Select Code**  
Most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory area select code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection register select code	0	1	1	0	SA2	SA1	SA0	RW

**Table 18: EEPROM Operating Modes**

Mode	RW Bit	WC	Bytes	Initial Sequence
Current address read	1	V <sub>IH</sub> or V <sub>IL</sub>	1	START, device select, RW = '1'
Random address read	0	V <sub>IH</sub> or V <sub>IL</sub>	1	START, device select, RW = '0', address
	1	V <sub>IH</sub> or V <sub>IL</sub>	1	reSTART, device select, RW = '1'
Sequential read	1	V <sub>IH</sub> or V <sub>IL</sub>	≥ 1	Similar to current or random address read
Byte write	0	V <sub>IL</sub>	1	START, device select, RW = '0'
Page write	0	V <sub>IL</sub>	≤ 16	START, device select, RW = '0'

**Figure 15: SPD EEPROM Timing Diagram**



**Table 19: Serial Presence-Detect EEPROM DC Operating Conditions**

All voltages referenced to VSS; VDDSPD = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
SUPPLY VOLTAGE	VDDSPD	2.3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V <sub>IH</sub>	VDDSPD x 0.7	VDDSPD + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V <sub>IL</sub>	-1	VDDSPD x 0.3	V
OUTPUT LOW VOLTAGE: I <sub>OUT</sub> = 3mA	V <sub>OL</sub>	–	0.4	V
INPUT LEAKAGE CURRENT: V <sub>IN</sub> = GND to VDD	I <sub>LI</sub>	–	10	μA
OUTPUT LEAKAGE CURRENT: V <sub>OUT</sub> = GND to VDD	I <sub>LO</sub>	–	10	μA
STANDBY CURRENT: SCL = SDA = VDD - 0.3V; All other inputs = VSS or VDD	I <sub>SB</sub>	–	30	μA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I <sub>DD</sub>	–	2	mA

**Table 20: Serial Presence-Detect EEPROM AC Operating Conditions**

All voltages referenced to VSS; VDDSPD = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	t <sub>AA</sub>	0.2	0.9	μs	1
Time the bus must be free before a new transition can start	t <sub>BUF</sub>	1.3		μs	
Data-out hold time	t <sub>DH</sub>	200		ns	
SDA and SCL fall time	t <sub>F</sub>		300	ns	2
Data-in hold time	t <sub>HD:DAT</sub>	0		μs	
Start condition hold time	t <sub>HD:STA</sub>	0.6		μs	
Clock HIGH period	t <sub>HIGH</sub>	0.6		μs	
Noise suppression time constant at SCL, SDA inputs	t <sub>I</sub>		50	ns	
Clock LOW period	t <sub>LOW</sub>	1.3		μs	
SDA and SCL rise time	t <sub>R</sub>		0.3	μs	2
SCL clock frequency	f <sub>SCL</sub>		400	KHz	
Data-in setup time	t <sub>SU:DAT</sub>	100		ns	
Start condition setup time	t <sub>SU:STA</sub>	0.6		μs	3
Stop condition setup time	t <sub>SU:STO</sub>	0.6		μs	
WRITE cycle time	t <sub>WRC</sub>		10	ms	4

- Notes: 1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (t<sub>WRC</sub>) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

**Table 21: Serial Presence-Detect Matrix**  
 "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT36VDDT12872	MT36VDDT25672	MT36VDDT51272
0	Number of bytes used by Micron	128	80	80	80
1	Total number of SPD memory bytes	256	08	08	08
2	Memory type	SDRAM DDR	07	07	07
3	Number of row addresses	13 or 14	0D	0D	0E
4	Number of column addresses	11 or 12	0B	0C	0C
5	Number of module ranks	2	02	02	02
6	Module data width	72	48	48	48
7	Module data width (continued)	0	00	00	00
8	Module voltage interface levels	SSTL 2.5V	04	04	04
9	SDRAM cycle time, $t_{CK}$ , CAS latency = 2.5, (see note 1)	6ns (-335) 7ns (-262/-26A) 7.5ns (-265)	60 70 75	60 70 75	60 70 75
10	SDRAM access from clock, $t_{AC}$ , CAS latency = 2.5	0.7ns (-335) 0.75ns (-262/-26A/-265)	70 75	70 75	70 75
11	Module configuration type	ECC	02	02	02
12	Refresh rate/ Type	7.81 $\mu$ s/SELF	82	82	82
13	SDRAM width (primary SDRAM)	4	04	04	04
14	Error-checking SDRAM data width	4	04	04	04
15	Minimum clock delay, back-to-back random column access	1 clock	01	01	01
16	Burst lengths supported	2, 4, 8	0E	0E	0E
17	Number of banks on SDRAM device	4	04	04	04
18	CAS latencies supported	2, 2.5	0C	0C	0C
19	CS latency	0	01	01	01
20	WE latency	1	02	02	02
21	SDRAM module attributes	Registered/Diff. Clock	26	26	26
22	SDRAM device attributes: general	Fast/Concurrent AP	C0	C0	C0
23	SDRAM cycle time, $t_{CK}$ , CAS latency = 2	7.5ns (-335/-262/-26A) 10ns (-265)	75 A0	75 A0	75 A0
24	SDRAM cycle time, $t_{CK}$ , CAS latency = 2	0.70ns (-335) 0.75ns (-262/-26A/-265)	70 75	70 75	70 75
25	SDRAM cycle time, $t_{CK}$ , CAS latency = 1	N/A	00	00	00
26	SDRAM access from CK, $t_{AC}$ , CAS latency = 1	N/A	00	00	00
27	Minimum row precharge time, $t_{RP}$	18ns (-335) 15ns (-262) 20ns (-26A/-265)	48 3C 50	48 3C 50	48 3C 50
28	Minimum row active to row active, $t_{RRD}$	12ns (-335) 15ns (-262/-26A/-265)	30 3C	30 3C	30 3C
29	Minimum RAS# to CAS# delay, $t_{RCD}$	18ns (-335) 15ns (-262) 20ns (-26A/-265)	48 3C 50	48 3C 50	48 3C 50
30	Minimum RAS# pulse width, $t_{RAS}$ (see note 2)	42ns (-335) 45ns (-262/-26A/-265)	2A 2D	2A 2D	2A 2D
31	Module rank density	128MB, 256MB, 512MB	80	01	02

**Table 21: Serial Presence-Detect Matrix**  
 "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

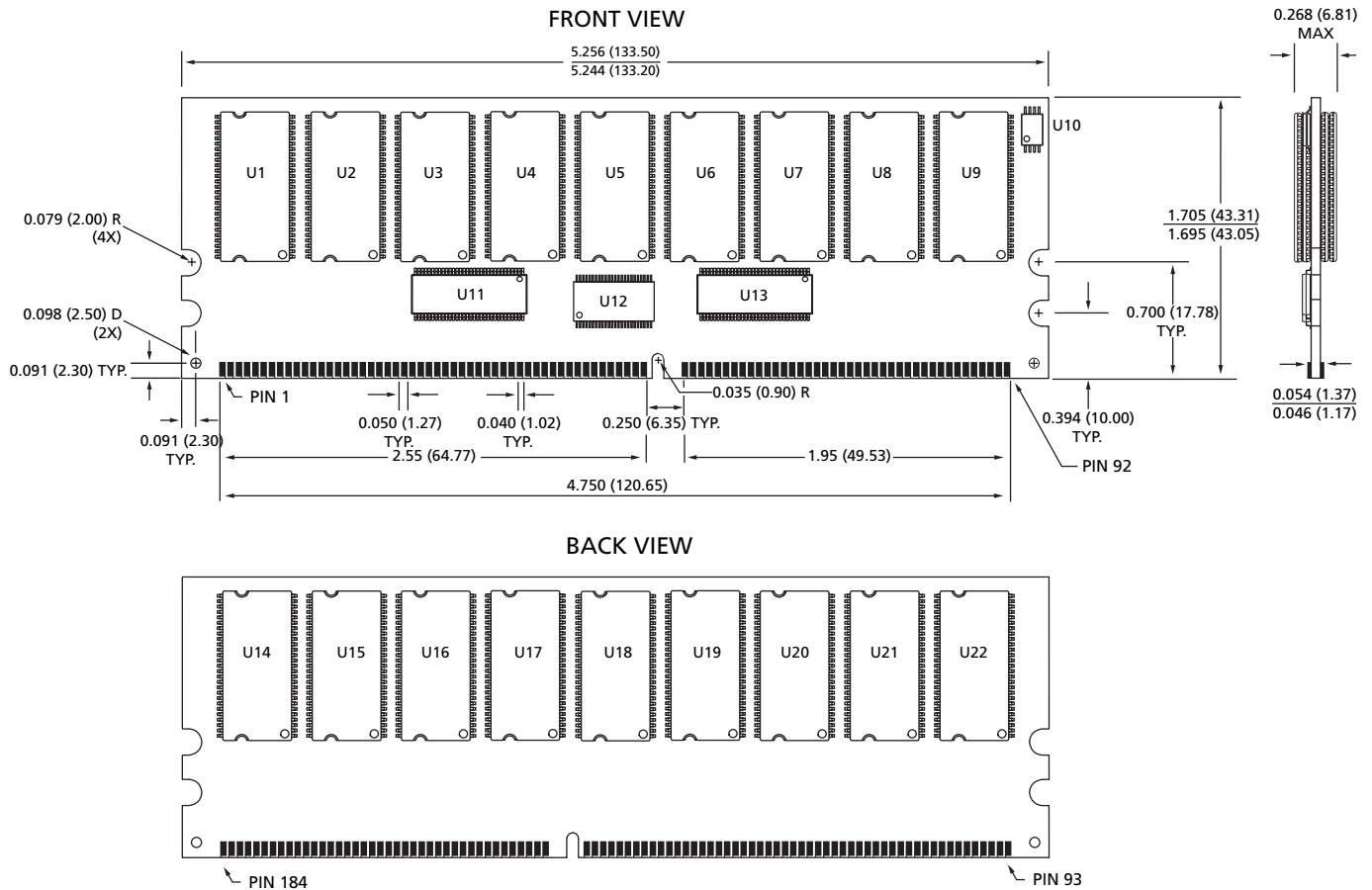
Byte	Description	Entry (Version)	MT36VDDT12872	MT36VDDT25672	MT36VDDT51272
32	Address and command setup time, $t_{IS}$ , (see note 2)	0.80ns (-335) 1ns (262/-26A/-265)	80 A0	80 A0	80 A0
33	Address and command hold time, $t_{IH}$ , (see note 2)	0.80ns (-335) 1ns (-262/-26A/-265)	80 A0	80 A0	80 A0
34	Data/Data mask input setup time, $t_{DS}$	0.45ns (-335) 0.50ns (-262/-26A/-265)	45 50	45 50	45 50
35	Data/Data mask input hold time, $t_{DH}$	0.45ns (-335) 0.50ns (-262/-26A/-265)	45 50	45 50	45 50
36-40	Reserved		00	00	00
41	Minimum active/auto refresh time, $t_{RC}$	60ns (-335/-262) 65ns (-26A/-265)	3C 41	3C 41	3C 41
42	Minimum auto refresh to active/ auto refresh command period, $t_{RFC}$	72ns (-335) 75ns (-262/-26A/-265) 120ns (4GB, all speeds)	48 4B –	48 4B –	48 4B –
43	Maximum cycle time, $t_{CK}(MAX)$	12ns (-335) 13ns (-262/-26A/-265)	30 34	30 34	30 34
44	Maximum DQS–DQ skew time, $t_{DQSQ}$	0.40ns (-335) 0.5ns (-262/-26A/-265)	2D 32	2D 32	2D 32
45	Maximum read data hold skew factor, $t_{QHS}$	0.50ns (-335) 0.75ns (-262/-26A/-265)	55 75	55 75	55 75
46	Reserved		00	00	00
47	DIMM height	Standard/Low-Profile	10/01	10/01	10/01
48–61	Reserved		00	00	00
62	SPD revision	Release 1.0	10	10	10
63	Checksum for bytes 0–62 Standard DIMM/Low-Profile DIMM	–335 –262 –26A –265	88/79 1B/0C 48/39 78/69	0A/FB 9D/90 CA/BB FA/EB	3C/2D CC/BD F9/EA 29/1A
64	Manufacturer's JEDEC ID code	MICRON	2C	2C	2C
65-71	Manufacturer's JEDEC ID code	(Continued)	00	00	00
72	Manufacturing location	01–12	01 - 0C	01 - 0C	01 - 0C
73-90	Module part number (ASCII)		Variable Data	Variable Data	Variable Data
91	PCB identification code	1–9	01–09	01–09	01–09
92	Identification code (continued)	0	00	00	00
93	Year of manufacture in BCD		Variable Data	Variable Data	Variable Data
94	Week of manufacture in BCD		Variable Data	Variable Data	Variable Data
95-98	Module serial number		Variable Data	Variable Data	Variable Data
99-127	Manufacturer-Specific data (RSVD)		–	–	–

- Notes: 1. Value for -26A  $t_{CK}$  is set at 7ns (0x70) for optimum BIOS compatibility. Actual device specification value is 7.5ns.
2. The value for  $t_{RAS}$  for -26A and -265 modules is calculated from  $t_{RC}$  -  $t_{RP}$ . Actual device spec is 40ns.
3. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster minimum slew rate is met.

## Module Dimensions

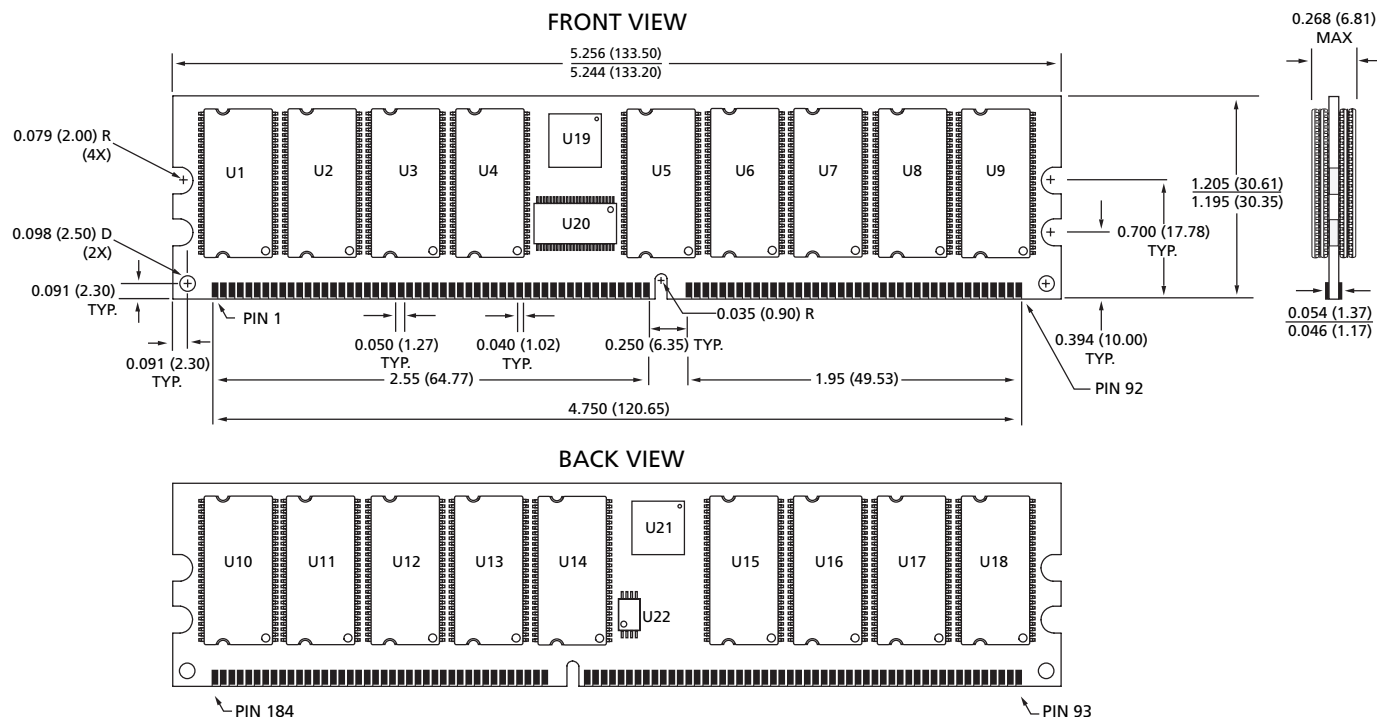
All dimensions are in inches (millimeters);  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.

**Figure 16: Standard 184-Pin DIMM Dimensions**





### Figure 17: Low-Profile 184-Pin DIMM Dimensions



## Data Sheet Designation

**Released (No Mark):** This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.



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