

DDR2 SDRAM SODIMM

MT8HTF3264HD – 256MB

MT8HTF6464HD – 512MB

MT8HTF12864HD – 1GB

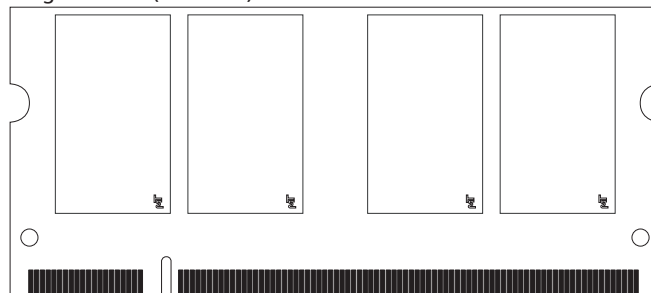
For component data sheet specifications, refer to Micron's Web site: www.micron.com/products/ddr2sdram

Features

- 200-pin, small outline, dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, or PC2-5300
- 256MB (16 Meg x 64), 512MB (32 Meg x 64) 1GB (64 Meg x 64)
- VDD = VDDQ = +1.8V
- VDDSPD = +1.7V to +3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 t_{CK}
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank

Figure 1: 200-Pin SODIMM (MO-224 R/C "A")

Height 1.18in. (29.97mm)



Options

- Package
200-pin SODIMM (lead-free)
- Frequency/CAS Latency¹
3.0ns @ CL = 5 (DDR2-667)²
3.75ns @ CL = 4 (DDR2-533)
5.0ns @ CL = 3 (DDR2-400)
- PCB Height
1.18in. (29.97mm)

Marking

Y
-667
-53E
-40E

Notes: 1. CL = CAS (READ) Latency.
2. Not available in 1GB density.

Table 1: Address Table

	256MB	512MB	1GB
Refresh Count	8K	8K	8K
Row Addressing	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	8 (BA0, BA1, BA2)
Device Page Size per Bank	1KB	1KB	1KB
Device Configuration	256Mb (16 Meg x 16)	512Mb (32 Meg x 16)	1Gb (64 Meg x 16)
Column Addressing	512 (A0–A8)	1K (A0–A9)	1K (A0–A9)
Module Rank Addressing	2 (S0#, S1#)	2 (S0#, S1#)	2 (S0#, S1#)

Table 2: Key Timing Parameters

Speed Grade	Data Rate (MT/s)			t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)
	CL = 3	CL = 4	CL = 5			
-667	–	533	667	15	15	55
-53E	400	533	–	15	15	55
-40E	400	400	–	15	15	55

Table 3: Part Numbers and Timing Parameters

PART NUMBER ¹	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - t_{RCD} - t_{RP})
MT8HTF3264HDY-667__	256MB	16 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT8HTF3264HDY-53E__	256MB	16 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT8HTF3264HDY-40E__	256MB	16 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT8HTF6464HDY-667__	512MB	32 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT8HTF6464HDY-53E__	512MB	32 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT8HTF6464HDY-40E__	512MB	32 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT8HTF12864HDY-667__	1GB	64 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT8HTF12864HDY-53E__	1GB	64 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT8HTF12864HDY-40E__	1GB	64 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes: 1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8HTF6464HDY-40EC2.

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Pin Assignments and Descriptions

Table 4: Pin Assignment

200-Pin SODIMM Front								200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	DQS2	101	A1	151	DQ42	2	Vss	52	DM2	102	A0	152	DQ46
3	Vss	53	Vss	103	VDD	153	DQ43	4	DQ4	54	Vss	104	VDD	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	Vss	6	DQ5	56	DQ22	106	BA1	156	Vss
7	DQ1	57	DQ19	107	BA0	157	DQ48	8	Vss	58	DQ23	108	RAS#	158	DQ52
9	Vss	59	Vss	109	WE#	159	DQ49	10	DM0	60	Vss	110	S0#	160	DQ53
11	DQS0#	61	DQ24	111	VDD	161	Vss	12	Vss	62	DQ28	112	VDD	162	Vss
13	DQS0	63	DQ25	113	CAS#	163	NC	14	DQ6	64	DQ29	114	ODT0	164	CK1
15	Vss	65	Vss	115	S1#	165	Vss	16	DQ7	66	Vss	116	NC	166	CK1#
17	DQ2	67	DM3	117	VDD	167	DQS6#	18	Vss	68	DQS3#	118	VDD	168	Vss
19	DQ3	69	NC	119	ODT1	169	DQS6	20	DQ12	70	DQS3	120	NC	170	DM6
21	Vss	71	Vss	121	Vss	171	Vss	22	DQ13	72	Vss	122	Vss	172	Vss
23	DQ8	73	DQ26	123	DQ32	173	DQ50	24	Vss	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51	26	DM1	76	DQ31	126	DQ37	176	DQ55
27	Vss	77	Vss	127	Vss	177	Vss	28	Vss	78	Vss	128	Vss	178	Vss
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56	30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	VDD	131	DQS4	181	DQ57	32	CK0#	82	VDD	132	Vss	182	DQ61
33	Vss	83	NC	133	Vss	183	Vss	34	Vss	84	NC	134	DQ38	184	Vss
35	DQ10	85	NC/BA2	135	DQ34	185	DM7	36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	VDD	137	DQ35	187	Vss	38	DQ15	88	VDD	138	Vss	188	DQS7
39	Vss	89	A12	139	Vss	189	DQ58	40	Vss	90	A11	140	DQ44	190	Vss
41	Vss	91	A9	141	DQ40	191	DQ59	42	Vss	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	Vss	44	DQ20	94	A6	144	Vss	194	DQ63
45	DQ17	95	VDD	145	Vss	195	SDA	46	DQ21	96	VDD	146	DQS5#	196	Vss
47	Vss	97	A5	147	DM5	197	SCL	48	Vss	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	Vss	199	VDDSPD	50	NC	100	A2	150	Vss	200	SA1

Note: Pin 85 is NC for 256MB and 512MB, BA2 for 1GB.

Figure 2: Pin Locations

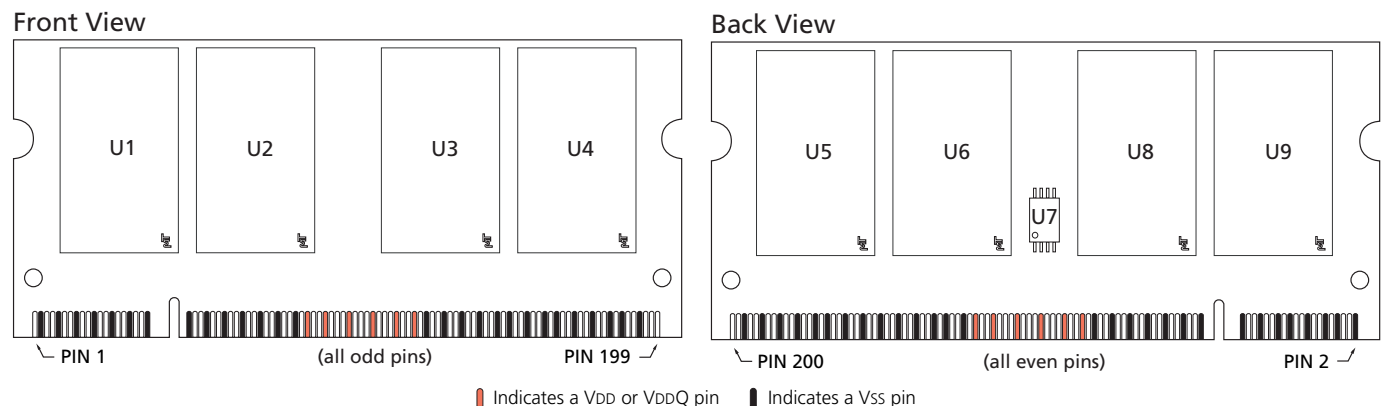


Table 5: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
114, 119	ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
30, 32, 164, 166	CK0, CK0# CK1, CK1#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
79, 80	CKE0, CKE1	Input	Clock Enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry, POWER-DOWN exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL ₁₈ input but will detect a LVCMOS LOW level once VDD is applied during first power-up. After Vref has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh operation VREF must be maintained to this input.
110, 115	S0#, S1#	Input	Chip Select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
108, 109, 113	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
85 (1GB), 106, 107	BA0, BA1, BA2 (1GB)	Input	Bank Address Inputs: BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied BA0–BA1/BA2 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
89, 90, 91, 92, 93, 94, 97, 98, 99, 100, 101, 102, 105	A0–A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/Write commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
10, 26, 52, 67, 130, 147, 170, 185	DM0–DM7 UDM = DM0, DM2, DM5, DM7 LDM = DM 1, DM3, DM4, DM6	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.

Table 5: Pin Descriptions

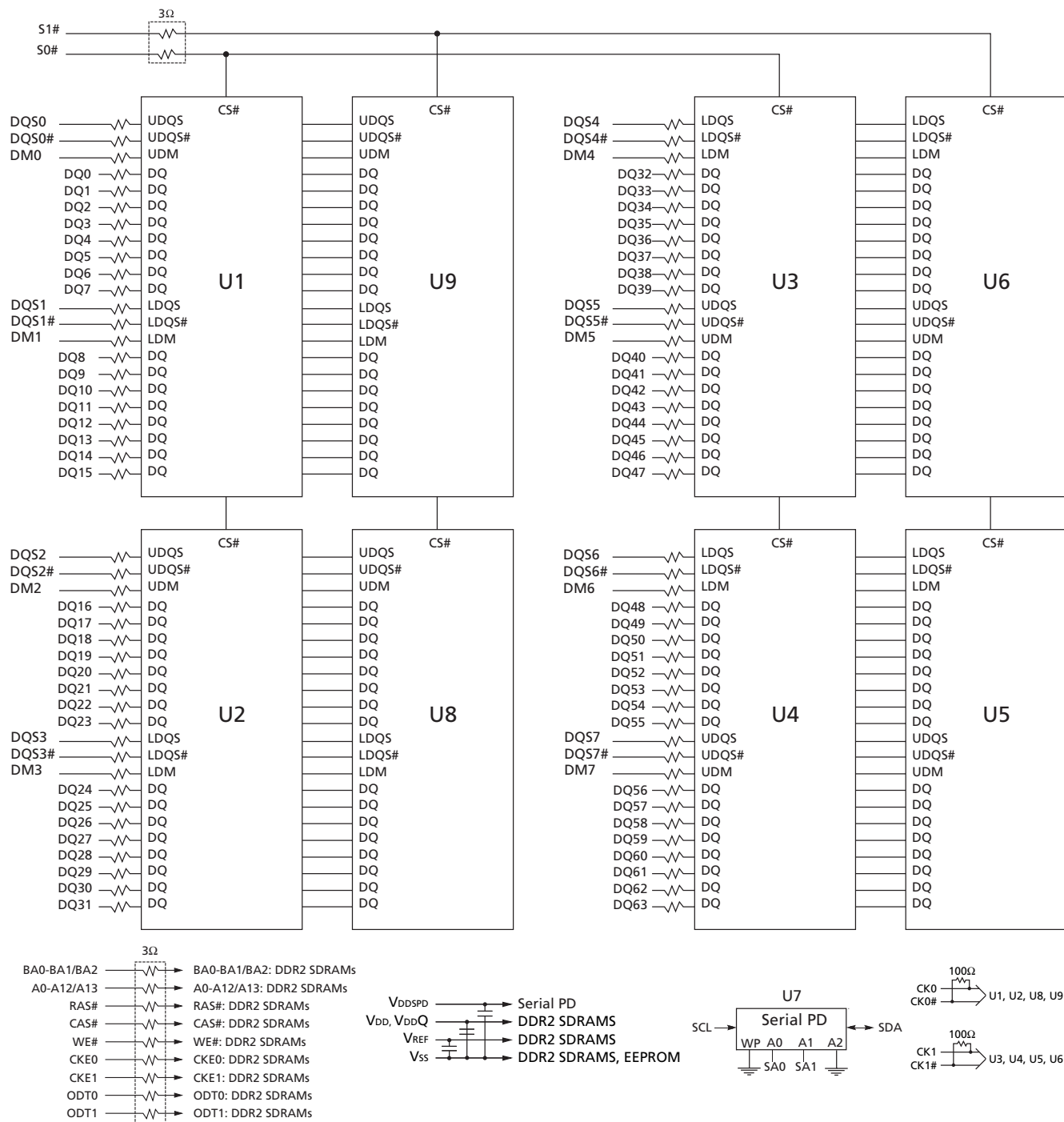
Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
4, 5, 6, 7, 14, 16, 17, 19, 20, 22, 23, 25, 35, 36, 37, 38, 43, 44, 45, 46, 55, 56, 57, 58, 61, 62, 63, 64, 73, 74, 75, 76, 123, 124, 125, 126, 134, 135, 136, 137, 140, 141, 142, 143, 151, 152, 153, 154, 157, 158, 159, 160, 173, 174, 175, 176, 179, 180, 181, 182, 189, 191, 192, 194	DQ0–DQ63	I/O	Data Input/Output: Bidirectional data bus.
11, 13, 29, 31, 49, 51, 68, 70, 129, 131, 146, 148, 167, 169, 186, 188	DQS0–DQS7, DQS0#–DQS7#	I/O	Data Strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
197	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
198, 200	SA0–SA1	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
195	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
81, 82, 87, 88, 95, 96, 103, 104, 111, 112, 117, 118	VDD	Supply	Power Supply: +1.8V ±0.1V.
1	VREF	Supply	SSTL_18 reference voltage.
2, 3, 8, 9, 12, 15, 18, 21, 24, 27, 28, 33, 34, 39, 40, 41, 42, 47, 48, 53, 54, 59, 60, 65, 66, 71, 72, 77, 78, 121, 122, 127, 128, 132, 133, 138, 139, 144, 145, 149, 150, 155, 156, 161, 162, 165, 168, 171, 172, 177, 178, 183, 184, 187, 190, 193, 196	VSS	Supply	Ground. Also connects to VDDS/VDDQ, VDDL, and VSSL on the DDR2 SDRAM device.
199	VDDSPD	Supply	Serial EEPROM positive power supply: +1.7V to +3.6V.
50, 69, 83, 84, 85 (256MB and 512MB), 86, 116, 120, 163	NC	–	No Connect: These pins should be left unconnected.

Functional Block Diagram

Unless otherwise noted, resistor values are 22Ω. Micron module part numbers are explained in the Module Part Numbering Guide at www.micron.com/support/numbering.html. Modules use the following DDR2 SDRAM devices: MT47H16M16BP (256MB); MT47H32M16BT (512MB); and MT47H64M16BT (1GB). Component data sheet specifications are available at: www.micron.com/products/ddr2sdram.

Figure 3: Functional Block Diagram



General Description

The MT8HTF3264HD, MT8HTF6464HD, and MT8HTF12864HD DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 256MB, 512MB, and 1GB memory modules organized in x64 configuration. DDR2 SDRAM modules use internally configured quad-bank (256MB, 512MB) or eight-bank (1GB) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $4n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Absolute Maximum DC Ratings

Symbol	Parameter		Min	Max	Units
VDD	VDD Supply Voltage Relative to Vss		-1.0	2.3	V
VDDQ	VDDQ Supply Voltage Relative to Vss		-0.5	2.3	V
VDDL	VDDL Supply Voltage Relative to Vss		-0.5	2.3	V
VIN, VOUT	Voltage on any Pin Relative to Vss		-0.5	2.3	V
T _{STG}	Storage Temperature		-55	100	°C
T _{case}	DDR2 SDRAM Device Operating Temperature (Ambient)		0	85	°C
T _{OPR}	Operating Temperature (Ambient)		0	65	°C
I _I	Input Leakage Current; Any input $0V \leq V_{IN} \leq V_{DD}$; VREF input $0V \leq V_{IN} \leq 0.95V$; (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE# S#, CKE	-40	40	μA
		CK, CK#	-20	20	
		DM	-10	10	
I _{OZ}	Output Leakage Current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQs and ODT are disabled	DQ, DQS, DQS#	-10	10	μA
I _{VREF}	VREF Leakage Current; VREF = Valid VREF level		-16	16	μA

Capacitance

At DDR2 data rates, Micron encourages designers to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

Table 7: DDR2 Idd Specifications and Conditions – 256MB

Values shown for DDR2 SDRAM components only

Parameter/Condition	Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current; $t_{CK} = t_{CK}(I_{DD})$, $t_{RC} = t_{RC}(I_{DD})$, $t_{RAS} = t_{RAS\ MIN}(I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD0}^a	380	340	320	mA
Operating one bank active-read-precharge current; $I_{OUT} = 0mA$; BL = 4, CL = CL(I _{DD}), AL = 0; $t_{CK} = t_{CK}(I_{DD})$, $t_{RC} = t_{RC}(I_{DD})$, $t_{RAS} = t_{RAS\ MIN}(I_{DD})$, $t_{RCD} = t_{RCD}(I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{DD4W} .	I_{DD1}^a	420	380	360	mA
Precharge power-down current; All device banks idle; $t_{CK} = t_{CK}(I_{DD})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	I_{DD2P}^b	40	40	40	mA
Precharge quiet standby current; All device banks idle; $t_{CK} = t_{CK}(I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	I_{DD2Q}^b	400	280	200	mA
Precharge standby current; All device banks idle; $t_{CK} = t_{CK}(I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD2N}^b	320	280	240	mA
Active power-down current; All device banks open; $t_{CK} = t_{CK}(I_{DD})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	I_{DD3P}^b	240	200	160	mA
		48	48	48	mA
Active standby current; All device banks open; $t_{CK} = t_{CK}(I_{DD})$, $t_{RAS} = t_{RAS\ MAX}(I_{DD})$, $t_{RP} = t_{RP}(I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD3N}^b	440	320	240	mA
Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL(I _{DD}), AL = 0; $t_{CK} = t_{CK}(I_{DD})$, $t_{RAS} = t_{RAS\ MAX}(I_{DD})$, $t_{RP} = t_{RP}(I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD4W}^a	880	740	580	mA
Operating burst read current; All device banks open, Continuous burst reads, $I_{OUT} = 0mA$; BL = 4, CL = CL(I _{DD}), AL = 0; $t_{CK} = t_{CK}(I_{DD})$, $t_{RAS} = t_{RAS\ MAX}(I_{DD})$, $t_{RP} = t_{RP}(I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD4R}^a	780	660	500	mA
Burst refresh current; $t_{CK} = t_{CK}(I_{DD})$; Refresh command at every $t_{RFC}(I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD5}^b	1,440	1,360	1,320	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	I_{DD6}^b	40	40	40	mA
Operating bank interleave read current; All device banks interleaving reads, $I_{OUT} = 0mA$; BL = 4, CL = CL(I _{DD}), AL = $t_{RCD}(I_{DD}) - 1 \times t_{CK}(I_{DD})$; $t_{CK} = t_{CK}(I_{DD})$, $t_{RC} = t_{RC}(I_{DD})$, $t_{RRD} = t_{RRD}(I_{DD})$, $t_{RCD} = t_{RCD}(I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See I _{DD7} Conditions for detail.	I_{DD7}^a	1,020	980	940	mA

Note: a: Value calculated as one module rank in this operating condition, and all other module ranks in I_{DD2P} (CKE LOW) mode.
b: Value calculated reflects all module ranks in this operating condition.

Table 8: DDR2 Idd Specifications and Conditions – 512MB

Values shown for DDR2 SDRAM components only

Parameter/Condition	Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RAS\ MIN}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD0}^a	500	460	460	mA
Operating one bank active-read-precharge current; $I_{OUT} = 0mA$; $BL = 4$, $CL = CL(IDD)$, $AL = 0$; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RAS\ MIN}(IDD)$, $t_{RCD} = t_{RCD}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{DD4W} .	I_{DD1}^a	600	540	520	mA
Precharge power-down current; All device banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	I_{DD2P}^b	40	40	40	mA
Precharge quiet standby current; All device banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	I_{DD2Q}^b	440	360	320	mA
Precharge standby current; All device banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD2N}^b	480	400	360	mA
Active power-down current; All device banks open; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	I_{DD3P}^b	280	240	200	mA
		80	80	80	mA
Active standby current; All device banks open; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RAS\ MAX}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD3N}^b	560	480	400	mA
Operating burst write current; All device banks open, Continuous burst writes; $BL = 4$, $CL = CL(IDD)$, $AL = 0$; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RAS\ MAX}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD4W}^a	940	780	620	mA
Operating burst read current; All device banks open, Continuous burst reads, $I_{OUT} = 0mA$; $BL = 4$, $CL = CL(IDD)$, $AL = 0$; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RAS\ MAX}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD4R}^a	960	800	640	mA
Burst refresh current; $t_{CK} = t_{CK}(IDD)$; Refresh command at every $t_{RFC}(IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD5}^b	1,760	1,680	1,600	mA
Self refresh current; CK and CK# at 0V; $CKE \leq 0.2V$; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	I_{DD6}^b	40	40	40	mA
Operating bank interleave read current; All device banks interleaving reads, $I_{OUT} = 0mA$; $BL = 4$, $CL = CL(IDD)$, $AL = t_{RCD}(IDD) - 1 \times t_{CK}(IDD)$; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RRD} = t_{RRD}(IDD)$, $t_{RCD} = t_{RCD}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See I_{DD7} Conditions for detail.	I_{DD7}^a	1,340	1,320	1,300	mA

Note: a: Value calculated as one module rank in this operating condition, and all other module ranks in I_{DD2P} (CKE LOW) mode.

b: Value calculated reflects all module ranks in this operating condition.

Table 9: DDR2 Idd Specifications and Conditions – 1GB

Values shown for DDR2 SDRAM components only

Parameter/Condition	Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RAS\ MIN}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD0}^a	560	460	460	mA
Operating one bank active-read-precharge current; $I_{OUT} = 0mA$; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RAS\ MIN}(IDD)$, $t_{RCD} = t_{RCD}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as Idd4W.	I_{DD1}^a	660	540	520	mA
Precharge power-down current; All device banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	I_{DD2P}^b	56	40	40	mA
Precharge quiet standby current; All device banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	I_{DD2Q}^b	520	360	320	mA
Precharge standby current; All device banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD2N}^b	560	400	320	mA
Active power-down current; All device banks open; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	I_{DD3P}^b	320	240	200	mA
		40	40	40	mA
Active standby current; All device banks open; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RAS\ MAX}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD3N}^b	600	440	400	mA
Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RAS\ MAX}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD4W}^a	1,100	780	660	mA
Operating burst read current; All device banks open, Continuous burst reads, $I_{OUT} = 0mA$; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RAS\ MAX}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD4R}^a	1,120	800	740	mA
Burst refresh current; $t_{CK} = t_{CK}(IDD)$; Refresh command at every $t_{RFC}(IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	I_{DD5}^b	2,160	2,000	1,920	mA
Self refresh current; CK and CK# at 0V; CKE $\leq 0.2V$; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	I_{DD6}^b	56	40	40	mA
Operating bank interleave read current; All device banks interleaving reads, $I_{OUT} = 0mA$; BL = 4, CL = CL(IDD), AL = $t_{RCD}(IDD) - 1 \times t_{CK}(IDD)$; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RRD} = t_{RRD}(IDD)$, $t_{RCD} = t_{RCD}(IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See Idd7 Conditions for detail.	I_{DD7}^a	1,640	1,440	1,440	mA

Note: a: Value calculated as one module rank in this operating condition, and all other module ranks in Idd2P (CKE LOW) mode.
b: Value calculated reflects all module ranks in this operating condition.



256MB, 512MB, 1GB: (x64, DR) 200-Pin DDR2 SDRAM SODIMM Electrical Specifications

AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets, available at www.micron.com/products/ddr2sdram. Module speed grades correlate with component speed grades as shown in the following table:

Table 10: Module and Component Speed Grade Table

Module Speed Grade	Component Speed Grade
-667	-3
-53E	-37E
-40E	-53E

Serial Presence-Detect

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figure 4, Data Validity, and Figure 5, Definition of Start and Stop).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 6, Acknowledge Response From Receiver).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 4: Data Validity

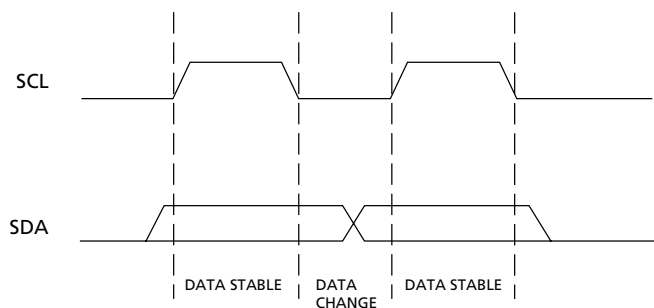


Figure 5: Definition of Start and Stop

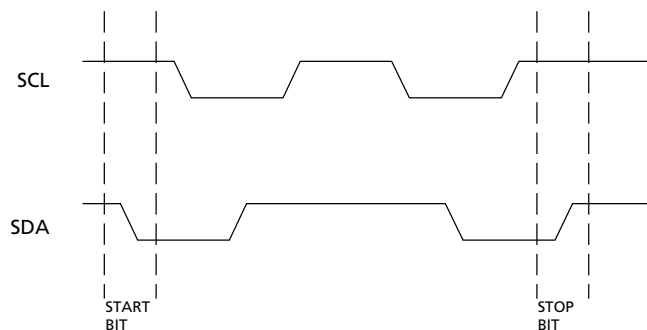


Figure 6: Acknowledge Response From Receiver

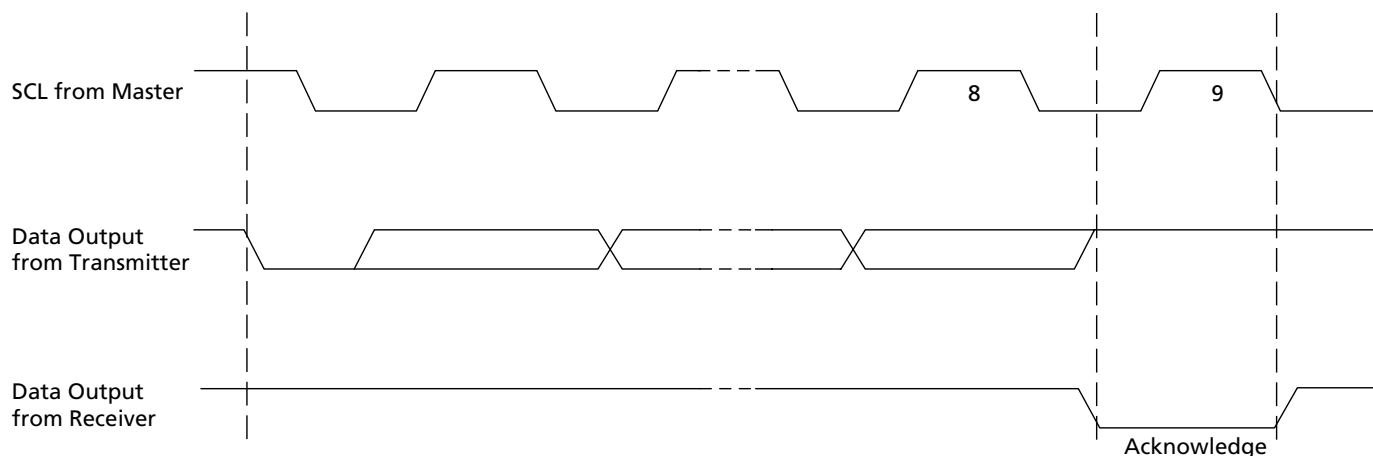


Table 11: EEPROM Device Select Code

The most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	RW

Table 12: EEPROM Operating Modes

Mode	RW Bit	WC	Bytes	Initial Sequence
Current Address Read	1	V _{IH} or V _{IL}	1	START, Device Select, RW = '1'
Random Address Read	0	V _{IH} or V _{IL}	1	START, Device Select, RW = '0', Address
	1	V _{IH} or V _{IL}	1	reSTART, Device Select, RW = '1'
Sequential Read	1	V _{IH} or V _{IL}	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V _{IL}	1	START, Device Select, RW = '0'
Page Write	0	V _{IL}	≤ 16	START, Device Select, RW = '0'

Figure 7: SPD EEPROM Timing Diagram

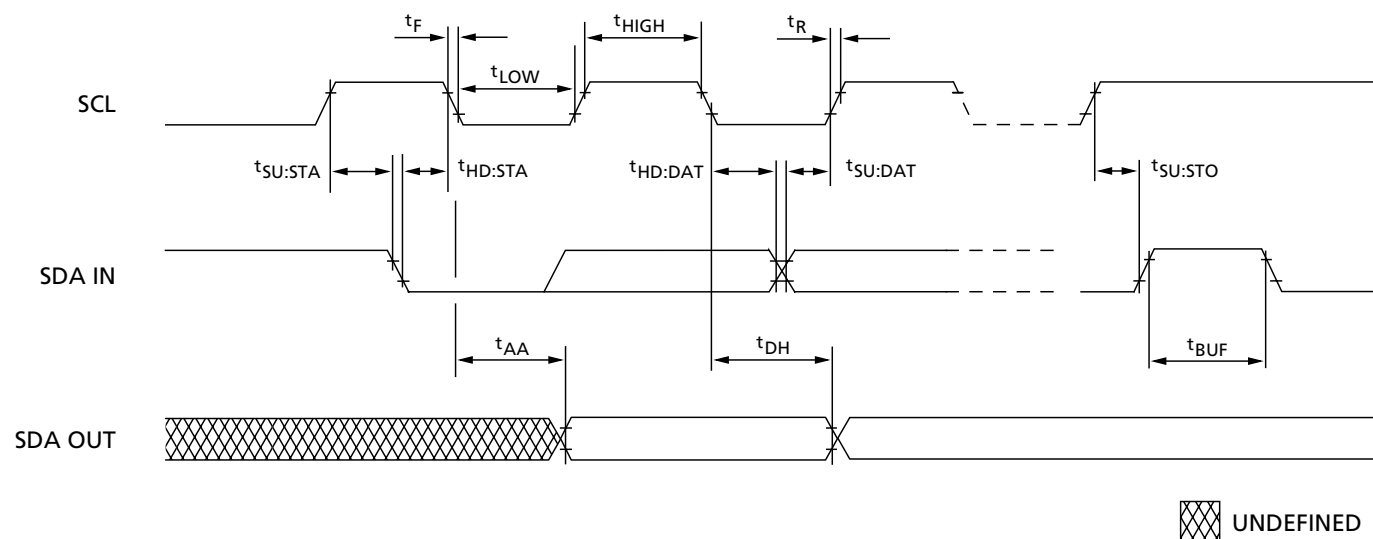


Table 13: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to VSS; VDDSPD = +1.7V to +3.6V

Parameter/Condition	Symbol	MIN	MAX	Units
Supply Voltage	VDDSPD	1.7	3.6	V
Input High Voltage: Logic 1; All inputs	V _{IH}	VDDSPD × 0.7	VDDSPD + 0.5	V
Input Low Voltage: Logic 0; All inputs	V _{IL}	-0.6	VDDSPD × 0.3	V
Output Low Voltage: I _{OUT} = 3mA	V _{OL}	–	0.4	V
Input Leakage Current: V _{IN} = GND to VDD	I _{LI}	0.10	3	μA
Output Leakage Current: V _{OUT} = GND to VDD	I _{LO}	0.05	3	μA
Standby Current	I _{SB}	1.6	4	μA
Power Supply Current, READ: SCL clock frequency = 100 KHz	I _{CC-R}	0.4	1	mA
Power Supply Current, WRITE: SCL clock frequency = 100 KHz	I _{CC-W}	2	3	mA

Table 14: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to VSS; VDDSPD = +1.7V to +3.6V

Parameter/Condition	Symbol	MIN	MAX	Units	Notes
SCL LOW to SDA data-out valid	t _{AA}	0.2	0.9	μs	1
Time the bus must be free before a new transition can start	t _{BUF}	1.3		μs	
Data-out hold time	t _{DH}	200		ns	
SDA and SCL fall time	t _F		300	ns	2
Data-in hold time	t _{HD:DAT}	0		μs	
Start condition hold time	t _{HD:STA}	0.6		μs	
Clock HIGH period	t _{HIGH}	0.6		μs	
Noise suppression time constant at SCL, SDA inputs	t _I		50	ns	
Clock LOW period	t _{LOW}	1.3		μs	
SDA and SCL rise time	t _R		0.3	μs	2
SCL clock frequency	f _{SCL}		400	KHz	
Data-in setup time	t _{SU:DAT}	100		ns	
Start condition setup time	t _{SU:STA}	0.6		μs	3
Stop condition setup time	t _{SU:STO}	0.6		μs	
WRITE cycle time	t _{WRC}		10	ms	4

- Notes:
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
 2. This parameter is sampled.
 3. For a reSTART condition, or following a WRITE cycle.
 4. The SPD EEPROM WRITE cycle time (t_{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 15: Serial Presence-Detect Matrix
 "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT8HTF3264HD	MT8HTF6464HD	MT8HTF12864HD
0	Number of SPD bytes used by Micron	128	80	80	80
1	Total number of bytes in SPD device	256	08	08	08
2	Fundamental memory type	DDR2 SDRAM	08	08	08
3	Number of row addresses on assembly	13	0D	0D	0D
4	Number of Column addresses on assembly	9, 10	09	0A	0A
5	DIMM height and module ranks	1.18in., Dual Rank	61	61	61
6	Module data width	64	40	40	40
7	Module data width (continued)	0	00	00	00
8	Module voltage interface levels	SSTL 1.8V	05	05	05
9	SDRAM cycle time, t_{CK} (CL = maximum value, see byte 18)	-667 -53E -40E	30 3D 50	30 3D 50	30 3D 50
10	SDRAM access from clock, t_{AC} (CL = maximum value, see byte 18)	-667 -53E -40E	45 50 60	45 50 60	45 50 60
11	Module configuration type		00	00	00
12	Refresh rate/type	7.81 μ s/SELF	82	82	82
13	SDRAM device width (primary SDRAM)	16	10	10	10
14	Error-checking SDRAM data width	N/A	00	00	00
15	Minimum clock delay, back-to-back random column access	1 clock	00	00	00
16	Burst lengths supported	4, 8	0C	0C	0C
17	Number of banks on SDRAM device	4 or 8	04	04	08
18	CAS latencies supported	-667 (5, 4, 3) -53E/-40E (4, 3)	38 18	38 18	38 18
19	Module thickness		01	01	01
20	DDR2 DIMM type	SODIMM	04	04	04
21	SDRAM module attributes		00	00	00
22	SDRAM device attributes: weak driver (01) and 50 Ω ODT (03)	-667 -53E/-40E	03 01	03 01	03 01
23	SDRAM cycle time, t_{CK} , max. CL - 1	-667 -53E/-40E	3D 50	3D 50	3D 50
24	SDRAM access from CK, t_{AC} , max. CL - 1	-667 -53E -40E	45 50 60	45 50 60	45 50 60
25	SDRAM cycle time, t_{CK} , max. CL - 2	-667 -53E/-40E(N/S)	50 00	50 00	50 00
26	SDRAM access from CK, t_{AC} , max. CL - 2	-667 -53E/-40E(N/S)	45 00	45 00	45 00
27	Minimum row precharge time, t_{RP}		3C	3C	3C
28	Minimum row active to row active, t_{RRD}		28	28	28
29	Minimum RAS# to CAS# delay, t_{RCD}		3C	3C	3C
30	Minimum RAS# pulse width, t_{RAS}	-667/-53E -40E	2D 28	2D 28	2D 28
31	Module rank density	128MB, 256MB, 512MB	20	40	80

Table 15: Serial Presence-Detect Matrix
 "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT8HTF3264HD	MT8HTF6464HD	MT8HTF12864HD
32	Address and command setup time, t_{IS_b}	-667 -53E -40E	20 25 35	20 25 35	20 25 35
33	Address and command hold time, t_{IH_b}	-667 -53E -40E	27 37 47	27 37 47	27 37 47
34	Data/ Data mask input setup time, t_{DS_b}	-667/-53E -40E	10 15	10 15	10 15
35	Data/ Data mask input hold time, t_{DH_b}	-667 -53E -40E	17 22 27	17 22 27	17 22 27
36	WRITE recovery time, t_{WR}		3C	3C	3C
37	WRITE to READ command delay, t_{WTR}	-667/-53E -40E	1E 28	1E 28	1E 28
38	READ-to-pPrecharge command delay, t_{RTP}		1E	1E	1E
39	Mem analysis probe		00	00	00
40	Extension for bytes 41 and 42		00	00	06
41	Min active auto refresh time, t_{RC}	-667/-53E -40E	3C 37	3C 37	3C 37
42	Minimum auto refresh to active/ auto refresh command period, t_{RFC}		4B	69	7F
43	SDRAM device max cycle time, t_{CKMAX}		80	80	80
44	SDRAM device max DQS-DQ skew time, t_{DQSQ}	-667 -53E -40E	18 1E 23	18 1E 23	18 1E 23
45	SDRAM device max read data hold skew factor, t_{QHS}	-667 -53E -40E	22 28 2D	22 28 2D	22 28 2D
46	PLL relock time		00	00	00
47-61	Optional features, not supported		00	00	00
62	SPD revision	Release 1.2	12	12	12
63	Checksum For bytes -62	-667 -53E -40E	E0 8B F2	1F CA 31	7F 2A 91
64	Manufacturer's JEDEC ID code	MICRON	2C	2C	2C
65-71	Manufacturer's JEDEC ID code	(Continued)	FF	FF	FF
72	Manufacturing location	01-12	01-0C	01-0C	01-0C
73-90	Module part number (ASCII)		Variable Data	Variable Data	Variable Data
91	PCB identification code	1-9	01-09	01-09	01-09
92	Identification code (continued)	0	00	00	00
93	Year of manufacture in BCD		Variable Data	Variable Data	Variable Data
94	Week of manufacture in BCD		Variable Data	Variable Data	Variable Data
95-98	Module serial number		Variable Data	Variable Data	Variable Data
99-127	Manufacturer-specific data (RSVD)		-	-	-

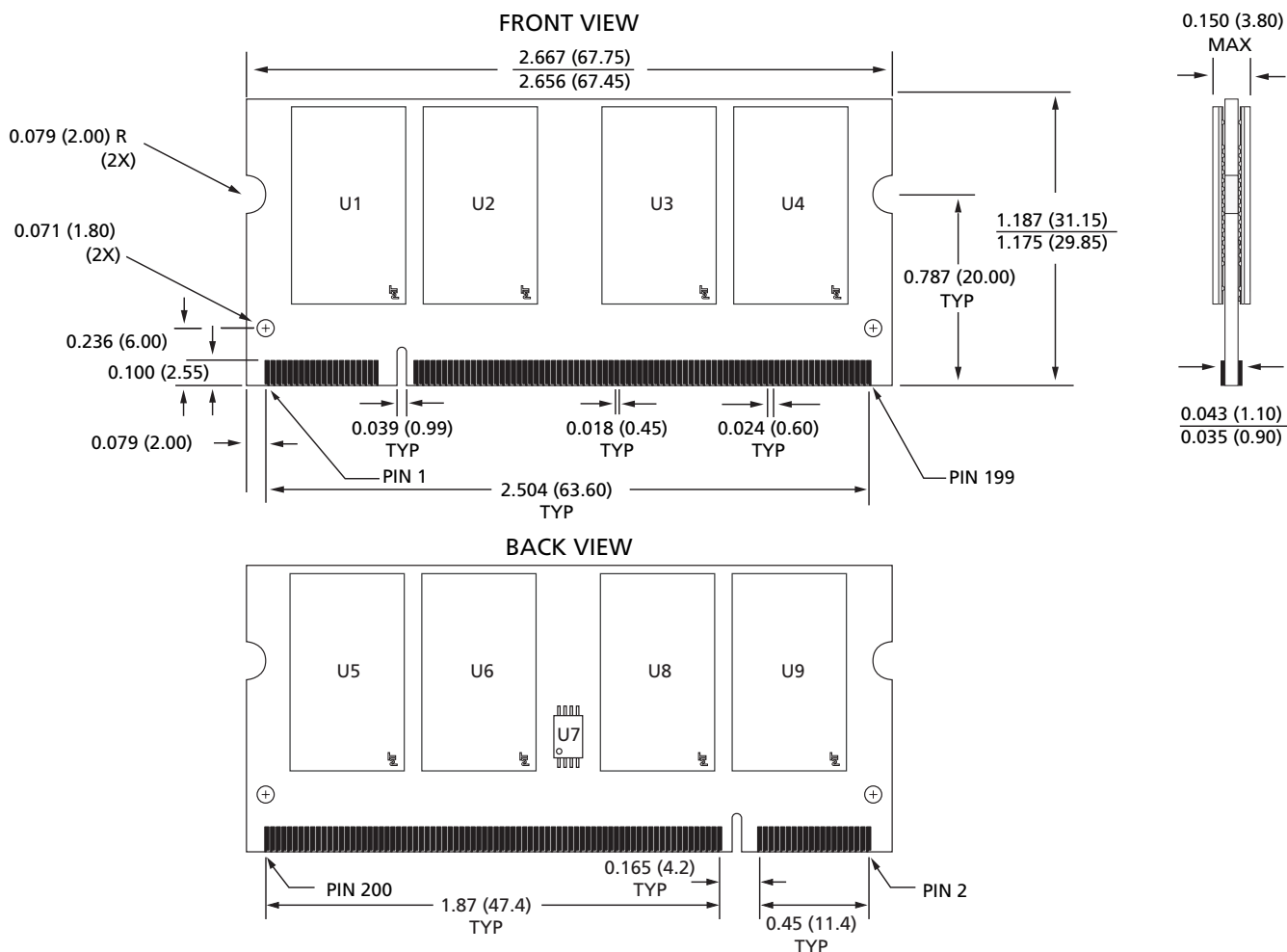
Notes: 1. The t_{RAS} SPD value shown is based on the JEDEC standard value of 45 ns; the actual device specification is $t_{RAS} = 40ns$.

Module Dimensions

All dimensions are in inches (millimeters); $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

Figure 8: 200-pin DDR2 SODIMM Dimensions



Data Sheet Designation

Released (No Mark): This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.



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