

DATA SHEET

74F168*, 74F169

4-bit up/down binary synchronous counter

* Discontinued part. Please see the Discontinued Product List in Section 1, page 21.

Product specification

1996 Jan 05

IC15 Data Handbook

4-bit up/down binary synchronous counter

74F169

FEATURES

- Synchronous counting and loading
- Up/Down counting
- Modulo 16 binary counter
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock
- Built-in carry look-ahead capability
- Presetable for programmable operation

DESCRIPTION

The 74F169 is a 4-bit synchronous, presetable Modulo 16 up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the Low-to-High transition of the clock.

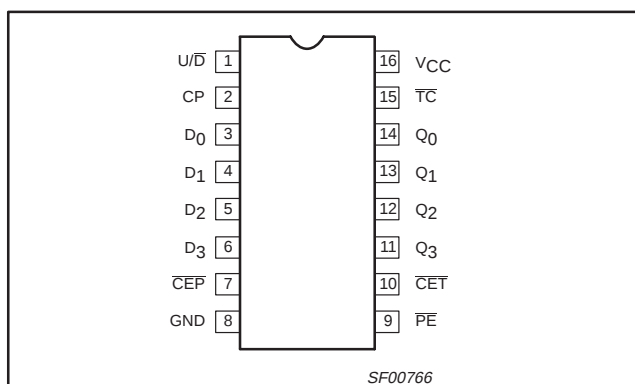
The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A Low level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

The direction of counting is controlled by the Up/Down ($U/\overline{D}$) input; a High will cause the count to increase, a Low will cause the count to decrease.

The carry look-ahead circuitry provides for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET}$, $\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be Low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal to the High level portion of the Q_0 output. The Low level $\overline{TC}$ pulse is used to enable successive cascaded stages.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F169	115MHz	35mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
16-pin plastic DIP	N74F169N	SOT38-4
16-pin plastic SO	N74F169D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

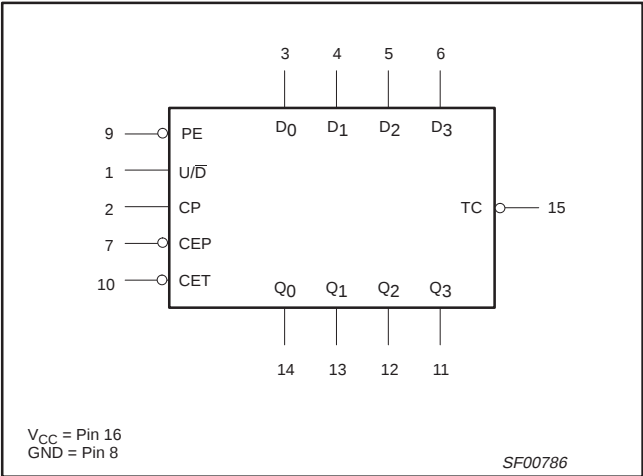
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20 μ A/0.6mA
$\overline{CEP}$	Count Enable parallel input (active Low)	1.0/1.0	20 μ A/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/2.0	20 μ A/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20 μ A/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
$U/\overline{D}$	Up/Down count control input	1.0/1.0	20 μ A/0.6mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μ A in the High state and 0.6mA in the Low state.

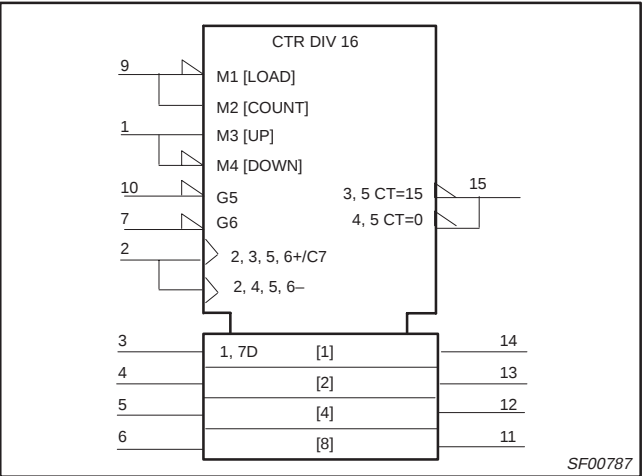
4-bit up/down binary synchronous counter

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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DESCRIPTION

The 74F169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is Low, the data on the $D_0 - D_3$ inputs enter the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be Low and $\overline{PE}$ must be High; the $U/\overline{D}$ input determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally High and goes Low, provided that $\overline{CET}$ is Low,

when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

- 1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$
- 2) Up: $\overline{TC} = Q_0 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$
- 3) Down: $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$

MODE SELECT — FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
CP	U/ $\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$	
$\uparrow$	X	X	X	L	L	L	(1)	Parallel load ($D_n \rightarrow Q_n$)
$\uparrow$	X	X	X	X	X	H	(1)	
$\uparrow$	h	L	L	h	X	Count Up	(1)	Count Up (increment)
$\uparrow$	L	L	L	h	X	Count Down	(1)	Count Down (decrement)
$\uparrow$	X	h	X	h	X	q_n	(1)	Hold (do nothing)
$\uparrow$	X	X	X	h	X	q_n	H	

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
 $\uparrow$ = Low-to-High clock transition

(1)= The $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL).

4-bit up/down binary synchronous counter

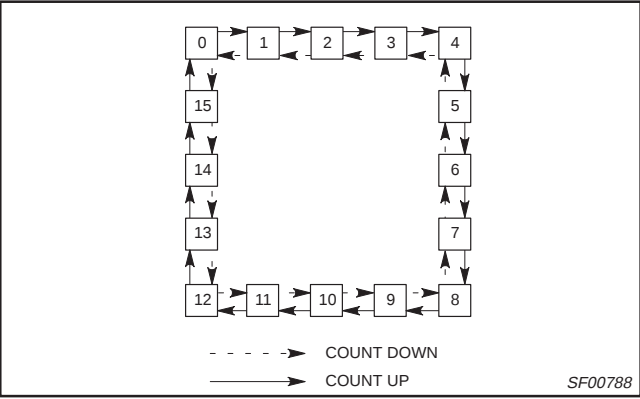
74F169

MODE SELECT TABLE

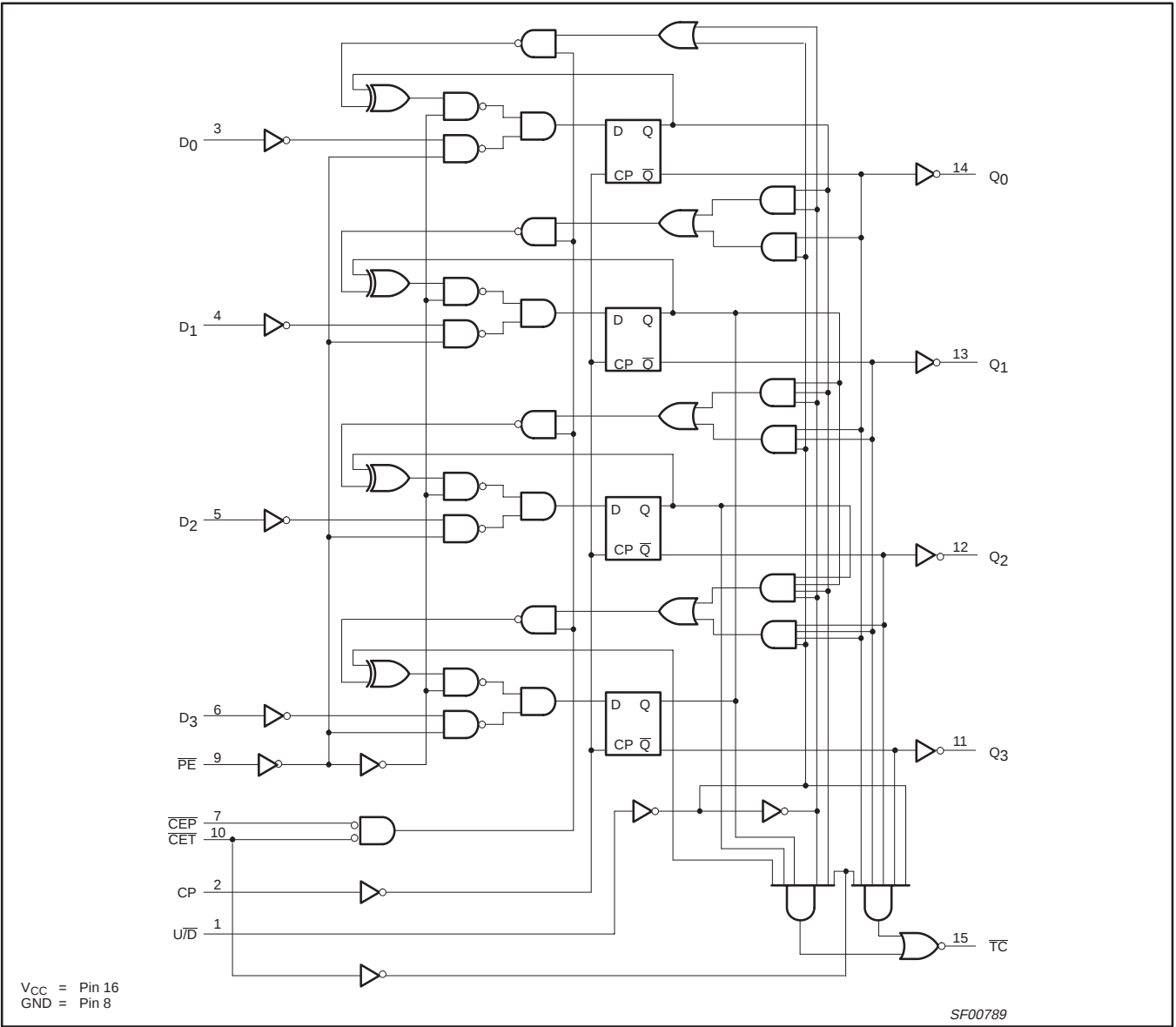
INPUTS				OPERATING MODE
PE	CEP	CET	U/D	
L	X	X	X	Load ($D_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = High Voltage
L = Low Voltage Level
X = Don't care

STATE DIAGRAM



LOGIC DIAGRAM



4-bit up/down binary synchronous counter

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APPLICATION

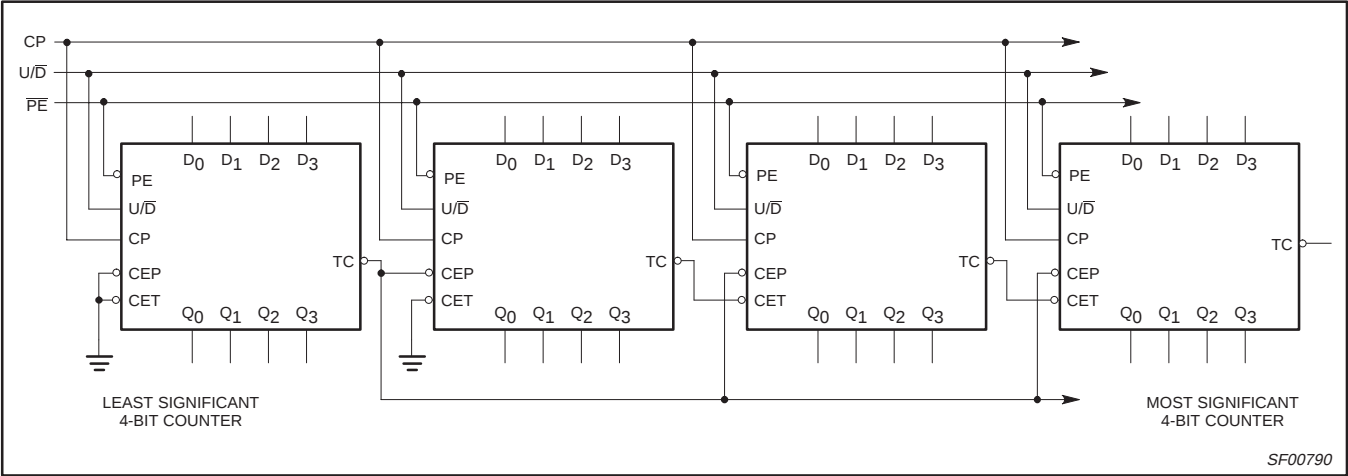


Figure 1. Synchronous Multistage Counting Scheme

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	−0.5 to +7.0	V
V _{IN}	Input voltage	−0.5 to +7.0	V
I _{IN}	Input current	−30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	−0.5 to +V _{CC}	V
I _{OUT}	Current applied to output in Low output state	40	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			−18	mA
I _{OH}	High-level output current			−1	mA
I _{OL}	Low-level output current			20	mA
T _{amb}	Operating free-air temperature range	0		70	°C

4-bit up/down binary synchronous counter

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ^{NO TAG}	LIMITS			UNIT	
				MIN	TYP NO TAG	MAX		
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	±10%V _{CC}	2.5		V	
				±5%V _{CC}	2.7	3.4		V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX	±10%V _{CC}		0.35	0.50	V
				±5%V _{CC}		0.35	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}			−0.73	−1.2	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7.0V				100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	Low-level input current	CET	V _{CC} = MAX, V _I = 0.5V				−1.2	mA
		Others	V _{CC} = MAX, V _I = 0.5V				−0.6	mA
I _{OS}	Short-circuit output current ^{NO TAG}		V _{CC} = MAX		−60		−150	mA
I _{CC}	Supply current (total) ⁴		V _{CC} = MAX			35	52	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured after applying a momentary 4.5V, then ground to the clock input with all other inputs grounded and all outputs open.

4-bit up/down binary synchronous counter

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Q _n (P _E , High or Low)	Waveform 1	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	9.5 13.0	ns ns
t _{PLH} t _{PHL}	Propagation delay CP to TC	Waveform 1	5.5 4.0	12.0 8.5	15.5 11.0	5.5 4.0	17.0 12.5	ns ns
t _{PLH} t _{PHL}	Propagation delay CET to TC	Waveform 2	2.5 2.5	4.5 6.0	6.0 8.0	2.5 2.5	7.0 9.0	ns ns
t _{PLH} t _{PHL}	Propagation delay U/D to TC	Waveform 3	3.5 4.0	8.5 8.0	15.0 10.5	3.5 4.0	15.5 12.0	ns ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		LIMITS		UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω		T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MIN	MAX	
t _s (H) t _s (L)	Setup time, High or Low D _n to CP	Waveform 4	4.0 4.0		4.5 4.5		ns ns
t _h (H) t _h (L)	Hold time, High or Low D _n to CP	Waveform 4	3.0 3.0		3.5 3.5		ns ns
t _s (H) t _s (L)	Set-up time, High or Low C _{EP} or C _{ET} to CP	Waveform 5	5.0 5.0		5.5 5.5		ns ns
t _h (H) t _h (L)	Hold time, High or Low C _{EP} or C _{ET} to CP	Waveform 5	0 0		0 0		ns ns
t _s (H) t _s (L)	Set-up time, High or Low P _E to CP	Waveform 4	8.0 8.0		9.0 9.0		ns ns
t _h (H) t _h (L)	Hold time, High or Low P _E to CP	Waveform 4	0 0		0 0		ns ns
t _s (H) t _s (L)	Set-up time, High or Low U/D to CP	Waveform 6	11.0 7.0		12.5 8.0		ns ns
t _h (H) t _h (L)	Hold time, High or Low U/D to CP	Waveform 6	0 0		0 0		ns ns
t _w (H) t _w (L)	CP _U or CP _D pulse width, High or Low	Waveform 1	5.0 5.0		5.5 5.5		ns ns

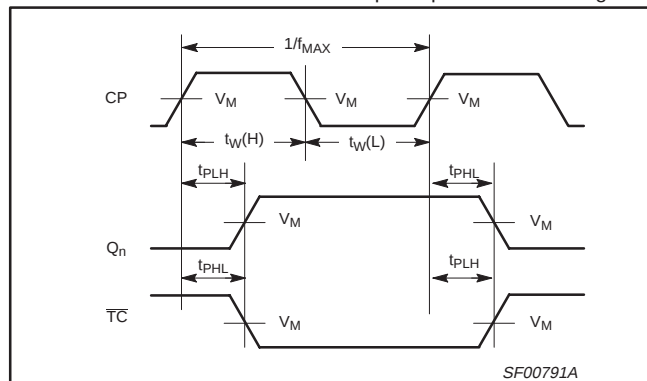
4-bit up/down binary synchronous counter

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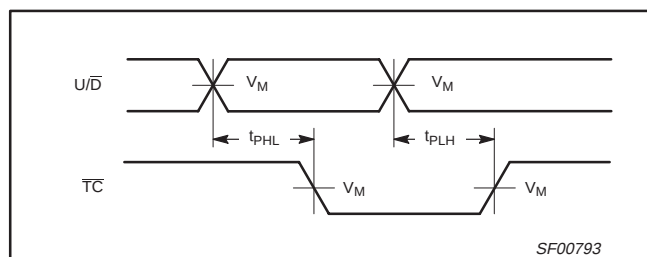
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$

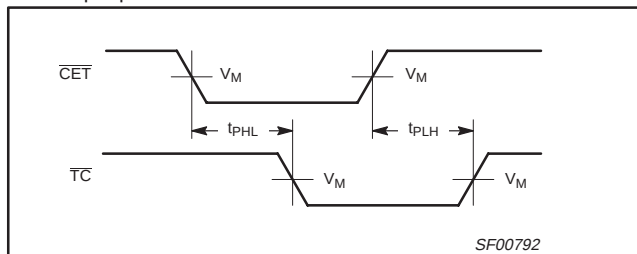
The shaded areas indicate when the input is permitted to change for predictable output performance.



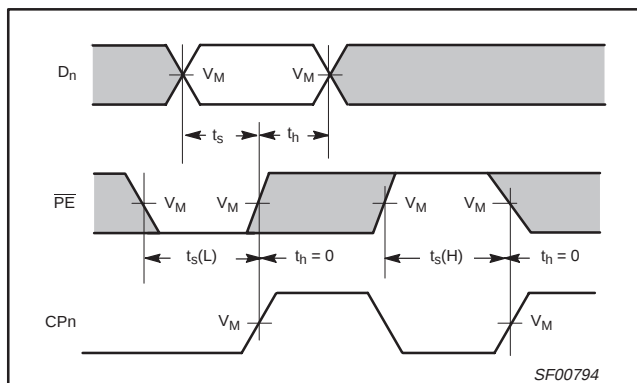
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



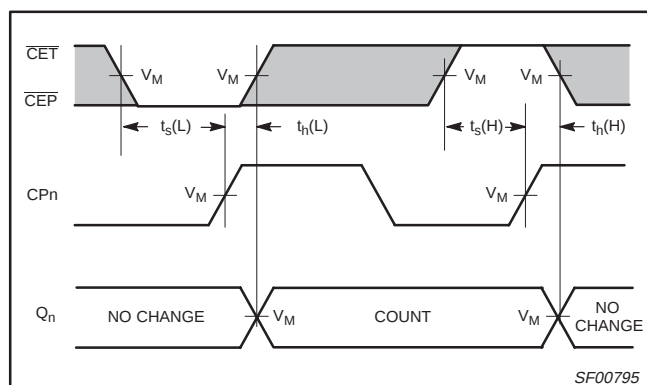
Waveform 3. Propagation Delay U/D Input to Terminal Count Output



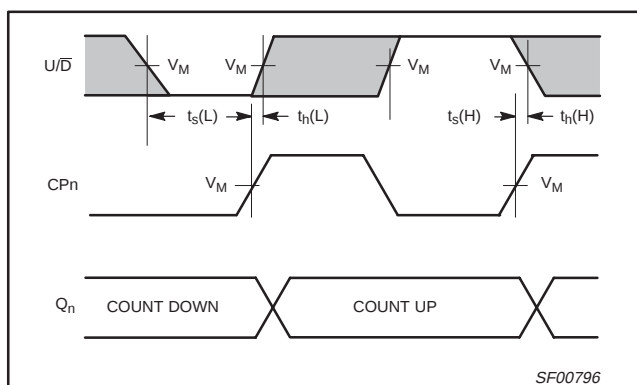
Waveform 2. Propagation Delays CET Input to Terminal Count Output



Waveform 4. Parallel Data and Parallel Enable Setup and Hold Times



Waveform 5. Count Enable Setup and Hold Times

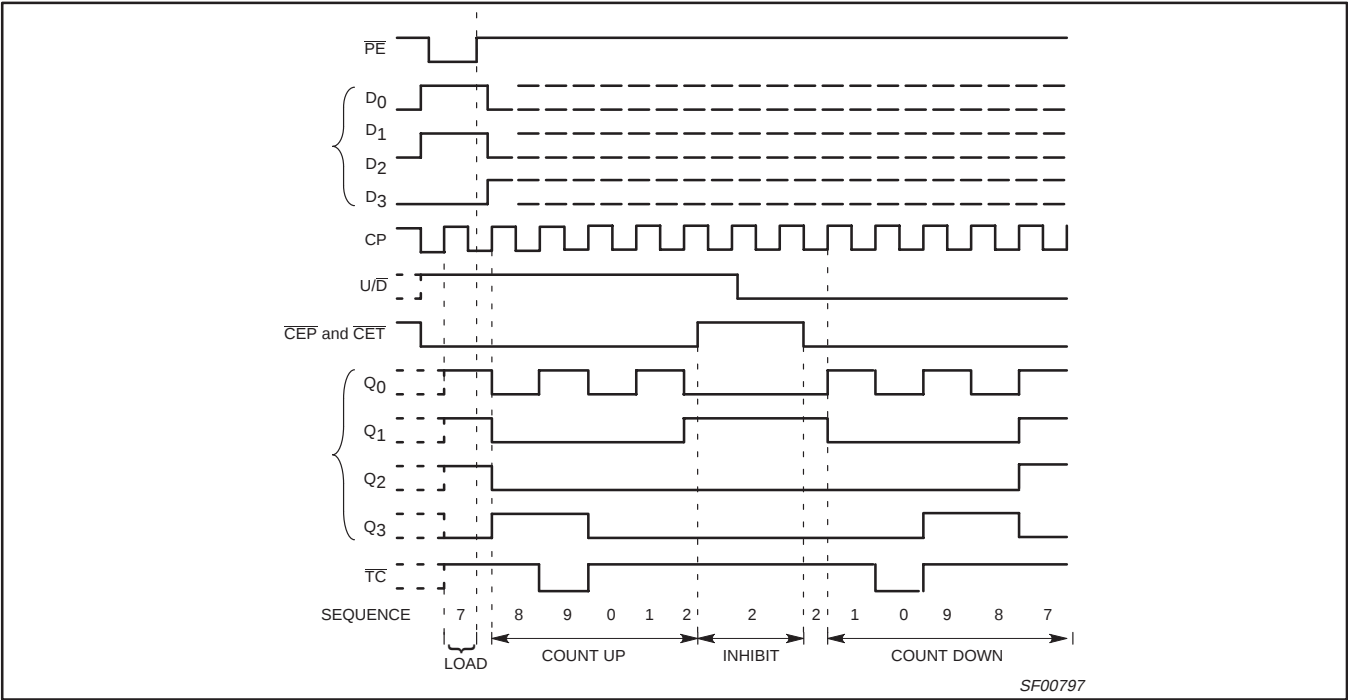


Waveform 6. Up/Down Control Setup and Hold Times

4-bit up/down binary synchronous counter

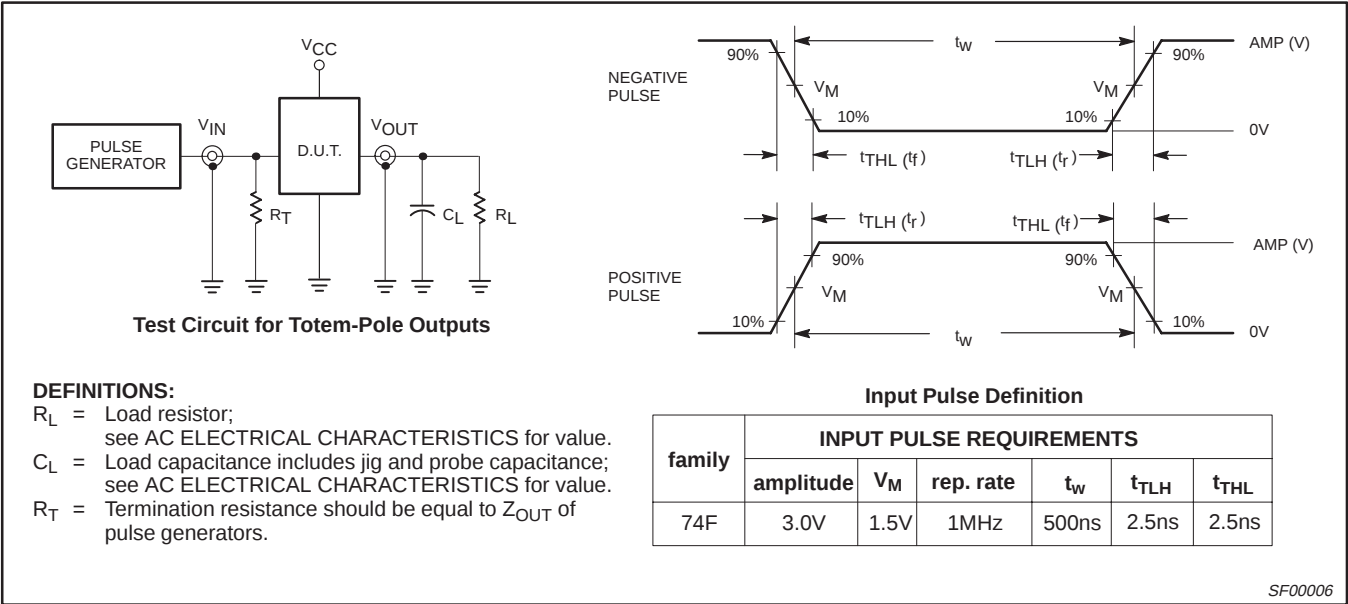
74F169

TIMING DIAGRAM (Typical Load, Count, and Inhibit Sequences)



- NOTES:**
The operation of the 74F169 is similar to the Illustration above.
1. Load (preset) to BCD seven
 2. Count up to eight, nine (maximum), zero, one, and two
 3. Inhibit
 4. Count down to one, zero (minimum), nine, eight, and seven

TEST CIRCUIT AND WAVEFORM

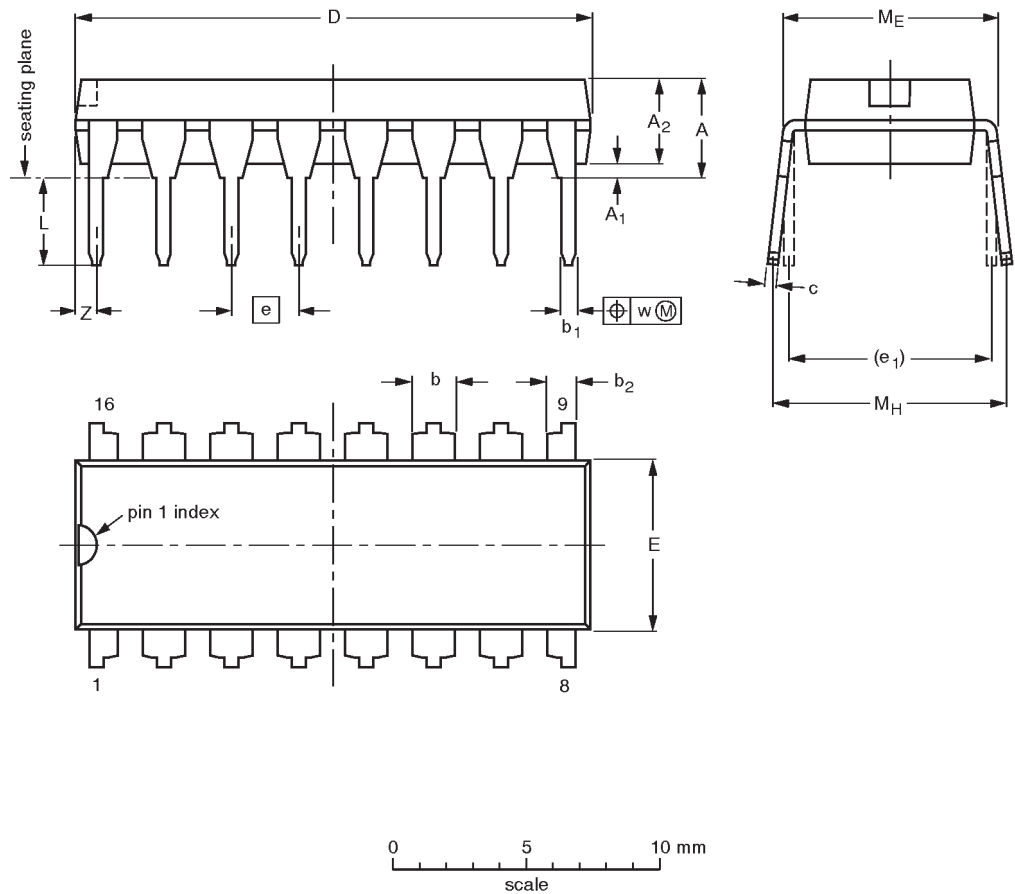


4-bit up/down binary synchronous counter

74F168*, 74F169

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

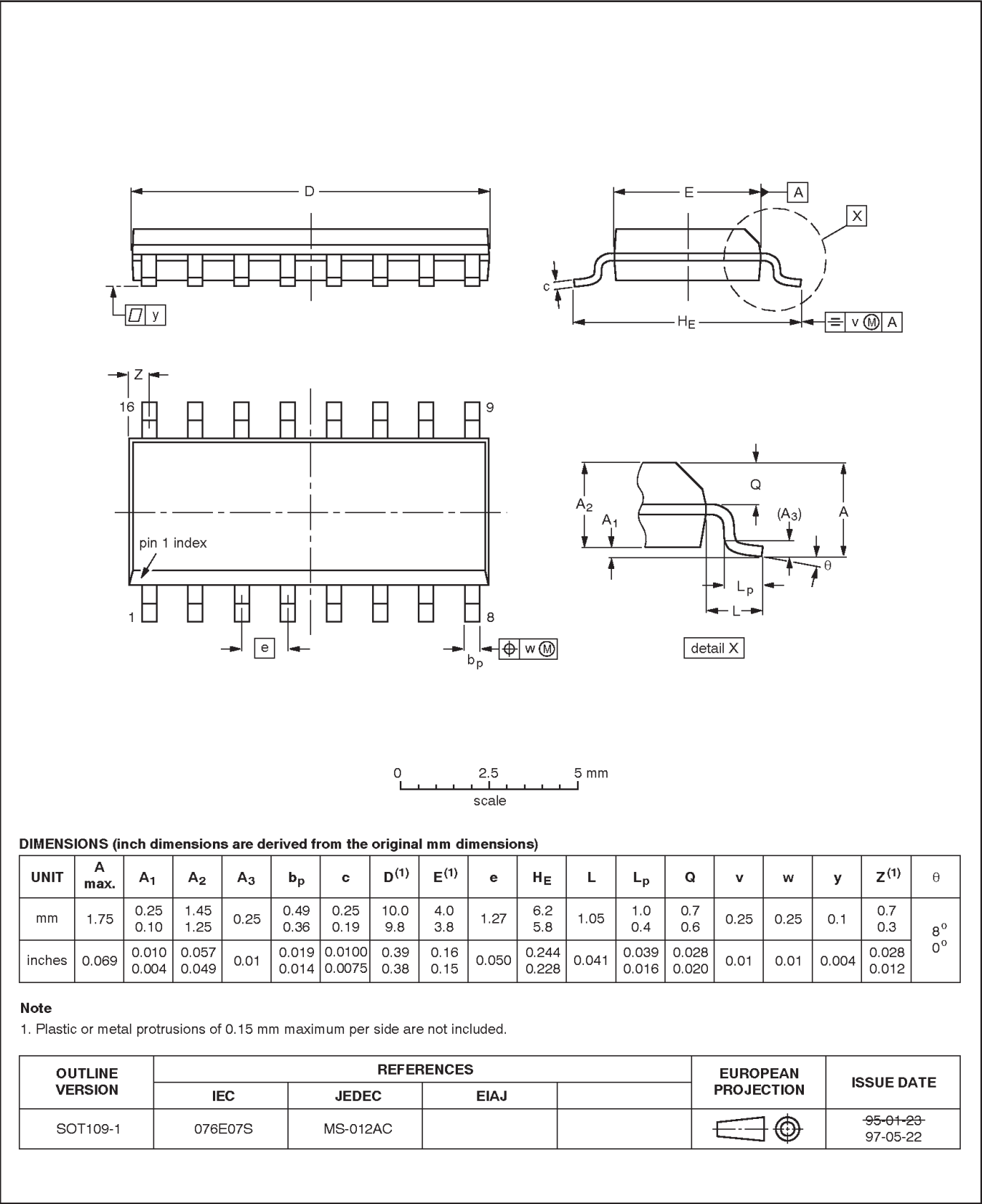
* Discontinued part. Please see the Discontinued Product List in Section 1, page 21.

4-bit up/down binary synchronous counter

74F168*, 74F169

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



* Discontinued part. Please see the Discontinued Product List in Section 1, page 21.

4-bit up/down binary synchronous counter

74F168*, 74F169

DEFINITIONS		
Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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