80515/80535

8-Bit Single-Chip Microcontroller

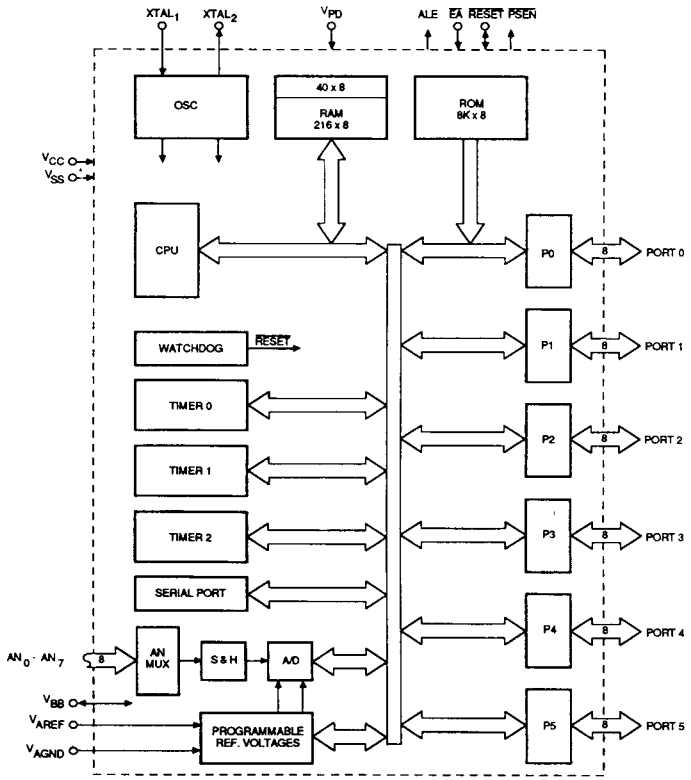
DISTINCTIVE CHARACTERISTICS

- 8K x 8 ROM (80515 only)
- 256 x 8 RAM
- Six 8-bit ports; 48 I/O lines
- Three 16-bit Timer/Event Counters
- Reload, capture, compare capabilities on Timer 2
- Full-Duplex Serial Port
- Twelve Interrupt Sources; four priority levels
- 8-bit A/D Converter
- Upward-compatible with 8051
- 16-bit Watchdog Timer
- VPD provides standby current for 40 bytes of RAM
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 μs
- 64K bytes Program Memory space
- 64K bytes Data Memory space

GENERAL DESCRIPTION

The 80515/80535 is a stand-alone, high-performance, single-chip microcontroller based on the 8051 architecture. While maintaining all the 8051 operating characteristics, the 80515/80535 incorporates several enhancements which significantly increase design flexibility and overall system performance. With on-board A/D Converter and Watchdog Timer, the 80515 is ideal for motor control applications ranging from automotive engines to vending machines. The 80535 is identical to the 80515 except that it lacks the on-chip ROM.

BLOCK DIAGRAM



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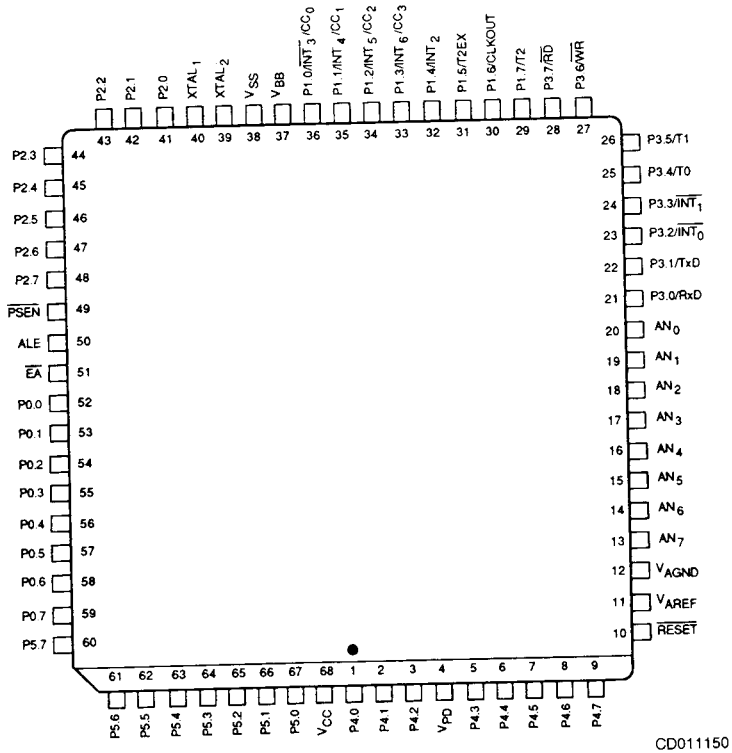
CONNECTION DIAGRAM
Top View



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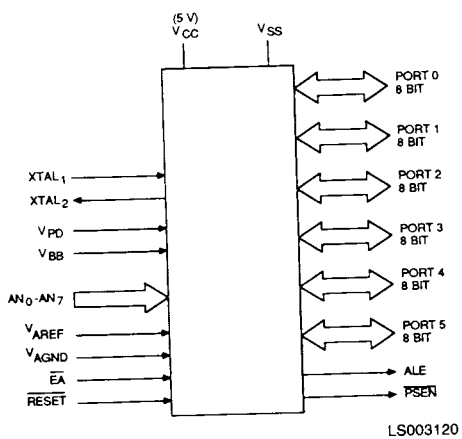
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

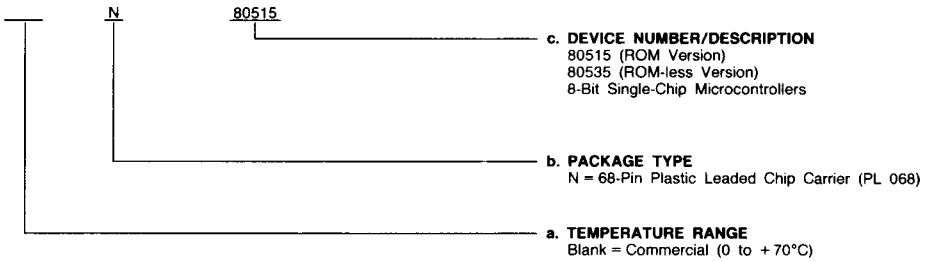


LS003120

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Temperature Range**
b. Package Type
c. Device Number



Valid Combinations
N80515
N80535

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Port 0 Port 0 (Input/Output; Open Drain)

Port 0 is an open-drain bidirectional I/O port. Port 0 pins that have "1"s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed LOW-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting "1"s. Port 0 can sink/source eight LS TTL inputs. Port 0 also outputs the code bytes during program verification in the 80515. External pullups are required during program verification.

Port 1 Port 1 (Input/Output)

Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 output buffers can sink/source four LS TTL inputs. Port 1 pins that have "1"s written to them are pulled HIGH by the internal pullups and — when in this state — can be used as inputs. As inputs, Port 1 pins that are externally being pulled LOW will source current (I_{IL} on the data sheet) because of the internal pullups. Port 1 also receives the LOW-order address bytes during program verification.

Port 1 also serves the functions of various special features as listed below:

Port	Symbol	Alternate Function
P1.0	$\overline{INT3}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{INT2}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input

Port 2 Port 2 (Input/Output)

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four LS TTL inputs. Port 2 pins having "1"s written to them are pulled HIGH by the internal pullups and — while in this state — can be used as inputs. As inputs, Port 2 pins externally being pulled LOW will source current (I_{IL}) because of the internal pullups.

Port 2 emits the HIGH-order address byte during fetches from External Program Memory and during accesses to External Data Memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting "1"s. During accesses to External Data Memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function register.

Port 2 also receives the HIGH-order address bits during ROM verification.

Port 3 Port 3 (Input/Output)

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four LS TTL inputs. Port 3 pins that have "1"s written to them are pulled HIGH by the internal pullups and — while in this state — can be used as inputs. As inputs, Port 3 pins externally being pulled LOW will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features as listed below:

Port	Symbol	Alternate Function
P3.0	RXD	Serial input port
P3.1	TXD	Serial output port
P3.2	$\overline{INT0}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{INT1}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{WR}$	External Data Memory write strobe
P3.7	$\overline{RD}$	External Data Memory read strobe

Port 4 Port 4 (Input/Output)

Port 4 is an 8-bit quasi-bidirectional I/O port. Port 4 can sink/source four LS-TTL loads.

Port 5 Port 5 (Input/Output)

Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source four LS-TTL loads.

$\overline{RST}$ $\overline{Reset}$ (Input; Active LOW)

A LOW level on this pin for the duration of two machine cycles while the oscillator is running resets the 80515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.

ALE Address Latch Enable (Output; Active HIGH)

Address Latch Enable output pulse for latching the LOW byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, allowing use for external-timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$ $\overline{Program\ Store\ Enable}$ (Input; Active LOW)

$\overline{PSEN}$ is the read strobe to External Program Memory. When the 80515 is executing code from External Program Memory, $\overline{PSEN}$ is activated twice each machine cycle — except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory. $\overline{PSEN}$ is not activated during fetches from Internal Program Memory.

$\overline{EA}$ $\overline{External\ Access\ Enable}$ (Input; Active LOW)

$\overline{EA}$ must be externally held LOW to enable the device to fetch code from external Program Memory locations 0000H to 1FFFH. If $\overline{EA}$ is held HIGH, the device executes from Internal Program Memory unless the program counter contains an address greater than 1FFFH. For the 80535, $\overline{EA}$ must be LOW.

$XTAL_1$ Crystal (Input)

Input to the inverting oscillator amplifier. When an external oscillator is used, $XTAL_1$ should be grounded.

$XTAL_2$ Crystal (Output)

Output of the inverting oscillator amplifier. $XTAL_2$ is also the input for the oscillator signal when using an external oscillator.

V_{CC} Power Supply

Supply voltage during normal operations.

V_{SS} Circuit Ground

V_{PD} Power-Down Supply
If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 bytes of the internal RAM. When V_{PD} is LOW, the RAM's current is drawn from V_{CC}.

V_{AREF} Reference Voltage for the A/D Converter

V_{AGND} Reference Ground for the A/D Converter

$AN_0 - AN_7$ Multiplexed Analog Inputs

V_{BB} Substrate Pin
Must be connected to V_{SS} through a capacitor (100 to 1000 nF) for proper operation of the A/D converter.

FUNCTIONAL DESCRIPTION

The architecture of the 80515 is based on the 8051 Microcontroller. The following 8051 features are retained in the 80515:

- Instruction set
- External memory expansion interface (Port 0 and Port 2)
- Full-duplex serial port
- Timer/counters 0 and 1
- Alternate functions on Port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM.

The 80515 contains an additional 128 byte of internal RAM and 4 Kbyte of internal ROM; thus a total of 256 byte RAM and 8 Kbyte ROM on-chip. The 80515 has a third 16-bit timer/controller with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with 8 analog inputs and programmable reference voltages, two additional quasi-bidirectional 8-bit ports, a programmable clock output (fosc/12), a RAM power-down supply, which supplies 40 byte with a typical current of 1 mA, and a powerful interrupt structure with 12 sources and 4 priority levels.

Figure 2 shows a detailed block diagram of the 80515.

CPU

The 80515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of Program Memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12-MHz crystal, 58% of the instructions execute in 1.0 μs.

Memory Organization

The 80515 manipulates operands in the four memory address spaces described below:

Program Memory

The 80515 has 8 Kbyte of on-chip ROM, while the 80535 has no internal ROM. The Program Memory can be externally expanded up to 64 Kbyte. If the $\overline{EA}$ pin is held HIGH, the 80515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through FFFFH are then fetched from the External Program Memory. If the $\overline{EA}$ pin is held LOW, the 80515 fetches all instructions from the External Program Memory. Since the 80535 has no internal ROM, pin $\overline{EA}$ must be tied LOW when using this device.

Data Memory

The Data Memory address space consists of an internal and an external memory space. The Internal Data Memory is divided into three physically separate and distinct blocks: the lower 128 byte of RAM; the upper 128 byte of RAM; and the 128-byte special function register (SFR) area. While the upper 128 byte of Data Memory and the SFR area share the same address locations, they are accessed only through different addressing modes. The lower 128 byte of Data Memory can be accessed through direct or register-indirect addressing; the upper 128 byte of RAM can be accessed through register-indirect addressing; and the special function registers are accessible only through direct addressing.

Four 8-register banks occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly accessible bit locations. The stack can be located anywhere in the Internal Data Memory address space, and the stack depths can be expanded up to 256 byte.

The External Data Memory can be expanded up to 64 Kbyte and can be accessed by instructions that use a 16-bit or 8-bit address.

All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 41 special function registers (SFRs) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in Table 1.

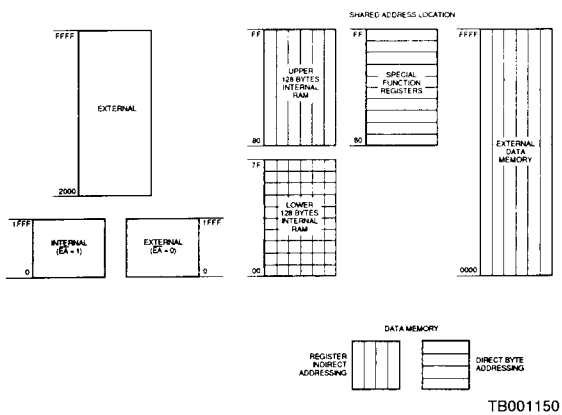


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Figure 1. Memory Address Spaces

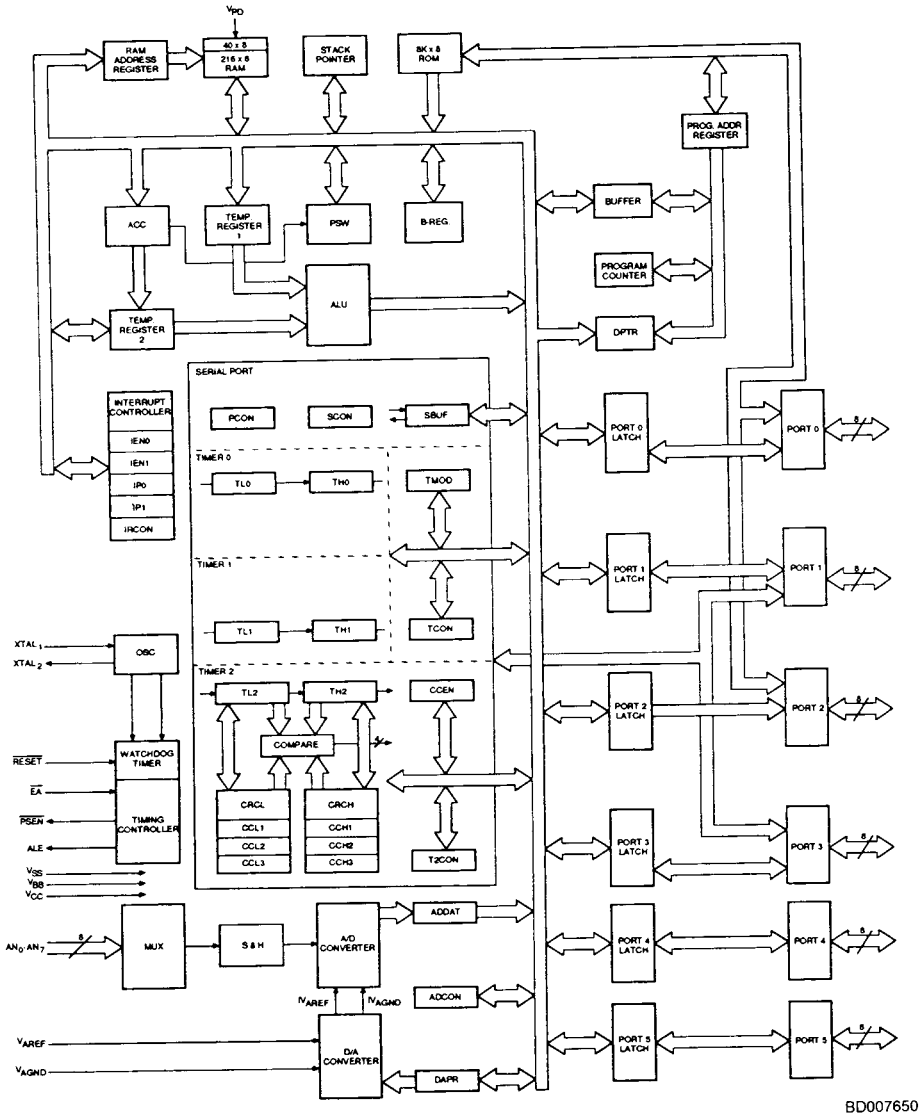


Figure 2. Detailed Block Diagram

TABLE 1. SPECIAL FUNCTION REGISTERS

Addr (HEX)	Symbol	Name	Default After Power-On Reset
* 80	P0	Port 0	11111111
81	SP	Stack Pointer	00000111
82	DPL	Data Pointer, LOW Byte	00000000
83	DPH	Data Pointer, HIGH Byte	00000000
87	PCON	Power Control Register	0XXXXXXX
* 88	TCON	Timer Control Register	00000000
89	TMOD	Timer Mode Register	00000000
8A	TL0	Timer 0, LOW Byte	00000000
8B	TL1	Timer 1, LOW Byte	00000000
8C	TH0	Timer 0, HIGH Byte	00000000
8D	TH1	Timer 1, HIGH Byte	00000000
* 90	P1	Port 1	11111111
* 98	SCON	Serial Port Control Register	00000000
99	SBUF	Serial Port Buffer Register	Indeterminate
* 0A0	P2	Port 2	11111111
* 0A9	IEN0	Interrupt Enable Register 0	00000000
0A9	IP0	Interrupt Priority Register 0	00000000
* 0B0	P3	Port 3	11111111
* 0B9	IEN1	Interrupt Enable Register 1	00000000
0B9	IP1	Interrupt Priority Register 1	00000000
* 0C0	IRCON	Interrupt Request Control Register	00000000
0C1	CCEN	Compare/Capture Enable Register	00000000
0C2	CCL1	Compare/Capture Register 1, LOW Byte	00000000
0C3	CCH1	Compare/Capture Register 1, HIGH Byte	00000000
0C4	CCL2	Compare/Capture Register 2, LOW Byte	00000000
0C5	CCH2	Compare/Capture Register 2, HIGH Byte	00000000
0C6	CCL3	Compare/Capture Register 3, LOW Byte	00000000
0C7	CCH3	Compare/Capture Register 3, HIGH Byte	00000000
* 0C8	T2CON	Timer 2 Control Register	00000000
0CA	CRCL	Compare/Reload/Capture Register, LOW Byte	00000000
0CB	CRCH	Compare/Reload/Capture Register, HIGH Byte	00000000
0CC	TL2	Timer 2, LOW Byte	00000000
0CD	TH2	Timer 2, HIGH Byte	00000000
* 0D0	PSW	Program Status Word Register	00000000
* 0D8	ADCON	A/D-Converter Control Register	00000000
0D9	ADDAT	A/D-Converter Data Register	00000000
0DA	DAPR	D/A-Converter Program Register	00000000
* 0E0	ACC	Accumulator	00000000
* 0E8	P4	Port 4	11111111
* 0F0	B	B Register	00000000
* 0F8	P5	Port 5	11111111

The SFRs marked with an asterisk (*) are both bit and byte-addressable.
Figure 1 illustrates the memory address spaces of the 80515.

I/O Ports

The 80515 has six 8-bit ports. Port 0 is an open-drain bidirectional I/O port, while Ports 1 through 5 are quasi-bidirectional I/O ports with internal pullups. That means, when configured as inputs, Ports 1 through 5 will pull HIGH and will source current when externally pulled LOW. Port 0 will float when configured as input.

Port 0 and Port 2 can be used to expand the Program and Data Memory externally. During an access to external memory, Port 0 emits the LOW-order address byte and reads/writes the data byte, while Port 2 emits the HIGH-order address byte. In this function, Port 0 is an open-drain port, but uses a strong internal pullup FET.

Timer/Counters

The 80515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

Timer/Counters 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{INT_0}$ and $\overline{INT_1}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

Timer 2

The term "timer 2" refers to a complex circuit consisting of the following registers:

T2CON	Timer 2 control register
TL2	Timer 2 register, low-byte
TH2	Timer 2 register, high-byte
CRCL	Compare/reload/capture register, low-byte
CRCH	Compare/reload/capture register, high-byte
CCL1	Compare/capture register 1, low-byte
CCH1	Compare/capture register 1, high-byte
CCL2	Compare/capture register 2, low-byte
CCH2	Compare/capture register 2, high-byte
CCL3	Compare/capture register 3, low-byte
CCH3	Compare/capture register 3, high-byte
CCEN	Compare/capture enable register

For brevity, the double-byte compare/reload/capture register is called the CRC register, the three double-byte compare/capture registers are called CC registers 1 to 3.

Six bits of Port 1 are used by the timer 2 circuit for special functions:

P1.0/$\overline{INT_3}$/CC_0	Compare output/capture input for the CRC register
P1.1/INT_4/CC_1	Compare output/capture input for CC register 1
P1.2/INT_5/CC_2	Compare output/capture input for CC register 2
P1.3/INT_6/CC_3	Compare output/capture input for CC register 3
P1.5/T2EX	External reload trigger input
P1.7/T2	External count or gate input to timer 2

To use the special functions on pins P1.5/T2EX and P1.7/T2 a one (1) must first be written into the appropriate bit latches. For pins P1.0 to P1.3, it depends on the special function whether the bit latches must contain a one (1) or not. Should those pins be used as interrupt or capture inputs, the corresponding bit latches must contain a one (1). If those pins are used as compare outputs, the value written to the bit latches depends on the compare modes established.

In addition to the operational modes "timer" or "counter," timer 2 provides the features of:

— 16-bit reload

— 16-bit compare

— 16-bit capture

Figure 3 shows a block diagram of the timer 2 circuit.

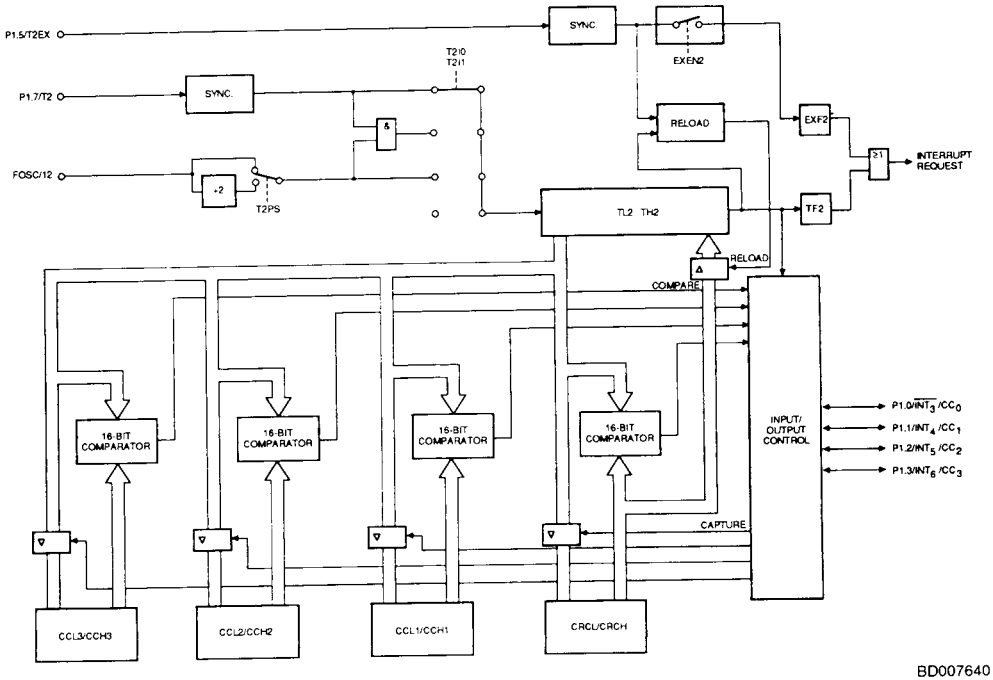


Figure 3. Block Diagram of Timer/Counter 2

The timer 2 can operate either as timer, event counter, or gated timer. In timer function, the count rate is derived from the oscillator frequency. A 2:1 prescaler offers the possibility to select a count rate of 1/12 or 1/24 of the oscillator frequency. Thus, the 16-bit timer 2 register (consisting of TL2 and TH2) is incremented every machine cycle or every second machine cycle. The prescaler is selected by bit T2PS in special function register T2CON (see Figure 4). If T2PS is cleared, the input frequency is 1/12 of the oscillator frequency; if T2PS is set, the 2:1 prescaler gates 1/24 of the oscillator frequency to the timer.

In gated timer function, the external input pin T2 (P1.7) functions as a gate to the input of timer 2. If T2 is high, the counted input is gated to the timer. T2 = 0 stops the counting procedure. This will facilitate pulse width measurements.

T2PS	I3FR	I2FR	T2R1	T2R0	T2CM	T2I1	T2I0	BIT
0CFH	0CEH	0CDH	0CCH	0CBH	0CAH	0C9H	0C8H	ADDRESS

SYMBOL	POSITION	FUNCTION
T2I0 T2I1	T2CON.0 T2CON.1	Timer 2 Input Selection. See Table 2.
T2CM	T2CON.2	Compare Mode Bit. When set, compare mode 1 is selected. T2CM = 0 selects compare mode 0.
T2R0 T2R1	T2CON.3 T2CON.4	Timer 2 Reload Mode Selection. See Table 3.
I2FR	T2CON.5	External Interrupt 2 Falling/Rising Edge Flag. When set, the interrupt 2 request flag IEX2 will be set on a positive transition at pin P1.4/$\overline{INT_2}$. I2FR = 0 specifies external interrupt 2 to be negative-transition active.
I3FR	T2CON.6	External Interrupt 3 Falling/Rising Edge Flag. When set, the interrupt 3 request flag IEX3 will be set on a positive transition at pin P1.0/$\overline{INT_3}$/CC_0. I3FR = 0 specifies external interrupt 3 to be negative-transition active.
T2PS	T2CON.7	Prescaler Select Bit. When set, timer 2 is clocked in the "timer" or "gated timer" function with 1/24 of the oscillator frequency. T2PS = 0 gates fosc/12 to timer 2. T2PS must be 0 for the counter operation of timer 2.

Figure 4. Timer 2 Control Register T2CON (0C8H)

In counter function, the timer 2 register is incremented in response to a 1-to-0 transition at its corresponding external input pin T2 (P1.7). In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a HIGH in one cycle and a LOW in the next cycle, the count is incremented. The new count value appears in the register during S1P1 of the cycle following the one in which the transition was detected. Since it takes two machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Note: The prescaler must be off for proper counter operation of timer 2, that means T2PS must be 0.

In either case, no matter whether timer 2 is configured as timer, event counter, or gated timer, a rolling over of the count from all 1s to all 0s sets the timer 2 overflow flag TF2 (bit 6 in SFR IRCON, Interrupt Request Control) which can generate an interrupt.

The input clock to timer 2 is selected by bits T2I0, T2I1, and T2PS as listed in Table 2.

TABLE 2. TIMER 2 INPUT SELECTION

T2I1	T2I0	Function
0	0	No Input Selected, Timer 2 Stops
0	1	Timer Function, Input Frequency = fosc/12 (T2PS = 0) or fosc/24 (T2PS = 1)
1	0	Counter Function, External Input Signal at Pin T2/P1.7
1	1	Gated Timer Function. Input Controlled by Pin T2/P1.7

Reload

The reload mode for timer 2 is selected by bits T2R0 and T2R1 in SFR T2CON as illustrated in Table 3. In mode 0, when timer 2 rolls over from all 1s to all 0s, it not only sets TF2 but also causes the timer 2 registers to be loaded with the 16-bit value in the CRC register which is preset by software. The reload will happen in the same machine cycle in which TF2 is set, thus overwriting the count value 0000H. In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the corresponding input pin T2EX/P1.5. In addition, this transition will set flag EXF2 if bit EXEN2 in SFRIEN1 is set. If the timer 2 interrupt is enabled, setting EXF2 will generate an interrupt. The external input pin T2EX is sampled

during S5P2 of every machine cycle. When the sampling shows a HIGH in one cycle and a LOW in the next cycle, a transition will be recognized. The reload of the timer 2 registers will then take place during S2P1 of the cycle following the one in which the transition was detected.

Figure 5 shows a functional diagram of the timer 2 reload modes.

TABLE 3. TIMER 2 RELOAD MODE SELECTION

T2R1	T2R0	Mode
0	X	Reload Disabled
1	0	Mode 0: Auto-Reload upon Timer 2 Overflow (TF2)
1	1	Mode 1: Reload upon Falling Edge at Pin T2EX/P1.5

T2R1 = 0 disables the reload modes 0 and 1. If the reload modes are disabled, and if EXEN2 is set, a negative transition at pin T2EX/P1.5 can be used as additional external interrupt input.

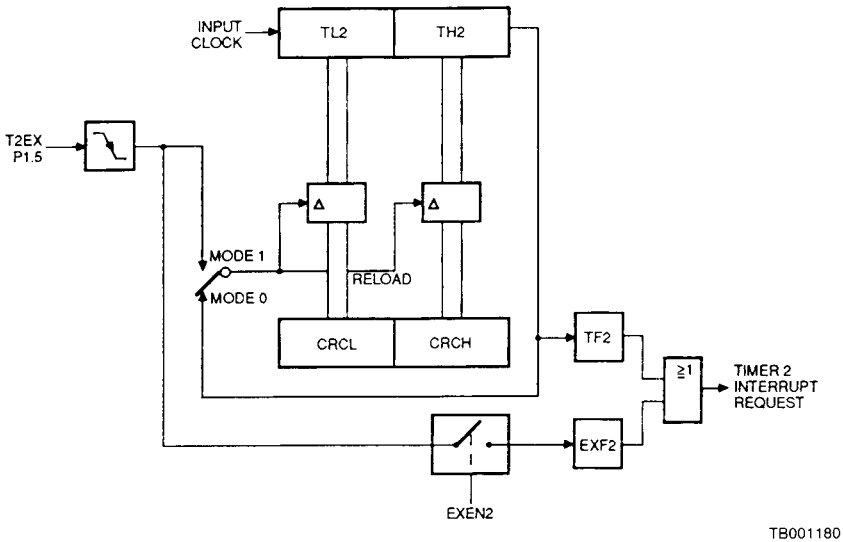


Figure 5. Timer 2 in Reload Mode

Compare

In compare mode, the 16-bit values stored in the dedicated compare registers are compared with the contents of the timer 2 registers (TL2 and TH2). If the count value in the timer 2 registers matches the stored one, an appropriate output signal is generated at the corresponding Port 1 pin, and interrupt is requested.

The compare modes are enabled by setting the appropriate bits in SFR CCEN (compare/capture enable register, see Figure 11). There are two different compare modes which are selected by bit T2CM in T2CON.

In mode 0, upon a match, the output signal changes from LOW to HIGH. It goes back to a LOW level on timer 2 overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer 2 circuit, and not by the user. Writing to the port will operate as a "dummy" instruction. Figure 6 shows a functional diagram of the Port 1 latches P1.0 to P1.3 in compare mode 0. The port latch is directly controlled by the two signals TF2 and compare. The input line from the internal bus and the "write-to-latch" line are disconnected when compare mode 0 is enabled.

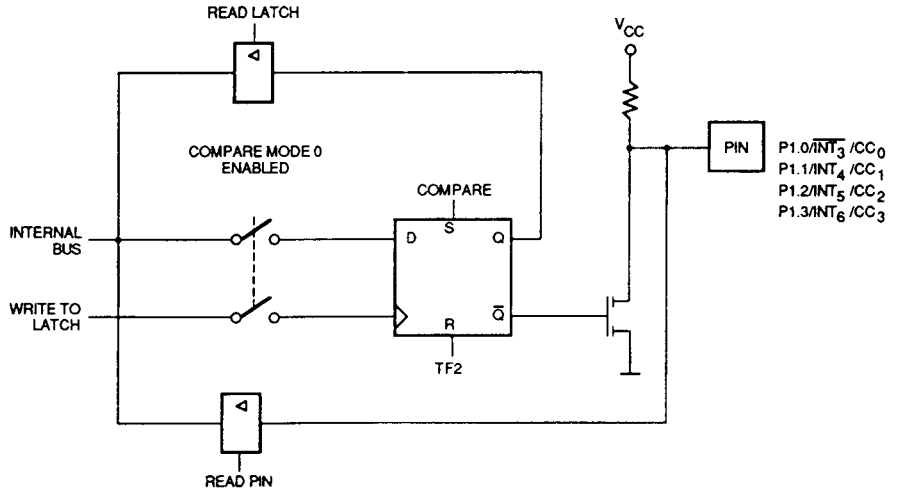


Figure 6. Functional Diagram of Port Latches P1.0 to P1.3 in Compare Mode 0

In mode 1, the software determines the transition of the output signal. If mode 1 is enabled, and the software writes to the appropriate output pin at Port 1, the new value will not appear at the output pin until the next compare event occurs. Thus, the user can select whether the output signal makes a 1-to-0 or a 0-to-1 transition at the time the t imer 2 count matches the stored compare value. Figure 7 shows a functional diagram of the Port 1 latches P1.0 to P1.3 in compare mode 1. In this function, the "port latch" consists of two separate latches. The "left" latch can be written to under software control, but this value will only be transferred to the "right" latch (and to the port pin) in response to a compare event. Note that the "right" latch is transparent as long as the internal compare signal is active. While the compare signal is active, a write operation to the port will change both latches. A "read-modify-write" instruction will read the user-controlled "left" latch, and write the modified value back to this "left" latch.

In both compare modes, the new value arrives at the Port 1 pin within the same machine cycle in which the internal compare signal is activated.

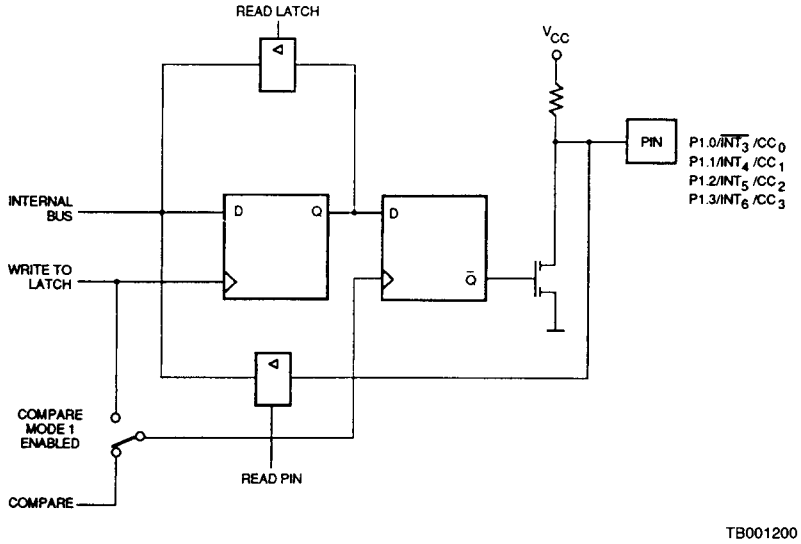
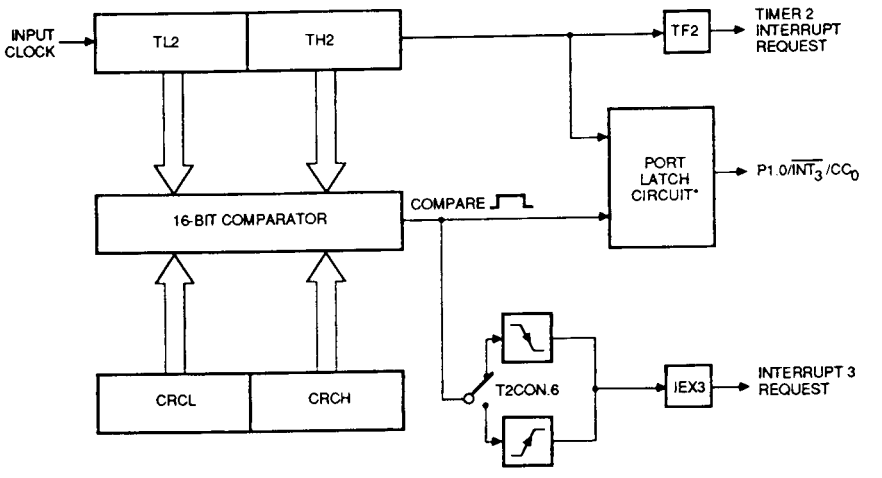


Figure 7. Functional Diagram of Port Latches P1.0 to P1.3 in Compare Mode 1

Figure 8 shows a functional diagram of timer 2 in the compare mode using the CRC register. Figure 9 shows the compare modes with reference to the CC register 1. Except for the symbolic names, this diagram applies also to the CC registers 2 and 3.

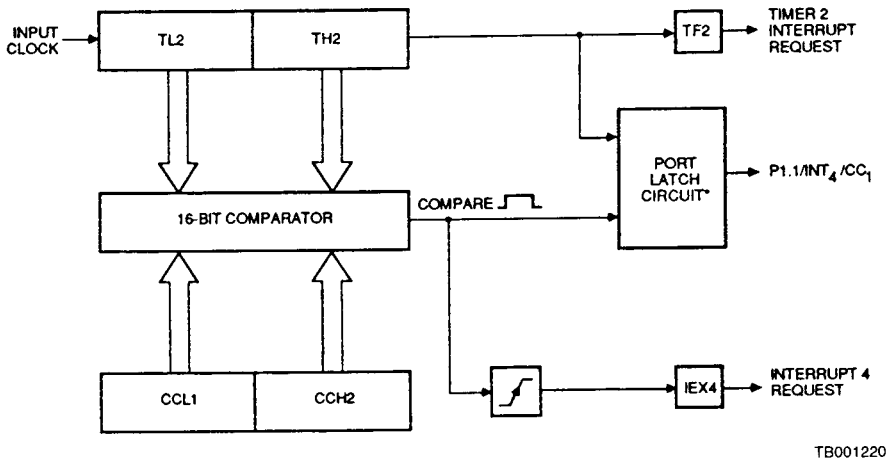
Note that the compare signal is active as long as the timer 2 contents are equal to the one of the appropriate compare register, and that it has a rising and a falling edge. Thus, when using the CRC register, it can be selected whether an interrupt should be caused when the compare signal goes active or inactive, depending on the status of bit I3FR in T2CON. For the CC registers 1 to 3 an interrupt is always requested when the compare signal goes active.

If the compare function is enabled, the corresponding Port 1 pin is dedicated to act as output. The level at the port pin can be read under software control, but the input line from the port pin to the interrupt system is disconnected. Thus, a change of the pin's level will not cause a setting of the corresponding interrupt flag. In the compare modes, the external interrupt request flags can only be set by the internally generated compare signal.



*See Figures 6 and 7.

Figure 8. Functional Diagram of Timer 2 in Compare Mode Using CRC Register



*See Figures 6 and 7.

Figure 9. Functional Diagram of Timer 2 in Compare Mode Using CC Register 1

Capture

Each of the three compare/capture registers and the CRC register can be used to latch the current 16-bit value in the timer 2 registers TL2 and TH2. Two different modes are provided for this function. In mode 0, an external event causes a latching of the timer 2 contents to a dedicated capture register. In mode 1, a capture will occur upon writing to the low-order byte of the dedicated 16-bit capture register. This mode is provided to allow the software to read the timer 2 contents "on the fly."

In mode 0, the external event causing a capture is:

— for CC registers 1 to 3: a positive transition at pins CC1 to CC3 of CC registers 1 to 3;

— for the CRC register: a positive or negative transition, depending on the status of bit I3FR in SFR T2CON, at pin CC0. If bit I3FR is cleared, a capture occurs in response to a negative transition, if bit I3FR is set in response to a positive transition at pin P1.0/$\overline{INT_3}$/CC_0.

In this mode, the appropriate Port 1 pin is used as input, and the port latch must be programmed to contain a one (1). The external input is sampled during S5P2 in every machine cycle. When the sampling shows a LOW (HIGH for input CC0, if it is programmed to be negative-transition-active) in one cycle and a HIGH (LOW) in the next cycle, a transition is recognized. The timer 2 contents are latched to the appropriate capture register during S3P1 in the cycle following the one in which the transition was identified.

In mode 0, a transition on the external capture inputs CC0 to CC3 will also cause setting of the corresponding external interrupt request flags IEX3 to IEX6. If the interrupts are enabled, an external capture signal will cause the CPU to vector to the appropriate interrupt service routine.

In mode 1, a capture occurs in response to a MOV instruction to the low-order byte of a capture register. The "write-to-register" signal (e.g., "write to CRCL") is used to initiate a capture. The value written to the dedicated capture register is irrelevant for this function. The timer 2 contents will be latched into the appropriate capture register in the cycle following the MOV instruction. In this mode no interrupt request will be generated.

In both capture modes the value latched in the machine cycle in w hich the capture occurs will be the actual contents of timer 2 in that machine cycle.

Figures 10-1 and 10-2 show functional diagrams of the capture function of timer 2. Figure 10-1 illustrates the operation for the CRC register, while Figure 10-2 shows the operation applying to the compare/capture register 1. This operation is the same for CC register 1 as well as for the CC registers 2 and 3. Substitute the symbols for the corresponding signals and names of CC registers 2 and 3 in Figure 10-2.

The two capture modes can be established individually for each capture register by bits in SFR CCEN (compare/capture enable register), with 2 bits for each capture register. That means, other than for the compare modes, it is possible to select mode 0 for one capture register and mode 1 for another register simultaneously. The bit positions and functions of CCEN are listed in Figure 11.

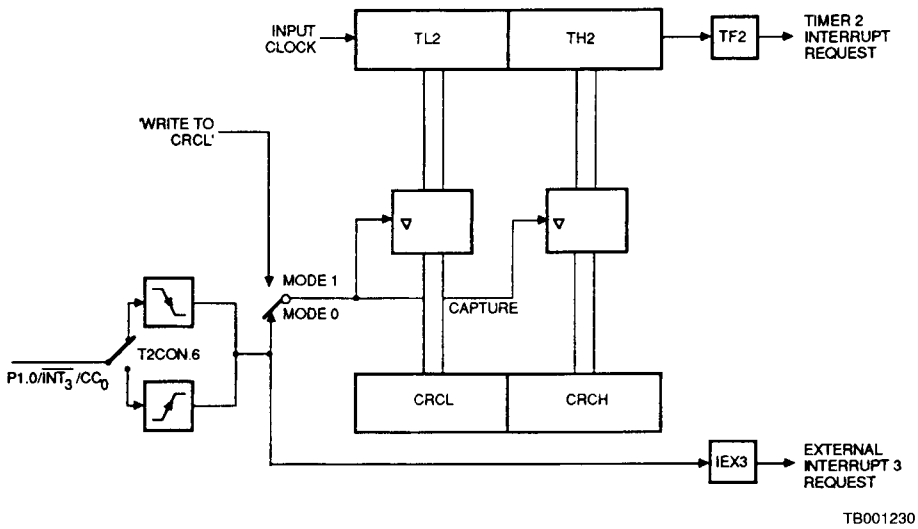


Figure 10-1. Functional Diagram of Timer 2 in Capture Mode Using CRC Register

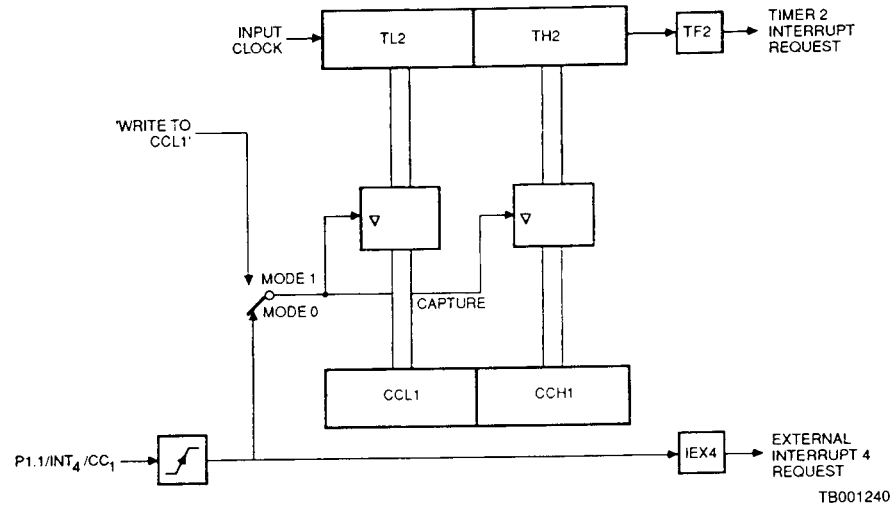


Figure 10-2. Functional Diagram of Timer 2 in Capture Mode Using CC Register 1

7	6	5	4	3	2	1	0	BIT

BIT		FUNCTION
1	**0**	**CRC Register**
0	0	Compare/Capture Disabled
0	1	Capture on Falling/Rising Edge at Pin P1.0/$\overline{INT_3}$/CC_0
1	0	Compare Enabled
1	1	Capture on Write Operation into Register CRCL
3	**2**	**CC Register 1**
0	0	Compare/Capture Disabled
0	1	Capture on Falling/Rising Edge at Pin P1.1/$\overline{INT_4}$/CC_1
1	0	Compare Enabled
1	1	Capture on Write Operation into Register CCL1
5	**4**	**CC Register 2**
0	0	Compare/Capture Disabled
0	1	Capture on Falling/Rising Edge at Pin P1.2/$\overline{INT_5}$/CC_2
1	0	Compare Enabled
1	1	Capture on Write Operation into Register CCL2
7	**6**	**CC Register 3**
0	0	Compare/Capture Disabled
0	1	Capture on Falling/Rising Edge at Pin P1.3/$\overline{INT_6}$/CC_3
1	0	Compare Enabled
1	1	Capture on Write Operation into Register CCL3

Figure 11. Compare/Capture Enable Register CCEN (0C1H)

Watchdog Timer

As a means of safe recovery from software or hardware upset, a watchdog timer is provided in the 80515. If the software fails to clear the watchdog timer at least every 65,532 μs, an internal hardware reset will be initiated. The software can be designed such that the watchdog times out if the program does not progress properly. The watchdog will also time out if the software error was due to hardware-related problems. This prevents the controller from malfunctioning for longer than 65 ms if a 12 MHz oscillator is used.

The watchdog timer is a 16-bit counter which is incremented once every machine cycle. After an external reset, the watchdog timer is disabled and cleared to 0000H. The counter is started by setting bit SWDT (bit 6 in SFR IEN1). After having been started, the watchdog timer 0000H by cannot be stopped by software. It can only be cleared to 0000H by first setting bit WDT (IEN0.6) and with the next instruction setting SWDT. Bit WDT will automatically be cleared during the third machine cycle after having been set. This double instruction clearing of the watchdog timer was implemented to minimize the chance of unintentionally clearing the watchdog. To prevent the watchdog from overflowing, it must be cleared periodically.

If the software fails to clear the watchdog in time, an internally generated watchdog reset is entered at the counter state FFFCH, which lasts four machine cycles. This internal reset differs from an external reset only to the extent that the watchdog timer is not disabled and bit WDTS (watchdog timer status, bit 6 in SFR IP0) is set. Bit WDTS allows the software to examine from which source the reset was initiated. If it is set, the reset was caused by a watchdog timer overflow.

Serial Port

The serial port of the 80515 permits the full-duplex communication between microcontrollers or between microcontrollers and peripheral devices. The serial port can operate in four modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. Eight bits are transmitted/received — eight data bits (LSB) first. The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: Ten bits are transmitted (through RxD) or received (through TxD) — a start bit (0), eight data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: Eleven bits are transmitted (through RxD) or received (through TxD) — a start bit (0), eight data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: Eleven bits are transmitted (through TxD) or received (through RxD) — a start bit (0), eight data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is the same as mode 2 in all respects except the baud rate; the baud rate in mode 3 is variable.

The variable baud rates can be generated by timer 1 or an internal baud rate generator.

A/D Converter

The 80515 provides an 8-bit A/D converter with eight multiplexed analog input channels on-chip. In addition, the A/D converter has a sample and hold circuit and offers the feature of software-programmable reference voltages. For the conversion, the method of successive approximation with a capacitor network is used.

Figure 12 shows a block diagram of the A/D converter. There are three user-accessible special function registers: ADCON (A/D converter control register), ADDAT (A/D converter data register), and DAPR (D/A converter program register) for the programmable reference voltages.

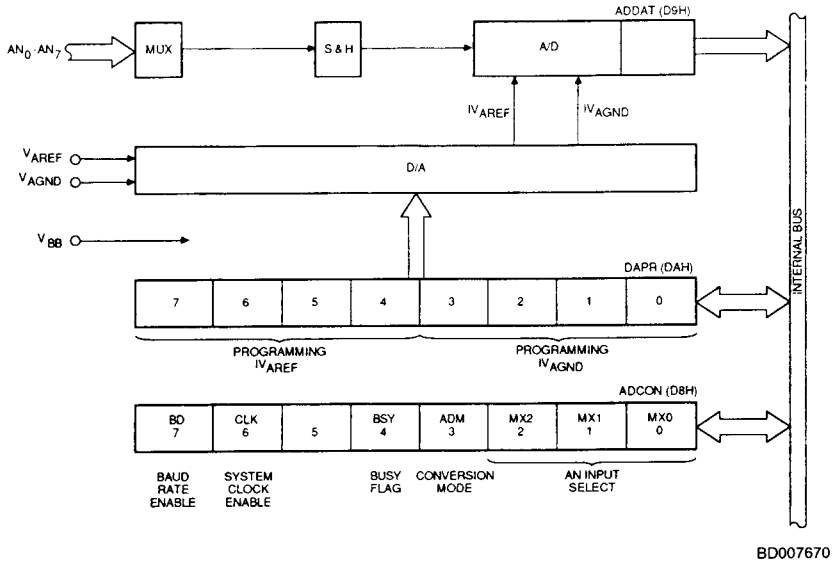


Figure 12. A/D Converter Block Diagram

Special function register ADCON, which is illustrated in Figure 13, is used to select one of the eight analog input channels to be converted, to specify a single or continuous conversion, and to check the status bit BSY, which signals whether a conversion is in progress or not.

BD	CLK	-	BSY	ADM	MX2	MX1	MX0	BIT
0DFH	0DEH	0DDH	0DCH	0DBH	0DAH	0D9H	0D8H	ADDRESS

SYMBOL	POSITION	FUNCTION
MX0 MX1 MX2	ADCON.0 ADCON.1 ADCON.2	Analog Input Channel Selection (see Table 4).
ADM	ADCON.3	A/D Conversion Mode. When set, a continuous is selected. If ADM = 0, the converter stops after one conversion.
BSY	ADCON.4	Busy Flag. This flag indicates whether a conversion is in progress (BSY = 1) or not (BSY = 1).
-	ADCON.5	Reserved (must be 0).
CLK	ADCON.6	System Clock Enable. When set, a clock signal with 1/12 the oscillator frequency is gated to pin P1.6/CLKOUT. CLK = 0 disables the clock output.
BD	ADCON.7	Baud Rate Enable. When set, the baud rate in mode 1 and 3 of the serial port is taken from the internal baud rate generator.

Figure 13. A/D Converter Control Register ADCON (0D8H)

TABLE 4. SELECTION OF THE ANALOG INPUT CHANNELS

MX2	MX1	MX0	Selected Channel	Pin
0	0	0	Analog Input 0	AN0
0	0	1	Analog Input 1	AN1
0	1	0	Analog Input 2	AN2
0	1	1	Analog Input 3	AN3
1	0	0	Analog Input 4	AN4
1	0	1	Analog Input 5	AN5
1	1	0	Analog Input 6	AN6
1	1	1	Analog Input 7	AN7

The special function register ADDAT holds the converted digital 8-bit data result. The data remains in ADDAT until it is overwritten by the next converted data. The new converted value will appear in ADDAT in the 15th machine cycle after a conversion has been started. ADDAT can be read and written to under software control. If the A/D converter of the 80515 is not used, register ADDAT can be used as an additional general-purpose register.

The SFR DAPR is provided for programming the internal reference voltages IV_{AREF} and IV_{AGND}. For this purpose the internal reference voltages can be programmed in steps of 1/16 with respect to the external reference voltages ($V_{AREF} - V_{AGND}$) by 4 bits each in register DAPR. Bits 0 to 3 specify IV_{AGND}, while bits 4 to 7 specify IV_{AREF}. A minimum of 1 V difference is required between the internal reference voltages for proper operation of the A/D converter. That means the internal reference voltage IV_{AREF} must always be programmed four steps higher than IV_{AGND} (in respect to the external reference voltage V_{AREF} which is specified as +5 V ±5%). The values of IV_{AGND} and IV_{AREF} are given by the formula:

$$IV_{AGND} = V_{AGND} + \frac{DAPR(0-3)}{16} (V_{AREF} - V_{AGND})$$

with DAPR(0 — 3) ≠ 0 and DAPR(0 — 3) < 13;

$$IV_{AREF} = V_{AGND} + \frac{DAPR(4-7)}{16} (V_{AREF} - V_{AGND})$$

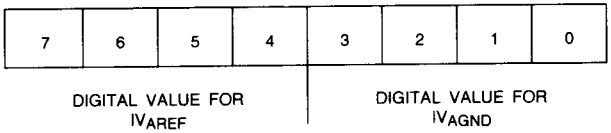
with DAPR(4 — 7) > 3;

where DAPR(0 - 3) is the contents of the low-order nibble, and DAPR(4 - 7) the contents of the high-order nibble of DAPR, taken as an unsigned decimal integer.

If DAPR(0 - 3) or DAPR(4 - 7) = 0, the internal reference voltages correspond to the external reference voltages V_{AGND} and V_{AREF}, respectively.

If $V_{AINPUT} > IV_{AREF}$, the conversion result is 0FFH; if $V_{AINPUT} < IV_{AGND}$, the conversion result is 00H (V_{AINPUT} is the analog input voltage).

Figure 14. shows special function register DAPR.



If the external reference voltages $V_{AGND} = 0$ and $V_{AREF} = +5$ V are applied, then the internal reference voltages IV_{AGND} and IV_{AREF} (shown in Table 5) can be adjusted via the special function register DAPR.

Figure 14. D/A Converter Program Register DAPR (0DAH)

TABLE 5. ADJUSTABLE INTERNAL REFERENCE VOLTAGES

Step	DAPR(0 – 3) DAPR(4 – 7)	IV_{AGND} (V)	IV_{AREF} (V)
0	0000	0.0	5.0
1	0001	0.3125	—
2	0010	0.625	—
3	0011	0.9375	—
4	0100	1.25	1.25
5	0101	1.5625	1.5625
6	0110	1.875	1.875
7	0111	2.1875	2.1875
8	1000	2.5	2.5
9	1001	2.8125	2.8125
10	1010	3.125	3.125
11	1011	3.4375	3.4375
12	1100	3.75	3.75
13	1101	—	4.0625
14	1110	—	4.375
15	1111	—	4.6875

Items marked with "—" are not allowed according to the rules listed above (IV_{AREF} at least four steps higher than IV_{AGND}).

A/D Converter Timing and Conversion Time

A conversion is started by writing into special function register DAPR. A "write-to-DAPR" will start a new conversion even if a conversion is currently in progress. The conversion begins with the next machine cycle. The busy flag will be set in the same machine cycle that the "write-to-DAPR" operation occurs. If the value written to DAPR is 00H, meaning that no adjustment of the internal reference voltages is desired, the conversion needs 15 machine cycles to be completed. Thus, the conversion time is 15 μs for 12-MHz oscillator frequency. For each adjustment of the internal reference voltages the conversion takes an additional time of 7 μs. Thus, if only one reference voltage needs to be programmed, the total conversion time takes 22 machine cycles; if both reference voltages are to be programmed the conversion time lasts 29 machine cycles.

After a conversion has been started by writing into SFR DAPR, the analog voltage at the selected input channel is sampled for five machine cycles (5 μs at 12-MHz oscillator frequency), which will then be held at the sampled level for the rest of the conversion time. The external analog source must be strong enough to source the current in order to load the sample and hold capacitance, being 25 pF, within those five machine cycles.

Conversion of the sampled analog voltage takes place between the 6th and 15th machine cycle after sampling has been completed. In the 15th machine cycle the converted result is moved to ADDAT, the busy flag (BSY) is cleared, and the A/D converter interrupt request flag IADC (bit 0 in SFR interrupt control register IRCON) is set. If a continuous conversion is established, the next conversion is automatically started in the following machine cycle.

The special feature of programmable internal reference voltages allows adjusting the internal voltage range to the range of the external analog input voltage; or it may be used to increase the resolution of the converted analog input voltage by starting a second conversion with a compressed internal reference voltage range close to the previously measured analog value.

Figures 15-1 and 15-2 illustrate these applications.

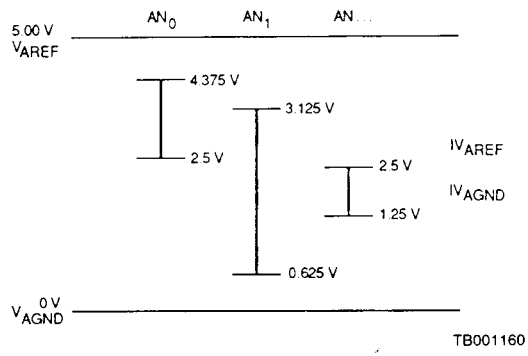


Figure 15-1. Adjusting the Internal Reference Voltages to the Range of the External Analog Voltages

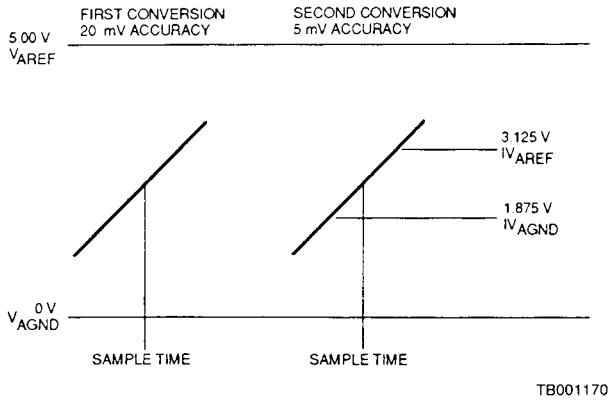


Figure 15-2. Increasing the Resolution of the A/D Result by Doi ng a Second Conversion

Interrupt Structure

The interrupt structure of the 80515 provides 12 interrupt sources and 4 priority levels. The 12 interrupt sources are organized as 6 pairs. Table 6 lists the interrupt sources and pairs of the 80515.

TABLE 6. INTERRUPT SOURCES

External Interrupt 0	— A/D Converter Interrupt
Timer 0 Interrupt	— External Interrupt 2
External Interrupt 1	— External Interrupt 3
Timer 1 Interrupt	— External Interrupt 4
Serial Port Interrupt	— External Interrupt 5
Timer 2 Interrupt	— External Interrupt 6

Some of these interrupt sources are activated by one, others are activated by two internal or external events. Each interrupt source has its own vector location in the program memory address space 00H to 6BH. In the following section the interrupt sources are discussed separately.

The external interrupts 0 and 1 ($\overline{INT_0}$ and $\overline{INT_1}$) can each be either level-activated or negative transition-activated, depending on bits IT0 and IT1 in register TCON. The flags that actually generate these interrupts are bits IE0 and IE1 in TCON. When an external interrupt is generated, the flag that generated this interrupt is cleared by the hardware when the service routine is vectored to only if the interrupt was transition-activated. If the interrupt was level-activated, then the external requesting source directly controls the request flag, rather than the on-chip hardware.

The timer 0 and timer 1 interrupts are generated by TF0 and TF1, which are set by a rollover in their respective timer/counter registers. When a timer interrupt is generated, the flag that generated it is cleared by the on-chip hardware when the service routine is vectored to.

The serial port interrupt is generated by the logical OR of RI and TI. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine will normally have to determine whether it was RI or TI that generated the interrupt, and the bit will have to be cleared in software.

The timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register IRCON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and the bit will have to be cleared in software.

The A/D converter interrupt is generated by bit IADC in register IRCON. It is set in the 15th, 22nd or 29th machine cycle, after a conversion has been started by a "write-to-DAPR," or, if continuous conversions are established, after the last conversion has been completed, depending on whether the internal reference voltages IV_{AGND} and IV_{AREF} have to be adjusted or not. When an A/D converter interrupt is generated, flag IADC will have to be cleared in software.

The external interrupt 2 ($\overline{INT_2}$) can be either positive or negative transition-activated, depending on bit I2FR in register T2CON. The flag that actually generates this interrupt is bit IEX2 in register IRCON. If an external interrupt 2 is generated, flag IEX2 is cleared by hardware when the service routine is vectored to.

Like the external interrupt 2, the external interrupt 3 can be either positive or negative transition-activated, depending on bit I3FR in register T2CON. The flag that actually generates this interrupt is bit IEX3 in register IRCON. In addition, this flag will be set if a compare event occurs at pin P1.0/$\overline{INT_3}$/CC_0 (timer 2 registers contents matches the contents of the CRC register), regardless of the compare mode established, the transition occuring at the pin, and of the external interrupt 3 being positive or negative transition-activated. Flag IEX3 is cleared by the on-chip hardware when the service routine is vectored to.

The external interrupts 4 (INT_4), 5 (INT_5), and 6 (INT_6) are positive transition-activated. The flags that actually generate these interrupts are bits IEX4, IEX5, and IEX6 in register IRCON. In addition, these flags will be set if a compare event occurs at the corresponding output pin P1.1/INT_4/CC_1, P1.2/INT_5/CC_2, and P1.3/INT_6/CC_3, regardless of the compare mode established and the transition at the respective pin. When an interrupt is generated, the flag that generated it is cleared by the on-chip hardware when the service routine is vectored to.

All of these bits that generate interrupts can be set or cleared by software, with the same result as though they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be canceled in software. The only exceptions are request flags IE0 and IE1. If the external interrupts 0 and 1 are programmed to be level-activated, IE0 and IE1 are controlled by the external source via pin $\overline{INT_0}$ and $\overline{INT_1}$, respectively. Thus, writing a one to these bits will not set the request flags IE0 and/or IE1. In this mode, external interrupts 0 and 1 can only be generated in software by writing a 0 to the corresponding pins $\overline{INT_0}$ (P3.2) and $\overline{INT_1}$ (P3.3), provided this will not affect any peripheral circuit connected to the pins. Figure 16 shows the special function register IRCON.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in the special function registers IEN0 and IEN1 (Figures 17-1 and 17-2). Note that IEN0 also contains a global disable bit, EAL, which disables all interrupts at once. Also note that in the 8051 the interrupt priority register IP is located at address 0B8H; in the 80515 this location is occupied by register IEN1.

EXF2	TF2	IEX6	IEX5	IEX4	IEX3	IEX2	IADC	BIT
0C7H	0C6H	0C5H	0C4H	0C3H	0C2H	0C1H	0C0H	ADDRESS

SYMBOL	POSITION	FUNCTION
IADC	IRCON.0	A/D Converter Interrupt Request Flag. Set by hardware at the end of a conversion. Must be cleared by software.
IEX2	IRCON.1	External Interrupt 2 Edge Flag. Set by hardware when external interrupt edge was detected. Cleared when interrupt processed.
IEX3	IRCON.2	External Interrupt 3 Edge Flag. Set by hardware when external interrupt edge was detected or when a compare event occured at pin P1.0/$\overline{INT_3}$/CC_0. Cleared when interrupt processed.
IEX4	IRCON.3	External Interrupt 4 Edge Flag. Set by hardware when external interrupt edge was detected or when a compare event occured at pin P1.1/$\overline{INT_4}$/CC_1. Cleared when interrupt processed.
IEX5	IRCON.4	External Interrupt 5 Edge Flag. Set by hardware when external interrupt edge was detected or when a compare event occured at pin P1.2/$\overline{INT_5}$/CC_2. Cleared when interrupt processed.
IEX6	IRCON.5	External Interrupt 6 Edge Flag. Set by hardware when external interrupt edge was detected or when a compare event occured at pin P1.3/$\overline{INT_6}$/CC_3. Cleared when interrupt processed.
TF2	IRCON.6	Timer 2 Overflow Flag. Set by a timer 2 overflow and must be cleared by software. If the timer 2 interrupt is enabled, TF2 = 1 will cause an interrupt.
EXF2	IRCON.7	Timer 2 External Reload Flag. Set when a reload is caused by a negative transition on pin T2EX and EXEN2 = 1. When the timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the timer 2 interrupt routine. Can be used as an additional external interrupt when the reload function is not used. EXF2 must be cleared by software.

Figure 16. Interrupt Request Control Register IRCON (0C0H)

EAL	WDT	ET2	ES	ET1	EX1	ET0	EX0	BIT
0AFH	0AEH	0ADH	0ACH	0ABH	0AAH	0A9H	0A8H	ADDRESS

SYMBOL	POSITION	FUNCTION
EX0	IEN0.0	Enables or Disables External Interrupt 0. If EX0 = 0, external interrupt 0 is disabled.
ET0	IEN0.1	Enables or Disables the Timer 0 Overflow Interrupt. If ET0=0, the timer 0 interrupt is disabled.
EX1	IEN0.2	Enables or Disables External Interrupt 1. If EX1 = 0, external interrupt 1 is disabled.
ET1	IEN0.3	Enables or Disables the Timer 1 Overflow Interrupt. If ET1=0, the timer 1 interrupt is disabled.
ES	IEN0.4	Enables or DIsables the Serial Port Interrupt. If ES = 0, the serial port interrupt is disabled.
ET2	IEN0.5	Enables or Disables Timer 2 Overflow or External Reload Interrupt. If ET2 = 0, the timer 2 interrupt is disabled.
WDT	IEN0.6	Watchdog Timer Reset Flag. Set to initiate a reset of the watchdog timer.
EAL	IEN0.7	Enables and Disables All Interrupts. If EAL = 0, no interrupt will be acknowledged. If EAL = 1, each interrupt is indidivually enabled or disabled by setting or clearing its enable bit.

Figure 17-1. Interrupt Enable Register IEN0 (0A8H)

EXEN2	SWDT	EX6	EX5	EX4	EX3	EX2	EADC	BIT
0BFH	0BEH	0BDH	0BCH	0BBH	0BAH	0B9H	0B8H	ADDRESS

SYMBOL	POSITION	FUNCTION
EADC	IEN1.0	Enables or Disables the A/D Converter Interrupt 0. If EADC = 0, the A/D converter is disabled.
EX2	IEN1.1	Enables or Disables External Interrupt 2. If EX2 = 0, external interrupt 2 is disabled.
EX3	IEN1.2	Enables or Disables External Interrupt 3/Capture/Compare Interrupt 0. If EX3 = 0, external interrupt 3 is disabled.
EX4	IEN1.3	Enables or Disables External Interrupt 4/Capture/Compare Interrupt 1. If EX4 = 0, external interrupt 4 is disabled.
EX5	IEN1.4	Enables or Disables External Interrupt 5/Capture/Compare Interrupt 2. If EX5 = 0, external 5 is disabled.
EX6	IEN1.5	Enables or Disables External Interrupt 6/Capture/Compare Interrupt 3. If EX6 = 0, external 6 is disabled.
SWDT	IEN1.6	Watchdog Timer Start/Reset Bit. Set to start/reset the watchdog timer.
EXEN2	IEN1.7	Enables or Disables the Timer 2 External Reload Interrupt. EXEN2 = 0 disables the timer 2 external reload interrupt. The external reload function is not affected by EXEN2.

Figure 17-2. Interrupt Enable Register IEN1 (0B8H)

Priority Level Structure

Each pair of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1 (Figure 18). A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another interrupt of the same or a lower priority. An interrupt of the highest priority level cannot be interrupted by another interrupt source.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced first. If requests from two interrupt sources of one interrupt pair are received simultaneously, the "left" interrupt source of each pair is serviced first. Thus within each priority level there is a second priority structure determined by the polling sequence, as follows:

High → Low		Priority
Interrupt Source Pair		
IE0	IADC	High
TF0	IEX2	
IE1	IEX3	↓
TF1	IEX4	
RI + TI	IEX5	
TF2 + EXF2	IEX6	Low

Note that the "priority within level" structure is only used to resolve simultaneous requests within the same priority level.

Figure 19 shows a block diagram of the priority level structure and Figure 20 illustrates the questing sources of the 80515's interrupt structure.

-	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0

-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0

The priority level of each pair of interrupt sources is determined by corresponding bits in IP0 and IP1 as follows:

BITS		CORRESPONDING INTERRUPT PAIR
IP1.0	IP0.0	IE0/IADC
0	0	Priority Level 0 (Lowest)
0	1	Priority Level 1
1	0	Priority Level 2
1	1	Priority Level 3 (Highest)
IP1.1	IP0.1	TF0/IEX2
IP1.2	IP0.2	IE1/IEX3
IP1.3	IP0.3	TF1/IEX4
IP1.4	IP0.4	RI+TI/IEX5
IP1.5	IP0.5	TF2+EXF2/IEX6

IP0.6 is the watchdog timer status bit WDTS. IP0.7, IP1.6, and IP1.7 are reserved.

Figure 18. Interrupt Priority Registers IP0 (0A9H) and IP1 (0B9H)

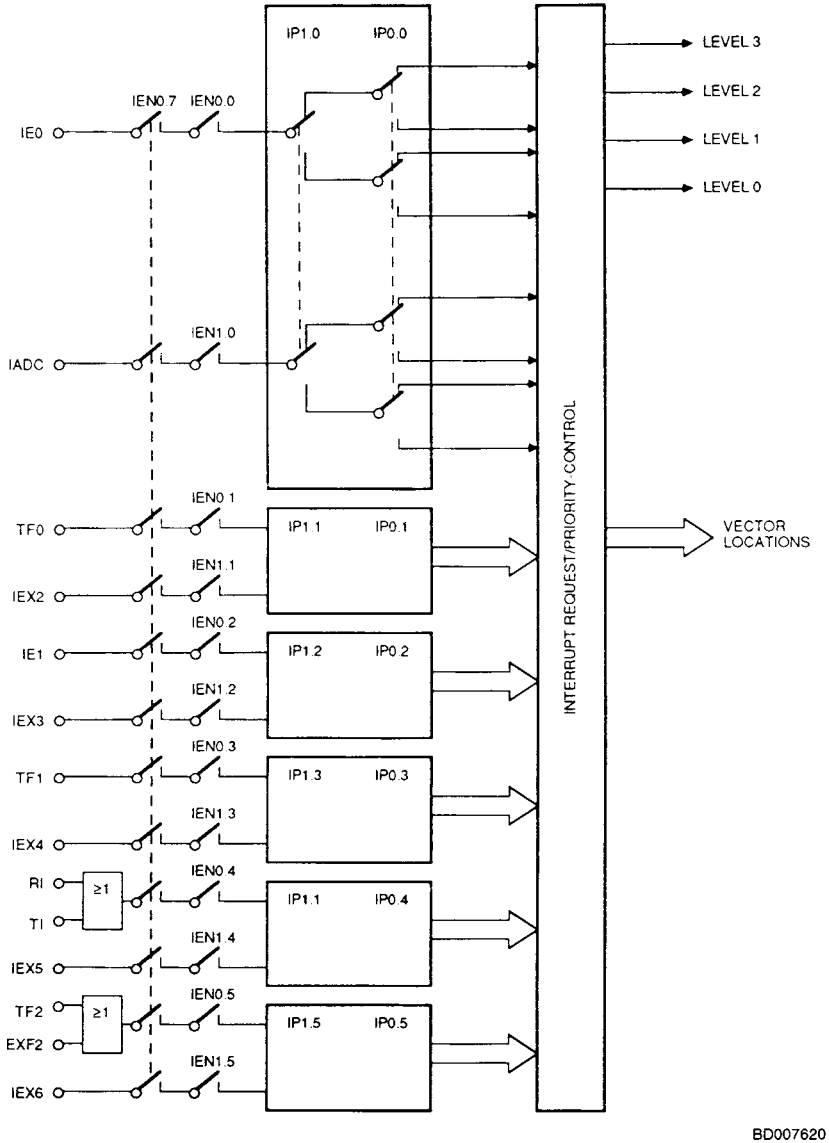


Figure 19. Priority Level Structure

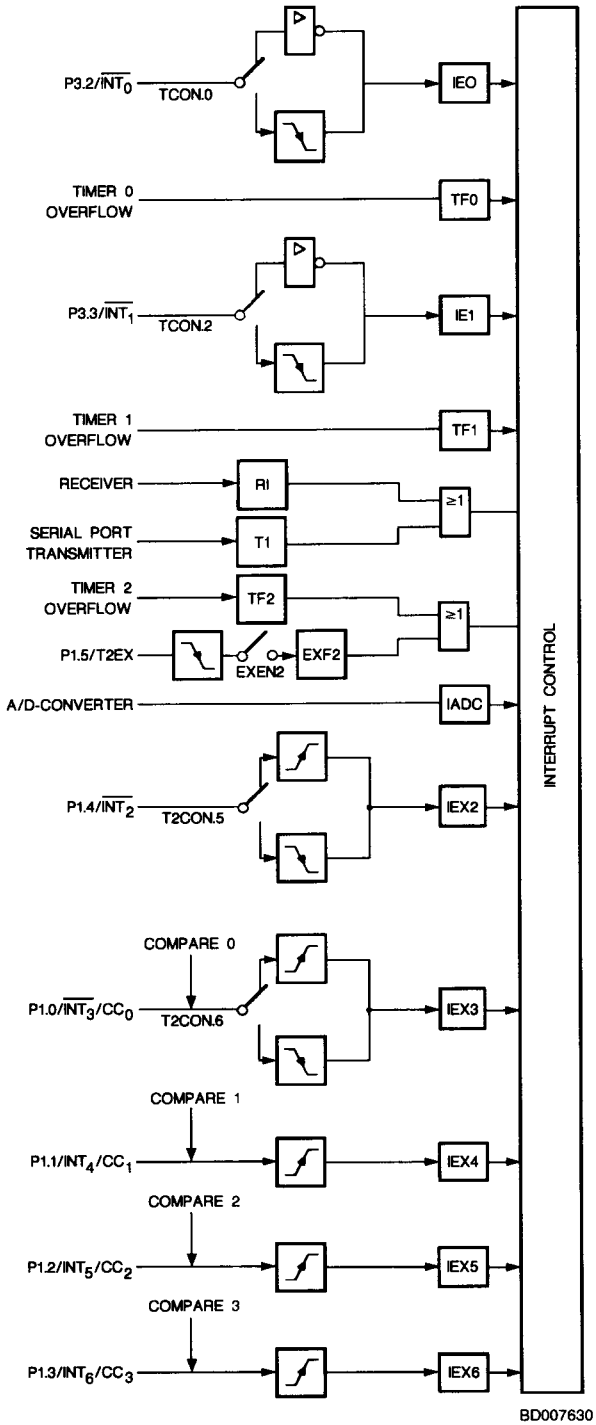


Figure 20. Interrupt Request Sources

How Interrupts Are Handled

The interrupt flags are sampled at S5P2 in every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

1) An interrupt of equal or higher priority is already in progress.
2) The current (polling) cycle is not the final cycle in the execution of the instruction in progress.
3) The instruction in progress is RETI or any access to registers IEN0, IEN1, IP0, or IP1.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring to any service routine. Condition 3 ensures that if the instruction in progress is RETI or any access to registers IEN0, IEN1, IP0, or IP1, then at least one more instruction will be executed before any interrupt is vectored to.

The polling cycle is repeated with every machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. Note then that if any interrupt flag is active but not being responded to for one of the above conditions, or if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

The polling cycle/LCALL sequence is illustrated in Figure 21.

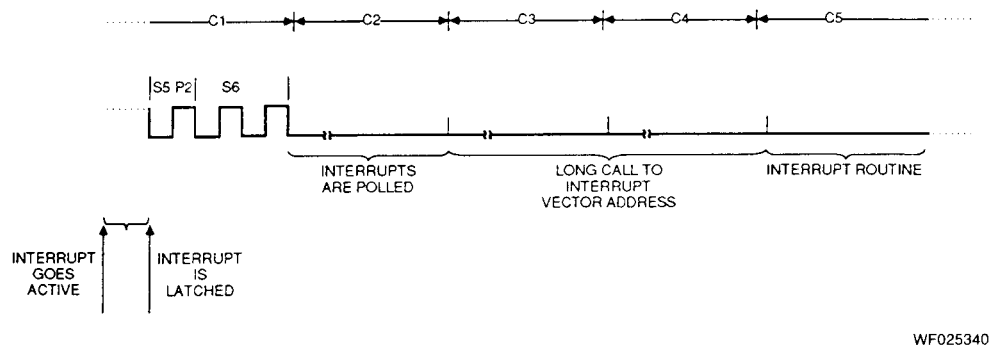


Figure 21. Interrupt Response Timing Diagram

Note that if an interrupt of higher priority level goes active prior to S5P2 in the machine cycle labled C3 in Figure 21, then in accordance with the above rules it will be vectored to during C5 and C6, without any instruction of the lower priority routine being executed.

Thus the processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate servicing routine. In some cases it also clears the flag that generated the interrupt, and in other cases it doesn't. It never clears the serial port (RI, TI), timer 2 (TF0, EXF2), or A/D converter flags. This has to be done in the user's software. It clears an external interrupt flag (IE0 or IE1) only if it was transition-activated. External interrupt flags IEX2 to IEX6 are always cleared. The hardware-generated LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to, as shown below.

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH
IADC	0043H
IEX2	004BH
IEX3	0053H
IEX4	005BH
IEX5	0063H
IEX6	006BH

Execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that this interrupt routine is no longer in progress, then pops the top 2 bytes from the stack and reloads the program counter. Execution of the interrupted program continues from where it was left off.

Note that a simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt was still in progress.

External Interrupts

The external interrupts 0 and 1 can be programmed to be level-activated or negative transition-activated by setting or clearing bit IT0 or IT1, respectively, in register TCON. If ITx = 0 (x = 0 or 1), external interrupt x is triggered by a detected LOW at the $\overline{INT_x}$ pin. If ITx = 1, external interrupt x is negative edge-triggered. In this mode, if successive samples of the $\overline{INT_x}$ pin show a HIGH in one cycle and a LOW in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx then requests the interrupt.

If the external interrupt 0 or 1 is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to de-activate the request before the interrupt service routine is completed, or else another interrupt will be generated.

The external interrupts 2 and 3 can be programmed to be negative or positive transition-activated by setting or clearing bit I2FR or I3FR in register T2CON. If IxFR = 0 (x = 2 or 3), external interrupt x is negative transition-activated. If IxFR = 1, external interrupt x is triggered by a positive transition.

The external interrupts 4, 5, and 6 are activated by a positive transition. The external timer 2 reload trigger interrupt request flag EXF2 will be activated by a negative transition at pin P1.5/T2EX, but only if bit EXEN2 is set.

Since the external interrupt pins ($\overline{INT_2}$ to $\overline{INT_6}$) are sampled once each machine cycle, an input HIGH or LOW should hold fo r at least 12 oscillator periods to ensure sampling. If the external interrupt is transition-activated, the external source has to hold the request pin LOW (HIGH for $\overline{INT_2}$ and $\overline{INT_3}$, if they are programmed to be negative transition-active) for at least one cycle, and then hold it HIGH (LOW) for at least one cycle to ensure that the transition is recognized so that the corresponding interrupt request flag will be set. The external interrupt request flags will automatically be cleared by the CPU when the service routine is called.

Response Time

If an external interrupt is recognized, its corresponding request flag is set at S5P2 in every machine cycle. The value is not actually polled by the circuitry until the next machine cycle. If the request is active and conditions are right for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction to be executed. The call itself takes two cycles. Thus, a minimum of three complete machine cycles will elapse between activation of an external interrupt request and the beginning of executing the first instruction of the service routine. Figure 21 shows interrupt response timings.

A longer response time would result if the request is blocked by one of the three previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final cycle, the additional wait time cannot be more than three cycles, since the longest instructions (MUL and DIV) are only four cycles long; and, if the instruction in progress is RETI or an access to registers IEN0, IEN1, IP0, or IP1, the additional wait time cannot be more than five cycles (a maximum of one more cycle to complete the instruction in progress, plus four cycles to complete the next instruction if the instruction is MUL or DIV).

Thus, in a single interrupt system, the response time is always more than three cycles and less than nine cycles.

RAM Backup Power Supply

The power-down mode in the 80515 allows reduction of V_{CC} to zero while saving 40 bytes of the on-chip RAM through a backup supply connected to the V_{PD} pin. In the following, the terms V_{CC} and V_{PD} are used to specify the voltages on pin V_{CC} and pin V_{PD}, respectively.

If $V_{CC} > V_{PD}$, the 40 bytes are supplied from V_{CC}. V_{PD} may then be LOW. If $V_{CC} < V_{PD}$, the current for the 40 bytes is drawn from V_{PD}. The addresses of these backup-powered RAM locations range from 88 to 127 (58H to 7FH). The current drawn from the backup power supply is typically 1 mA, Max. 3 mA.

To utilize this feature, the user's system — upon detecting that a power failure is imminent — would interrupt the processor in some manner to transfer relevant data to the 40 bytes in on-chip RAM and enable the backup power supply to the V_{PD} pin. Then a reset should be accomplished before V_{CC} falls below its operating limit. When power returns, a power-on reset should be accomplished, and the backup supply needs to stay on long enough to resume normal operation. Figure 22 illustrates the timing on a power failure.

System Clock Output

For peripheral devices requiring a system clock, the 80515 provides a clock output signal derived from the oscillator frequency as an alternate output function on pin P1.6/CLKOUT. If bit CLK is set (bit 6 of special function register ADCON), a clock signal with 1/12 the oscillator frequency is gated to pin P1.6/CLKOUT. To use this function the Port 1 pin must first be programmed to a one (1).

Figure 23 shows the timing of this system clock signal with respect to signal ALE and the internal states. The system clock is HIGH during S3P1 and S3P2 of every machine cycle and LOW during all other states. Thus, the duty cycle of the clock signal is 1:6. Also shown is the timing with respect to an external data memory access. The system clock coincides with the last state (S3) in which an $\overline{RD}$ or $\overline{WR}$ signal is active.

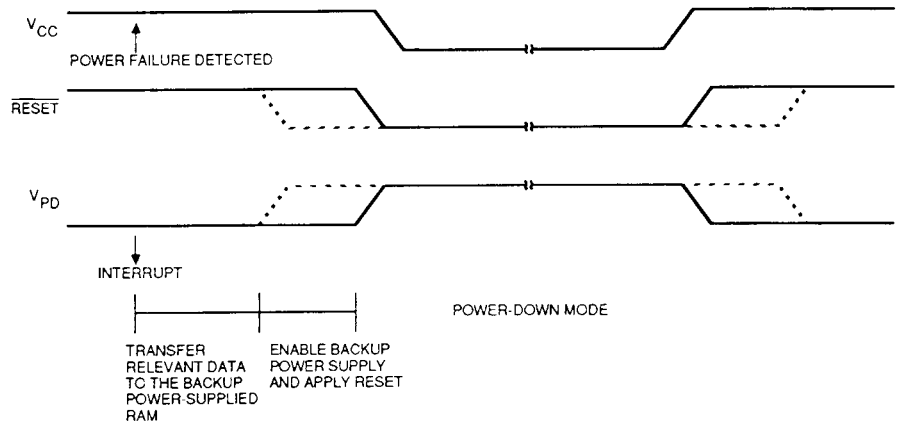


Figure 22. Reset and RAM Backup Power Timing

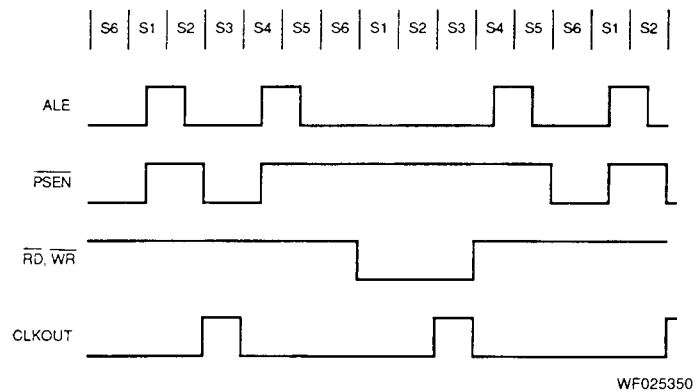


Figure 23. System Clock Timing Overview

More About the On-Chip Oscillator

The on-chip oscillator of the 80515, like the 8051, is a single-stage inverter (Figure 24), intended for use as a crystal-controlled, positive-reactance oscillator (Figure 25). In this application the crystal is operated in its fundamental response mode as an inductive reactance in parallel resonance with a capacitance external to the crystal. The crystal specifications and capacitance values (C_1 and C_2 in Figure 25) are not critical. 30 pF can be used in these positions at any frequency with good quality crystals. A ceramic resonator can be used in place of the crystal in cost-critical applications. When a ceramic resonator is used, C_1 and C_2 are normally selected to be of somewhat higher values, typically 47 pF. The manufacturer of the ceramic resonator should be consulted for recommendations on the values of these capacitors.

To drive the 80515 with an external clock source, apply the external clock signal to $XTAL_2$ and ground $XTAL_1$, as shown in Figure 26. A pullup resistor is suggested because the logic levels at $XTAL_2$ are not TTL.

Sometimes an external clock with the frequency of the oscillator is needed. For this application the circuit shown in Figure 27 is recommended. The CMOS driver (or inverter) should be placed as close as possible to the oscillator circuit. Be sure to take into account the impedances of the circuit and the CMOS driver input.

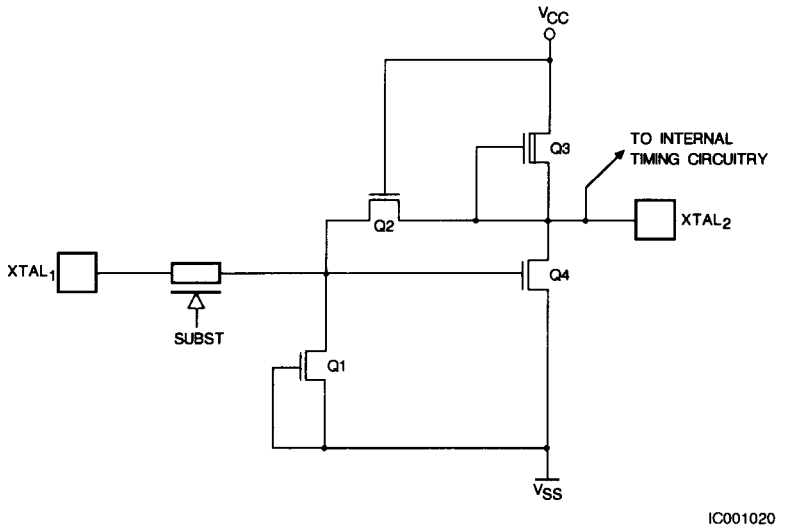


Figure 24. On-Chip Oscillator Circuitry

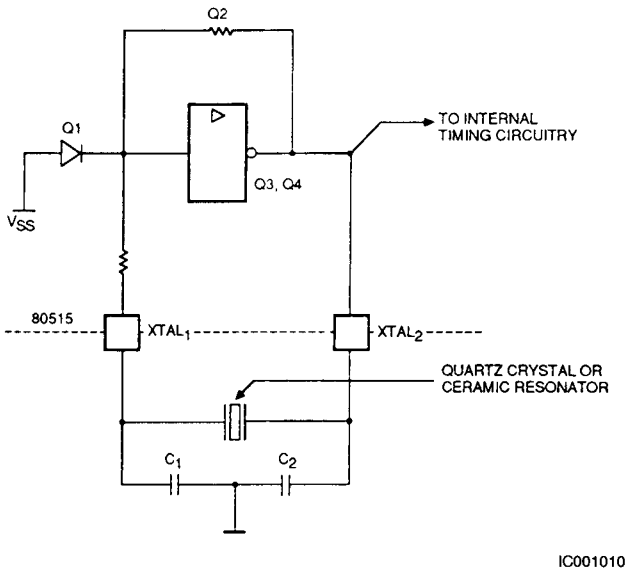


Figure 25. Using the On-Chip Oscillator

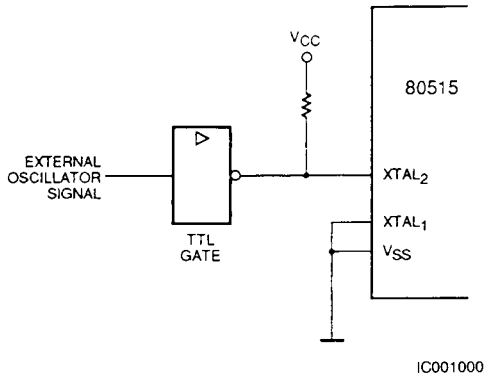


Figure 26. Driving with an External Clock Source

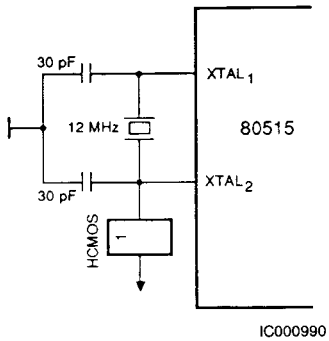


Figure 27. Generating a System Clock from the Oscillator Circuit

Register PCON

The special function register PCON is located at address 87H. In this register only bit 7, which is SMOD, is implemented. The other bit positions (PCON.0 to PCON.6) are reserved and should not be used. SMOD is used to double the baud rate for the serial port. If SMOD is set to one, the baud rate is doubled when the serial port is operating in either mode 1, 2, or 3. The reset value of SMOD is 0. Note that PCON is not bit-addressable, therefore byte instructions must be used to alter SMOD.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin
with Respect to Ground(V_{SS}) ..... −0.5 to +7.0 V
Power Dissipation ..... 2 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... 5.0 V ± 10%
Ground (V_{SS}) ..... 0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

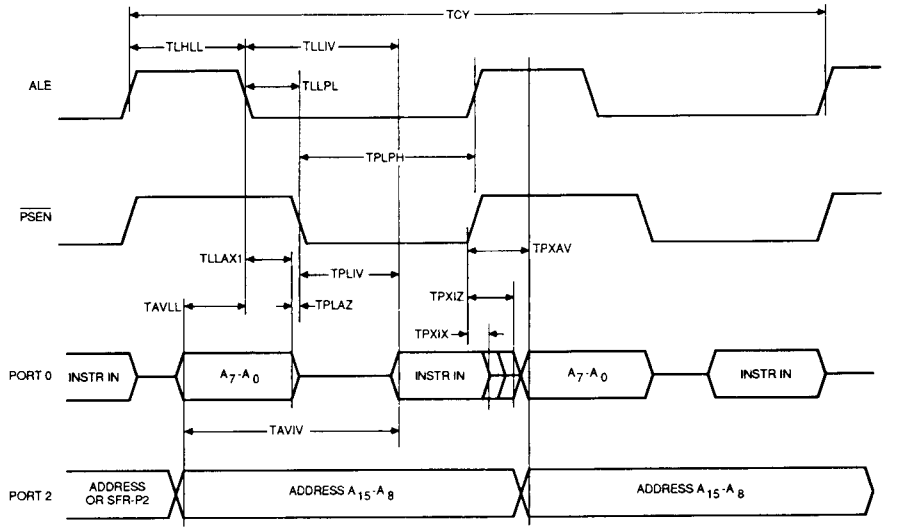
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		−0.5	0.8	V
V_{IH}	Input HIGH Voltage (Except $\overline{RESET}$ and $XTAL_2$)		2.0	V_{CC} +0.5	V
V_{IH1}	Input HIGH Voltage to $XTAL_2$)	$XTAL_1$ to V_{SS}	2.5	V_{CC} +0.5	V
V_{IH2}	Input HIGH Voltage to $\overline{RESET}$		3.0		V
V_{PD}	Power-Down Voltage	V_{CC} = 0 V	3	5.5	V
V_{OL}	Output LOW Voltage, Ports 1, 2, 3, 4, 5	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output LOW Voltage, Port 0, ALE, $\overline{PSEN}$	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output HIGH Voltage, Ports 1, 2, 3, 4, 5	I_{OH} = −80 μA	2.4		V
V_{OH1}	Output HIGH Voltage, Port 0, ALE, $\overline{PSEN}$	I_{OH} = −400 μA	2.4		V
I_{IL}	Logic 0 Input Current, Ports 1, 2, 3, 4, 5	V_{IL} = 0.45 V		−800	μA
I_{IL2}	Logic 0 Input Current, $XTAL_2$	$XTAL_1 = V_{SS}$ V_{IL} = 0.45 V		−2.5	mA
I_{IL3}	Input LOW Current to $\overline{RESET}$ for Reset	V_{IL} = 0.45 V		−500	μA
I_{L1}	Input Leakage Current to Port 0, $\overline{EA}$	$0V < V_{IN} < V_{CC}$		±10	μA
I_{CC}	Power Supply Current 80515/80535	All Outputs Disconnected		210	mA
I_{PD}	Power-Down Current	V_{CC} = 0 V		3	mA
C_{IO}	Capacitance of I/O Buffer	f_c = 1 MHz		10	pF

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (C_L for Port 0, ALE, and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Parameter Symbol	Parameter Description	12 MHz Clock		Variable Clock		Unit
		Min.	Max.	Min.	Max.	
1/TCLCL	Cycle Time			1.2	12	MHz
TLHLL	ALE Pulse Width	127		2TCLCL-40		ns
TAVLL	Address Setup to ALE	53		TCLCL-30		ns
TLLAX1	Address Hold After ALE	48		TCLCL-35		ns
TLLIV	ALE to Valid Instruction In		233		4TCLCL-100	ns
TLLPL	ALE to $\overline{PSEN}$	58		TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		3TCLCL-35		ns
TPLIV	$\overline{PSEN}$ to Valid Instruction In		150		3TCLCL-100	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ*	Input Instruction Float After $\overline{PSEN}$		63		TCLCL-20	ns
TPXAV*	Address Valid After $\overline{PSEN}$	75		TCLCL-8		ns
TAVIV	Address to Valid Instruction In		302		5TCLCL-115	ns
TPLAZ	Address Float to $\overline{PSEN}$		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL-100		ns
TLLAX2	Address Hold After ALE	132		2TCLCL-35		ns
TRLDV	$\overline{RD}$ to Valid Data In		252		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL-70	ns
TLLDV	ALE to Valid Data In		517		8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		9TCLCL-165	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	3TCLCL-50	3TCLCL + 50	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	203		4TCLCL-130		ns
TWHLH	$\overline{WR}$ or $\overline{RD}$ HIGH to ALE HIGH	43	123	TCLCL-40	TCLCL + 40	ns
TQVWX	Data Valid to $\overline{WR}$ Transition	33		TCLCL-50		ns
TQVWH	Data Setup Before $\overline{WR}$	433		7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	33		TCLCL-50		ns
TRLAZ	Address Float After $\overline{RD}$		20		20	ns

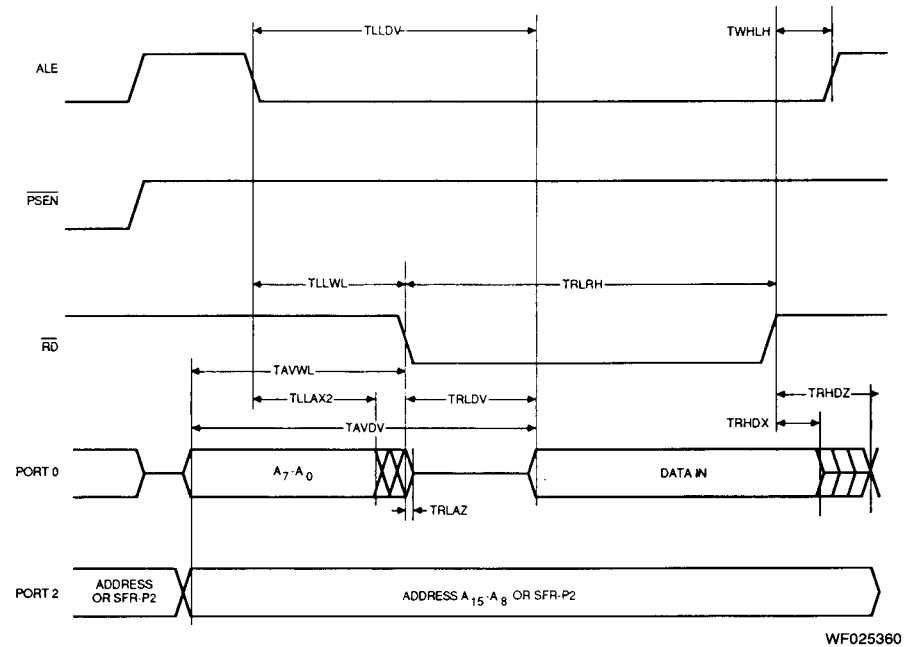
* Interfacing the 80515 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

SWITCHING WAVEFORMS



WF025420

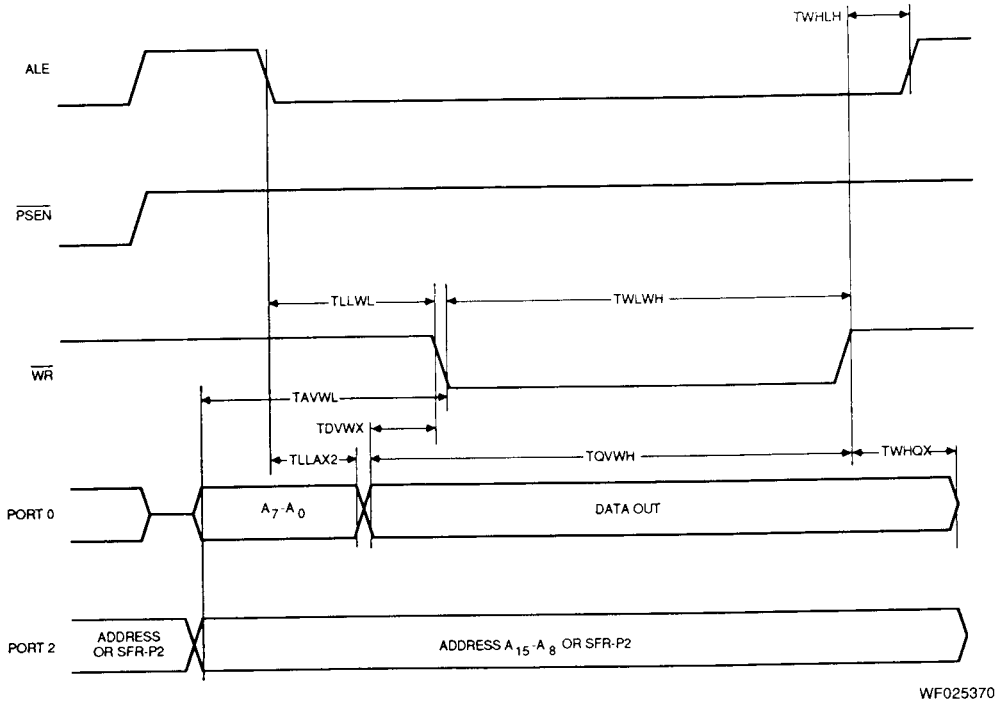
Program Memory Read Cycle



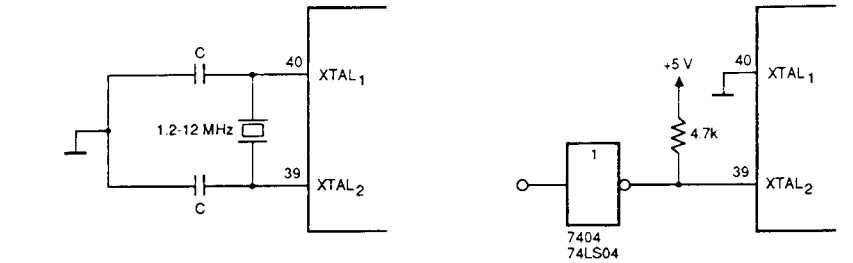
WF025360

Data Memory Read Cycle

SWITCHING WAVEFORMS (Cont'd.)



Data Memory Write Cycle



C = 30 pF ±10 pF

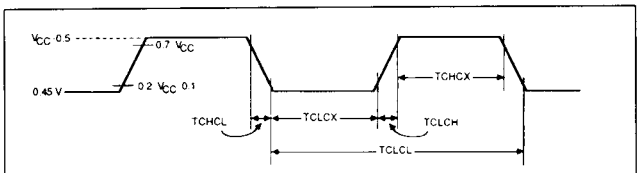
Crystal Oscillator Mode

Driving from External Source

Recommended Oscillator Circuits

EXTERNAL CLOCK DRIVE

Parameter Symbol	Parameter Description	Min.	Max.	Unit
1/TCLCL	Oscillator Frequency	1.2	12	MHz
TCHCX	HIGH Time	20		ns
TCLCX	LOW Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns



WF025390

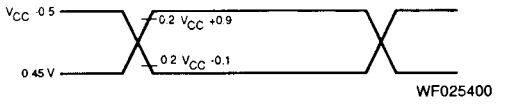
External Clock Drive Waveform

SERIAL PORT TIMING — SHIFT REGISTER MODE

(Load Capacitance = 80 pF)

Parameter Symbol	Parameter Description	12 MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL – 133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL – 117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL – 133	ns

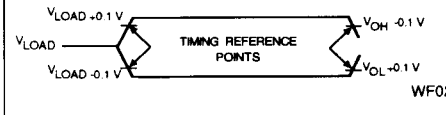
AC Testing



WF025400

AC INPUTS DURING TESTING ARE DRIVEN AT V_{CC} – 0.5 FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT V_{IH} MIN. FOR A LOGIC "1" AND V_{IL} MAX. FOR A LOGIC "0."

Input/Output Waveform



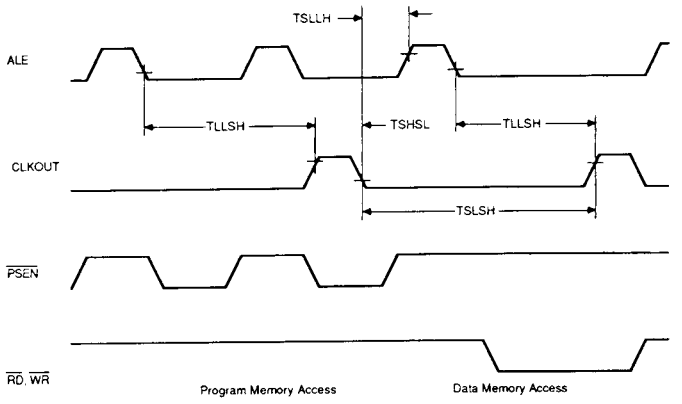
WF025410

FOR TIMING PURPOSES, A PORT PIN IS NO LONGER FLOATING WHEN A 100 mV CHANGE FROM LOAD OCCURS. IT BEGINS TO FLOAT WHEN A 100 mV CHANGE FROM THE LOADED V_{OH}/V_{OL} LEVEL OCCURS. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Float Waveform

SYSTEM CLOCK TIMING

Parameter Symbol	Parameter Description	12 MHz clock		Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		Unit
		Min.	Max.	Min.	Max.	
TLLSH	ALE to CLKOUT	543		7TCLCL-40		ns
TSHSL	CLKOUT HIGH Time	127		2TCLCL-40		ns
TSLSH	CLKOUT LOW Time	793		10TCLCL-40		ns
TSLLH	CLKOUT LOW to ALE HIGH	43	123	TCLCL-40	TCLCL + 40	ns



System Clock Timing

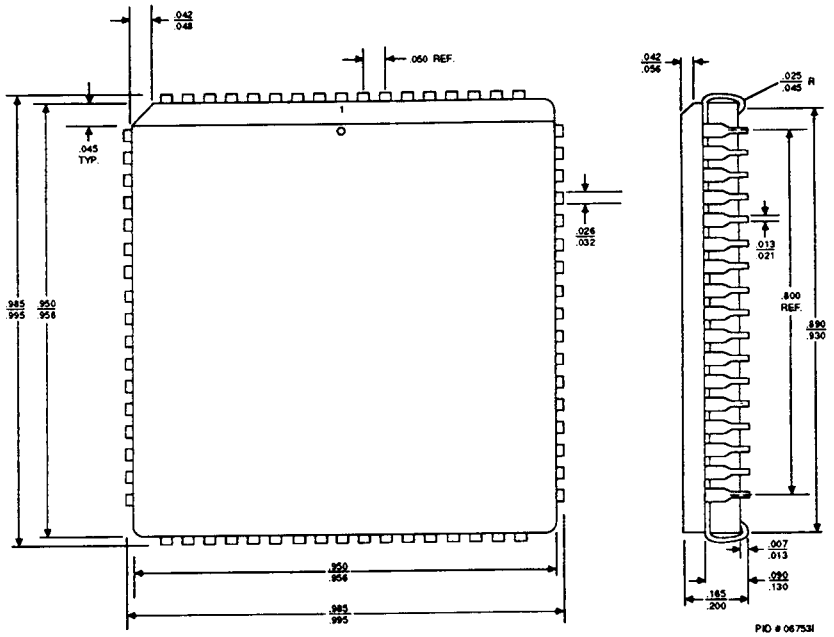
A/D Converter Characteristics (V_{CC} = 5 V ±10%; V_{SS} = 0 V; V_{AREF} = V_{CC} ±5%; V_{AGND} = V_{SS} ±0.2 V; T_A = 0 to +70°C)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{AINPUT}	Analog Input Voltage		V_{AGND}-0.2	V_{AREF}+0.2	V
C_I	Analog Input Capacitance	(See Note 3)			pF
T_S	Sample Time			5 TCY	μs
T_C	Conversion Time (Including Sample Time)	for $IV_{AREF} = V_{AREF}$ and $IV_{AGND} = V_{AGND}$		15 TCY	μs
		for $IV_{AREF} \neq V_{AREF}$ and $IV_{AGND} = V_{AGND}$ or for $IV_{AREF} = V_{AREF}$ and $IV_{AGND} \neq V_{AGND}$		22 TCY	μs
		for $IV_{AREF} \neq V_{AREF}$ and $IV_{AGND} \neq V_{AGND}$		29 TCY	μs
	Differential Non-Linearity	$IV_{AREF} = V_{AREF} = V_{CC}$ $IV_{AGND} = V_{AGND} = V_{SS}$ R_i of Analog Input Source ≤ 10 kΩ		±1	LSB
	Integral Non-Linearity			±1	LSB
	Offset Error			±1	LSB
	Gain Error			±1	LSB
I_{REF}	V_{AREF} Supply Current			5	mA

Notes: 1. The internal resistance of the analog source must be less than 10 kΩ to assure full loading of the sample capacitance during sample time.
2. The internal resistance of the analog reference voltage source must be less than 1 kΩ.
3. Typical values are 25 pF.

PHYSICAL DIMENSIONS*

PL 068



*For reference only.

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