FAIRCHILD SEMICONDUCTOR TM

February 1997

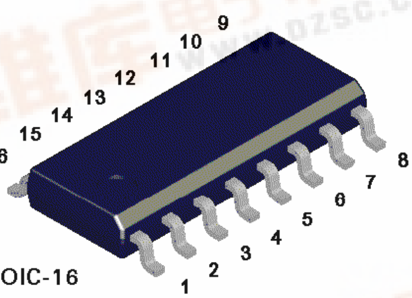
NDM3001
3 Phase Brushless Motor Driver

General Description

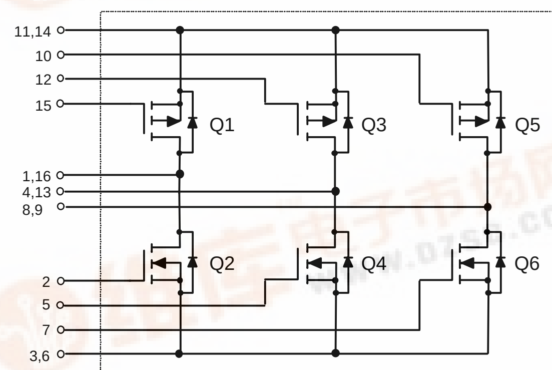
The NDM3001 three phase brushless motor driver consists of three N-Channel and P-Channel MOSFETs in a half bridge configuration. These devices are produced using Fairchild's proprietary, high cell density DMOS technology. This very high density process is tailored to minimize on-state resistance which reduces power loss, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage 3 phase motor driver such as disk drive spindle motor control and other half bridge applications.

Features

- ±2.9 A, ±30 V, 2.5W
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Industry standard SOIC-16 surface mount package.



SOIC-16



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDM3001	Units
V_{DSS}	Drain-Source Voltage (All Types)		±30	V
V_{GSS}	Gate-Source Voltage (All Types)		±20	V
I_D	Drain Current Q1+Q4 or Q1+Q6 or Q3+Q2 - Continuous Q3+Q6 or Q5+Q2 or Q5+Q4		±2.9	A
	- Pulsed	(Note 1a & 2)	±10	
P_D	Total Power Dissipation	(Note 1a)	2.5	W
	Q1+Q4 or Q1+Q6 or Q3+Q2 or Q3+Q6 or Q5+Q2 or Q5+Q4	(Note 1b)	1.6	
		(Note 1c)	1.4	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C

THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient Q1+Q4 or Q1+Q6 or Q3+Q2 or Q3+Q6 or Q5+Q2 or Q5+Q4 (Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case Q1+Q4 or Q1+Q6 or Q3+Q2 or Q3+Q6 or Q5+Q2 or Q5+Q4 (Note 1)	20	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Type	Min	Typ	Max	Units
OFF CHARACTERISTICS								
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = ± 250 µA		All	±30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = ±24 V, V_{GS} = 0 V		All			±1	µA
			T_J=55°C				±10	µA
I_{GSS}	Gate - Body Leakage, Forward	V_{GS} = ±20 V, V_{DS} = 0 V		All			±100	nA
ON CHARACTERISTICS (Note 3)								
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA		Q1, Q3, Q5	- 1	-1.6	-2	V
			T_J=125°C		- 0.75	-1.3	-1.5	
		V_{DS} = V_{GS}, I_D = 250 µA		Q2, Q4, Q6	1	1.5	2	
			T_J=125°C		0.75	1.2	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -2.9 A		Q1, Q3, Q5		0.19	0.24	Ω
			T_J=125°C			0.27	0.45	
		V_{GS} = -4.5 V, I_D = -2.2 A				0.3	0.36	
		V_{GS} = 10 V, I_D = 2.9 A		Q2, Q4, Q6		0.09	0.115	
			T_J=125°C			0.126	0.221	
		V_{GS} = 4.5 V, I_D = 2.2 A				0.13	0.16	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = -5 V		Q1, Q3, Q5	-10			A
		V_{GS} = 10 V, V_{DS} = 5 V		Q2, Q4, Q6	10			
DYNAMIC CHARACTERISTICS								
C_{iss}	Input Capacitance	Q1, Q3, Q5 V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		Q1, Q3, Q5		260		pF
				Q2, Q4, Q6		185		
C_{oss}	Output Capacitance			Q1, Q3, Q5		140		pF
		Q2, Q4, Q6	V_{DS} =	Q2, Q4, Q6		115		
C_{rss}	Reverse Transfer Capacitance	15 V, V_{GS} = 0 V, f = 1.0 MHz		Q1, Q3, Q5		50		pF
				Q2, Q4, Q6		40		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 3)							
$t_{D(on)}$	Turn - On Delay Time	Q1, Q3, Q5 V_{DD} = -15 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	Q1, Q3, Q5		10	40	ns
			Q2, Q4, Q6		9	40	
t_r	Turn - On Rise Time		Q1, Q3, Q5		13	40	ns
			Q2, Q4, Q6		21	40	
$t_{D(off)}$	Turn - Off Delay Time	Q2, Q4, Q6 V_{DD} = 15 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	Q1, Q3, Q5		21	90	ns
			Q2, Q4, Q6		21	90	
t_f	Turn - Off Fall Time		Q1, Q3, Q5		5	50	ns
			Q2, Q4, Q6		8	50	
Q_g	Total Gate Charge	Q1, Q3, Q5 V_{DS} = -10 V, I_D = -3.0 A, V_{GS} = -10 V	Q1, Q3, Q5		10	25	nC
			Q2, Q4, Q6		9.5	25	
Q_{gs}	Gate-Source Charge		Q1, Q3, Q5		1.6		nC
		Q2, Q4, Q6 V_{DS} = 10 V, I_D = 3.0 A, V_{GS} = 10 V	Q2, Q4, Q6		1.5		
Q_{gd}	Gate-Drain Charge		Q1, Q3, Q5		3		nC
			Q2, Q4, Q6		2.5		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1, Q3, Q5			-1.2	A
			Q2, Q4, Q6			1.2	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -3.0 A (Note 3)	Q1, Q3, Q5		-0.8	-1.3	V
		V_{GS} = 0 V, I_S = 3.0 A (Note 3)	Q2, Q4, Q6		0.8	1.3	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = ±3.0 A, dI_F/dt = 100 A/µs	All			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

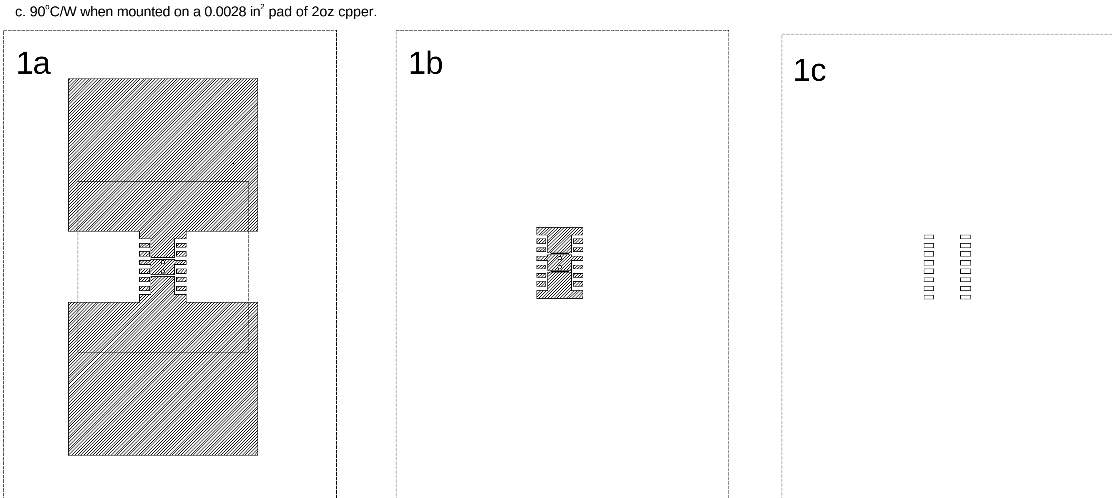
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)} @ T_J$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in^2 pad of 2oz cpper.

b. 80°C/W when mounted on a 0.027 in^2 pad of 2oz cpper.

c. 90°C/W when mounted on a 0.0028 in^2 pad of 2oz cpper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

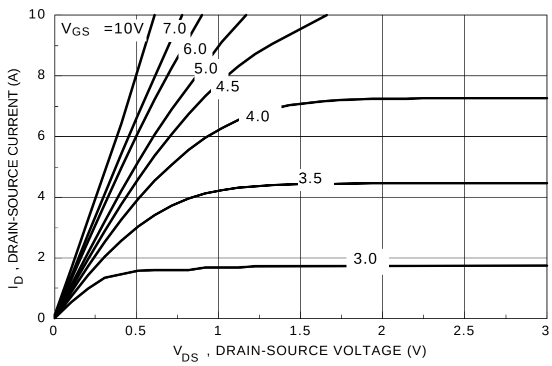


Figure 1. N-Channel On-Region Characteristic.

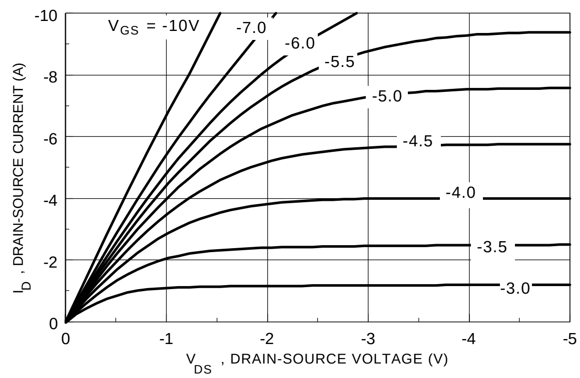


Figure 2. P-Channel On-Region Characteristics.

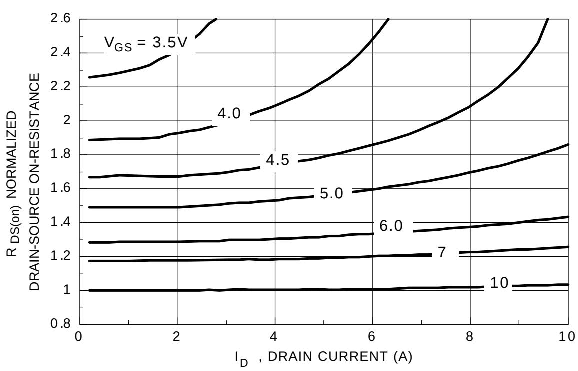


Figure 3. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

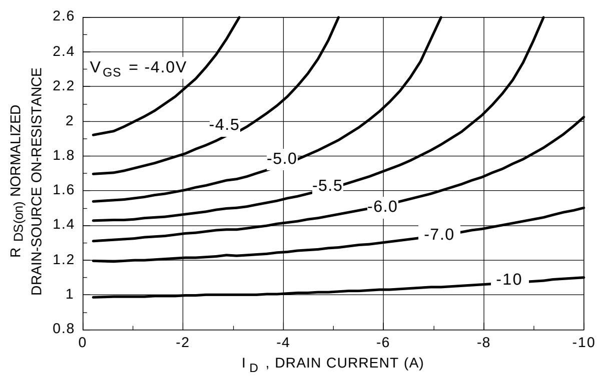


Figure 4. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

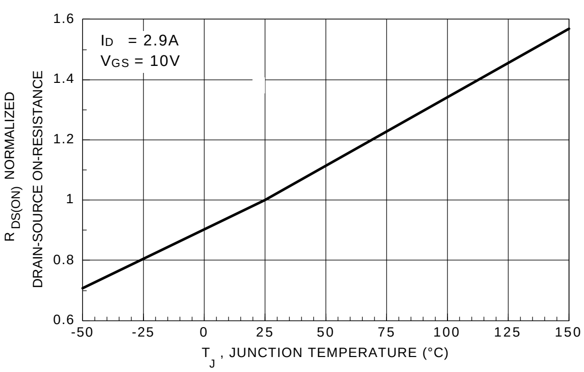


Figure 5. N-Channel On-Resistance Variation with Temperature.

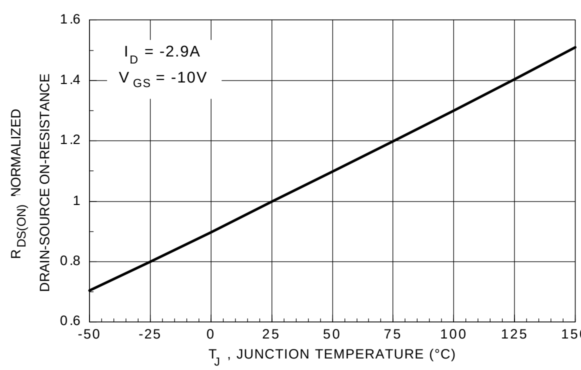


Figure 6. P-Channel On-Resistance Variation with Temperature.

Typical Electrical Characteristics

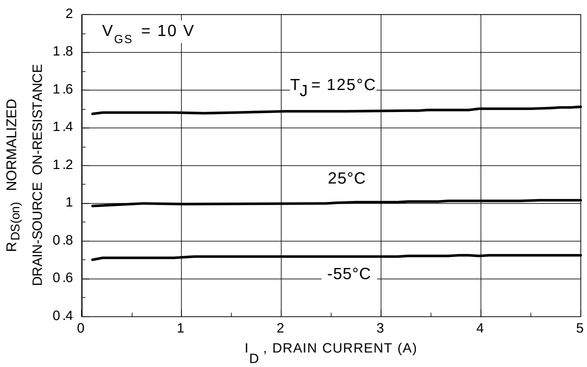


Figure 7. N-Channel On-Resistance Variation with Drain Current and Temperature.

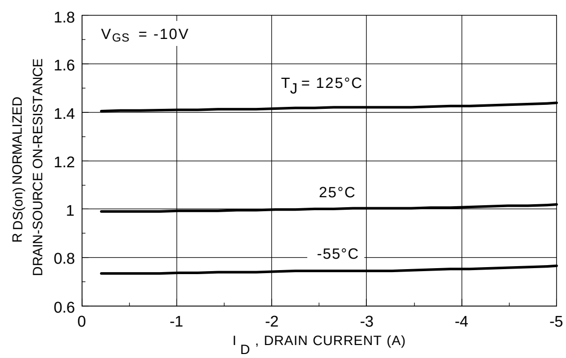


Figure 8. P-Channel On-Resistance Variation with Drain Current and Temperature.

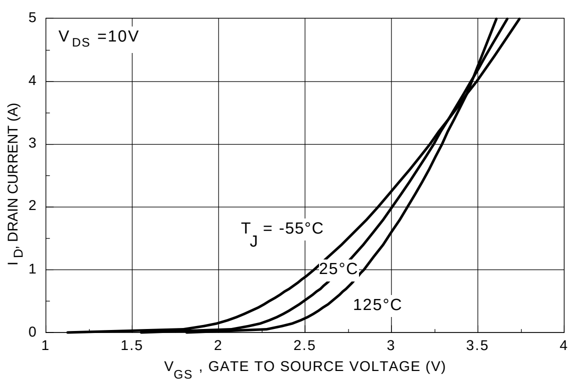


Figure 9. N-Channel Transfer Characteristics.

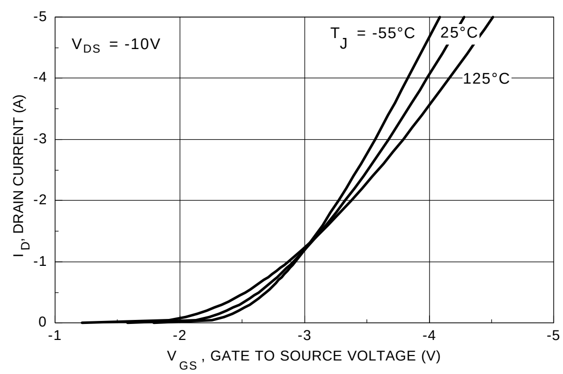


Figure 10. P-Channel Transfer Characteristics.

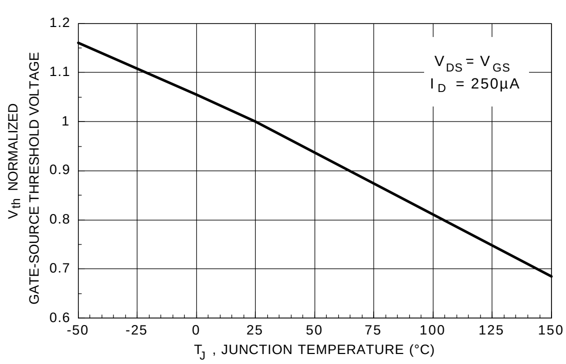


Figure 11. N-Channel Gate Threshold Variation with Temperature.

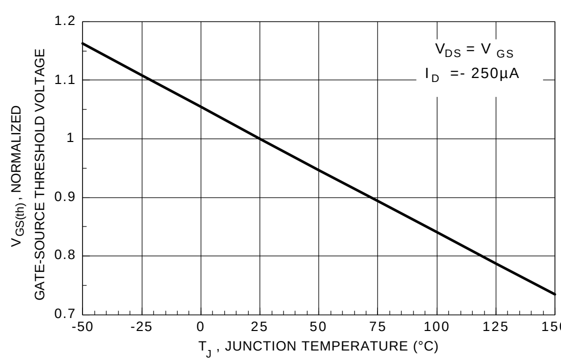


Figure 12. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

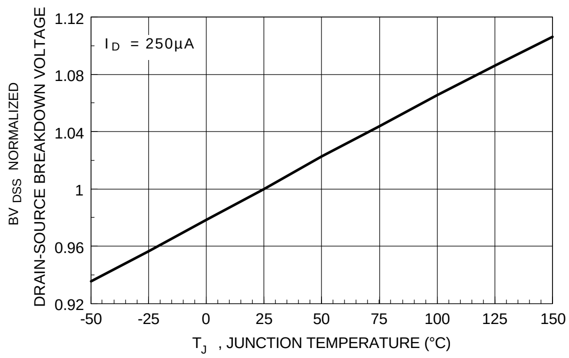


Figure 13. N-Channel Breakdown Voltage Variation with Temperature.

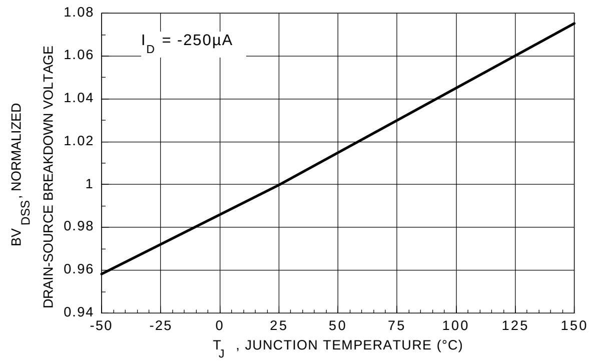


Figure 14. P-Channel Breakdown Voltage Variation with Temperature.

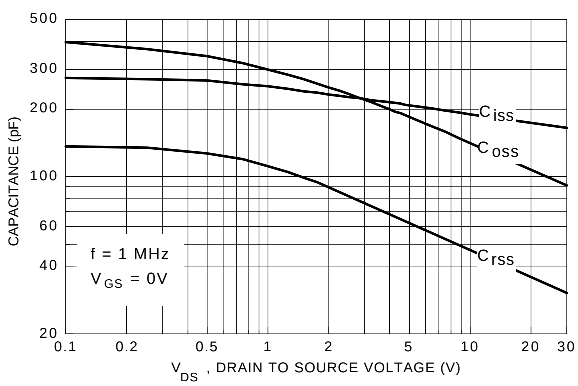


Figure 15. N-Channel Capacitance Characteristics.

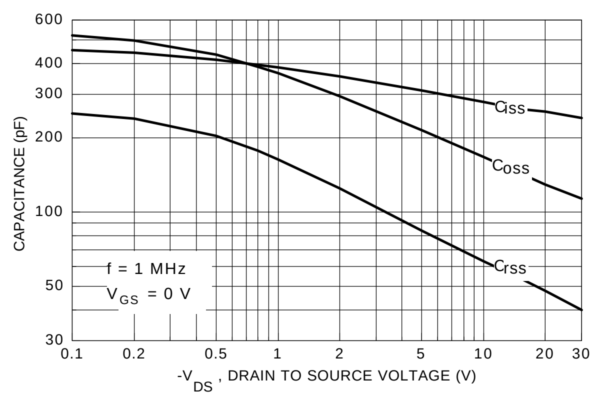


Figure 16. P-Channel Capacitance Characteristics.

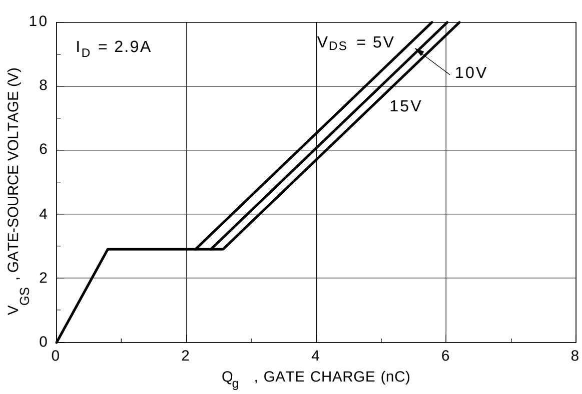


Figure 17. N-Channel Gate Charge Characteristics.

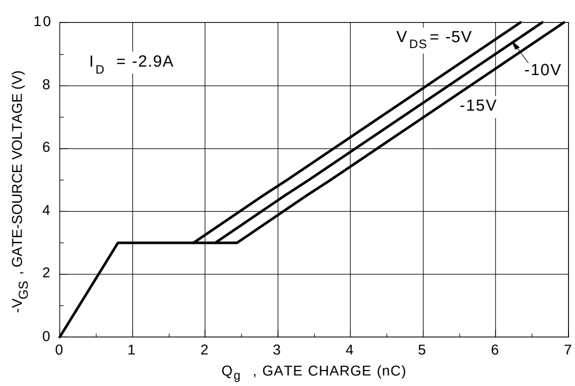


Figure 18. P-Channel Gate Charge Characteristics.

Typical Electrical Characteristics

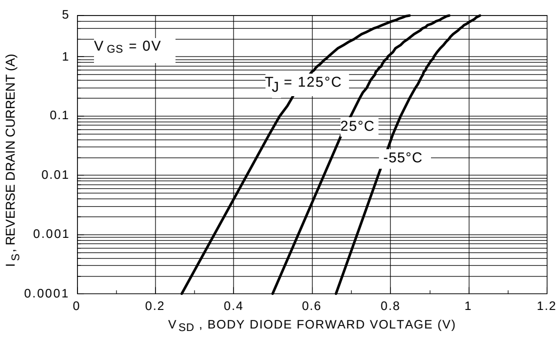


Figure19. N-Channel Body Diode Forward Voltage Variation with Source Current and Temperature.

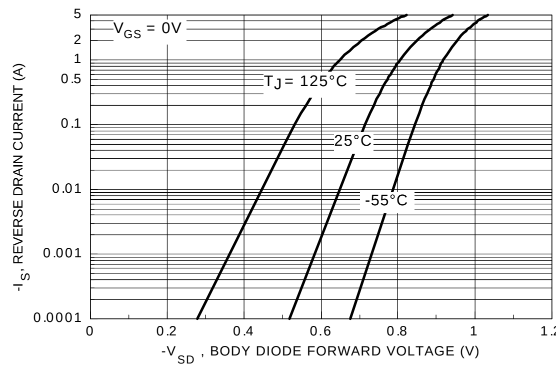


Figure 20. P-Channel Body Diode Forward Voltage Variation with Source Current and Temperature.

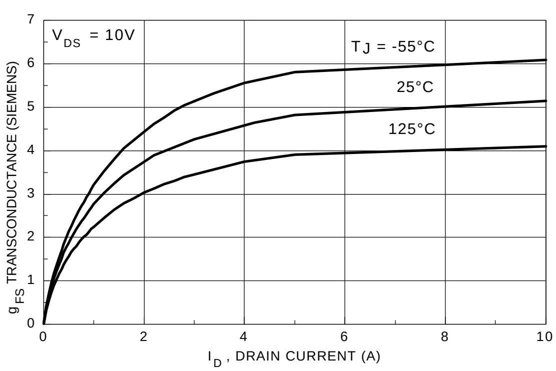


Figure 21. N-Channel Transconductance Variation with Drain Current and Temperature.

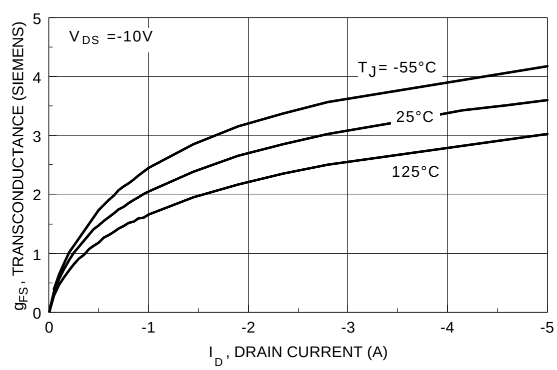


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

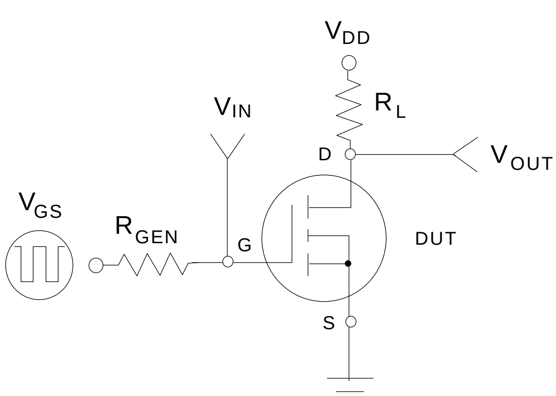


Figure 23. N or P-Channel Switching Test Circuit.

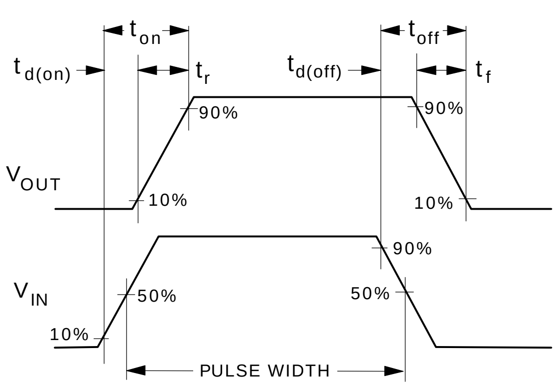


Figure 24. N or P-Channel Switching Waveforms.

Typical Thermal and Electrical Characteristics

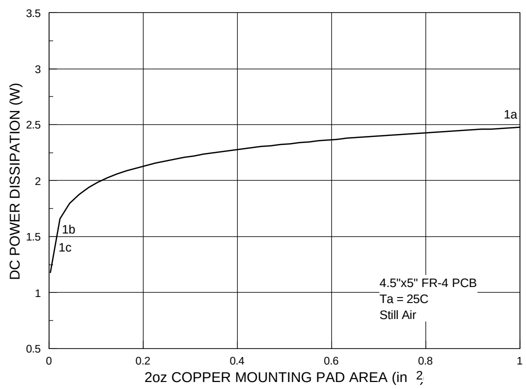


Figure 25. SOIC-16 3 Leadframe Device DC Power Dissipation versus Copper Mounting Pad Area.

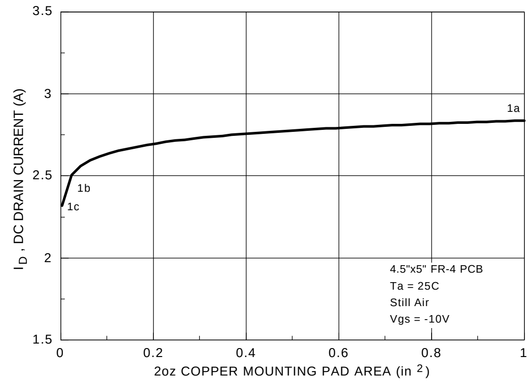


Figure 26. P-Ch DC Drain Current Capability versus Copper Mounting Pad Area.

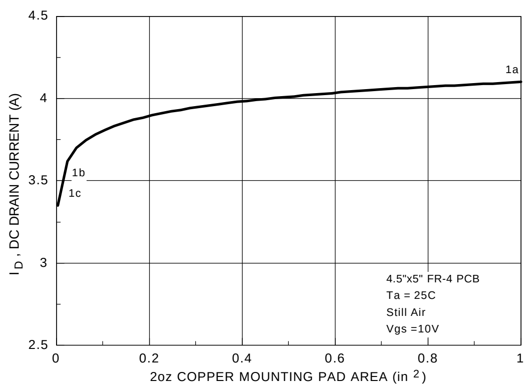


Figure 27. N-Ch DC Drain Current Capability versus Copper Mounting Pad Area.

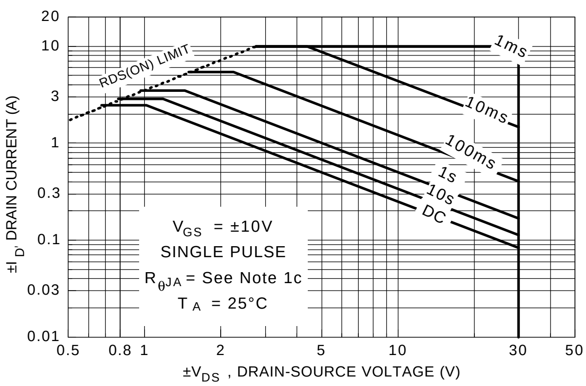


Figure 28. P-Ch Typical Safe Operating Area.

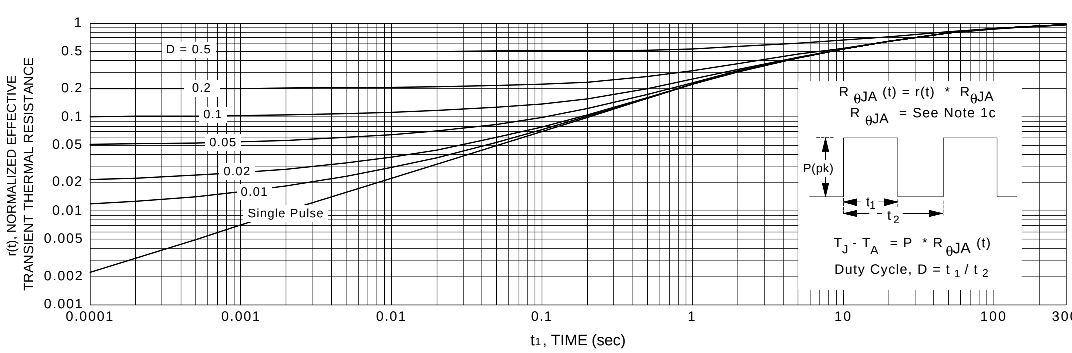


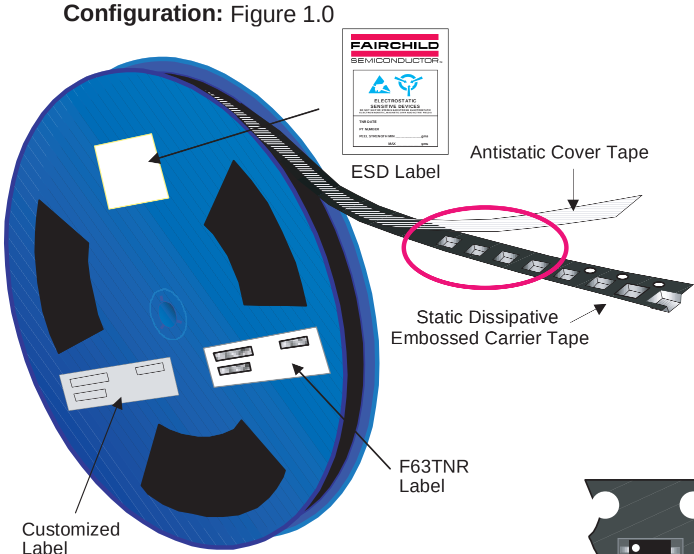
Figure 29. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

SOIC-16 Tape and Reel Data and Package Dimensions

FAIRCHILD SEMICONDUCTOR™

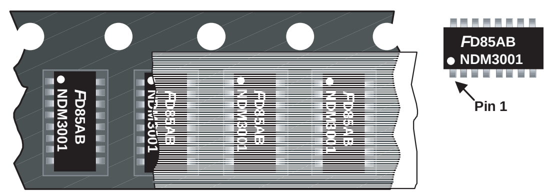
SOIC(16lds) Packaging Configuration: Figure 1.0



Packaging Description:

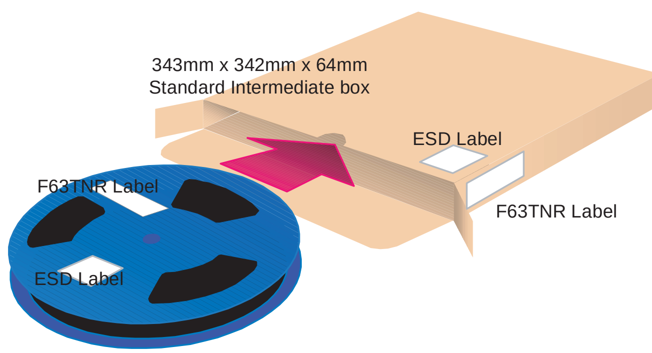
SOIC-16 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



SOIC-16 Unit Orientation

SOIC (16lds) Packaging Information		
Packaging Option	Standard (no flow code)	L86Z
Packaging type	TNR	Rail/Tube
Qty per Reel/Tube/Bag	2,500	45
Reel Size	13" Dia	-
Box Dimension (mm)	343x64x343	530x130x83
Max qty per Box	5,000	13,500
Weight per unit (gm)	0.1437	0.1437
Weight per Reel (kg)	0.7735	-
Note/Comments		



F63TNR Label sample

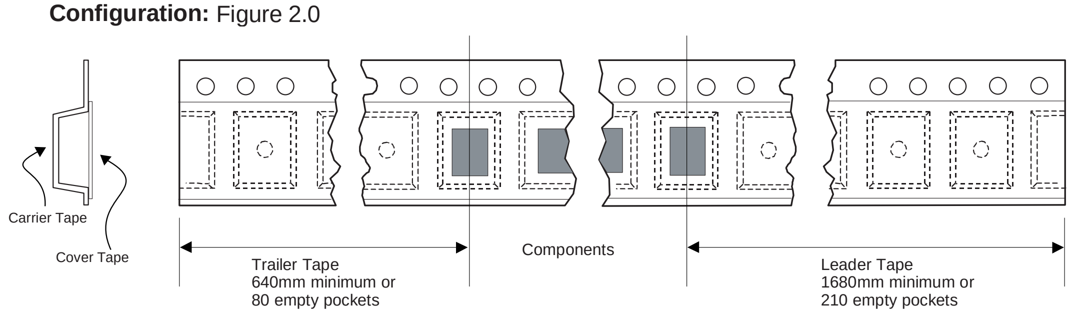
LOT: CBVK741B019 QTY: 2500

FSID: NDM3000 SPEC:

D/C1: D9842 QTY1: SPEC REV:
D/C2: QTY2: CPN:

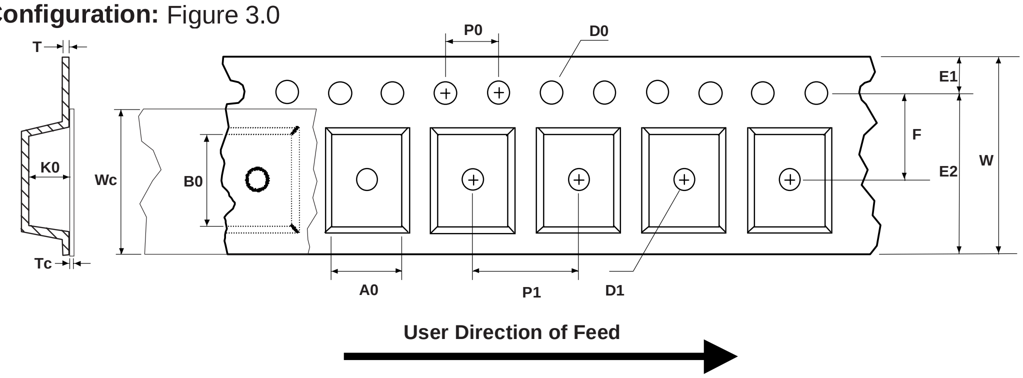
N/F: F (F63TNR)3

SOIC(16lds) Tape Leader and Trailer Configuration: Figure 2.0



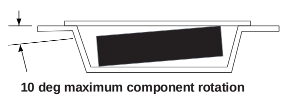
SOIC-16 Tape and Reel Data and Package Dimensions, continued

SOIC(16lds) Embossed Carrier Tape Configuration: Figure 3.0

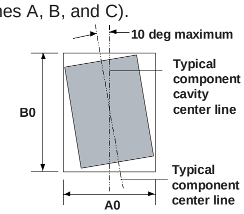


Dimensions are in millimeter													
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SOIC(16lds) (16mm)	6.60 +/-0.30	10.35 +/-0.25	16.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	14.25 min	7.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.40 +/-0.40	0.450 +/-0.150	13.0 +/-0.3	0.06 +/-0.02

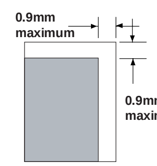
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

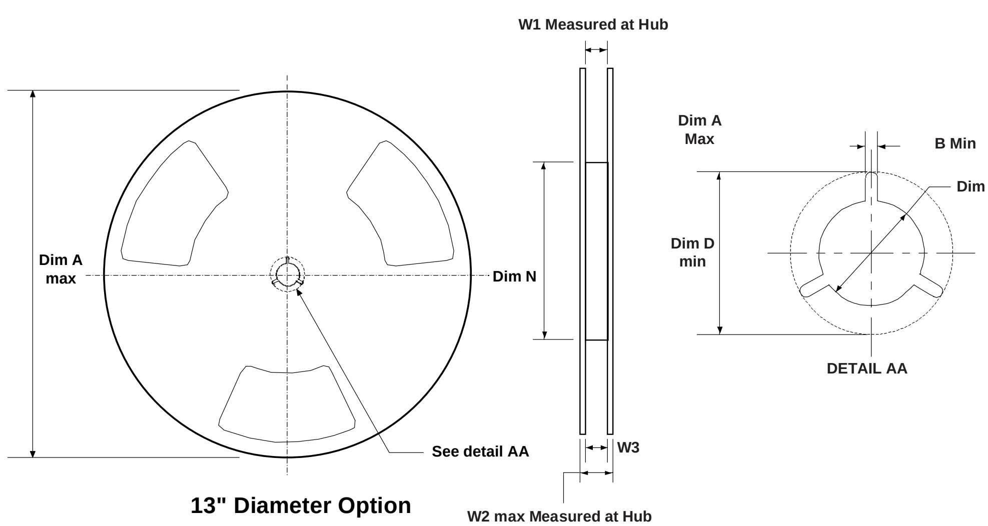


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

SOIC(16lds) Reel Configuration: Figure 4.0

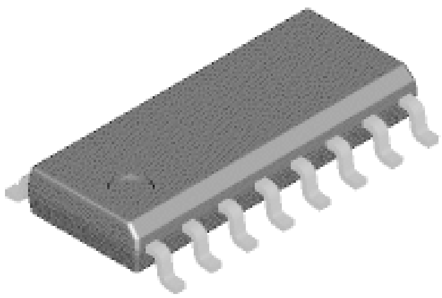


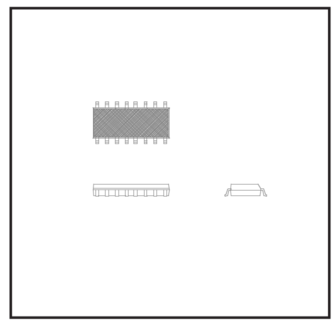
13" Diameter Option

Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
16mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.646 +0.078/-0.000 16.4 +2/0	0.882 22.4	0.626 – 0.764 15.9 – 19.4

SOIC-16 Tape and Reel Data and Package Dimensions, continued

SOIC-16 (FS PKG Code S3)



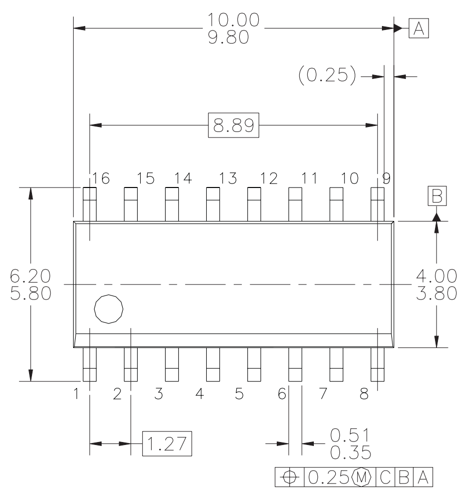


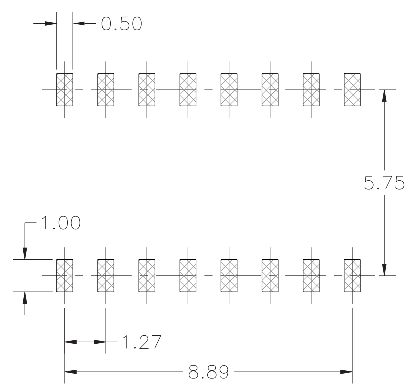
1:1

Scale 1:1 on letter size paper

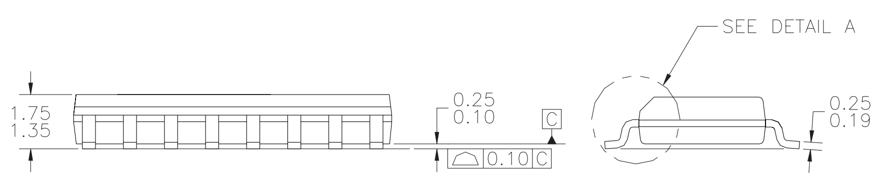
Dimensions shown below are in:
inches [millimeters]

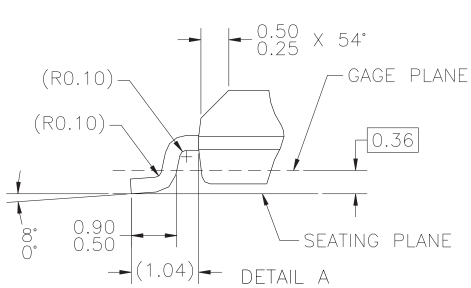
Part Weight per unit (gram): 0.1437





LAND PATTERN RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) STANDARD LEAD FINISH:
200 MICROINCHES / 5.08 MICRONS MIN.
LEAD/TIN (SOLDER) ON COPPER.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
CoolFET™
CROSSVOLT™
E²CMOS™
FACT™
FACT Quiet Series™
FAST®
FASTr™
GTO™
HiSeC™
ISOPLANAR™
MICROWIRE™
POP™
PowerTrench™
QFET™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
TinyLogic™
UHC™
VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.