

NL27WZ02

Dual 2-Input NOR Gate

The NL27WZ02 is a high performance dual 2-input NOR Gate operating from a 1.65 V to 5.5 V supply.

- Extremely High Speed: t_{PD} 2.5 ns (typical) at $V_{CC} = 5.0$ V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs
- LVTTL Compatible – Interface Capability With 5.0 V TTL Logic with $V_{CC} = 3.0$ V
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Replacement for NC7WZ02
- Chip Complexity: FET = 112



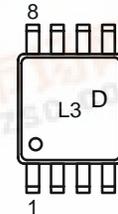
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



US8
US SUFFIX
CASE 493



D = Date Code

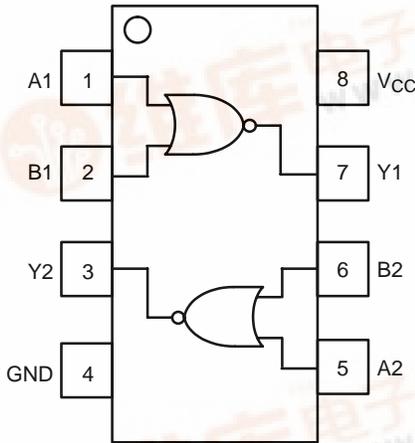


Figure 1. Pinout

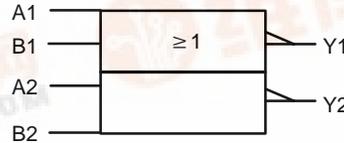


Figure 2. Logic Symbol

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

PIN ASSIGNMENT

Pin	Function
1	A1
2	B1
3	Y2
4	GND
5	A2
6	B2
7	Y1
8	V_{CC}

FUNCTION TABLE

Input		Output $Y = \bar{A} + \bar{B}$
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L



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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage	-0.5 to +7.0	V
I _{IK}	DC Input Diode Current V _I < GND	-50	mA
I _{OK}	DC Output Diode Current V _O < GND	-50	mA
I _O	DC Output Sink Current	±50	mA
I _{CC}	DC Supply Current per Supply Pin	±100	mA
I _{GND}	DC Ground Current per Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+150	°C
θ _{JA}	Thermal Resistance (Note 1)	250	°C/W
P _D	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V _I	Input Voltage (Note 5)	0	5.5	V
V _O	Output Voltage (HIGH or LOW State)	0	V _{CC}	V
T _A	Operating Free-Air Temperature	-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 1.8 V ±0.15 V V _{CC} = 2.5 V ±0.2 V V _{CC} = 3.0 V ±0.3 V V _{CC} = 5.0 V ±0.5 V	0 0 0 0	20 20 10 5	ns/V

5. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 2.3 to 5.5	0.75 V _{CC} 0.7 V _{CC}			0.75 V _{CC} 0.7 V _{CC}		V
V _{IL}	Low-Level Input Voltage		1.65 2.3 to 5.5			0.25 V _{CC} 0.3 V _{CC}		0.25 V _{CC} 0.3 V _{CC}	V
V _{OH}	High-Level Output Voltage V _{IN} = V _{IL} or V _{IH}	I _{OH} = -100 μA I _{OH} = -4 mA I _{OH} = -8 mA I _{OH} = -12 mA I _{OH} = -16 mA I _{OH} = -24 mA I _{OH} = -32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V _{CC} - 0.1 1.29 1.9 2.2 2.4 2.3 3.8	V _{CC} 1.5 2.1 2.4 2.7 2.5 4.0		V _{CC} - 0.1 1.29 1.90 2.20 2.40 2.30 3.80		V
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH} or V _{OH}	I _{OL} = 100 μA I _{OL} = 4 mA I _{OL} = 8 mA I _{OL} = 12 mA I _{OL} = 16 mA I _{OL} = 24 mA I _{OL} = 32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		0.0 0.08 0.20 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I _{IN}	Input Leakage Current	V _{IN} = V _{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 3.0 ns

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay (Figure 3 and 4)	R _L = 1 MΩ, C _L = 15 pF	1.8 ± 0.15	2.0	7.4	9.5	2.0	9.7	ns
2.5 ± 0.20			1.2	3.3	5.4	1.2	5.8		
3.3 ± 0.30		R _L = 1 MΩ, C _L = 15 pF R _L = 500 Ω, C _L = 50 pF	0.8	2.6	3.9	0.8	4.3		
			1.2	3.2	4.8	1.2	5.2		
5.0 ± 0.50	R _L = 1 MΩ, C _L = 15 pF R _L = 500 Ω, C _L = 50 pF	0.5	1.9	3.1	0.5	3.3			
		0.8	2.5	3.7	0.8	4.0			

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	2.5	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC} 10 MHz, V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	9.0 11.0	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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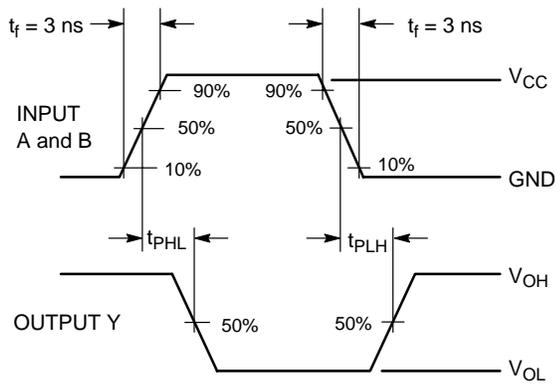
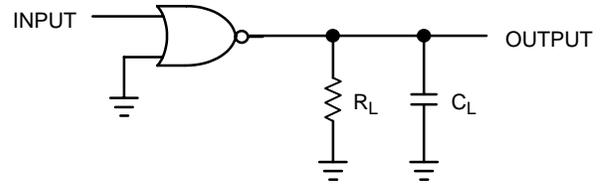


Figure 3. Switching Waveform



A 1-MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

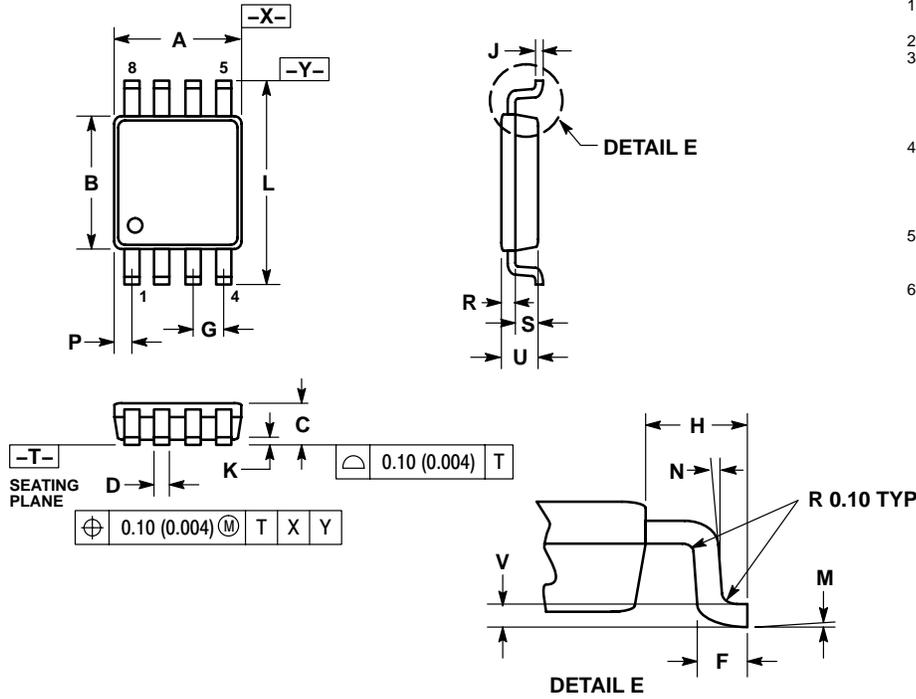
DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix		
NL27WZ02US	NL	2	7	WZ	02	US	US8	178 mm, 3000 Unit

NL27WZ02

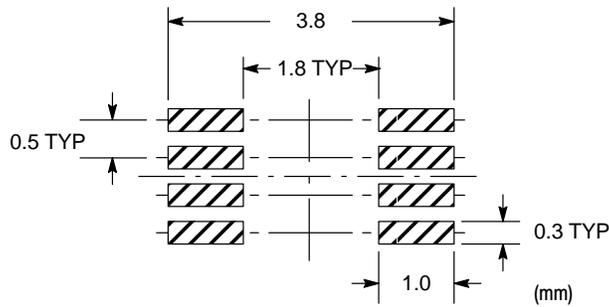
PACKAGE DIMENSIONS

US8
US SUFFIX
CASE 493-02
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
 4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
 5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800").
 6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ± 0.0508 (0.0002").

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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