

NL27WZ126

Dual Buffer with 3-State Outputs

The NL27WZ126 is a high performance dual noninverting buffer operating from a 2.3 V to 5.5 V supply.

- Extremely High Speed: t_{PD} 2.6 ns (typical) at $V_{CC} = 5\text{ V}$
- Designed for 2.3 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs and Outputs
- LVTTL Compatible – Interface Capability With 5 V TTL Logic with $V_{CC} = 3\text{ V}$
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- 3-State OE Input is Active-High
- Replacement for NC7WZ126
- Chip Complexity = 72 FETs

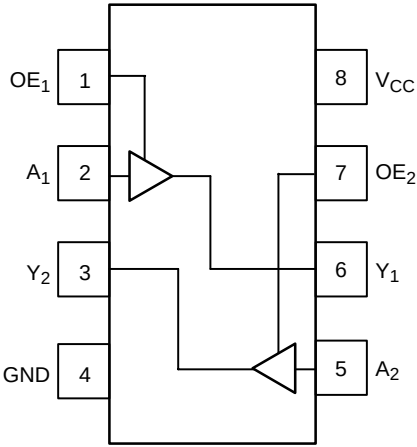


Figure 1. Pinout (Top View)

PIN ASSIGNMENT	
Pin	Function
1	OE
2	A ₁
3	Y ₂
4	GND
5	A ₂
6	Y ₁
7	OE ₂
8	V _{CC}

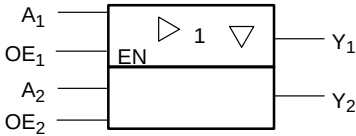


Figure 2. Logic Symbol

FUNCTION TABLE		
Input		Output
OE _n	A _n	Y _n
H	H	H
H	L	L
L	X	Z

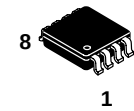
X = Don't Care
n = 1, 2



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MARKING DIAGRAM



US8
US SUFFIX
CASE 493-01



D = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V _I	DC Input Voltage	− 0.5 to + 7.0	V
V _O	DC Output Voltage	− 0.5 to + 7.0	V
I _{IK}	DC Input Diode Current V _I < GND	− 50	mA
I _{OK}	DC Output Diode Current V _O < GND	− 50	mA
I _O	DC Output Sink Current	± 50	mA
I _{CC}	DC Supply Current per Supply Pin	± 100	mA
I _{GND}	DC Ground Current per Ground Pin	± 100	mA
T _{STG}	Storage Temperature Range	− 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+ 150	°C
θ _{JA}	Thermal Resistance (Note 1)	250	°C/W
P _D	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage Operating Data Retention Only	2.3 1.5	5.5 5.5	V
V _I	Input Voltage (Note 5)	0	5.5	V
V _O	Output Voltage (HIGH or LOW State)	0	5.5	V
T _A	Operating Free-Air Temperature	− 40	+ 85	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 2.5 V ± 0.2 V V _{CC} = 3.0 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0 0	20 10 5	ns/V

5. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.3 to 5.5	0.7 V _{CC}			0.7 V _{CC}		V
V _{IL}	Low-Level Input Voltage		2.3 to 5.5			0.3 V _{CC}		0.3 V _{CC}	V
V _{OH}	High-Level Output Voltage V _{IN} = V _{IH}	I _{OH} = 100 μA	2.3 to 5.5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V
		I _{OH} = -8 mA	2.3	1.9	2.1		1.9		
		I _{OH} = -12 mA	2.7	2.2	2.4		2.2		
		I _{OH} = -16 mA	3.0	2.4	2.7		2.4		
		I _{OH} = -24 mA	3.0	2.3	2.5		2.3		
		I _{OH} = -32 mA	4.5	3.8	4.0		3.8		
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.3 to 5.5			0.1		0.1	V
		I _{OL} = 8 mA	2.3		0.20	0.3		0.3	
		I _{OL} = 12 mA	2.7		0.22	0.4		0.4	
		I _{OL} = 16 mA	3.0		0.28	0.4		0.4	
		I _{OL} = 24 mA	3.0		0.38	0.55		0.55	
		I _{OL} = 32 mA	4.5		0.42	0.55		0.55	
I _{IN}	Input Leakage Current	V _{IN} = V _{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I _{OFF}	Power Off-Output Leakage Current	V _{OUT} = 5.5 V	0			1		10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1		10	μA
I _{OZ}	3-State Output Leakage	V _{IN} = V _{IL} or V _{IH} 0 V ≤ V _{OUT} ≤ 5.5 V	2.3 to 5.5			±0.5		±5	μA

AC ELECTRICAL CHARACTERISTICS (t_R = t_F = 3.0 ns)

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay AN to YN (Figures 3 and 4, Table 1)	R _L = 1 MΩ C _L = 15 pF	2.5 ± 0.2	1.0		7.5	1.0	8	ns
		R _L = 1 MΩ C _L = 15 pF	3.3 ± 0.3	0.8		5.2	0.8	5.5	
		R _L = 500 Ω C _L = 50 pF		1.2		5.7	1.2	6.0	
		R _L = 1 MΩ C _L = 15 pF R _L = 500 Ω C _L = 50 pF	5.0 ± 0.5	0.5 0.8		4.5 5.0	0.5 0.8	4.8 5.3	
t _{OSLH} t _{OSHL}	Output to Output Skew (Note 6)	R _L = 500 Ω C _L = 50 pF	3.3 ± 0.3			1.0		1.0	ns
		R _L = 500 Ω C _L = 50 pF	5.0 ± 0.5			0.8		0.8	
t _{PZH} t _{PZL}	Output Enable Time (Figures 5, 6 and 7, Table 1)	R _L = 250 Ω C _L = 50 pF	2.5 ± 0.2	1.8		8.5	1.8	9.0	ns
			3.3 ± 0.3	1.2		6.2	1.2	6.5	
			5.0 ± 0.5	0.8		5.5	0.8	5.8	
t _{PHZ} t _{PLZ}	Output Enable Time (Figures 5, 6 and 7, Table 1)	R _L and R1 = 500 Ω C _L = 50 pF	2.5 ± 0.2	1.5		8.0	1.5	8.5	ns
			3.3 ± 0.3	0.8		5.7	0.8	6.0	
			5.0 ± 0.5	0.3		4.7	0.3	5.0	

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. This specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	2.5	pF
C_{OUT}	Output Capacitance	$V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance (Note 7)	10 MHz, $V_{CC} = 3.3 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	9	pF
		10 MHz, $V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	11	

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

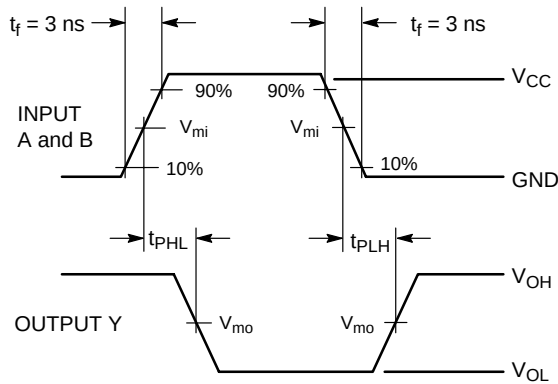
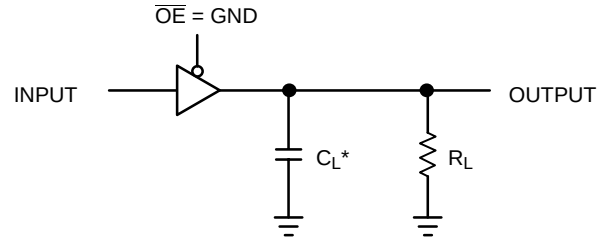


Figure 3. Switching Waveform



*Includes all probe and jig capacitance.
A 1 MHz square input wave is recommended for propagation delay tests.

Figure 4. T_{PLH} or T_{PHL}

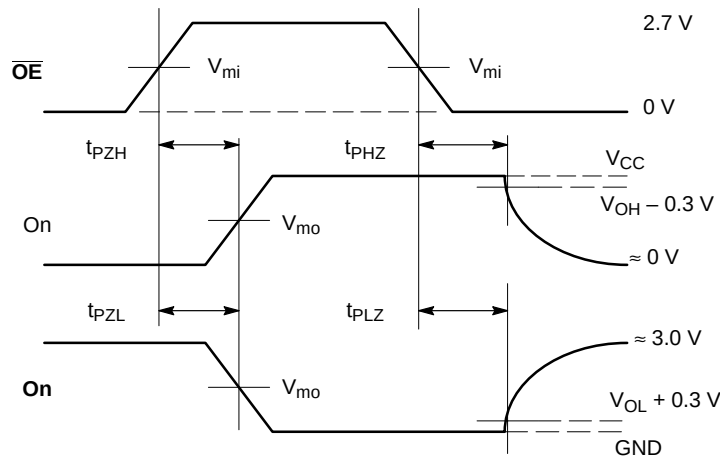


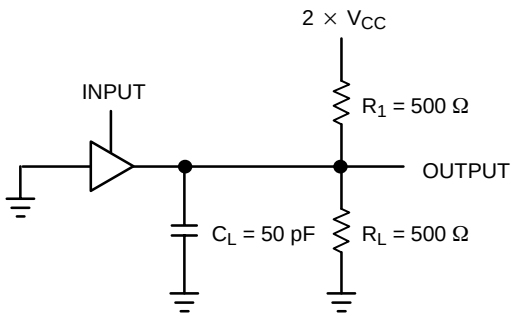
Figure 5. AC Output Enable and Disable Waveform

Table 1. Output Enable and Disable Times

$t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$

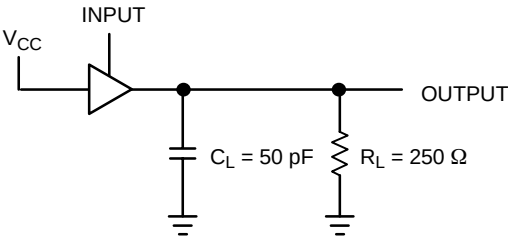
Symbol	V_{CC}		
	$3.3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	$2.5 \text{ V} \pm 0.2 \text{ V}$
V_{mi}	1.5 V	1.5 V	$V_{CC}/2$
V_{mo}	1.5 V	1.5 V	$V_{CC}/2$

NL27WZ126



A 1 MHz square input wave is recommended for propagation delay tests.

Figure 6. T_{PZL} or T_{PLZ}



A 1 MHz square input wave is recommended for propagation delay tests.

Figure 7. T_{PZH} or T_{PHZ}

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix		
NL27WZ126US	NL	2	7	WZ	126	US	US8	178 mm, 3000 Units

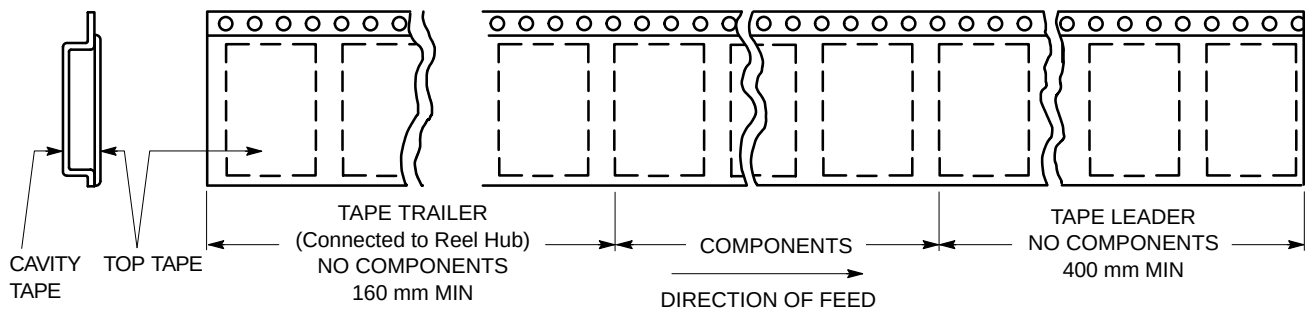


Figure 8. Tape Ends for Finished Goods

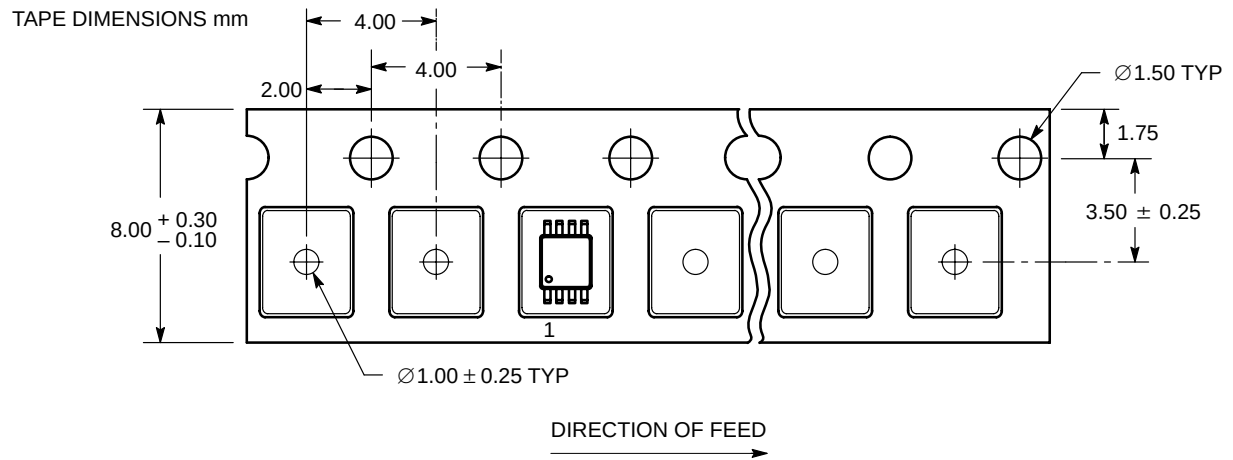


Figure 9. US8 Reel Configuration/Orientation

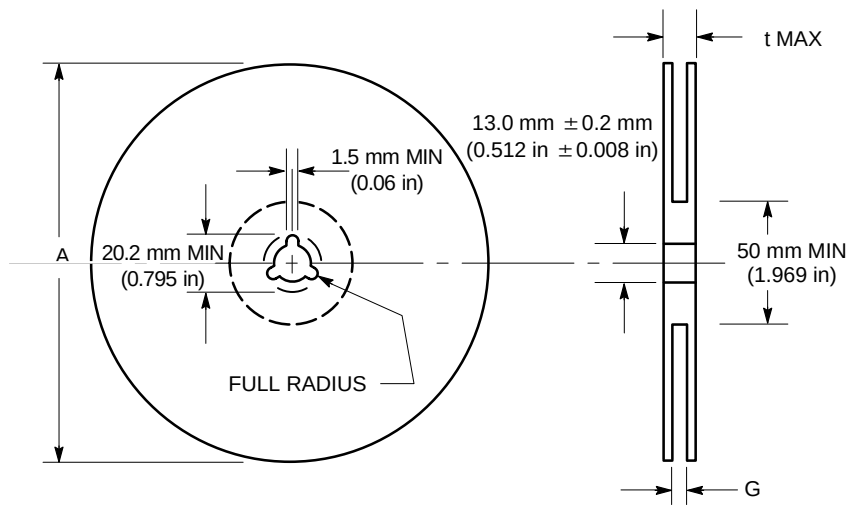


Figure 10. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	US	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

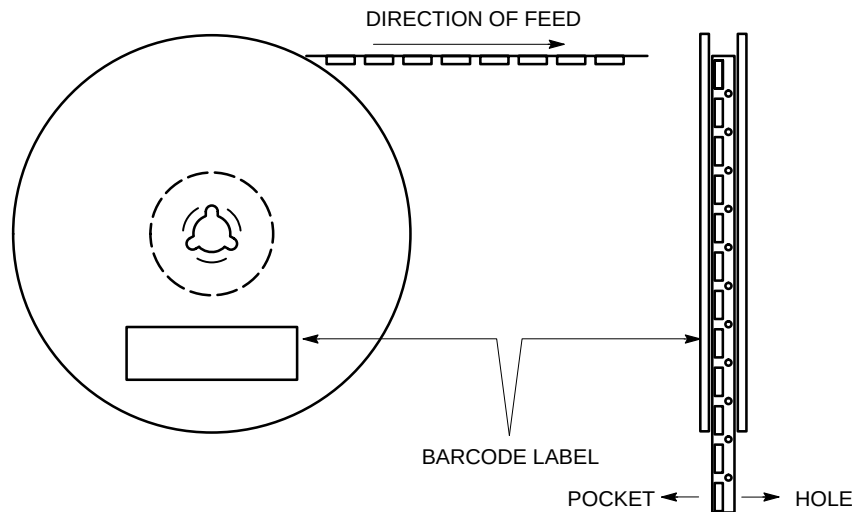
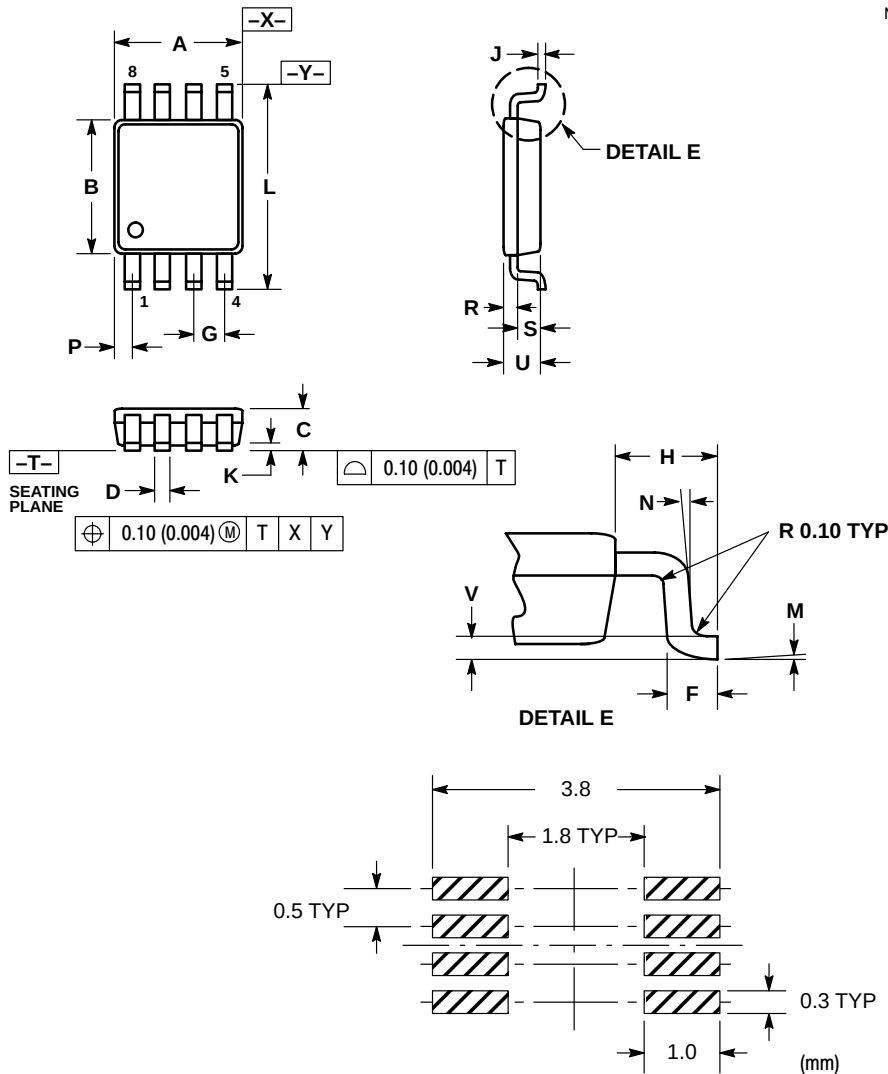


Figure 11. Reel Winding Direction

NL27WZ126

PACKAGE DIMENSIONS

US8
US SUFFIX
CASE 493-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 INCH).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ± 0.0508 (0.0002").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0°	6°	0°	6°
N	5°	10°	5°	10°
P	0.28	0.44	0.011	0.017
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

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