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003588

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National Semiconductor

NMC2764 65,536-Bit (8192 × 8) UV Erasable PROM

Parameter/Order Number	NMC2764-2 / NMC2764H-2	NMC2764 / NMC2764H	NMC2764-3 / NMC2764H-3	NMC2764-4 / NMC2764H-4	NMC2764-25 / NMC2764H-25	NMC2764-30 / NMC2764H-30	NMC2764-45 / NMC2764H-45
Access Time (ns)	200	250	300	450	250	300	450
V_{CC} Power Supply	5V ± 5%	5V ± 5%	5V ± 5%	5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

General Description

The NMC2764 is a high speed 64k UV erasable and electrically reprogrammable EPROM, ideally suited for applications where fast turnaround and pattern experimentation are important requirements.

The NMC2764 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, XMOS™ technology, National's high-speed N-channel MOS silicon gate technology.

XMOS™ is a trademark of National Semiconductor Corp.
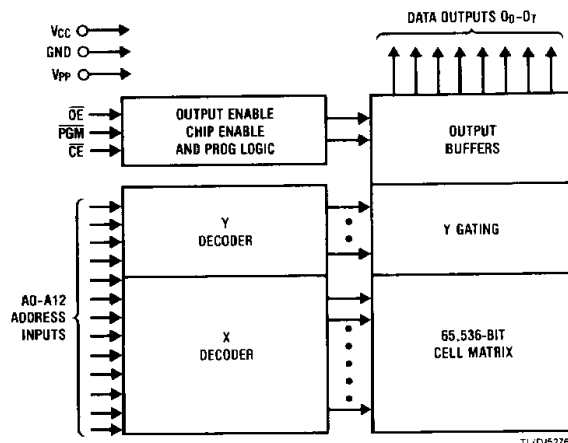TRI-STATE® is a registered trademark of National Semiconductor Corp.

Features

- Access time down to 200 ns, XMOS™ technology
- Compatible to high speed (8 MHz) microprocessors, zero wait state
- Low power consumption
  Active power: 525 mW max
  Standby power: 105 mW max (80% savings)
- Single 5V power supply
- ± 10% power supply tolerance available
- Extended temperature range available (NMC2764E and NMC2764HE), −40°C to +85°C, 250 ns ± 5% power supply
- 10 ms programming available (NMC2764H), an 80% time savings
- TTL compatible inputs/outputs
- Two-line control
- TRI-STATE® output
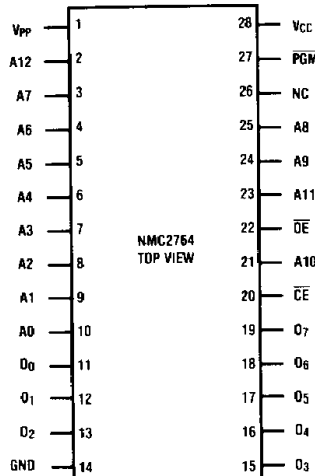
Block and Connection Diagrams

Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

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Dual-In-Line Package

27C256 27256	27C128 27128	27C32 2732	27C16 2716		NMC2764 TOP VIEW		27C16 2716	27C32 2732	27C128 27128	27C256 27256
V_{PP}	V_{PP}			V_{PP} — 1	28 — V_{CC}				V_{CC}	V_{CC}
A12	A12			A12 — 2	27 — $\overline{PGM}$				$\overline{PGM}$	A14
A7	A7	A7	A7	A7 — 3	26 — NC		V_{CC}	V_{CC}	A13	A13
A6	A6	A6	A6	A6 — 4	25 — A8		A8	A8	A8	A8
A5	A5	A5	A5	A5 — 5	24 — A9		A9	A9	A9	A9
A4	A4	A4	A4	A4 — 6	23 — A11		V_{PP}	A11	A11	A11
A3	A3	A3	A3	A3 — 7	22 — $\overline{OE}$		$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A2	A2	A2	A2	A2 — 8	21 — A10		A10	A10	A10	A10
A1	A1	A1	A1	A1 — 9	20 — $\overline{CE}$		$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
A0	A0	A0	A0	A0 — 10	19 — O_7		O_7	O_7	O_7	O_7
O_0	O_0	O_0	O_0	O_0 — 11	18 — O_6		O_6	O_6	O_6	O_6
O_1	O_1	O_1	O_1	O_1 — 12	17 — O_5		O_5	O_5	O_5	O_5
O_2	O_2	O_2	O_2	O_2 — 13	16 — O_4		O_4	O_4	O_4	O_4
GND	GND	GND	GND	GND — 14	15 — O_3		O_3	O_3	O_3	O_3

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Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC2764 pins.

IM-B30M73/Printed in U.S.A.

Absolute Maximum Ratings (Note 1)

Temperature Under Bias $-10°C$ to $+80°C$
Storage Temperature $-65°C$ to $+125°C$
All Input or Output Voltages with
  Respect to Ground $+6.5V$ to $-0.3V$
V_{PP} Supply Voltage with Respect
  to Ground During Programming $+22V$ to $-0.3V$
Power Dissipation   1.5W
Lead Temperature (Soldering, 10 seconds)   300°C

Operating Conditions (Note 9)

Temperature Range
  NMC2764-2, NMC2764, NMC2764-3,
  NMC2764-4, NMC2764-25, NMC2764-30,
  NMC2764-45, NMC2764H-2, NMC2764H,
  NMC2764H-3, NMC2764H-4, NMC2764H-25,
  NMC2764H-30, NMC2764H-45   0°C to 70°C
  √ NMC2764E, NMC2764HE√ $-40°C$ to $+85°C$
V_{CC} Power Supply (Notes 2 and 3)
  NMC2764-2, NMC2764, NMC2764-3,
  NMC2764-4, NMC2764E, NMC2764H-2,
  NMC2764H, NMC2764H-3, NMC2764H-4,
  NMC2764HE $5V \pm 5\%$
  NMC2764-25, NMC2764-30, NMC2764-45,
  NMC2764H-25, NMC2764H-30,
  NMC2764H-45 $5V \pm 10\%$
V_{PP} Power Supply $V_{PP} = V_{CC}$

READ OPERATION

DC and Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
I_{LI}	Input Load Current	$V_{IH} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE} = V_{IH}$			20	mA
I_{CC2} (Note 3)	V_{CC} Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$, I/O = 0 mA		70	100	mA
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400 \mu A$	2.4			V

AC Characteristics

| Symbol	Parameter	Conditions	NMC2764-2 NMC2764H-2		NMC2764E NMC2764HE NMC2764-25 NMC2764H-25 NMC2764 NMC2764H		NMC2764-30 NMC2764H-30 NMC2764-3 NMC2764H-3		NMC2764-45 NMC2764H-45 NMC2764-4 NMC2764H-4		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		100		120		150	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	85	0	105	0	130	ns
t_{OH} (Note 5)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

Capacitance (Note 5) ($T_A = +25°C$, $f = 1$ MHz)

Symbol	Parameter	Conditions	Typ (Note 4)	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 2)
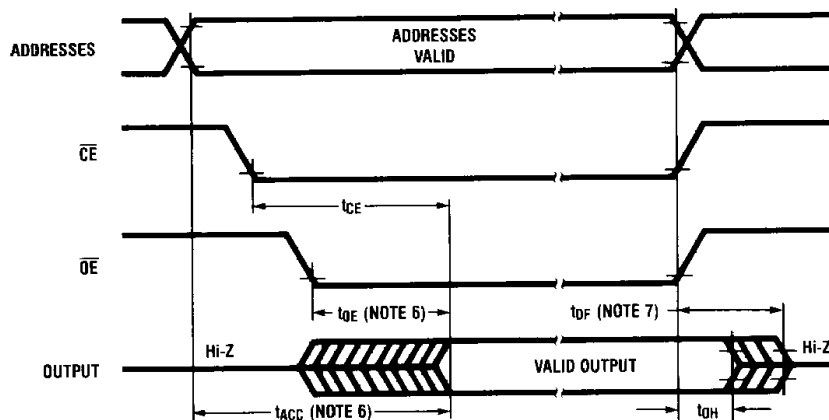
TL/D/5276-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. $I_{CC2} \leq$ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 5: This parameter is only sampled and is not 100% tested.

Note 6: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 7: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH} (DC) $-0.1V$
Low to TRI-STATE, the measured V_{OL} (DC) $+0.1V$

Note 8: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 9: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

PROGRAMMING (Note 1)

DC Programming Characteristics (Notes 2 and 3) ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (All Inputs)	$V_{IH} = V_{CC}$ or GND			10	μA
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400 \mu A$	2.4			V
I_{CC2}	V_{CC} Supply Current (Active)				100	mA
V_{IL}	Input Low Level (All Inputs)		-0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

AC Programming Characteristics $T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

Symbol	Parameter	Conditions	NMC2764 Devices			NMC2764H Devices			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AS}	Address Set-Up Time		2			2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			2			μs
t_{DS}	Data Set-Up Time		2			2			μs
t_{AH}	Address Hold Time		0			0			μs
t_{DH}	Data Hold Time		2			2			μs
t_{DF}	Output Enable to Output Float Delay		0		130	0		130	ns
t_{VS}	V_{PP} Set-Up Time		2			2			μs
t_{PW}	$\overline{PGM}$ Pulse Width During Programming		45	50	55	9	10	11	ms
t_{CES}	$\overline{CE}$ Set-Up Time		2			2			μs
t_{OE}	Data Valid from $\overline{OE}$				150			150	ns

AC Test Conditions

V_{CC}	$5V \pm 5\%$
V_{PP}	$21V \pm 0.5V$
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3)
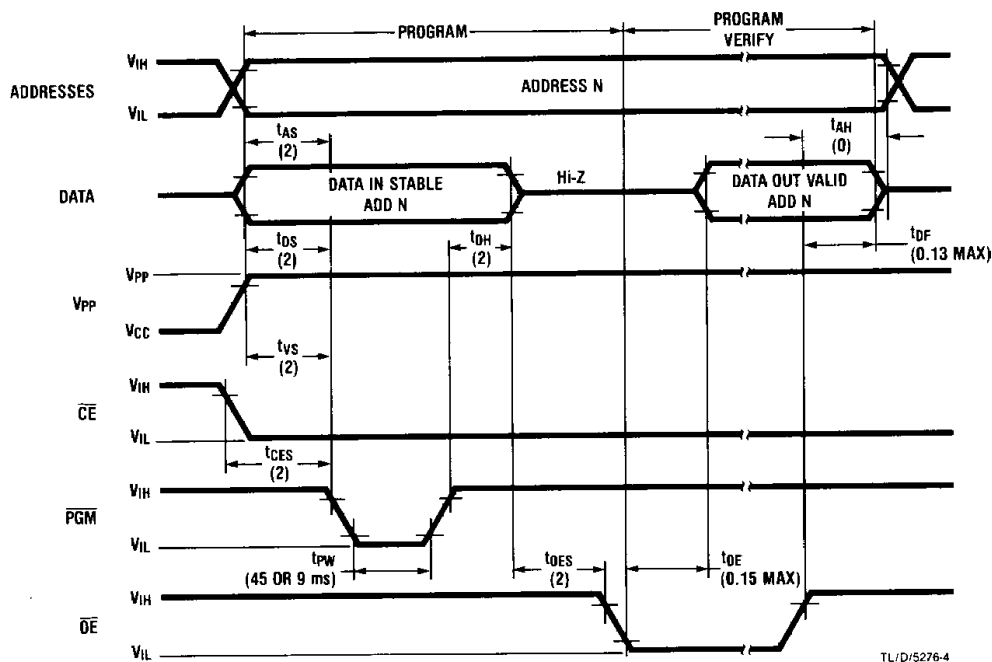
Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

The input timing reference level is 1V for a V_{IL} and 2V for a V_{IH}.

t_{OE} and t_{OH} are characteristics of the device but must be accommodated by the programmer.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp. The NMC2764 must not be inserted into or removed from a board with Vpp at 21V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the Vpp pin during programming is 21.5V. Care must be taken when switching the Vpp supply to prevent overshoot exceeding this 21.5V maximum specification. A 0.1 μF capacitor is required across Vpp, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC2764 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

Read Mode

The NMC2764 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The NMC2764 has a standby mode which reduces the active power dissipation by 80%, from 525 mW to 105 mW. The NMC2764 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, National has provided two control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ (pin 20) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 22V on pin 1 (V_{PP}) will damage the NMC2764.

Initially, and after each erasure, all bits of the NMC2764 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC2764 is in the programming mode when the V_{PP} input is at 21V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. It is required that a 0.1 μF capacitor be placed across V_{PP}, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 21V. When the address and data are stable, a 50 ms (10 ms for the NMC2764H devices) active low TTL program pulse is applied to $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms (11 ms for the NMC2764H devices).

Programming of multiple NMC2764s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC2764s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC2764s.

TABLE I. MODE SELECTION

Pins Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	Hi-Z

X can be either V_{IL} or V_{IH}.

Functional Description (Continued)

Program Inhibit

Programming multiple NMC2764s in parallel with different data is also easily accomplished. A high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other NMC2764s from being programmed. Except for $\overline{CE}$ (or $\overline{PGM}$), all like inputs (including $\overline{OE}$) of the parallel NMC2764s may be common. A TTL low level pulse applied to a NMC2764 $\overline{CE}$ and $\overline{PGM}$ input with V_{PP} at 21V will program that NMC2764.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{CE}$ and $\overline{OE}$ at V_{IL}. However, $\overline{PGM}$ is at V_{IH}.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC2764 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms ($\overset{\circ}{A}$). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 $\overset{\circ}{A}$ –4000 $\overset{\circ}{A}$ range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC2764 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NMC2764 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the NMC2764 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC2764 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms ($\overset{\circ}{A}$). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm² power rating. The NMC2764 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.
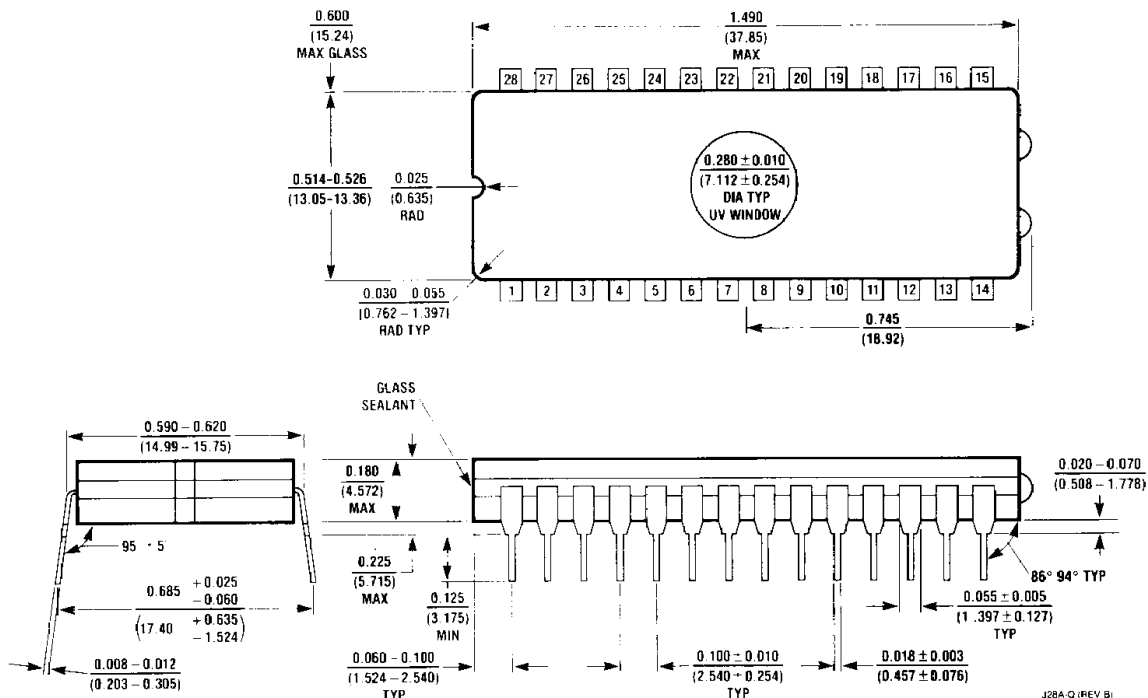
Note: The NMC2764-4 and NMC2764H-4 may take up to 60 minutes for complete erasure to occur.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board traces.

Physical Dimensions inches (millimeters)

0.600
(15.24)
MAX GLASS

1.490
(37.85)
MAX

0.514–0.526
(13.05–13.36)

0.025
(0.635)
RAD

0.280 ± 0.010
(7.112 ± 0.254)
DIA TYP
UV WINDOW

0.030 0.055
(0.762 – 1.397)
RAD TYP

0.745
(18.92)

GLASS
SEALANT

0.590 – 0.620
(14.99 – 15.75)

0.180
(4.572)
MAX

0.020 – 0.070
(0.508 – 1.778)

95° ± 5°

0.685 +0.025 / –0.060
(17.40 +0.635 / –1.524)

0.225
(5.715)
MAX

0.125
(3.175)
MIN

86° 94° TYP

0.055 ± 0.005
(1.397 ± 0.127)
TYP

0.008 – 0.012
(0.203 – 0.305)

0.060 – 0.100
(1.524 – 2.540)
TYP

0.100 ± 0.010
(2.540 ± 0.254)
TYP

0.018 ± 0.003
(0.457 ± 0.076)

J28A-Q (REV B)

UV Window Cavity Dual-In-Line Package (J)
NS Package Number J28A-Q