NUD3048

FET Switch

100 V, 800 mΩ, N−Channel, TSOP−6

The NUD3048 provides a single device solution for a number of applications requiring a low power, high voltage, FET switch. The package includes a gate resistor and gate to source zener clamp. This switch can accommodate a wide range of input voltages, making it compatible with most current logic levels. Its 100 V rating makes it compatible with 48 V telecom applications.

Features

- 100 V Rating On Gate 2
- Integrated 100 k R_g Option
- Integrated ESD Diode Protection
- Low Threshold Voltage
- Pb−Free Package is Available

Typical Applications

- FET Switch
- Inverter
- Level Shifter
- Inrush Limiter
- Relay Driver

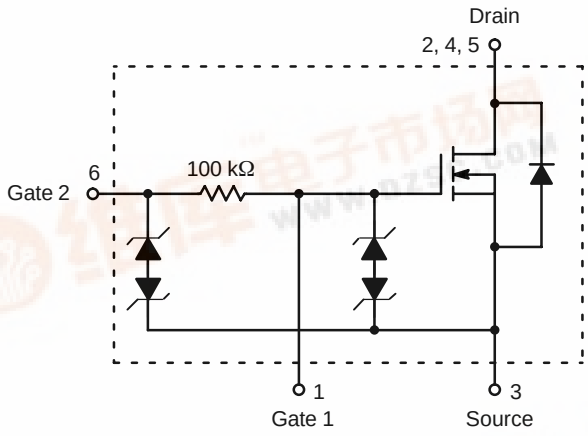

Figure 1. Block Diagram

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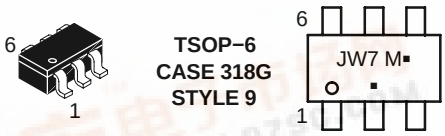
http://onsemi.com

MARKING DIAGRAM



JW7 = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUD3048MT1	TSOP−6	3000 / Tape & Reel
NUD3048MT1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{DSS}	Drain to Source Voltage – Continuous	100	V
V_{G1SS}	Gate to Source Voltage – Continuous @ 1.0 mA	15	V
I_D	Drain Current – Continuous (T_A =25°C) (Note 1) (Note 2)	0.7 1.2	A
P_D	Power Dissipation (T_A =25°C) (Note 1) (Note 2)	0.66 1.56	W
V_{G2SS}	Gate Resistor to Source Voltage – Continuous	100	V
T_{Jmax}	Maximum Junction Temperature	150	°C
$R_{\theta JA}$	Thermal Impedance (Junction−to−Ambient) (Note 1) Thermal Impedance (Junction−to−Ambient) (Note 2)	190 80	°C/W
ESD	Human Body Model (HBM) Class 2 Machine Model Class A According to EIA/JESD22/A114 Specification	2000 100	V V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_J =25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain to Source Leakage Current (V_{DS} = 80 V, V_{GS} = 0 V)	I_{DSS}	−	20	100	μA
Gate Body Leakage Current (V_{GS} =10 V, V_{DS} = 0 V) (V_{GS} = 10 V, V_{DS} = 0 V, T_J = 125°C)	 I_{GSS} I_{GSS}	 − −	 3.0 6.0	 10 20	μA
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 1.0 mA)	V_{GS}	1.3	1.7	2.0	V
Drain to Source Resistance (V_{GS} = 4.5 V, I_D = 100 mA)	$R_{DS(on)}$	−	0.65	0.82	Ω
Drain to Source Resistance (V_{GS} = 10 V, I_D = 100 mA)	$R_{DS(on)}$	−	0.6	0.72	Ω
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 5.0 V, V_{GS} = 0 V, f = 10 kHz)	C_{iss}	−	135	−	pF
Output Capacitance (V_{DS} = 5.0 V, V_{GS} = 0 V, f = 10 kHz)	C_{oss}	−	75	−	pF
Transfer Capacitance (V_{DS} = 5.0 V, V_{GS} = 0 V, f = 10 kHz)	C_{rss}	−	26	−	pF
GATE BIAS CHARACTERISTICS					
Gate Resistor	R_G	75	100	125	kΩ
Gate Zener Breakdown Voltage (I_Z = 1.0 mA) (Note 3) Gate Zener Breakdown Voltage (I_Z = 3.0 mA) (Note 4)	V_Z	15 100	17 115	− −	V

1. Min pad, 1 oz. Cu.
2. 1 inch pad, 1 oz Cu.
3. Measured from gate 1 to source.
4. Measured from gate 2 to source.

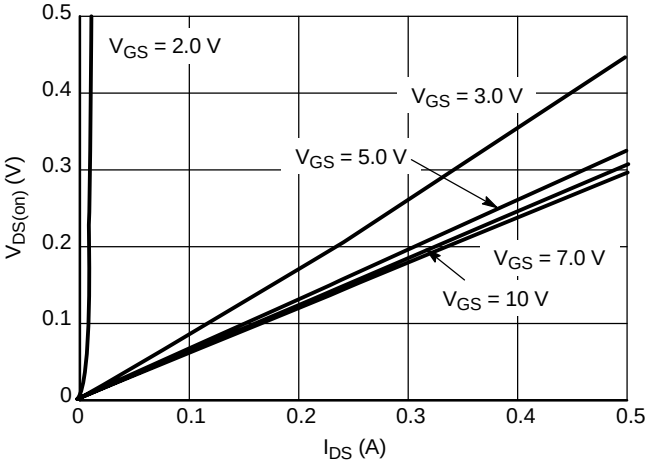


Figure 2. $V_{DS(on)}$ Variation with I_{DS} and Gate Voltage

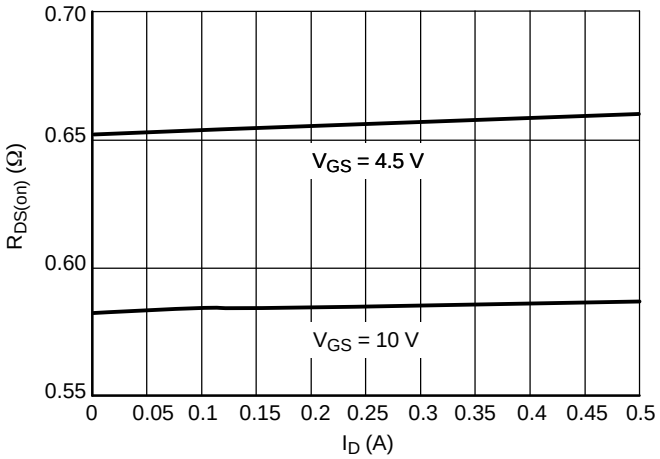


Figure 3. On Resistance Variation with Drain Current and Gate Voltage

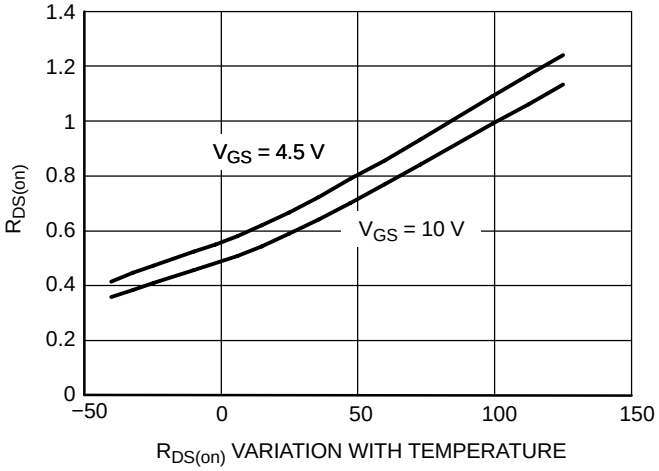


Figure 4. Variation of $R_{DS(on)}$ with Temperature and Gate Voltage at I_D = 100 mA

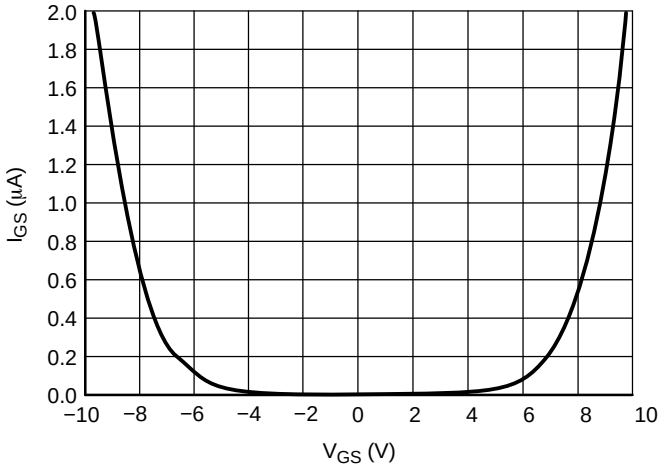


Figure 5. Gate Leakage Current Variation with Gate Voltage

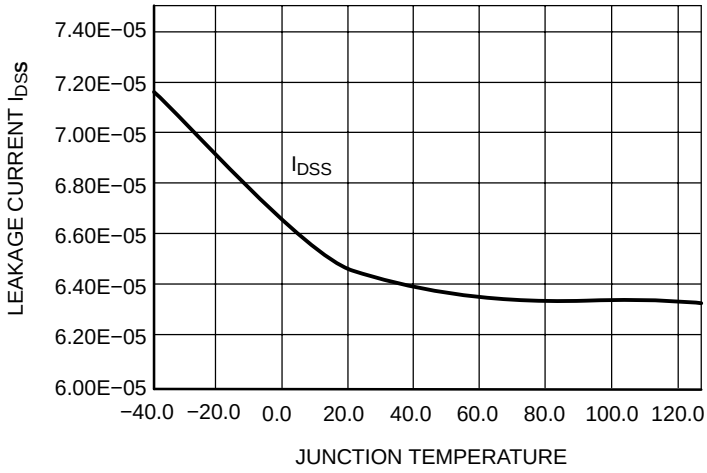
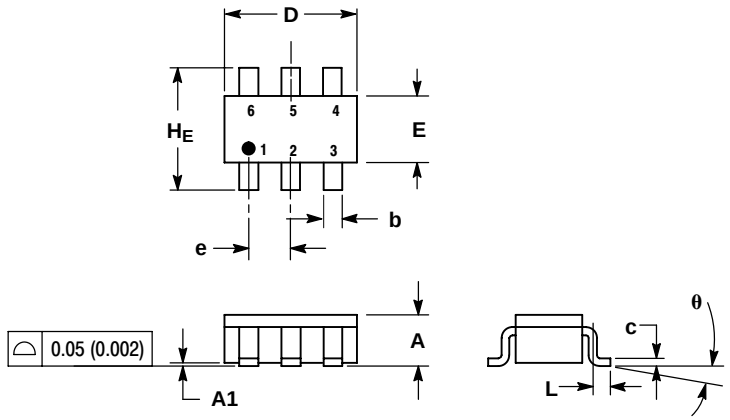


Figure 6. Variation of Leakage Current I_{DSS} (A) with V_{GS} = 0 V and V_{DS} = 100 V

NUD3048

PACKAGE DIMENSIONS

TSOP−6
CASE 318G−02
ISSUE P

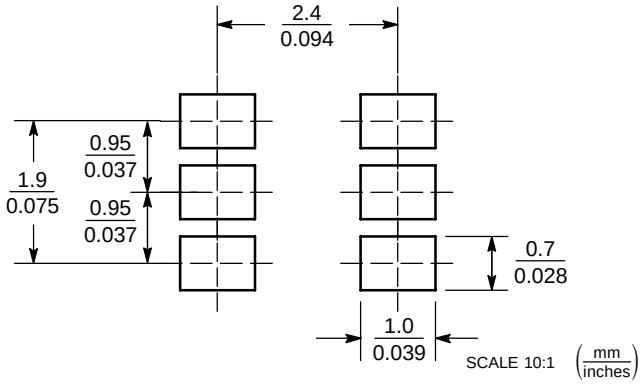


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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