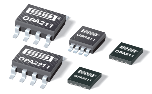


OPA211
OPA2211

SBOS377D–OCTOBER 2006–REVISED FEBRUARY 2008

1.1nV/√Hz Noise, Low Power, Precision Operational Amplifier in Small DFN-8 Package

FEATURES

- **LOW VOLTAGE NOISE: 1.1nV/√Hz at 1kHz**
- **INPUT VOLTAGE NOISE: 80nV$_{PP}$ (0.1Hz to 10Hz)**
- **THD+N: –136dB (G = 1, f = 1kHz)**
- **OFFSET VOLTAGE: 125μV (max)**
- **OFFSET VOLTAGE DRIFT: 0.35μV/°C (typ)**
- **LOW SUPPLY CURRENT: 3.6mA/Ch (typ)**
- **UNITY GAIN STABLE**
- **GAIN BANDWIDTH PRODUCT: 80MHz (G = 100) 45MHz (G = 1)**
- **SLEW RATE: 27V/μs**
- **16-BIT SETTLING: 700ns**
- **WIDE SUPPLY RANGE: ±2.25V to ±18V, +4.5V to +36V**
- **RAIL-TO-RAIL OUTPUT**
- **OUTPUT CURRENT: 30mA**
- **DFN-8 (3×3mm), MSOP-8, AND SO-8**

APPLICATIONS

- **PLL LOOP FILTER**
- **LOW-NOISE, LOW-POWER SIGNAL PROCESSING**
- **16-BIT ADC DRIVERS**
- **DAC OUTPUT AMPLIFIER**
- **ACTIVE FILTERS**
- **LOW-NOISE INSTRUMENTATION AMPS**
- **ULTRASOUND AMPLIFIERS**
- **PROFESSIONAL AUDIO PREAMPLIFIERS**
- **LOW-NOISE FREQUENCY SYNTHESIZERS**
- **INFRARED DETECTOR AMPLIFIERS**
- **HYDROPHONE AMPLIFIERS**
- **GEOPHONE AMPLIFIERS**
- **MEDICAL**

DESCRIPTION

The OPA211 series of precision operational amplifiers achieves very low 1.1nV/√Hz noise density with a supply current of only 3.6mA. This series also offers rail-to-rail output swing, which maximizes dynamic range.

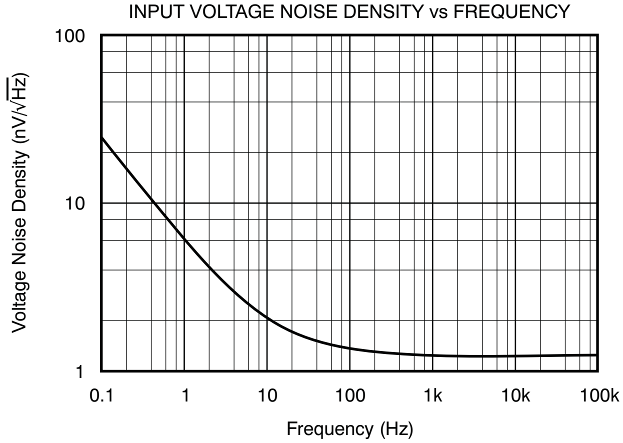
The extremely low voltage and low current noise, high speed, and wide output swing of the OPA211 series make these devices an excellent choice as a loop filter amplifier in PLL applications.

In precision data acquisition applications, the OPA211 series of op amps provides 700ns settling time to 16-bit accuracy throughout 10V output swings. This ac performance, combined with only 125μV of offset and 0.35μV/°C of drift over temperature, makes the OPA211 ideal for driving high-precision 16-bit analog-to-digital converters (ADCs) or buffering the output of high-resolution digital-to-analog converters (DACs).

The OPA211 series is specified over a wide dual-power supply range of ±2.25V to ±18V, or single-supply operation from +4.5V to +36V.

The OPA211 is available in the small DFN-8 (3×3mm), MSOP-8, and SO-8 packages. A dual version, the OPA2211, is available in the DFN-8 (3×3mm) or an SO-8 PowerPAD™ package. This series of op amps is specified from T_A = –40°C to +125°C.

INPUT VOLTAGE NOISE DENSITY vs FREQUENCY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
Supply Voltage	V_S = (V+) – (V–)	40	V
Input Voltage		(V–) – 0.5 to (V+) + 0.5	V
Input Current (Any pin except power-supply pins)		±10	mA
Output Short-Circuit(2)		Continuous	
Operating Temperature	(T_A)	–55 to +150	°C
Storage Temperature	(T_A)	–65 to +150	°C
Junction Temperature	(T_J)	200	°C
ESD Ratings	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Short-circuit to $V_S/2$ (ground in symmetrical dual supply setups), one amplifier per package.

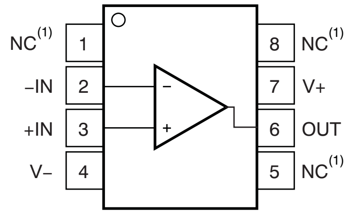
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	SINGLE	SHUTDOWN	DUAL	PACKAGE DESIGNATOR	PACKAGE MARKING
Standard Grade						
OPA211AI	DFN-8 (3×3mm)(2)	✓	✓		DRG	OBDQ
	MSOP-8(2)	✓	✓		DGK	OBCQ
OPA211AI	SO-8	✓			D	A TI OPA 211
OPA2211AI	DFN-8 (3×3mm)(3)			✓	DRG	OBHQ
	SO-8 PowerPAD(3)			✓	DDA	A TI OPA 2211
High Grade(3)						
OPA211I	DFN-8 (3×3mm)	✓	✓		DRG	OBDQ
	MSOP-8	✓	✓		DGK	OBCQ
	SO-8	✓			D	TI OPA 211
OPA2211I	DFN-8 (3×3mm)			✓	DRG	OBHQ
	SO-8 PowerPAD			✓	DDA	TI OPA 2211

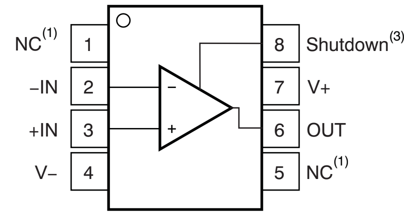
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Available Q2, 2008.
(3) Available Q3, 2008.

PIN CONFIGURATIONS

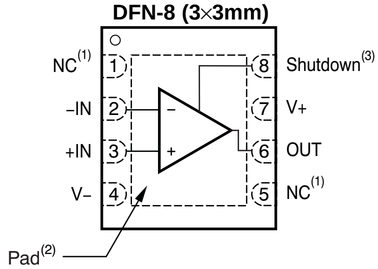
OPA211
SO-8



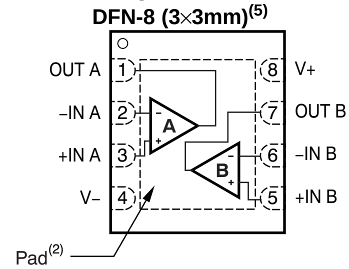
OPA211
MSOP-8(4)



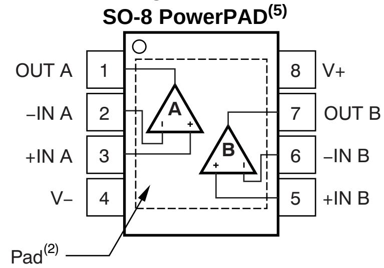
OPA211(4)
DFN-8 (3×3mm)



OPA2211
DFN-8 (3×3mm)(5)



OPA2211
SO-8 PowerPAD(5)



(1) NC denotes no internal connection. Pin can be left floating or connected to any voltage between (V–) and (V+).
(2) Exposed thermal die pad on underside; connect thermal die pad to V–.
(3) Shutdown function:
- Device enabled: (V–) ≤ $V_{SHUTDOWN}$ ≤ (V+) – 3V
- Device disabled: $V_{SHUTDOWN}$ ≥ (V+) – 0.35V

(4) Available Q2, 2008.
(5) Available Q3, 2008.

ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V

BOLDFACE limits apply over the specified temperature range, T_A = –40°C to +125°C.
At T_A = +25°C and R_L = 10kΩ, unless otherwise noted.

PARAMETER		CONDITIONS	Standard Grade OPA211A, OPA2211A MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±15V		±30	±125	µV
Drift	**dV_{OS}/dT**			**0.35**		**µV/°C**
vs Power Supply	PSRR	V_S = ±2.25V to ±18V		0.1	1	µV/V
Over Temperature					**3**	**µV/V**
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = 0V		±60	±175	nA
Over Temperature					**±200**	**nA**
Offset Current	I_{OS}	V_{CM} = 0V		±25	±100	nA
Over Temperature					**±150**	**nA**
NOISE						
Input Voltage Noise	e_n	f = 0.1Hz to 10Hz		80		nV_{PP}
Input Voltage Noise Density		f = 10Hz		2		nV/√Hz
		f = 100Hz		1.4		nV/√Hz
		f = 1kHz		1.1		nV/√Hz
Input Current Noise Density	i_n	f = 10Hz		3.2		pA/√Hz
		f = 1kHz		1.7		pA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	V_S ≥ ±5V	(V–) + 1.8		(V+) – 1.4	V
		V_S < ±5V	(V–) + 2		(V+) – 1.4	V
Common-Mode Rejection Ratio	**CMRR**	**V_S ≥ ±5V, (V–) + 2V ≤ V_{CM} ≤ (V+) – 2V**	**114**	**120**		**dB**
		V_S < ±5V, (V–) + 2V ≤ V_{CM} ≤ (V+) – 2V	**110**	**120**		**dB**
INPUT IMPEDANCE						
Differential				20k ‖ 8		Ω ‖ pF
Common-Mode				10^9 ‖ 2		Ω ‖ pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	**A_{OL}**	**(V–) + 0.2V ≤ V_O ≤ (V+) – 0.2V, R_L = 10kΩ**	**114**	**130**		**dB**
	A_{OL}	(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, R_L = 600Ω	110	114		dB
Over Temperature	**A_{OL}**	**(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, I_O ≤ 15mA**	**110**			**dB**
	A_{OL}	**(V–) + 0.6V ≤ V_O ≤ (V+)–0.6V 15mA < I_O ≤ 30mA**	**103**			**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	G = 100		80		MHz
		G = 1		45		MHz
Slew Rate	SR			27		V/µs
Settling Time, 0.01%	t_S	V_S = ±15V, G = –1, 10V Step, C_L = 100pF		400		ns
0.0015% (16-bit)		V_S = ±15V, G = –1, 10V Step, C_L = 100pF		700		ns
Overload Recovery Time		G = –10		500		ns
Total Harmonic Distortion + Noise	THD+N	G = +1, f = 1kHz, V_O = $3V_{RMS}$, R_L = 600Ω		0.000015		%
				–136		dB

ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V (continued)

BOLDFACE limits apply over the specified temperature range, T_A = –40°C to +125°C.
At T_A = +25°C and R_L = 10kΩ, unless otherwise noted.

PARAMETER		CONDITIONS	Standard Grade OPA211A, OPA2211A			UNIT
			MIN	TYP	MAX	
OUTPUT						
Voltage Output	V_{OUT}	**R_L = 10kΩ, A_{OL} ≥ 114dB**	**(V–) + 0.2**		**(V+) – 0.2**	**V**
		R_L = 600Ω, A_{OL} ≥ 110dB	(V–) + 0.6		(V+) – 0.6	V
		I_O < 25mA, A_{OL} ≥ 110dB	**(V–) + 0.6**		**(V+) – 0.6**	**V**
Short-Circuit Current	I_{SC}			+30/–45		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			pF
Open-Loop Output Impedance	Z_O	1MHz		5		Ω
SHUTDOWN						
Shutdown Pin Input Voltage		Device shutdown	(V+) – 0.35			V
		Device enabled			(V+) – 3	V
POWER SUPPLY						
Specified Voltage	V_S		±2.25		±18	V
Quiescent Current (per channel)	I_Q	I_{OUT} = 0A		3.6	4.5	mA
Over Temperature					**6**	**mA**
TEMPERATURE RANGE						
Specified Range		T_A	–40		+125	°C
Operating Range		T_A	–55		+150	°C
Thermal Resistance						
DFN (3mm × 3mm)	θ_{JA}	Soldered to approximately 5cm × 5cm copper area		65		°C/W
	θ_{JC}			57		°C/W
MSOP-8	θ_{JA}			200		°C/W
SO-8	θ_{JA}			150		°C/W
SO-8 PowerPAD	θ_{JA}	Test board 1in × 0.5in heat-spreader, 1oz copper		52		°C/W
	θ_{JC}			43		°C/W

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

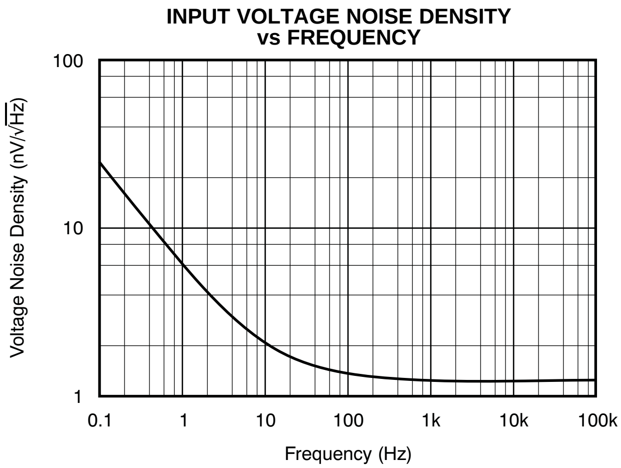


Figure 1.

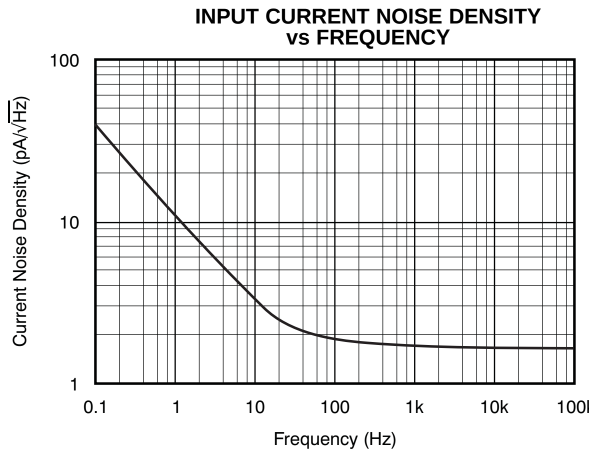


Figure 2.

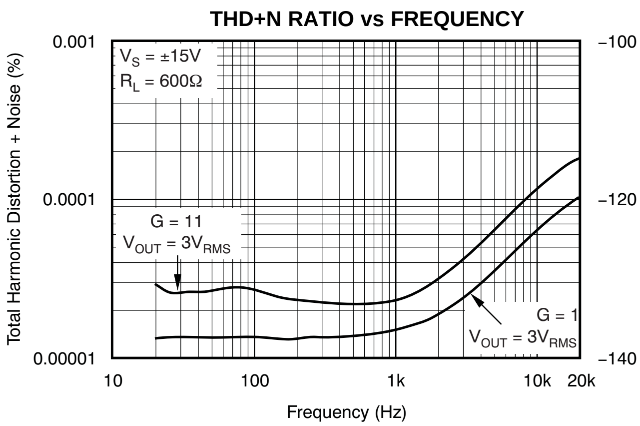


Figure 3.

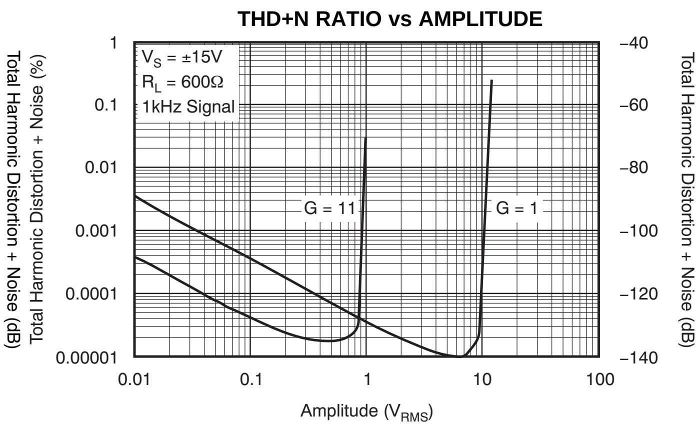


Figure 4.

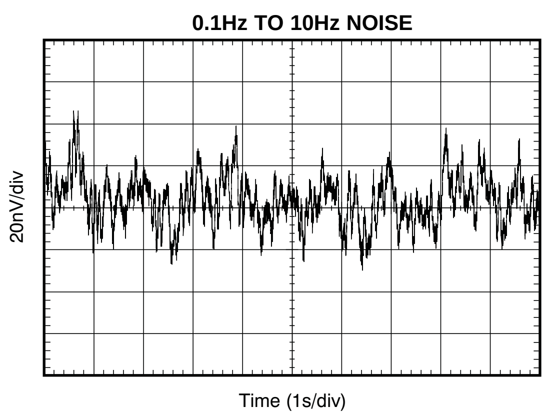


Figure 5.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

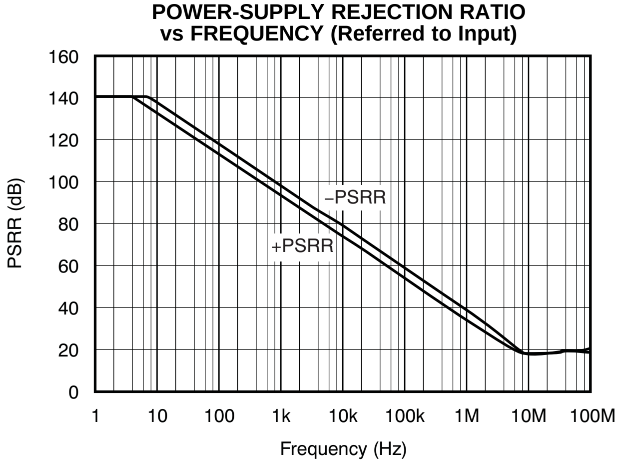


Figure 6.

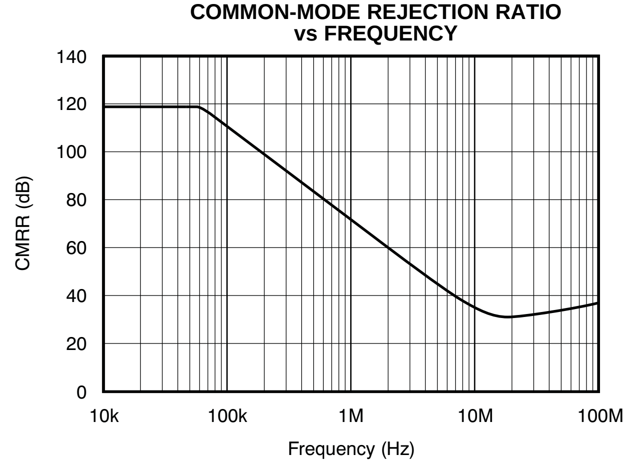


Figure 7.

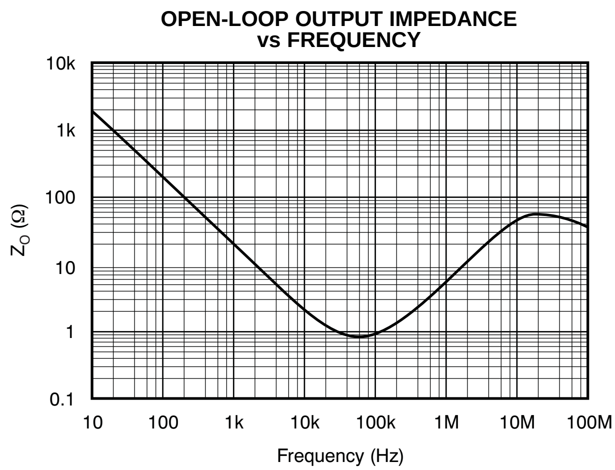


Figure 8.

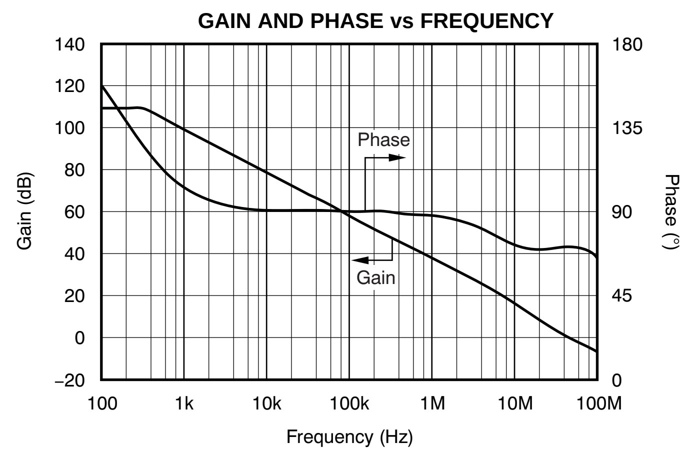


Figure 9.

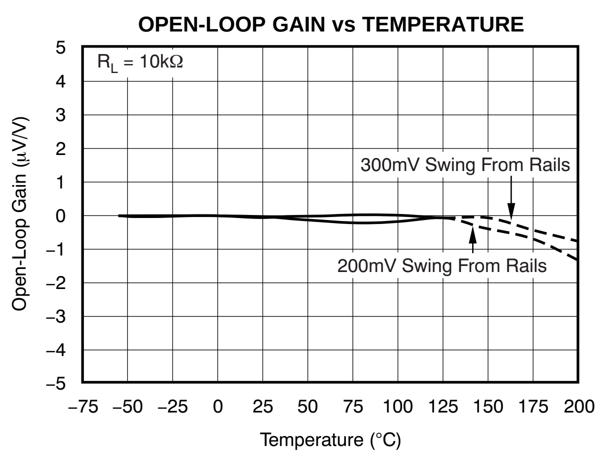


Figure 10.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

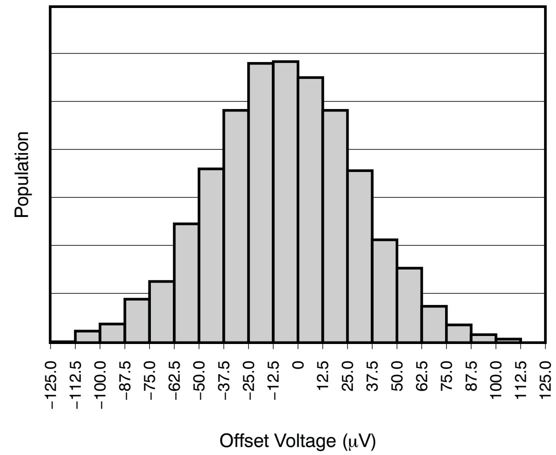


Figure 11.

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

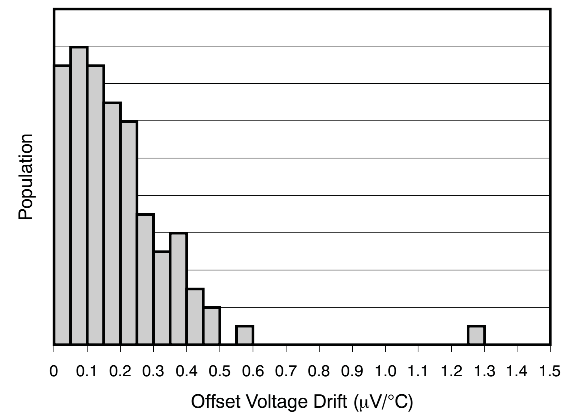


Figure 12.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

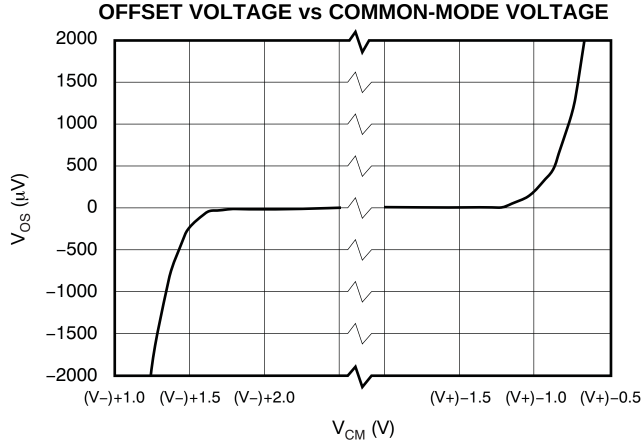


Figure 13.

V_{OS} WARMUP

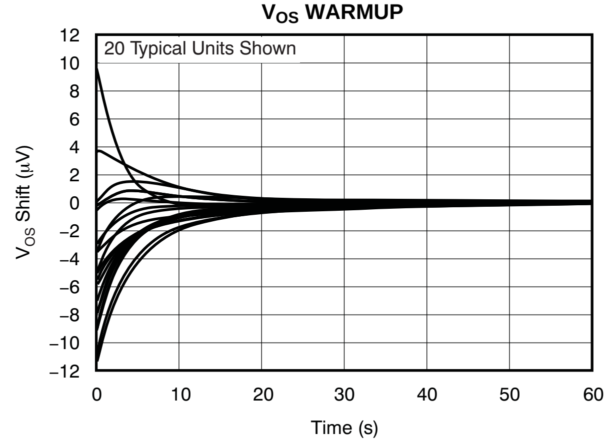


Figure 14.

INPUT OFFSET CURRENT vs SUPPLY VOLTAGE

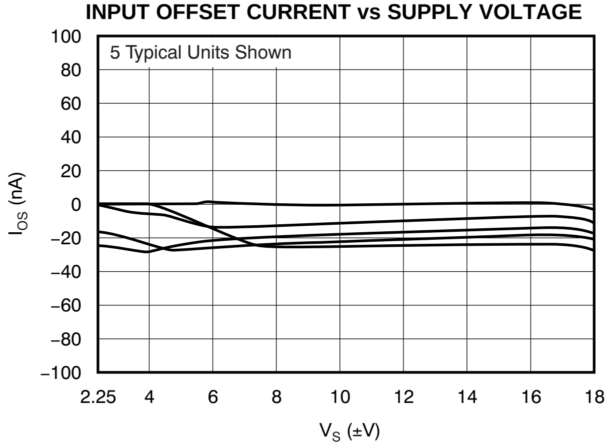


Figure 15.

INPUT OFFSET CURRENT vs COMMON-MODE VOLTAGE

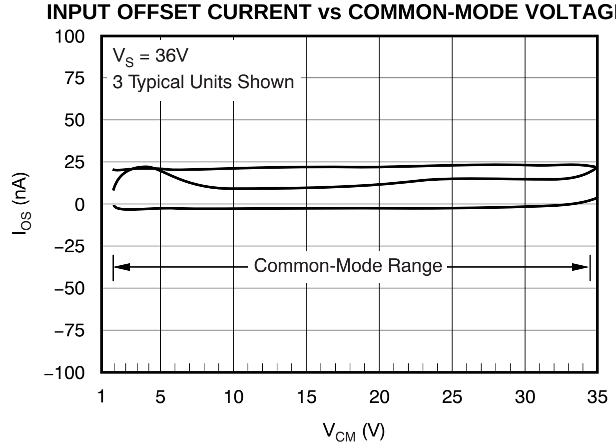


Figure 16.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

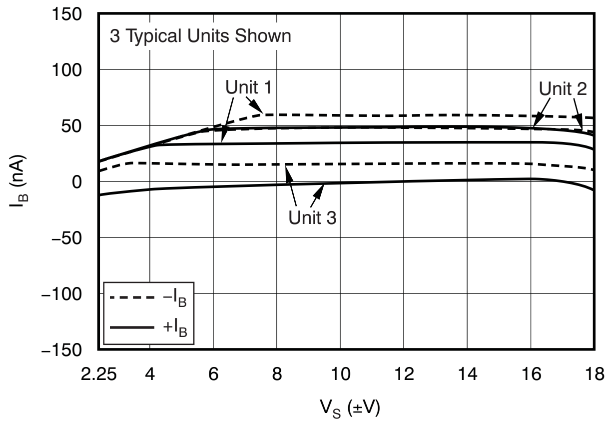


Figure 17.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

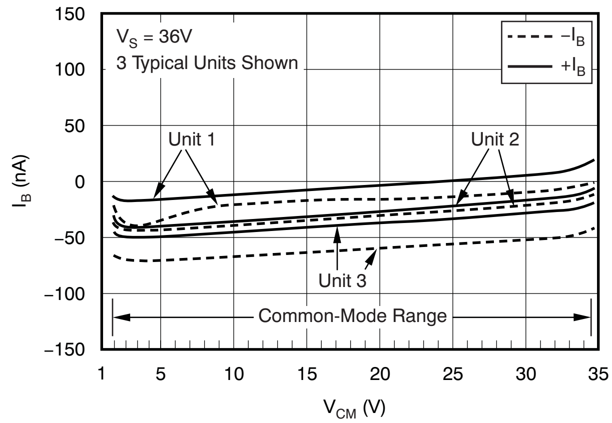


Figure 18.

QUIESCENT CURRENT vs TEMPERATURE

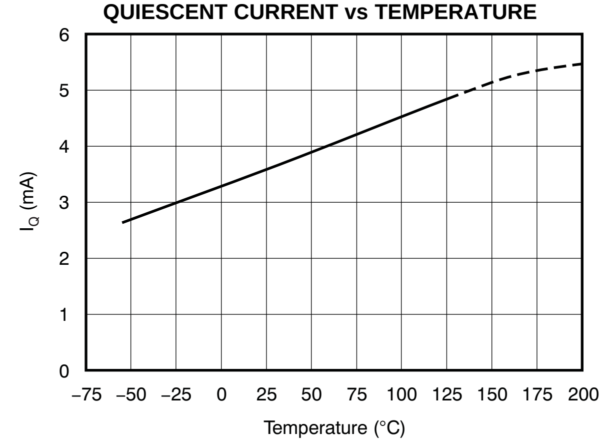


Figure 19.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

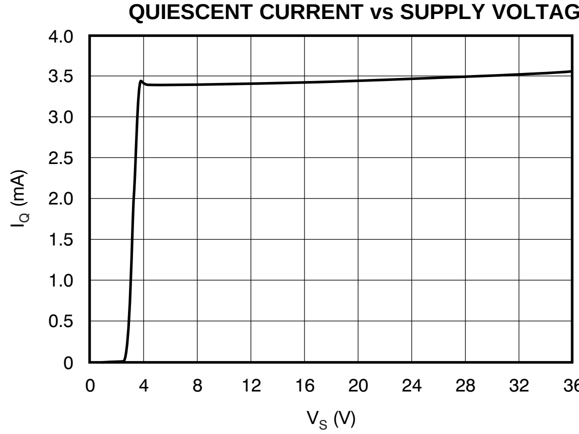


Figure 20.

NORMALIZED QUIESCENT CURRENT vs TIME

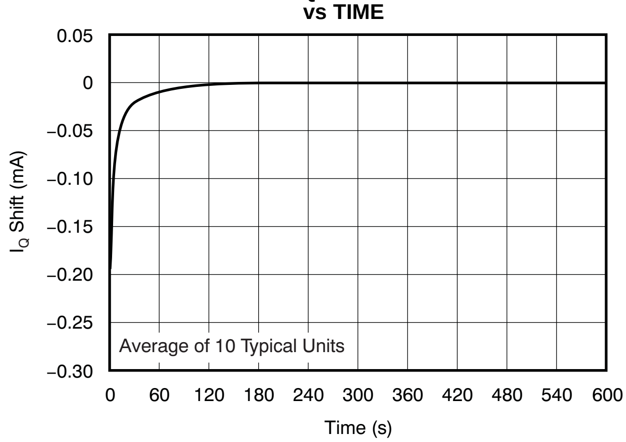


Figure 21.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

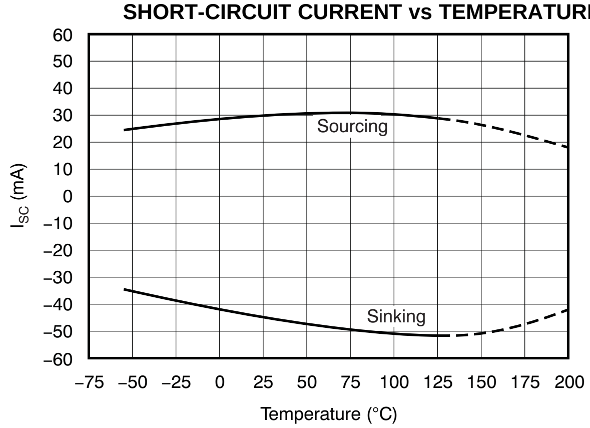


Figure 22.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE (100mV)

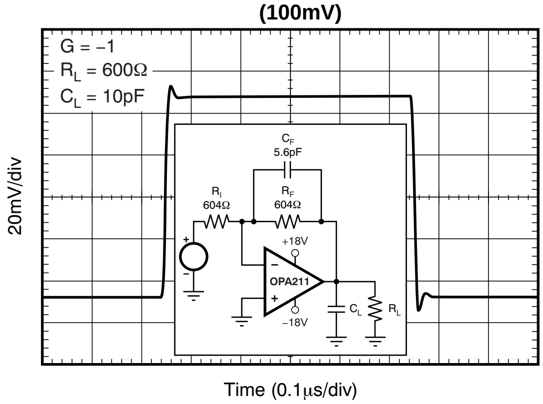


Figure 23.

SMALL-SIGNAL STEP RESPONSE (100mV)

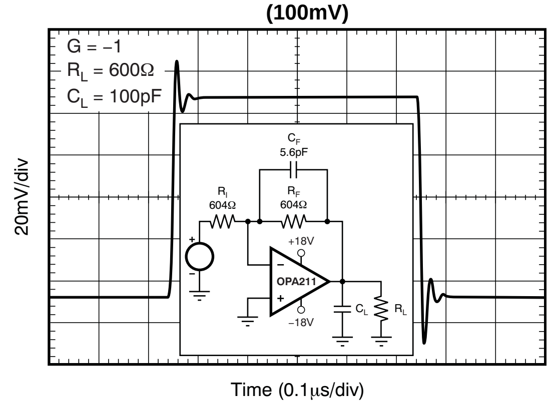


Figure 24.

SMALL-SIGNAL STEP RESPONSE (100mV)

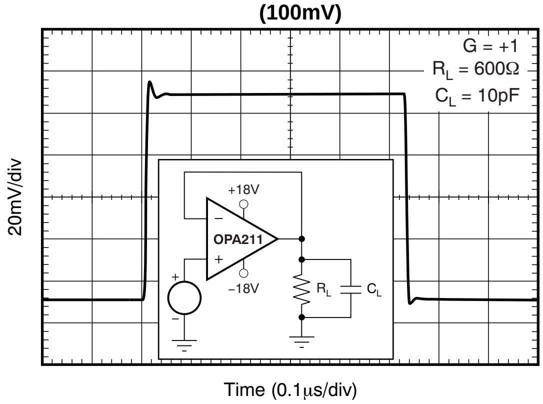


Figure 25.

SMALL-SIGNAL STEP RESPONSE (100mV)

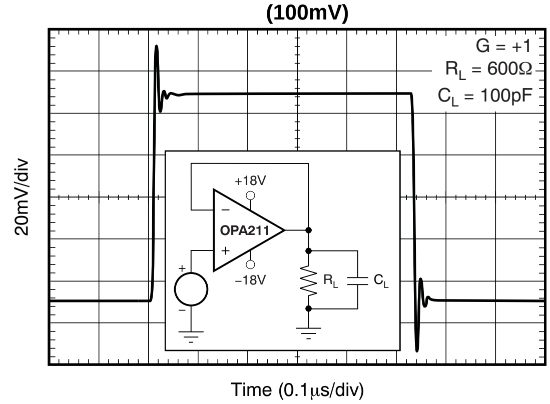


Figure 26.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

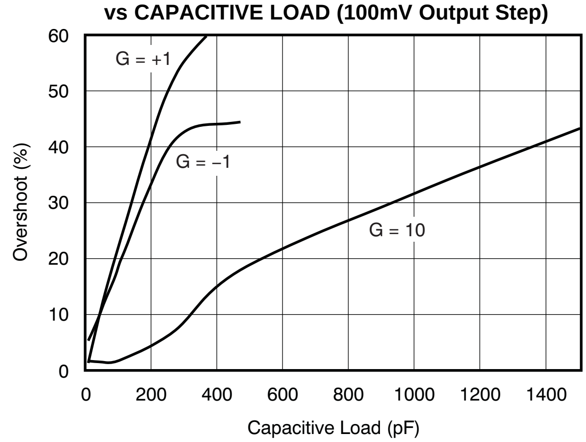


Figure 27.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

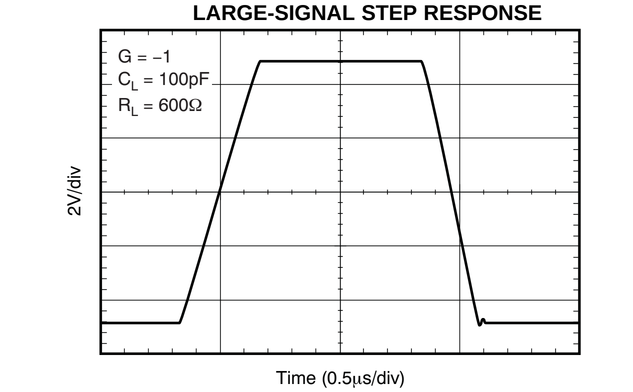


Figure 28.

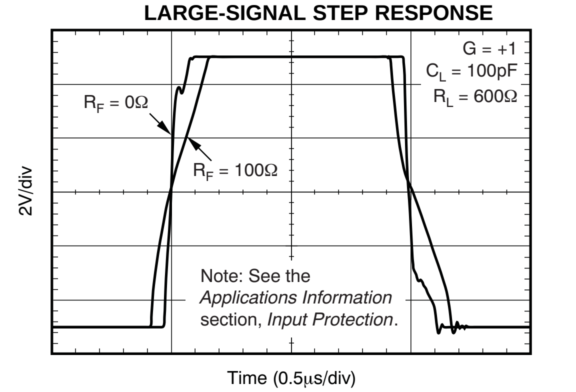


Figure 29.

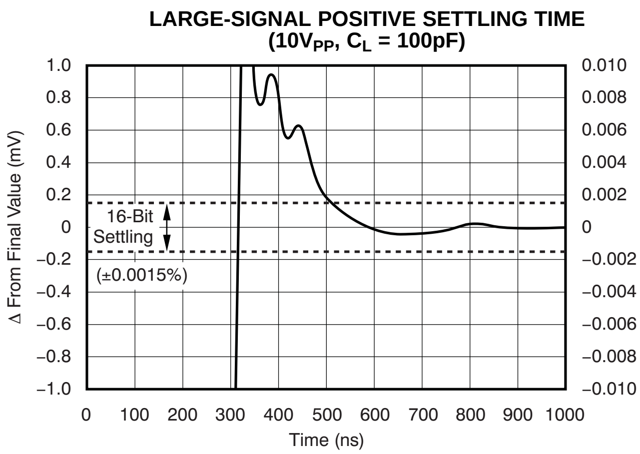


Figure 30.

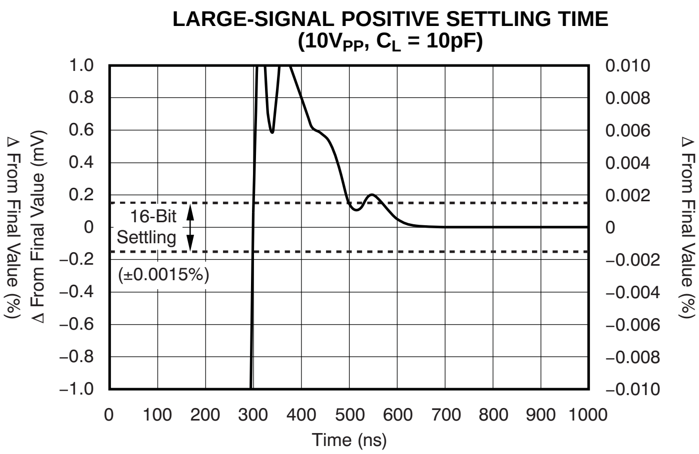


Figure 31.

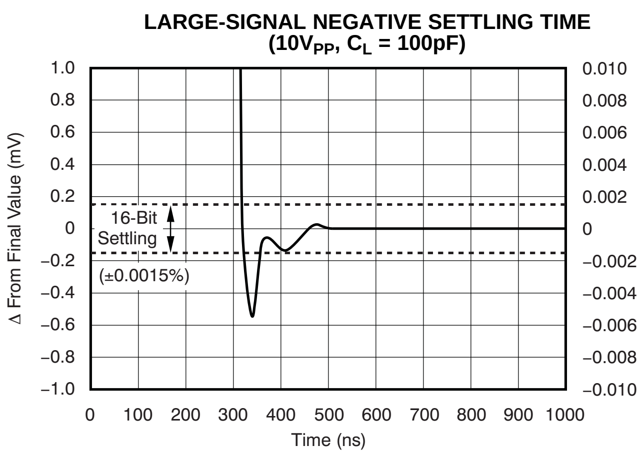


Figure 32.

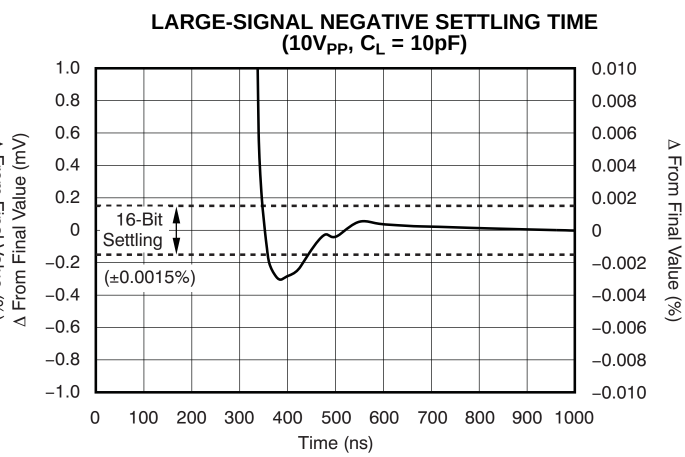


Figure 33.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

NEGATIVE OVERLOAD RECOVERY

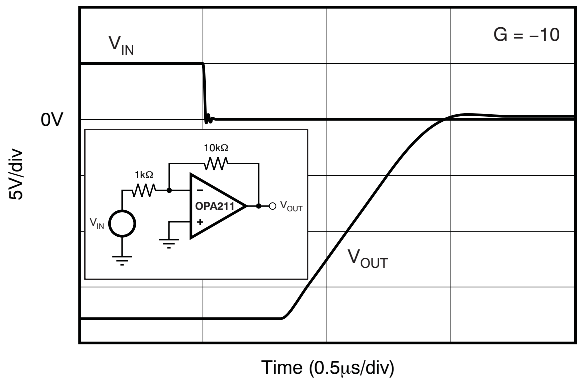


Figure 34.

POSITIVE OVERLOAD RECOVERY

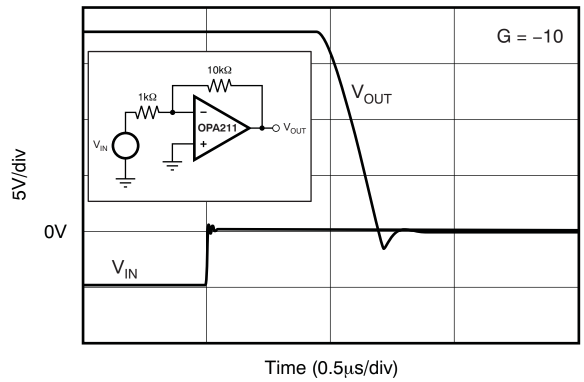


Figure 35.

OUTPUT VOLTAGE vs OUTPUT CURRENT

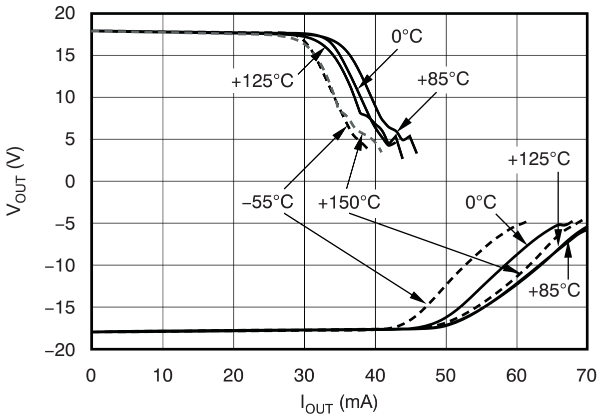


Figure 36.

NO PHASE REVERSAL

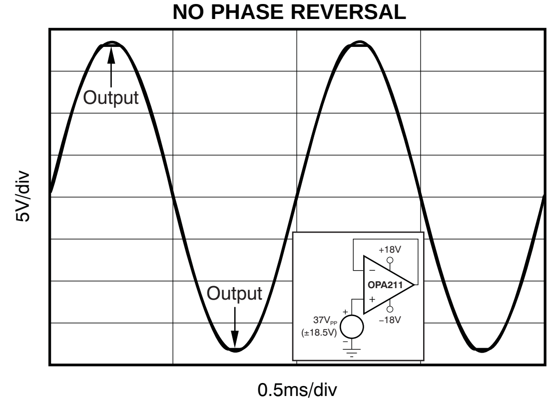


Figure 37.

APPLICATION INFORMATION

The OPA211 and OPA2211 are unity-gain stable, precision op amps with very low noise. Applications with noisy or high impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate. Figure 38 shows a simplified schematic of the OPA211. This die uses a SiGe bipolar process and contains 180 transistors.

OPERATING VOLTAGE

OPA211 series op amps operate from ±2.25V to ±18V supplies while maintaining excellent performance. The OPA211 series can operate with as little as +4.5V between the supplies and with up to +36V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA211 series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25V with the negative supply at –5V or vice-versa.

The common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range, T_A = –40°C to +125°C. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

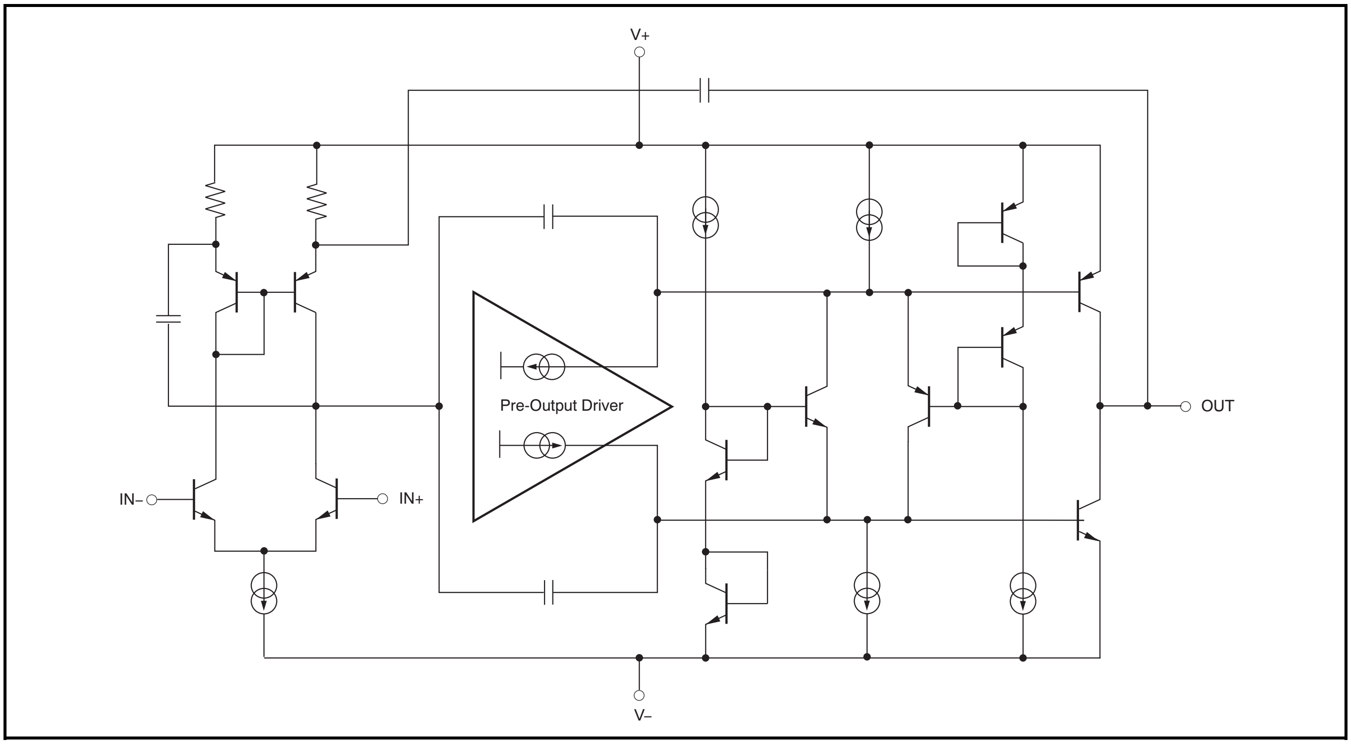


Figure 38. OPA211 Simplified Schematic

INPUT PROTECTION

The input terminals of the OPA211 are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 39. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 29 of the Typical Characteristics. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low noise performance of the OPA211. See the *Noise Performance* section of this data sheet for further information on noise calculation. Figure 39 shows an example implementing a current-limiting feedback resistor.

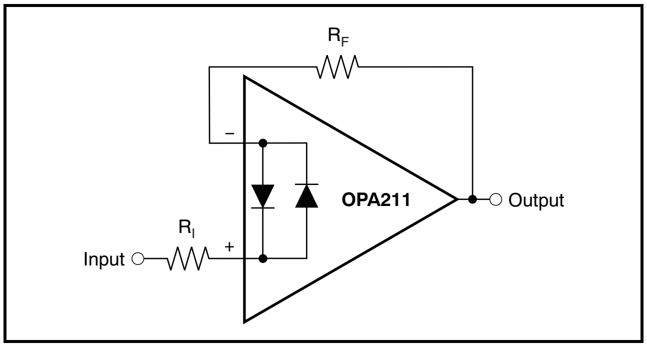


Figure 39. Pulsed Operation

NOISE PERFORMANCE

Figure 40 shows total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with total circuit noise calculated. The OPA211 has very low voltage noise, making it ideal for low source impedances (less than 2kΩ). A similar precision op amp, the OPA227, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10kΩ to 100kΩ). Above 100kΩ, a FET-input op amp such as the OPA132 (very low current noise) may provide improved performance. The equation in Figure 40 is shown for the calculation of the total circuit noise. Note that e_n = voltage noise, i_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38×10^{-23} J/K, and T is temperature in K. For more details on calculating noise, see the *Basic Noise Calculations* section.

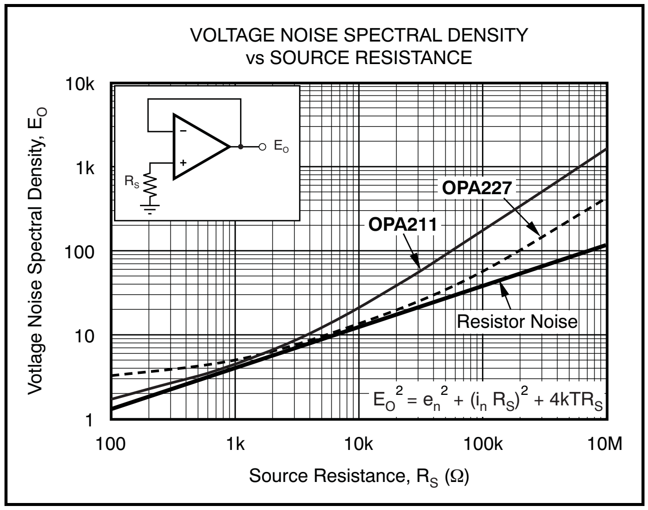


Figure 40. Noise Performance of the OPA211 in Unity-Gain Buffer Configuration

BASIC NOISE CALCULATIONS

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 40. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 40 depicts total noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

Figure 41 illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

TOTAL HARMONIC DISTORTION MEASUREMENTS

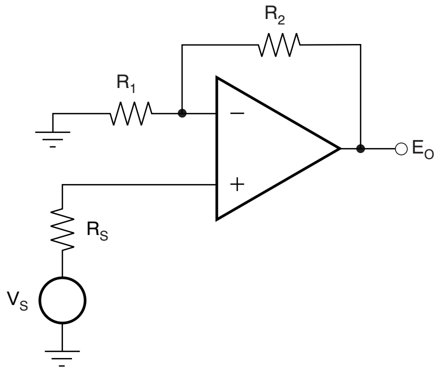
OPA211 series op amps have excellent distortion characteristics. THD + Noise is below 0.0001% (G = +1, V_O = 3V_{RMS}) throughout the audio frequency range, 20Hz to 20kHz, with a 600Ω load.

The distortion produced by OPA211 series op amps is below the measurement limit of many commercially available equipment. However, a special test circuit illustrated in Figure 42 can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. Figure 42 shows a circuit that causes the op amp distortion to be 101 times greater than normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

Noise in Noninverting Gain Configuration



Noise at the output:

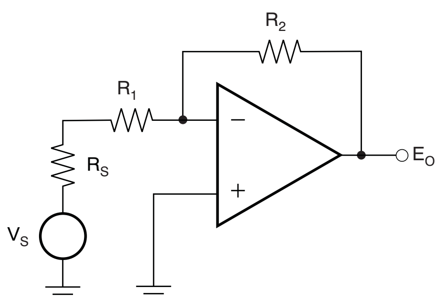
$$E_O^2 = \left[1 + \frac{R_2}{R_1}\right]^2 e_n^2 + e_1^2 + e_2^2 + (i_nR_2)^2 + e_S^2 + (i_nR_S)^2 \left[1 + \frac{R_2}{R_1}\right]^2$$

Where $e_S = \sqrt{4kTR_S} \times \left[1 + \frac{R_2}{R_1}\right]$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left[\frac{R_2}{R_1}\right]$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left[1 + \frac{R_2}{R_1 + R_S}\right]^2 e_n^2 + e_1^2 + e_2^2 + (i_nR_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \times \left[\frac{R_2}{R_1 + R_S}\right]$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left[\frac{R_2}{R_1 + R_S}\right]$ = thermal noise of R_1

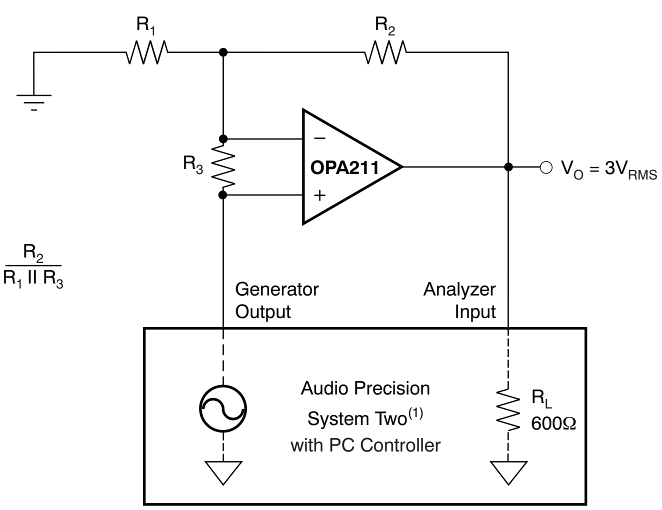
$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA211 series op amps at 1kHz, $e_n = 1.1\text{nV}/\sqrt{\text{Hz}}$ and $i_n = 1.7\text{pA}/\sqrt{\text{Hz}}$.

Figure 41. Noise Calculation in Gain Configurations

Signal Gain $= 1 + \frac{R_2}{R_1}$

Distortion Gain $= 1 + \frac{R_2}{R_1 \parallel R_3}$



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
11	101	100Ω	1kΩ	11Ω

NOTE: (1) Measurement BW = 80kHz.

Figure 42. Distortion Test Circuit

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA211AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA211AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA211AIDGKR	PREVIEW	MSOP	DGK	8	2500	TBD	Call TI	Call TI
OPA211AIDGKT	PREVIEW	MSOP	DGK	8	250	TBD	Call TI	Call TI
OPA211AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA211AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA211AIDRGR	PREVIEW	SON	DRG	8	1000	TBD	Call TI	Call TI
OPA211AIDRGT	PREVIEW	SON	DRG	8	250	TBD	Call TI	Call TI
OPA2211AIDDA	PREVIEW	SO Power PAD	DDA	8	75	TBD	Call TI	Call TI
OPA2211AIDDAR	PREVIEW	SO Power PAD	DDA	8	2500	TBD	Call TI	Call TI
OPA2211AIDRGR	PREVIEW	SON	DRG	8	1000	TBD	Call TI	Call TI
OPA2211AIDRGT	PREVIEW	SON	DRG	8	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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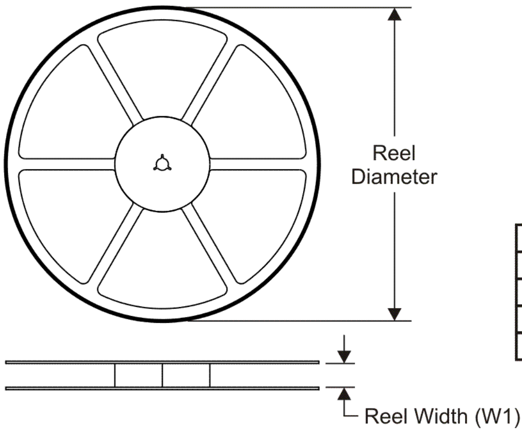
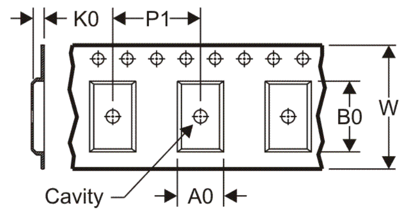
TAPE AND REEL INFORMATION

REEL DIMENSIONS

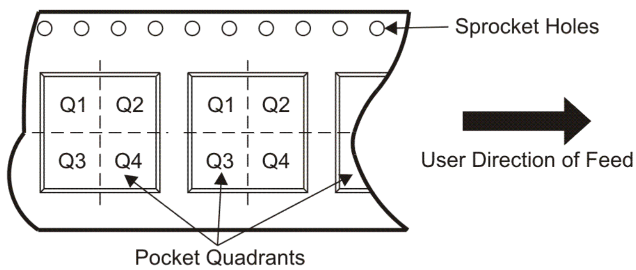


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

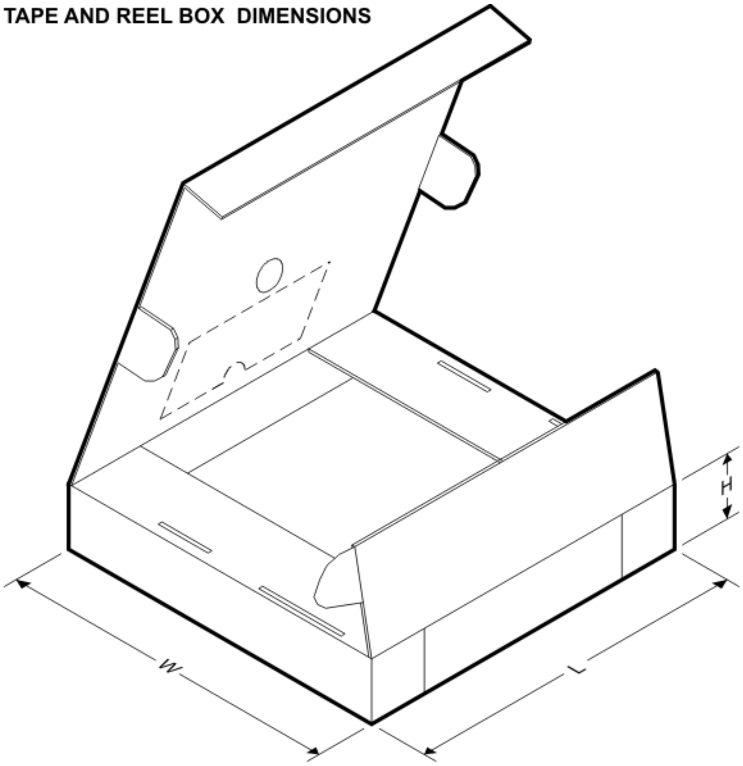
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA211AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

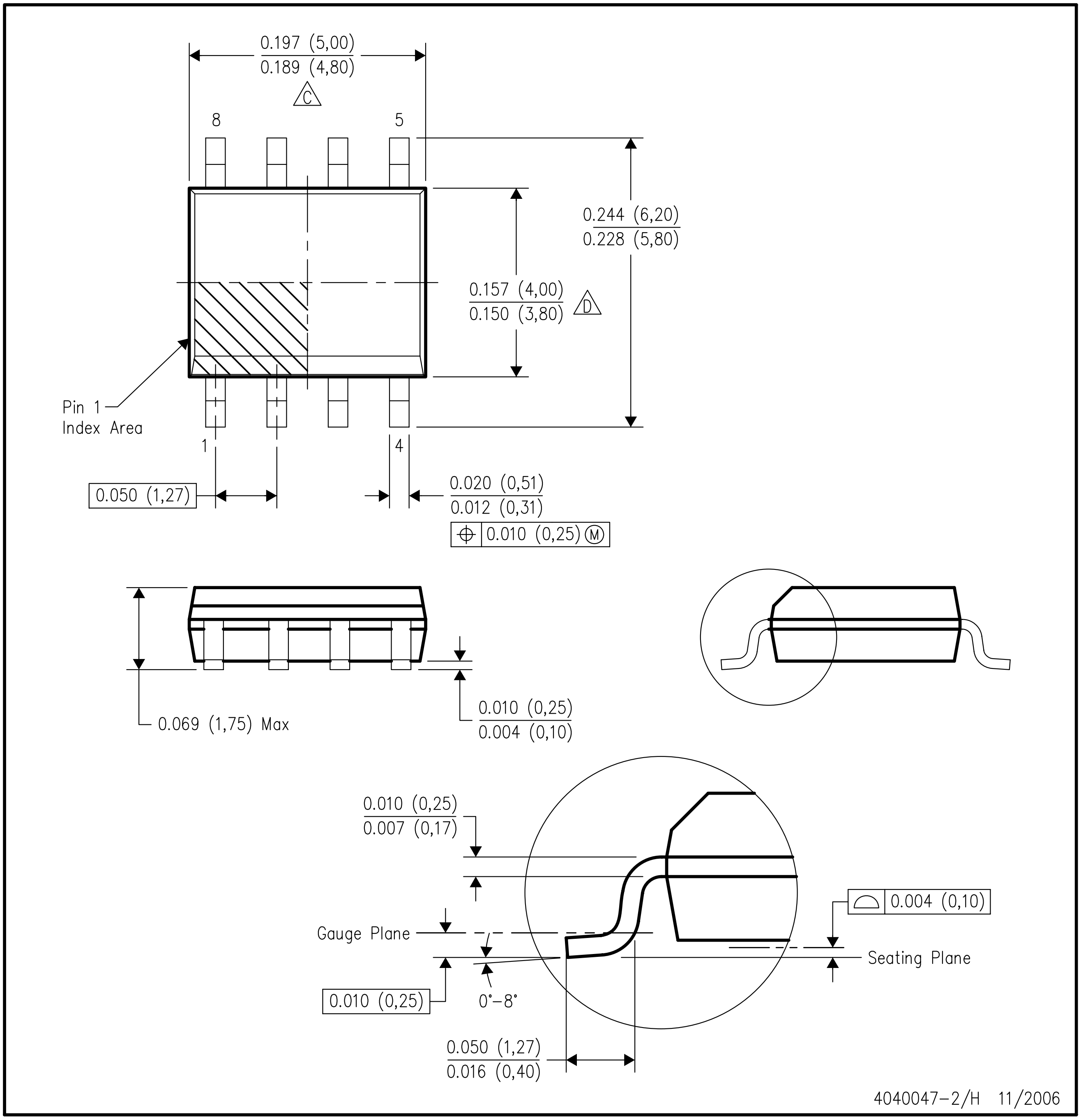
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

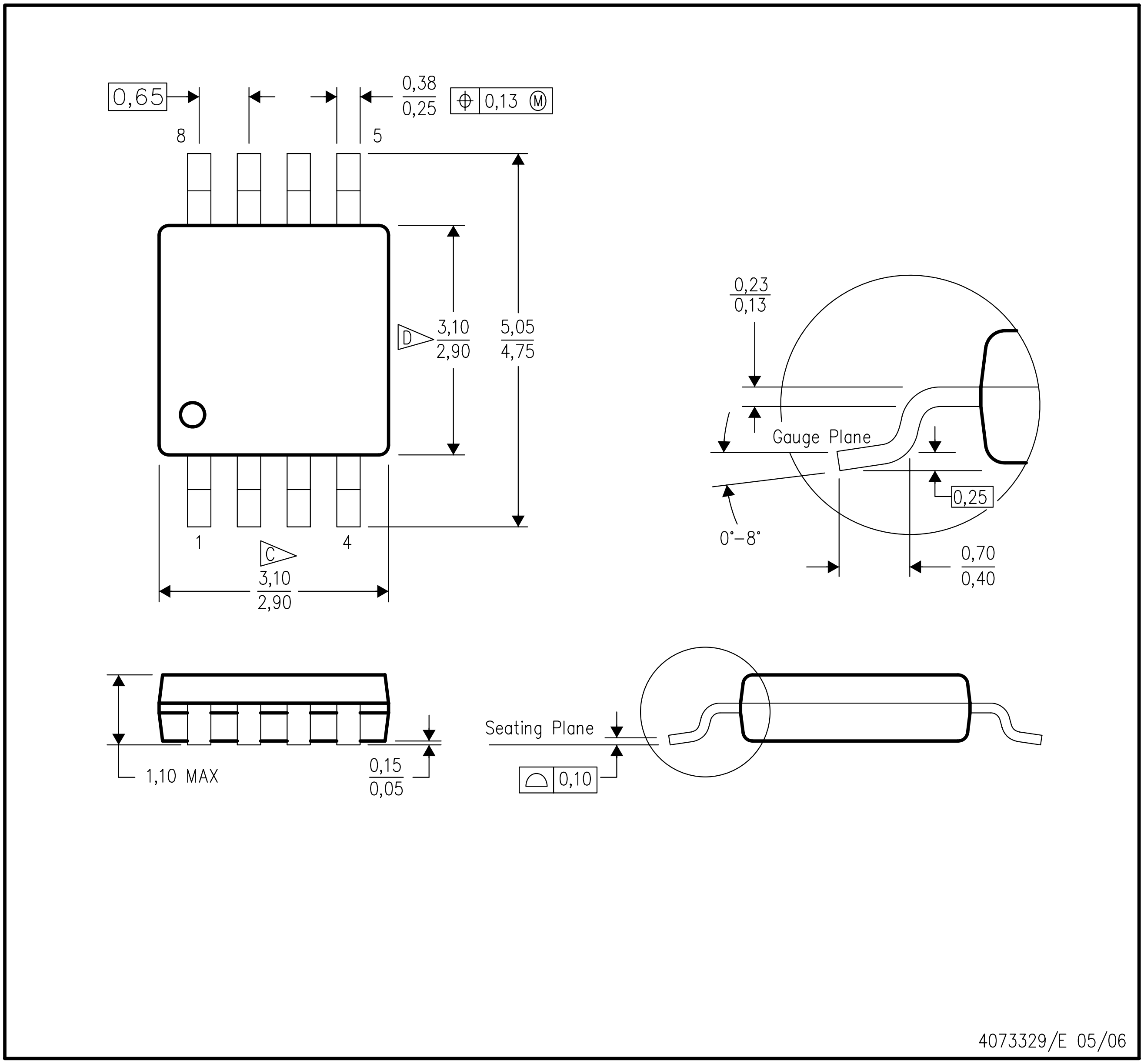
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA211AIDR	SOIC	D	8	2500	346.0	346.0	29.0

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



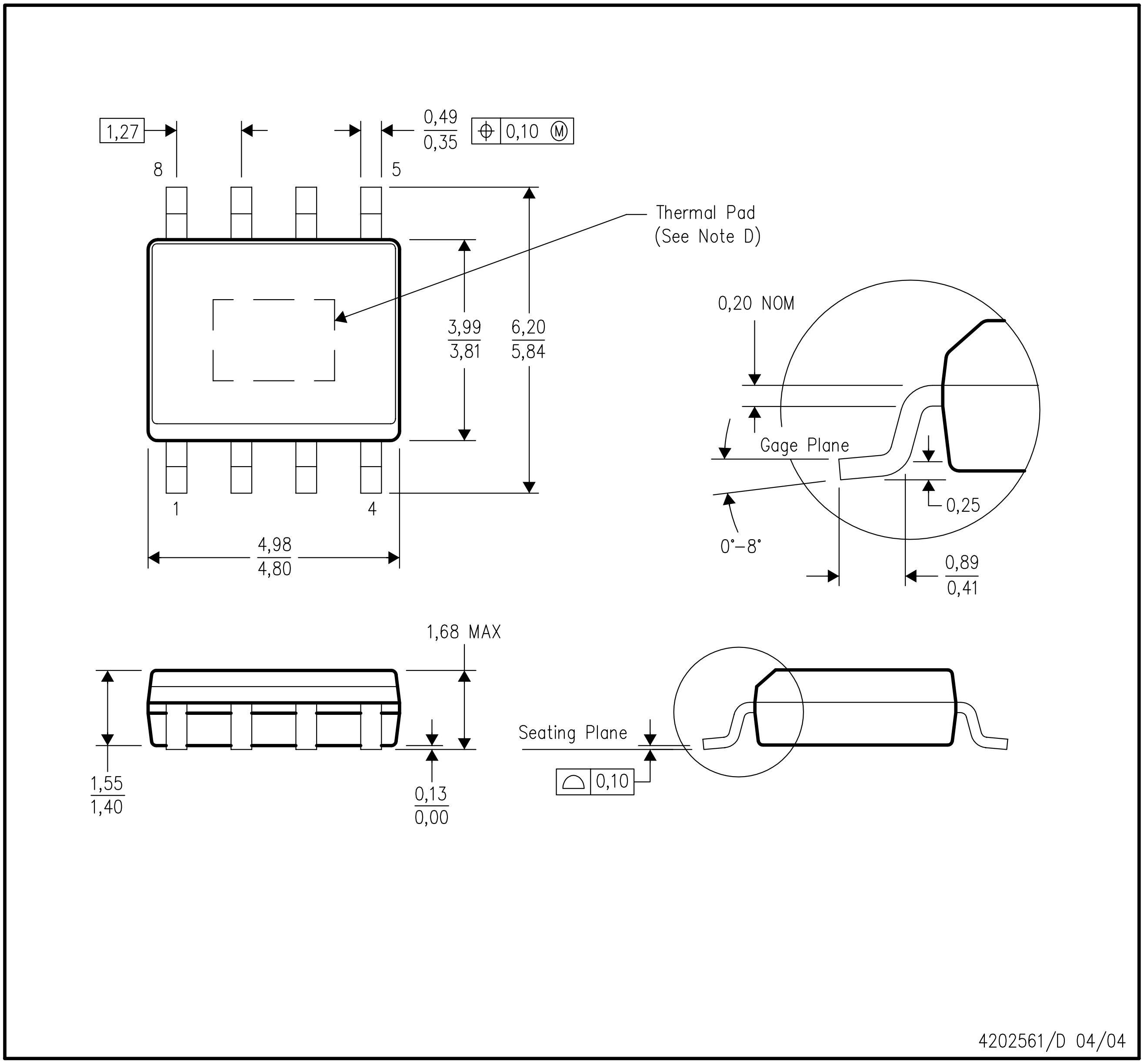
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.

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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
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RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
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		Wireless	www.ti.com/wireless

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